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Yield-driven power-delay-optimal CMOS full-adder design complying with automotive product specifications of PVT variations and NBTI degradations

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Abstract We present the detailed results of the application of mathematical optimization algorithms to transistor sizing in a full-adder cell design, to obtain the maximum expected fabrication yield. The approach takes into account all the fabrication process parameter variations specified in an industrial PDK, in addition to operating condition range and NBTI aging. The final design solutions present transistor sizing, which depart from intuitive transistor sizing criteria and show dramatic yield improvements, which have been verified by Monte Carlo SPICE analysis.

Keywords Yield · Circuit sizing · CMOS · Statistical variations · NBTI · Leakage · Delay

1 Introduction

The full-adder cell is one of the most fundamental and frequently used building blocks in the critical paths of arithmetic circuits both in microprocessors and application-specific digital signal processing architectures. While its basic usage is in binary additions, it is also a pivotal element for other operations like subtraction, multiplication, division, address calculation, time counting, etc. [1]. Therefore, improvements in the characteristics of full-adder circuits to a great extent improve the performance of an entire chip [2–4] and as such they have been the subject of research for decades.

The effective design of integrated circuits (ICs) relies on the optimization of basic circuit performance such as operating speed, power dissipation, and area. In earlier CMOS technology nodes (0.35 µm or higher), the impact of process variations on circuit performance was small [5]. The standard design approach assumed worst-case deterministic electrical and physical properties of devices and performance predictable over the device life time. In recent years, with the continued downscaling in CMOS technology, it has become very challenging to maintain the level of manufacturing control and uniformity, which resulted in the enormous increase in process variability. Moreover, in further scaled nanometric regime (<65 nm), devices that were intended to be identical differ in their electrical characteristics, which can also lead to functional failures [6]. Such intra-die variations (mismatch between two identical devices) can have significantly higher influence on the behavior of the circuit than other inter-die (global) process variations in the present technology nodes. Overall, the fluctuations in device dimensions and physical parameters are imposing a significant threat in meeting the desired timing and power criteria ultimately degrading the fabrication outcome of ICs (yield).

In addition to statistical variations, fluctuations in operating parameters (e.g., supply voltage and temperature) already exist, which significantly deviate circuit performance from their expected values. As an example, the higher temperature decreases the threshold voltage, which may be good for speed but not for static power. Similarly, a circuit designed to operate at 1 V may work at 0.95 V due to fluctuation in supply voltage, and eventually operate at lower speed than the intended speed. In particular application domains, the fluctuation of the operating conditions make circuit performance (delay and power figures) hardly predictable and reduce the effective yield of the IC fabrication.

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Finally, an additional dimension in IC reliability and yield assessment comes from device aging effects, which degrade the reliability of the circuit and even system operation over time. Aging degradation mechanisms such as negative bias temperature instability (NBTI) is threatening state of the art circuit and product life by impacting PMOS devices [7] over the years. Again, such effect assumes a paramount importance in application domains where the product life cycle is in the order of years.

On the whole, the sources of process variations, operating condition variations, and aging degradation effects combine together and can pull the actual circuit operation out of the application requirements, reducing the production yield. Therefore, circuit optimization for yield has become a crucial as well as complex task in IC design. In fact, a high degree of reliability—and consequently high yield—is achievable only if *the devices in the circuit are cooperatively resistant* against statistical (inter-die and intra-die) and operating condition variations in conjunction with aging degradation effects.

Within this vision, the proposed work presents the application of a mathematical methodology capable of searching the circuit design space to find the optimal sizing of all devices in a CMOS full-adder circuit in order to maximize the yield, referring to speed and power specifications, with respect to operating variations as from automotive application specifications, process variations, and aging degradation phenomena. The target full-adder cell has 28 transistors. Different from approaches that focus on threshold voltage variations only, the presented approach takes into account all sources of local and global variability specified in the Process Development Kit of a 40-nm technology from STMicroelectronics. The target range of temperature was -40 to 125 °C and supply voltage range was +/–10 % fluctuations over nominal value. The complete optimal sizing has been carried out for 12 different specification bounds of targeted performance figures (leakage power, total power, and propagation delays) in order to have large generalized spectrum of performance specification versus yield. Reported circuit sizing solutions cannot be achieved by manual circuit design criteria. The estimated yields before and after optimizations have been verified by SPICE level Monte Carlo simulations.

We remark that this work does not develop novel variation-aware and NBTI-aware device/circuit models.

The rest of the paper is organized as follows: Sect. 2, after reporting previous related works, explains the statistical and operating variations and NBTI aging degradation along with evidence of their impact on delay and power performance figures. Section 3 shows the design goals (i.e., performance specification setup for CMOS full adder), circuit parameter setup, and optimization problem formulation. Section 4 reports the optimization methodology. Section 5 is devoted to the analysis of robust circuit sizing results for 12 different specification bounds, followed by the validation of estimated yield through Monte Carlo analysis in Sect. 6.

2 Background and related works

2.1 Statistical and operating variation impact

Process variations have always existed in spite of designers' choices. However, they have been gaining increasing importance with the scaling in device dimensions and challenging state of art circuit reliability. Global variations (e.g., oxide thickness) come from chip-to-chip, wafer-to-wafer, or batch-to-batch variations [5,6]. Such process variations have long-range influences and affect every device of the same type in an identical fashion [8]. Local process parameters (e.g., threshold voltage) characterize the short-range influences. Local process variations may occur due to random dopant fluctuations, line edge and width roughness (LER and LWR), fixed charges in the gate dielectric, interface roughness, and other fluctuations that affect every device in a chip individually. Local process parameters can cause mismatch between devices and may disturb fundamental design principles of creating constant differences and ratios of currents and voltages. For scaled CMOS technology nodes ($<$90 nm), the impact of local variability has become as important as global process variations on the circuit behavior [8,9].

Operating conditions strongly define the electrical behavior of the devices, as well. This is immediate for the operational supply voltage as it determines internal node voltages in the circuits. On the other hand, the carrier mobility and threshold voltage are strongly temperature dependent [5].

2.2 Aging degradations impact

Once a chip is manufactured and tested for correct functionality, it is expected to work for intended life time at the tested voltage and temperature. However, aging mechanisms such as NBTI threaten the circuit and product life time [7,10,11]. NBTI takes place in negatively biased ($V_{GS} < 0$ V) PMOS at elevated temperatures and is a consequence of interface trap generation at the interface of Si/oxide.

In conventional silicon-based MOS, transistor annealing in hydrogen ambient was an effective solution to control the interface trap instabilities for long time. However, the continuing MOS dimension shrinking trends, (i.e., aggressive oxide thickness scaling leading to higher oxide field) along with process modifications (such as nitridation of oxides) and higher operation temperatures (due to higher power density) led to accelerate the bond breaking at the interface over time during the device operation [9,12]. The traps increase the threshold voltage and reduce the channel mobility due to scattering. Overall, the drain current degrades over time

and parametric reliability becomes a significant concern. The magnitude of NBTI degradation depends on stress time, temperature, and electrical field across the gate oxide [12].

Interestingly, most of the effects of device aging mechanisms can be understood by the growth of threshold voltage (V_T). In general, aging-induced increment in V_T causes a (disadvantageous) increase in propagation delays and a (favorable) reduction in static power over time.

SPICE level evaluation of the impact of NBTI can be obtained by ad hoc compact models integrated in the simulation engine that changes the threshold voltage according to the simulated stress on devices. For an analytic model of threshold voltage drift due to NBTI, the reader may refer to [13].

2.3 Related works

Several design time transistor sizing techniques to optimize cell delay and/or power have been proposed in the literature.

The approach proposed in [14] introduces variation-tolerant gate sizing incorporating statistical timing model. The approach formulates the statistical objective and timing constraints and solves the resulting nonlinear optimization problem, at the expense of a high computational complexity.

In [15], the authors report an automatic method for sizing the transistors in CMOS gates based on the feedback control system to optimize the gates of small and large fain-in. However, the primary goal was to enhance noise robustness.

Other proposed gate sizing techniques [16–19] rely on the notion of capturing the delay distribution by performing statistical static timing analysis instead of static timing analysis. Then, gate sizing is carried out using either nonlinear programming technique or statistical sensitivity-based heuristic procedure.

In [20], the authors present an optimization scheme based on polynomial delay model for gate sizing incorporating process variations. In the technique, the delay constraints are modified in order to integrate the uncertainties in the transistor widths and effective channel length due to process variations based on the uncertainty ellipsoid method. Spatial correlations of intra-die width and channel length have also been considered in optimization.

In [21,22], the authors reported a statistically aware dual-Vt and sizing optimization considering variability both in performance and leakage in the design.

In [23–25], the authors reported SQP/least square and WCD algorithm-based interactive circuit sizing and yield optimization for analog and digital circuits considering statistical variations in a defined range of operating conditions.

Other approaches based on convex formulation using second-order conic program and binning model have been reported in [26,27], respectively, for statistical power optimization in circuits subjected to timing yield constraints.

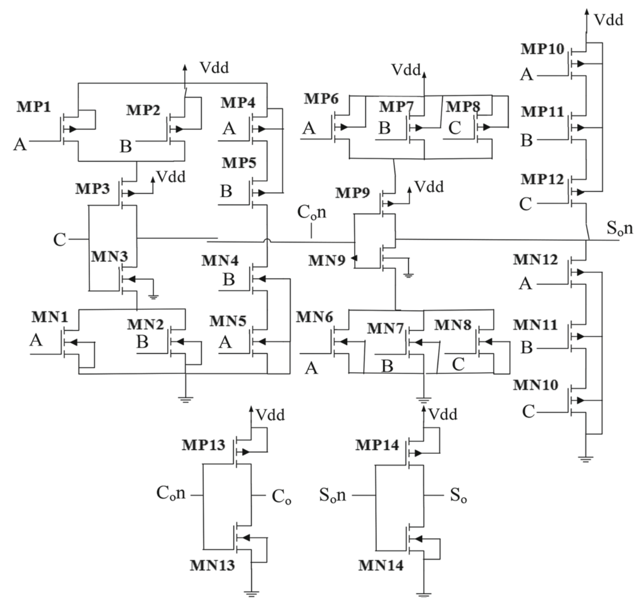


Fig. 1 Target CMOS full-adder circuit

Some other gate sizing techniques based on the robust optimization are proposed in [20,28]. Such techniques illustrate by adding the robust constraints to the original constraints and modeling the intrachip (mismatch) variations as Gaussian variables contained in constant probability density uncertainty ellipsoid, centered at nominal values.

3 Motivation and problem statement

Figure 1 shows the target full-adder cell topology, which consists of 14 nMOS and 14 pMOS transistors in mirror configuration.

Figure 2 depicts the impact of some process variations on performance figures of the cell, resulting from SPICE simulation, referring to the target 40-nm low-power (LP) standard-threshold-voltage CMOS process development kit (PDK) from STMicroelectronics. It can be seen (in upper graph) that, under the influence of one of the dominating process parameters, PAR1[1], the *power* figure goes out of the prescribed bound ($< 6\,\mu$W), and an unpredictable behavior of the same *power* figure is experimented with the variations in *tox_core*. At the same time, delay figures (in bottom graph) show an increase of 2 % and 34 % under the influence of single-process parameter variation. As an example, impact of process variations (PAR1 and mismatch between two nMOS transistors) on *delay* figure is shown for the worst-case delay arc, i.e., *delayHL_nodeB_Co* (delay is estimated when input

[1] PAR1 is one of the most dominant global process parameters characterized in the target technology PDK. It depends on several physical process parameters through confidential equations.

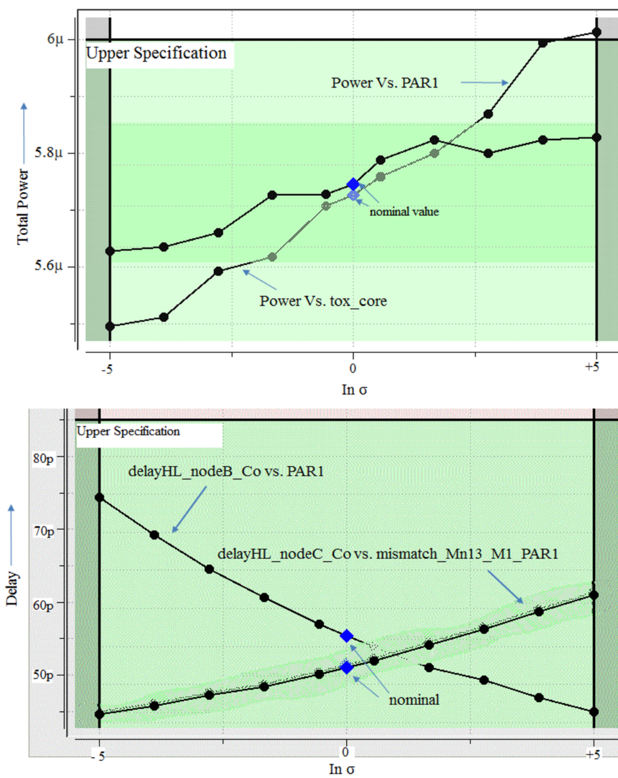


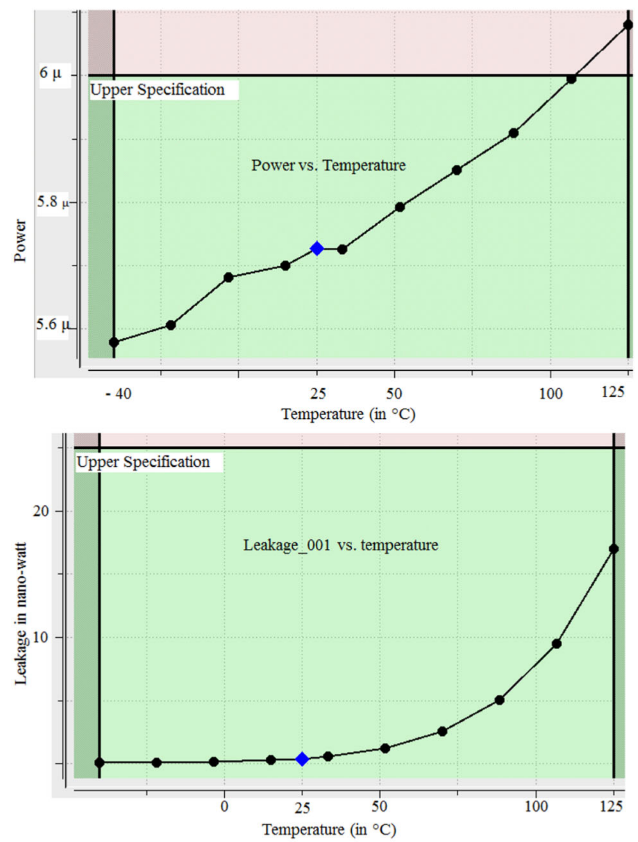
Fig. 2 Impact of statistical variations alone on performances

node B takes the transition from *high to low* and output *node Co*). Obviously, the combined effect of all process variations can be considerably more complex on performances.

The impacts of temperature and supply voltage obtained by SPICE simulations are shown in Fig. 3, referring to the same technology node. The total power (upper plot) and the static power, i.e., leakage (middle plot) exhibits approximately 6 % and 312 % increase, respectively, when the temperature increases to 125 °C. The reported plot is for leakage combination *'ABC* = 001'. Also, the propagation delay (*delayHL_nodeA_Co*, lower plot) increases approx. 17 % at –5 % V_{DD}.

Figure 4 shows the $|\Delta V_T|$ versus time (in years) for DC stress obtained in the target 40-nm pMOS (NBTI degradation) at supply voltage of 1V and 25 °C temperature. ΔV_T is the degradation in threshold voltage over time, which indirectly contributes to the degradation in the device performance.

Figure5a, b shows the impact of NBTI degradation for 3 years' operation on propagation delays of the full-adder cell at nominal and worst-case conditions in temperature and supply voltage. At nominal operating conditions, (temp = 25 °C and supply voltage = 1 V), the delay (e.g., delayHL_nodeB_Co) rises by 9 %, while it rises by 70 % at worst-case operating conditions (temperature −40 °C and supply voltage 0.95 V).



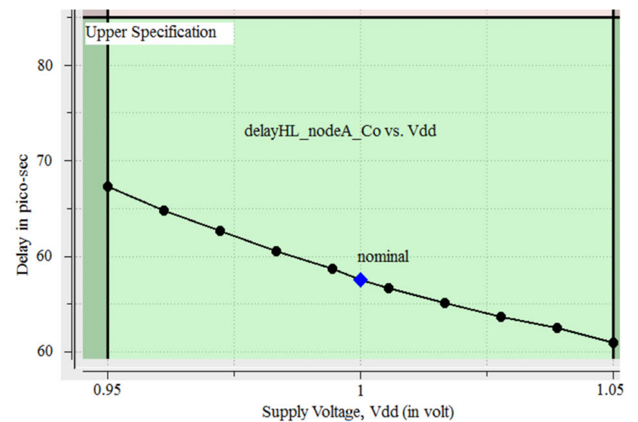


Fig. 3 Impact of operating variation on circuit performances

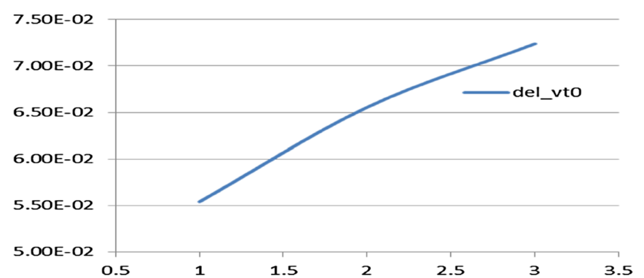


Fig. 4 Del_VT0 versus time (in years)

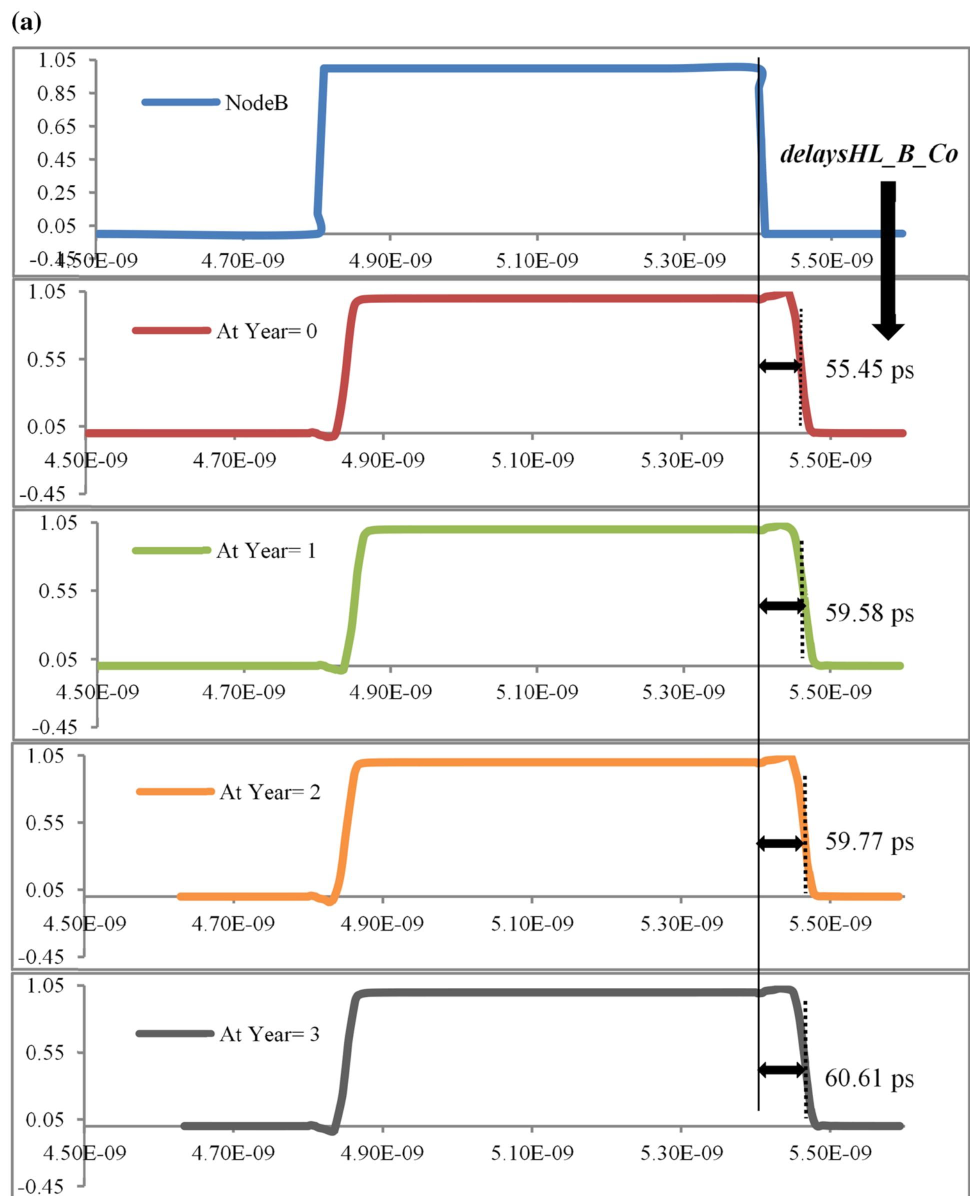


Fig. 5 **a** Impact of NBTI degradation on delay at nominal operating conditions (temp= 25 °C, V_{dd} = 1V, aging = 0 year) **b** Impact of NBTI degradation on delay at worst-case operating conditions (temp= −40 °C, V_{dd} = 0.95 V, aging = 3 year)

The circuit design parameters that we can tune in order to mitigate all the discussed variation impacts are the geometrical sizes of the transistors in the cell. In this respect, Fig. 6 clearly shows that the different performance figures may have similar or contrary dependence on the dimensions of an individual transistor. As an example, different dependences of some *delays* and *power* performances have been shown with the change in the width of $nMOS_3$ (WN3) transistor in predefined bound. Therefore, we should ideally probe the design space to find the optimal sizing of all transistors at which the circuit under test is robust against a whole set of targeted statistical variations, fully functional for operating variations in temperature and supply voltage, and working for the intended life time.

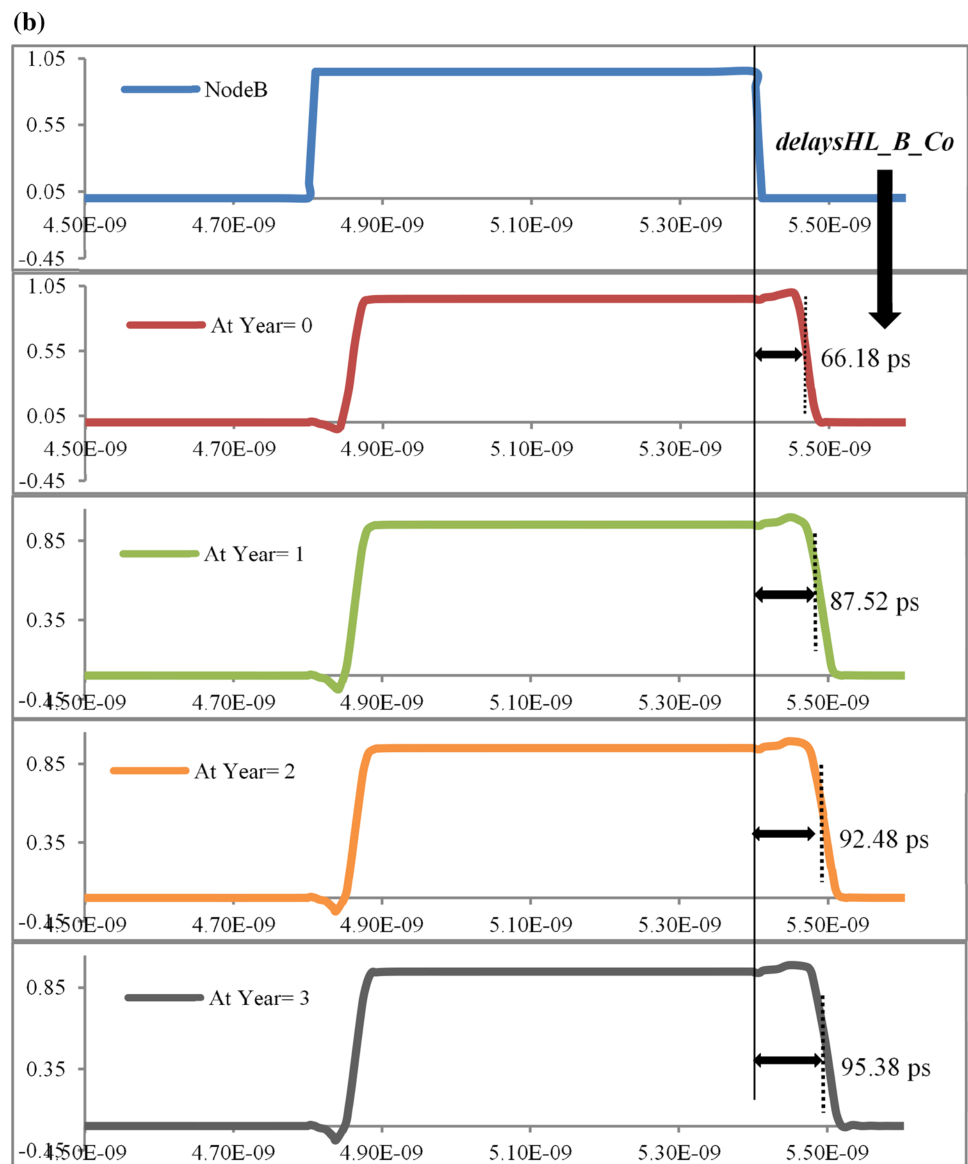
As a consequence of the reported observations, we aim at finding the optimal values of the 56 widths and lengths of the devices in the target cell that maximizes the expected yield (percentage of compliant instances) with respect to a set of performance bounds on total power, static power, and speed, considering local/global process variations, operating variations, and aging degradation.

4 Problem formalization and design goal

4.1 Methodology setup

A primary requisite to perform aging degradation aware circuit sizing and optimization is the possibility of performing transistor- level simulation supporting fresh as well as degraded over time device operation. Our work employs the MOS Reliability Analysis tool (MOSRA) tool within the

Fig. 5 continued



HSPICE simulator [29]. The built-in HSPICE MOSRA tool is divided into prestress analysis (fresh simulations at zero aging time) and poststress analysis, which can be set up for several years with desired intervals of time [13].

Interactive mathematical optimization and verification have been performed using the WiCkeD^{TM} tool, which reduces the expensive design time and efforts needed to maximize the circuit performance and yield [30].

The fabrication process information has been accessed from the 40-nm CMOS low-power standard-threshold-voltage PDK, which includes nominal values as well as statistical variations of each transistor model in the processes.

4.2 Design goal setup

Table 1 reports the full list of performance figures for which the optimization of the target full-adder circuit has been accomplished. Propagation delay refers to a load capacitance equivalent to an inverter cell in the target technology. Table 1 also presents the performance data obtained by SPICE/MOSRA simulation at nominal (col. 2) and worst-case operating (WCO) conditions in supply voltage, temperature, and NBTI aging (col. 3) together.

The reported data indicate that propagation delay (e.g., *Delay_HL_b*) increases by approximately 70 % in WCO conditions. Similarly, leakage power shows several order of increment in WCO. Notably, leakage currents, depend on the device parameters like doping profile, gate oxide thickness, channel dimensions, etc., as well as on temperature, are substantially affected by the values of the logic signals at the input of the cell, and the influence of the process and operating variations can be different for different input combinations [31]. Therefore, the optimization has been carried out for all possible input combinations in the full adder [32].

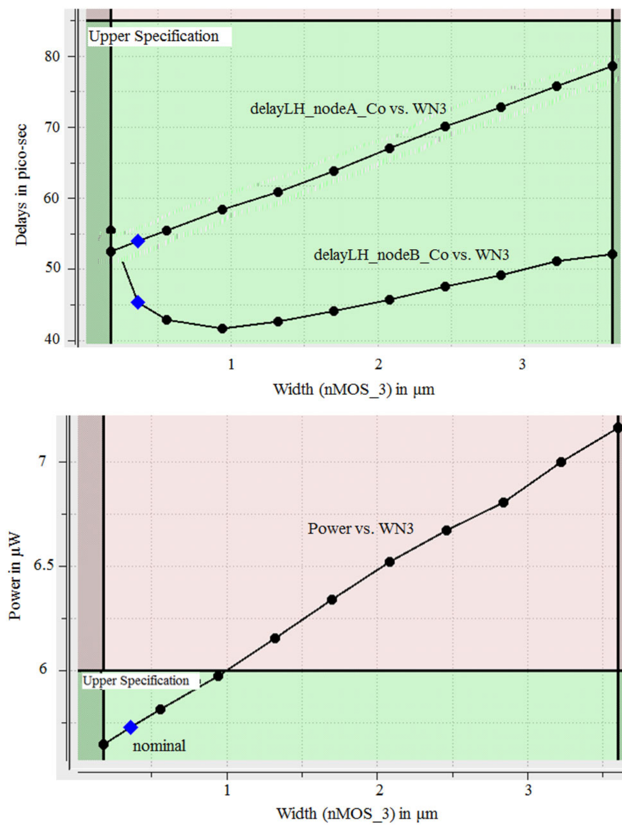


Fig. 6 Transistor dimension (design parameters) dependence on circuit performances

Table 1 Performance figures and their simulated values at nominal and worst-case operating conditions

Performances Figures	Performances values at simulation	
	Nominal (1 V, 25 °C, 0 year)	Worst-case [V, °C, aging years]
Delay_HL_a	57.51 ps	94.20 ps [0.95,0,3]
Delay_HL_b	55.45 ps	95.38 ps [0.95,0,3]
Delay_HL_c	51.20 ps	83.31 ps [0.95,0,3]
Delay_LH_a	54.25 ps	68.45 ps [0.95,0,3]
Delay_LH_b	45.42 ps	62.11 ps [0.95,0,3]
Delay_LH_c	49.15 ps	63.24 ps [0.95,0,3]
Leakage_000	315.83pW	13.62nW [1.05,125,0]
Leakage_001	412.12pW	29.07nW [1.05,125,0]
Leakage_010	379.27pW	23.69nW [1.05,125,0]
Leakage_011	388.08pW	31.95nW [1.05,125,0]
Leakage_100	386.39pW	23.49nW [1.05,125,0]
Leakage_101	373.92pW	28.13nW [1.05,125,0]
Leakage_110	378.92pW	25.54nW [1.05,125,0]
Leakage_111	328.39pW	28.07nW [1.05,125,0]
Total power	5.73uW	6.764uW [1.05,125,0]

4.3 Circuit parameters setup and problem formulation

The circuit behavior is determined by parameters that can be grouped into three different categories, namely design, operating, and process parameters. Operating parameters define the characteristics of the circuit during measurements. Process parameters define them at the time of production. In order to fulfill a particular set of performance bounds, the designer can tune the design parameters, which can be generically represented as a vector $X_d = \left[X_{d,1} X_{d,2}, \ldots, X_{d,nxd}\right]^T \in R^n_{Xd}$, so that the objective of circuit optimization is to calculate the optimal X_d. In CMOS cell design, the channel dimensions (length and width) of nMOS and pMOS devices of the circuit constitute the design parameters, so that in our design case we have a 56 element vector:

$$X_d = [W_{\mathrm{nMOS1}}, W_{\mathrm{nMOS2}}, \ldots, W_{\mathrm{nMOS14}}, L_{\mathrm{nMOS1}}, L_{\mathrm{nMOS2}}, \ldots, L_{\mathrm{nMOS14}}, W_{pMOS1}, W_{\mathrm{pMOS2}}, \ldots, W_{\mathrm{pMOS14}}, L_{\mathrm{pMOS1}}, L_{\mathrm{pMOS2}}, \ldots, L_{\mathrm{pMOS14}}]^T$$

with

$$W_{\mathrm{nMOSi}} \in \{180\mathrm{n} : 3600\mathrm{n}\}, \quad W_{\mathrm{pMOSi}} \in \{180\mathrm{n} : 7200\mathrm{n}\}, \quad L_{\mathrm{nMOSi}}, L_{\mathrm{pMOSi}} \in \{40\mathrm{n} - 180\mathrm{n}\}, i = 1, 2, 3 \ldots 14$$

as per the PDK boundaries. During the optimization process, the design parameter values are tuned with predefined step sizes for lengths and widths on manufacturing grid, set to 2.5 nm and 4 nm, respectively.

Statistical parameters are generically represented by a vector $X_s = \left[X_{s,1} X_{s,2} \ldots X_{s,k} \ldots X_{s,nxd}\right]^T \in R^n_{Xs}$, each element of the vector being a process parameter subjected to statistical variations according to the PDK specification, e.g., $X_s = [t_{ox}, Dxl, Dxw, \ldots \text{etc.}]$. A set of parameters as well as their probability density functions are defined according to the PDK confidential data.

Operating parameters, generically a vector $X_r = \left[X_{r,1} X_{r,2} \ldots X_{r,nxd}\right]^T \in R^n_{Xr}$ are given in a specified range and the circuit must be fully functional as long as the operating parameters are in the given interval. In our

Table 2 Statistical and operating variations

Description		Lower	Initial	Upper
Operating parameters				
V_{DD}	Supply voltage	0.95 V	1 V	1.05 V
Temp	Temperature	−40 °C	25 °C	125 °C
Age	NBTI	0 year	0 year	3 year

Table 3 Optimization at [a]*nominal* and [b]*worst-case* operating conditions

Spec(s) →	{delays, pow} < {65 ps, 6 μW}			{delays, pow} < {75 ps, 6 μW}			{delays, pow} < {85 ps, 6 μW}			{delays, pow} < {90 ps, 6 μW}		
Performances ↓	Leakage <15nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW
Delay_HL_a	40.79p	40.66p	36.08p	47.32p	45.50p	49.65p	56.57p	53.46p	55.06p	58.66p	48.67p	55.20p
	(60.7p)	(61.42p)	(55.76p)	(72.16p)	(68.54p)	(74.4p)	(84.32p)	(80.81p)	(84.11p)	(88.71p)	(73.43p)	(84.07p)
Delay_HL_b	44.01p	57.7p	39.37p	45.10p	48.45p	43.58p	54.21p	55.37p	55.06p	52.54p	58.50p	58.72p
	(66.72p)	(88.67p)	(62.2p)	(70.94p)	(75.53p)	(65.8p)	(84.48p)	(83.88p)	(84.24p)	(80.89p)	(88.85p)	(89.41p)
Delay_HL_c	40.99p	40.58p	38.52p	40.17p	42.54p	32.40p	51.56p	45.46p	48.96p	59.39p	43.65p	47.96p
	(65.21p)	(64.57p)	(61.38p)	(60.99p)	(65.15p)	(47.33p)	(75.36p)	(70.06p)	(75.50p)	(89.91p)	(66.54p)	(72.14p)
Delay_LH_a	52.41p	52.10p	52.37p	60.11p	64.34p	56.45p	56.98p	58.73p	50.96p	66.35p	63.39p	51.96p
	(61.86p)	(62.79p)	(62.43p)	(72.15p)	(74.75p)	(66.4p)	(66.49p)	(69.06p)	(61.41p)	(79.68p)	(74.89p)	(62.42p)
Delay_LH_b	35.44p	33.96p	36.35p	37.46p	31.92p	25.89p	39.89p	37.09p	34.97p	35.84p	38.93p	43.74p
	(47.04p)	(45.04p)	(45.98p)	(48.3p)	(40.94p)	(32.58p)	(50.48p)	(47.53p)	(45.30p)	(44.18p)	(50.63p)	(55.23p)
Delay_LH_c	54.65p	25.66p	38.99p	45.46p	47.28p	32.18p	46.79p	48.85p	41.43p	34.92p	46.79p	47.01p
	(65.42n)	(32.35p)	(46.31p)	(54.46p)	(56.78p)	(38.2p)	(56.22p)	(58.42p)	(50.51p)	(42.55p)	(57.32p)	(56.61p)
Leakage_000	242.8p	264.2p	348.3p	226.5p	302.6p	252.1p	146.9p	190.6p	144.9p	184.7p	204.8p	252.1p
	(5.212n)	(6.576n)	(9.7n)	(5.44n)	(6.544n)	(6.41n)	(3.821n)	(3.954n)	(4.064n)	(4.18n)	(5.14n)	(5.95n)
Leakage_001	261.0p	341.7p	329.2p	227.1p	274.4p	293.9p	150.0p	187.0p	184.5p	208.2p	211.7p	240.9p
	(8.242n)	(12.17n)	(11.43n)	(6.86n)	(10.1n)	(10.53n)	(4.724n)	(6.014n)	(7.048n)	(5.84n)	(6.44n)	(9.4n)
Leakage_010	311.6p	355.0p	445.8p	251.2p	406.3p	293.8p	146.9p	221.6p	186.9p	216.5p	196.7p	270.2p
	(9.76n)	(13.98n)	(14.56n)	(6.66n)	(9.33n)	(9.21n)	(3.884n)	(4.774n)	(6.382n)	(3.98n)	(5.89n)	(7.38n)
Leakage_011	240.7p	248.0p	272.7p	251.6p	313.3p	312.8p	152.4p	205.8p	191.7p	227.3p	192.0p	232.1p
	(9.672n)	(14.48n)	(18.4n)	(11.73n)	(12.92n)	(22.25n)	(6.288n)	(7.643n)	(9.849n)	(7.03n)	(8.24n)	(8.41
Leakage_100	258.7p	368.7p	372.5p	205.0p	267.1p	324.7p	169.1p	193.9p	169.0p	188.7p	199.3p	230.3p
	(7.722n)	(12.11n)	(14.02n)	(7n)	(6.5n)	(8.55n)	(4.215n)	(4.872n)	(5.429n)	(3.90n)	(5.39n)	(6.5n)
Leakage_101	251.0p	306.3p	283.7p	212.8p	263.2p	316.9p	162.8p	179.0p	184.3p	205.4p	206.5p	210.8p
	(11.55n)	(19.94n)	(22.91n)	(14.45n)	(16.93n)	(18.36n)	(5.414n)	(7.942n)	(10.58n)	(8.50n)	(8.23n)	(12.15n)
Leakage_110	265.3p	272.9p	288.3p	257.2p	355.4p	307.5p	190.1p	244.4p	222.8p	247.8p	210.2p	263.6p
	(10.77n)	(19.11n)	(22.54n)	(14.28n)	(14.86n)	(14.97n)	(8.512n)	(8.971n)	(11.27n)	(7.75n)	(10.3n)	(12.9n)
Leakage_111	260.3p	277.2p	265.4p	247.2p	325.9p	283.6p	174.9p	226.1p	206.4p	260.2p	207.9p	244.0p
	(14.03n)	(19.98n)	(20.9n)	(14.27n)	(17.33n)	(15.6n)	(6.563n)	(9.662n)	(6.985n)	(7.84n)	(9.58n)	(16.64n)
Total Power	04.90 μ	5.218 μ	5.067 μ	04.27 μ	04.86 μ	4.269 μ	3.546 μ	4.315 μ	4.115 μ	04.31 μ	04.30 μ	04.16 μ
	(5.787 μ)	(6.141 μ)	(5.987 μ)	(5.032 μ)	(5.73 μ)	(5.046 μ)	(4.163 μ)	(5.077 μ)	(4.806 μ)	(5.13 μ)	(5.06 μ)	(4.9 μ)

[a] Optimization at nominal operating conditions: {temp} = {25 °C}, {V_{DD}} = {1V}, {Aging} = {0 years}, (No statistical variations, No aging, No worst-case operating conditions).
[b] Optimization at full worst-case operating conditions range: {temp} = {−40 °C to 125 °C}, {V_{DD}} = {0.95-1.05V}, {Age} = {0–3 years}, (No statistical variations)—shown in brackets

case study, temperature and supply voltage variations have been specified, so that $X_r = \left[\text{temp}, V_{DD}\right]^T$ with temp $\in$ $\{-40 \text{ to } 125\,°\text{C}\}$ for automotive applications, and $V_{DD} \in$ 0.95–1.05 V, respectively. NBTI degradation has also been formally considered as an operating parameter, so that the optimized full adder must be fully functional for the intended life time. Table 2 summarizes the operating and aging boundaries used in the optimization of the full-adder cell.

5 Optimization methodology

The optimization procedure is a simulation intensive task. To save the amount of the numerical simulation cost, it is reasonable to first optimize the circuit safety margin without including the process variations [23,33]. Thus, the optimization task has been divided into a nominal optimization phase and a subsequent yield optimization assuming process variations.

5.1 Nominal optimization considering worst-case conditions in temperature, supply voltage, and NBTI degradation

Let vector $f = [f_1, f_2, \ldots f_{nf}]$ be the vector of performance figures, with lower bound vector f^L and upper bound vector f^U, respectively, for the desired performance specification. Moreover, if any additional feasibility constraints exist in the circuit, such as geometrical and electrical, such constraints also need to be fulfilled in order to have feasible design. We can always formally represent feasibility constraints as $c\,(X_d) \geq 0$. Therefore, including the constraint fulfillment, the target condition for the nominal operating conditions is as follows:

$$c\,(X_d) \geq 0 \text{ AND } f^L \leq f\,(X_d) \leq f^U. \tag{1}$$

However, the nominal optimization (NO) is intended to achieve the sizing values for design parameters X_d that satisfy (1) in a defined range of operating parameters like temperature, V_{DD}, and/or aging. As the operating parameters are denoted by vector X_r, f will also depend on the operating conditions and the problem specification is

$$c\,(X_d) \geq 0 \text{ AND } f^L \leq f\,(X_d, X_r) \leq f^U,$$
$$X_r^{\text{L}} \leq X_r \leq X_r^{\text{U}}. \tag{2}$$

The ultimate goal of NO is to fulfill/overfulfill each specification as much as possible, for the specified range in operating conditions, in the defined design space. Standard algorithms like sequential quadratic, least square, and parametric distance can be used to search the optimal dimensions of each transistor for NO [33]. The algorithm can be selected by thoughtful inspection over the relation between the performance and design/operating parameters.

5.2 Yield optimization considering statistical variations at worst-case operating conditions

Yield optimization aims at maximizing the number of circuit instances that fulfill the specified performance figures

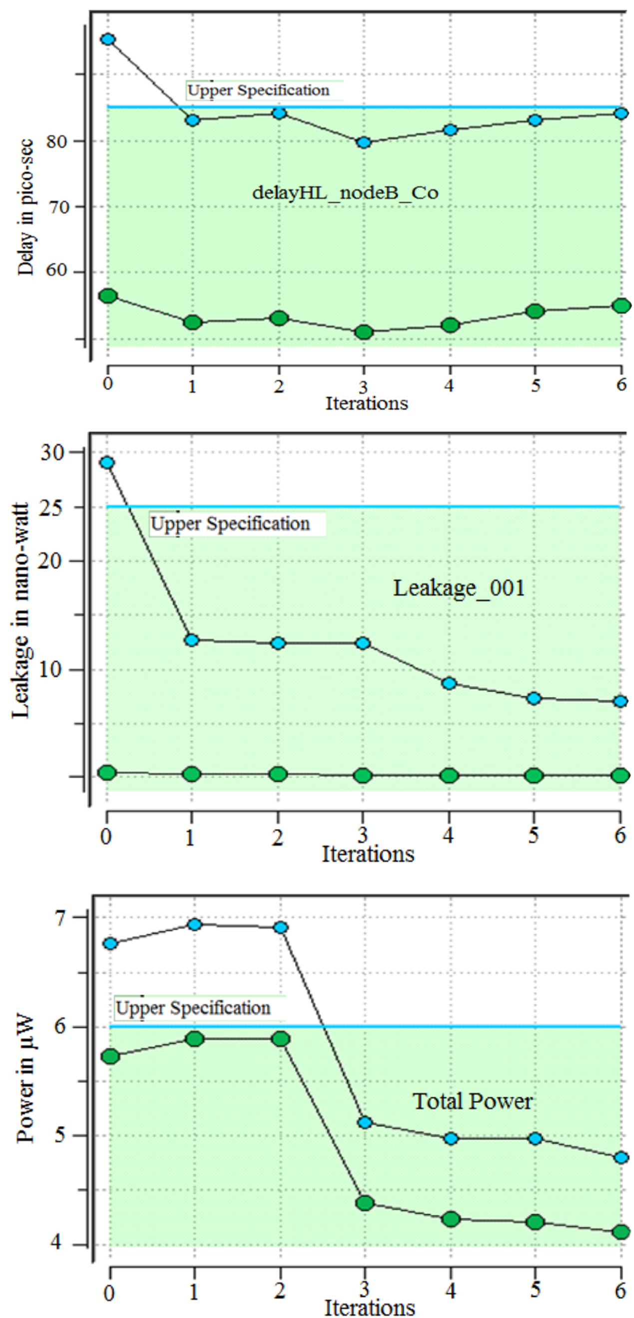


Fig. 7 Progressive fulfillment of violated performances (shown for delays $<$ 85 ps, leakage $<$ 25 nW, and total power $<$ 6 µW specifications)

Table 4 *Yield optimization and ** worst-case distance (WCD) in sigma (σ)

Spec(s)→	{delays, pow} < {65 ps, 6 µW}			{delays, pow} < {75 ps, 6 µW}			{delays, pow} < {85 ps, 6 µW}			{delays, pow} < {90 ps, 6 µW}		
Performances ↓	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW
Delay_HL_a	41.89p	38.60p	39.56p	44.57p	41.99p	42.38p	45.97p	42.66p	41.41p	48.08p	44.12p	42.4p
	(0.406)	(1.357)	(1.021)	(1.428)	(2.072)	(1.599)	(2.452)	(2.89)	(3.08)	(2.70)	(3.76)	(3.38)
Delay_HL_b	39.93p	38.11p	37.68p	43.24p	44.44p	42.51p	45.60p	41.94p	41.70p	48.63p	40.44p	43.68p
	(1.013)	(1.191)	(1.244)	(1.455)	(1.106)	(1.592)	(2.392)	(3.05)	(3.05)	(2.41)	(3.91)	(3.93)
Delay_HL_c	39.93p	35.98p	35.80p	40.58p	41.75p	35.75p	40.95p	37.71p	39.30p	47.83p	39.70p	39.81p
	(0.766)	(1.514)	(1.773)	(1.879)	(1.540)	(2.929)	(3.051)	(3.35)	(3.61)	(2.40)	(4.16)	(3.52)
Delay_LH_a	47.23p	48.95p	45.83p	54.8p	52.12p	48.17p	55.56p	54.14p	48.25p	59.33p	52.74p	49.25p
	(1.333)	(1.129)	(1.949)	(1.876)	(1.996)	(2.497)	(2.915)	(3.45)	(4.32)	(2.82)	(3.54)	(3.57)
Delay_LH_b	36.87p	38.1p	38.03p	39.62p	37.16p	28.77p	45.60p	40.62p	39.83p	36.66p	42.40p	43.82p
	(2.557)	(2.255)	(2.759)	(3.353)	(4.671)	(5.883)	(3.516)	(4.23)	(4.11)	(6.10)	(4.79)	(3.94)
Delay_LH_c	47.1p	41.6p	41.01p	45.18p	47.17p	41.22p	52.87p	51.67p	44.25p	39.26p	54.52p	49.18p
	(1.239)	(2.462)	(2.893)	(3.193)	(3.272)	(3.758)	(3.326)	(4.04)	(4.32)	(5.80)	(3.42)	(3.80)
Leakage_000	228.13p	262.77p	254.5p	208.8p	254.58p	225.1p	151.5p	198.1p	224.3p	180.66p	208p	243.62p
	(2.886)	(3.604)	(4.111)	(3.548)	(3.850)	(3.649)	(3.966)	(4.34)	(4.18)	(3.88)	(4.16)	(4.61)
Leakage_001	237.1p	290.75p	280.7p	220.7p	260.1p	260.9p	147.16p	194.5p	235.56p	199.78p	215.7p	233.34p
	(2.250)	(2.708)	(3.313)	(2.395)	(3.400)	(2.938)	(3.366)	(3.68)	(3.69)	(3.20)	(3.80)	(3.73)
Leakage_010	259.95p	279.3p	291.8p	227.7p	308.24p	268.2p	154.79p	229.2p	286.23p	224.51p	186p	287.53p
	(2.064)	(2.381)	(3.068)	(2.262)	(3.092)	(3.074)	(2.859)	(3.49)	(3.48)	(3.84)	(3.82)	(3.48)
Leakage_011	215.74p	214.11p	222.5p	210.9p	260.7p	192.9p	141.21p	205.2p	251.2p	215.5p	182.3p	223.32p
	(1.592)	(1.754)	(2.462)	(1.804)	(3.612)	(2.897)	(2.905)	(3.67)	(3.68)	(3.10)	(3.32)	(3.77)
Leakage_100	263.44p	279.3p	294.7p	167.1p	204.42p	259.5p	156.83p	192.3p	208.6p	177.58p	229.2p	206.46p
	(1.951)	(2.349)	(2.984)	(2.765)	(3.651)	(3.089)	(3.793)	(3.52)	(3.54)	(4.04)	(3.43)	(4.08)
Leakage_101	231.83p	234.75p	241.5p	170.8p	191.57p	199.8p	158.93p	169.6p	199.5p	176.94p	216.4p	185.02p
	(1.461)	(1.884)	(2.502)	(1.901)	(3.101)	(3.098)	(2.766)	(3.49)	(3.52)	(3.10)	(3.83)	(3.46)
Leakage_110	245.26p	207.9p	247.8p	200.5p	274.2p	237.4p	172.44p	220.2p	281.87p	240.1p	229.5p	247.3p
	(1.593)	(1.996)	(2.213)	(1.722)	(2.089)	(3.578)	(2.929)	(3.11)	(3.22)	(2.81)	(3.13)	(3.42)
Leakage_111	231.76p	204.1p	243.2p	190.1p	266.14p	206.4p	159.82p	200.2p	271.01p	235.28p	226p	222.03p
	(1.650)	(2.327)	(2.572)	(1.755)	(2.766)	(3.161)	(3.321)	(4.24)	(4.23)	(3.19)	(3.70)	(3.62)
Total power	4.098 µ	4.05 µ	4.366 µ	4.16 µ	4.529 µ	3.532 µ	3.484 µ	3.943 µ	4.17 µ	3.95 µ	4.32 µ	4.09 µ
	(5.380)	(5.255)	(5.602)	(5.454)	(5.891)	(4.568)	(4.50)	(5.49)	(5.45)	(5.13)	(5.68)	(5.37)

* Yield Optimization at full worst-case operating conditions range {temp} = {−40 to 125 °C}, {V_{DD}} = {0.95–1.05 V}, {Age} = {0–3 years} including all local and global process variations

** Worst-case distance (WCD) in sigma for all performance figures in all combinations of specifications. Shown in brackets

Table 5 Estimated Yield (in %) of each performance figure in all combinations of specifications

Spec(s)→	Worst-Case Distance (WCD) in sigma (σ)											
	{delays, pow} < {65 ps, 6 µW}			{delays, pow} < {75 ps, 6 µW}			{delays, pow} < {85 ps, 6 µW}			{delays, pow} < {90 ps, 6 µW}		
Performances ↓	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW	Leakage <15 nW	Leakage <20 nW	Leakage <25 nW
Delay_HL_a	65.53	91.47	84.70	92.18	98.17	94.61	99.38	99.81	99.95	99.65	99.99	99.96
Delay_HL_b	84.22	88.16	89.31	92.94	86.23	94.38	99.11	99.87	100	99.14	99.98	99.99
Delay_HL_c	78.01	93.39	95.85	97	93.8	99.81	99.87	99.96	99.98	99.11	100	99.98
Delay_LH_a	90.83	86.89	97.50	96.99	97.7	99.4	99.86	99.99	100	99.7	99.97	100
Delay_LH_b	99.49	98.66	99.69	99.98	100	100	99.99	100	100	100	100	100
Delay_LH_c	88.74	99.32	99.79	99.91	99.97	100	99.96	100	100	100	99.99	100
Leakage_000	99.86	99.98	100	99.98	99.98	99.97	99.99	100	100	99.99	100	100
Leakage_001	98.89	99.71	99.97	99.22	99.99	99.88	99.99	99.99	99.99	99.97	99.99	99.99
Leakage_010	98.01	99.08	99.94	98.69	99.94	99.89	99.85	99.99	99.99	99.99	99.99	99.99
Leakage_011	94.28	96.16	99.37	96.54	99.55	99.83	99.85	99.98	99.88	99.94	99.97	99.99
Leakage_100	97.36	99.10	99.9	99.72	99.99	99.94	99.99	99.99	99.99	99.99	99.97	99.99
Leakage_101	92.82	97.02	99.4	97.17	99.89	99.88	99.69	99.98	99.98	99.90	99.99	99.98
Leakage_110	94.4	97.76	98.65	95.79	98.17	99.63	99.93	99.98	99.99	99.81	99.96	99.99
Leakage_111	95.0	99.05	99.53	96.05	99.78	99.96	99.97	99.99	99.97	99.98	99.99	99.99
Total power	100	100	100	100	100	100	100	100	100	100	100	100
Total Yield	46.3	69.55	78.2	80.6	81.88	90.19	97.99	99.69	99.81	99.04	99.79	99.92

and design constraints, which is equivalent to maximizing design robustness to process variations. Without loss of generality, here we consider each individual specification denoted as a lower bound $f_i(X_s, X_d) \geq b_i$. Here, all variable process parameters are collected in vector X_s, while X_d is the vector of design parameters as before. Therefore, the region of process parameter values that fulfill a particular specification 'i' can be defined as follows (for lower bound):

$$A_i(X_d) = \{X_s | f_i(X_s, X_d) \geq b_i\} \quad (3)$$

The parametric yield Y_i is the percentage of circuit that fulfills specification 'i' and can be formally expressed as the probability that the process parameter values fall in the above defined area

$$Y_i(X_d) = int_{A_i(X_d)} |2\pi C|^{-\frac{1}{2}} \times \exp(-\frac{1}{2}(X_s - X_{s0})^T C^{-1}(X_s - X_{s0})\,ds \quad (4)$$

The argument of the integral is the probability density function of the multi-normal distribution. Ultimately, the set of process parameter vectors that fulfill all the specifications in the acceptance region can be represented as follows:

$$A(d) = \bigcap_i A_i(X_d) \quad (5)$$

and the definition of yield can be extended accordingly.

According to a typical Monte Carlo approach, statistical process variations can be modeled by generating a vector of N random samples of the process parameter vector X_s, namely $X_s(1), \ldots X_s(N)$, thus generating a matrix of N columns each corresponding to an instance of the process parameter vector. The N instances of the circuit design so generated are simulated in SPICE yielding N performance result vectors $f(k) = f(X_d, X_r, X_s(k))$, $k = 1 \ldots\ldots N$. The parametric yield Y is estimated as the percentage of samples that dwell within the specification bounds $f^L \leq f(k) \leq f^U$.

The yield maximization algorithm concentrates on the computation of the worst-case distance (WCD) [33–35]. WCD can be considered as a reference to measure the robustness of a design. The WCD value (β_{wc}) represents the robustness as the distance between the worst-case point and the mean values of performance. Intuitively, if the process conditions causing violations are close to the mean value, then there will be severe parametric yield loss. Therefore, an important measure for the robustness of circuit performance $f_i(X_s, X_d)$ is the worst-case distance $\beta_{\mathrm{wc}}^{(i)}$, which is the shortest distance, measured as multiples of the standard deviation (σ) of the particular performance, between the mean value of X_s and any process condition that causes $f_i(X_d, X_r, X_s)$ to fall outside the required boundaries. The worst-case distance is a function of the design parameters X_d and it is the goal function to maximize over X_d, thereby achieving a design centered in the process parameter space with respect to the specification bounds [30,33].

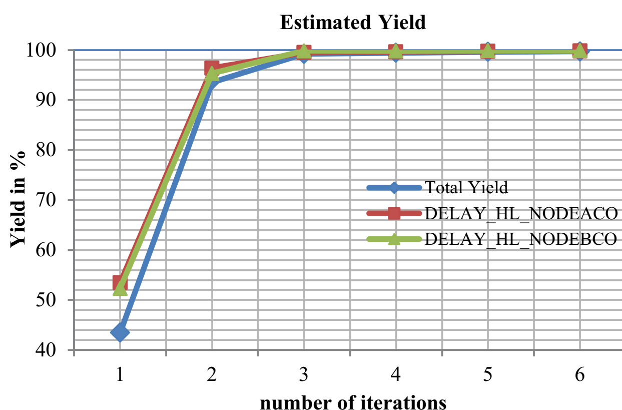


Fig. 8 Progressive yield improvement (specification case: delays < 85 ps, leakage < 25 nW, and total power <6 µW)

6 Circuit sizing and optimization results of full-adder design

6.1 Target performance specification bounds

We carried out the sizing and optimization of the targeted CMOS full- adder circuit for 12 different specifications sets referring to delay and power performance. In order to obtain the robust full- adder design for maximum achievable performance setup, the specifications for 'delays' and 'leakage power' are relaxed as follows:

- <65 ps, <75 ps, <85 ps and <90 ps.
- <15 nW to <25 nW with the step of 5 nW, respectively.

The specification for total power dissipation are always set to < 6 µW. It is evident from Table 1 that at worst-case operating conditions, still at nominal process conditions, the leakage as well as delays performances goes out of the specification bounds. Even for the most relaxed specification bounds {delays < 90 ps, leakage < 25nW, total power < 6 µW}, the delays (*delay_HL_a, delay_HL_b*), the leakage (combinations 001,011, 101, 110, and 111), and the total power go out of specification bounds. In fact, the scenario is more worse for other tighten specification bounds. This violation of the specifications may lead to failure of the circuit operation.

Table 6 Circuit sizing (in nm)

Design Parameters	Initial Sizing	{del, leak, Pow} <{65p, 15n, 6µ}	{del, leak, pow} <{65p, 20n, 6µ}	{del, leak, pow} <{65p, 255n, 6µ}	{del, leak, Pow} <{75p, 15n, 6µ}	{del, leak, pow} <{75p, 20n, 6µ}	{del, leak, pow} <{75p, 25n, 6µ}	{del, leak, Pow} <{85p, 15n, 6µ}	{del, leak, pow} <{85p, 20n, 6µ}	{del, leak, pow} <{85p, 25n, 6µ}	{del, leak, Pow} <{90p, 15n, 6µ}	{del, leak, pow} <{90p, 20n, 6µ}	{del, leak, pow} <{90p, 25n, 6μ}
$(W/L)_{nMOS1}$	360/45	372/60	500/84	876/88	360/80	468/88	380/78	268/96	520/66	608/76	1304/58	496/180	420 /94
$(W/L)_{nMOS2}$	360/45	312/44	280/42	440/70	268/48	640/72	840/50	196/60	508/86	472/54	860/76	496/74	260 /52
$(W/L)_{nMOS3}$	360/45	184/48	268/48	316/54	216/58	212/80	244/54	180/74	188/60	184/50	284/54	184/74	184 /54
$(W/L)_{nMOS4}$	360/45	212/42	256/42	356/44	212/68	272/50	204/46	188/68	248/62	212/44	240/62	260/40	200 /46
$(W/L)_{nMOS5}$	360/45	540/44	700/44	924/46	576/54	588/44	588/50	404/52	576/48	460/48	492/54	676/74	492 /44
$(W/L)_{nMOS6}$	360/45	340/146	524/102	368/66	192/112	204/84	212/158	248/142	224/134	208/134	280/68	252/52	220 /106
$(W/L)_{nMOS7}$	360/45	492/124	192/66	256/92	520/70	1040/114	188/152	436/64	512/52	1596/76	752/158	560/74	532 /96
$(W/L)_{nMOS8}$	360/45	184/152	580/66	396/54	212/58	196/132	196/128	184/84	224/70	248/138	192/128	236/114	240 /120
$(W/L)_{nMOS9}$	360/45	184/54	192/56	196/56	196/52	196/52	188/52	180/56	184/50	184/60	184/58	180/74	184 /46
$(W/L)_{nMOS10}$	540/45	944/136	212/108	232/136	216/52	416/74	308/116	484/72	380/62	436/66	212/76	288/66	240 /114
$(W/L)_{nMOS11}$	540/45	276/98	324/126	272/112	584/62	244/130	356/62	340/62	276/58	1760/64	340/64	468/160	932 /70
$(W/L)_{nMOS12}$	540/45	228/56	208/56	408/76	384/84	684/116	228/66	184/56	276/108	268/64	200/58	284/80	308 /56
$(W/L)_{nMOS13}$	360/45	184/60	208/68	200/64	196/70	196/74	188/50	180/62	188/58	188/54	184/64	192/54	188 /58
$(W/L)_{nMOS14}$	360/45	572/66	192/64	208/54	464/112	204/142	188/78	200/66	212/68	228/80	192/60	240/86	448 /68
$(W/L)_{pMOS1}$	720/45	1576/64	2240/62	2448/60	1836/76	2404/66	1752/56	1072/68	1564/74	1064/50	1456/78	2064/76	1424/58
$(W/L)_{pMOS2}$	720/45	796/132	1100/130	1320/100	696/74	872/116	1132/82	912/168	960/110	764/88	832/118	1008/94	980 /96
$(W/L)_{pMOS3}$	720/45	384/54	556/52	840/60	420/56	472/58	348/52	432/64	608/68	484/58	584/76	584/86	380 /54
$(W/L)_{pMOS4}$	720/45	2868/116	2604/88	2824/76	1640/90	1684/102	3020/90	1692/104	1908/100	1544/90	2116/136	1360/88	1480/94
$(W/L)_{pMOS5}$	720/45	336/60	400/50	624/54	352/58	500/60	316/48	332/70	500/68	464/64	712/84	576/62	496 /104
$(W/L)_{pMOS6}$	720/45	912/148	336/122	736/58	2700/136	2616/140	224/66	188/98	944/106	2936/134	776/130	728/180	3760/158
$(W/L)_{pMOS7}$	720/45	1512/116	2436/120	2020/96	348/84	1456/158	1084/112	664/158	328/140	364/126	628/144	2384/136	780 /150
$(W/L)_{pMOS8}$	720/45	860/84	1208/82	864/108	508/162	1512/150	2496/88	512/106	2160/116	416/158	716/130	360/126	2944/162
$(W/L)_{pMOS9}$	720/45	192/48	220/48	240/46	220/48	220/52	212/42	184/62	192/46	196/44	192/76	180/56	184 /46
$(W/L)_{pMOS10}$	1080/45	528/80	2224/130	1524/116	388/94	332/78	232/154	224/128	664/110	1072/106	276/152	460/136	288 /118
$(W/L)_{pMOS11}$	1080/45	204/140	872/114	300/98	700/76	312/130	312/150	228/54	432/98	484/78	268/138	456/94	500 /74
$(W/L)_{pMOS12}$	1080/45	524/132	256/68	384/80	480/94	680/108	308/124	620/106	468/102	504/98	276/100	480/164	328 /68
$(W/L)_{pMOS13}$	720/45	192/44	220/44	240/44	220/46	220/46	212/42	184/48	192/50	196/46	192/50	180/50	184 /46
$(W/L)_{pMOS14}$	720/45	200/70	236/120	244/78	220/108	244/148	212/98	192/150	284/146	376/126	212/154	344/168	356 /130

6.2 Nominal optimization results

Table 3 reports the optimization results at nominal operating conditions (temp = 25 °C, VDD = 1 V, Aging = 0 years), and for the full range of worst-case operating conditions; {temp} = {–40 to 125 °C}, {VDD–} = {0.95–1.05 V}, {Age} = {0–3 years} for the 12 different specification bounds (each column in the tables refers to one of the 12 specification sets). The two optimizations have been carried out simultaneously, and the worst-case optimized values have been placed in brackets in the same table. The impact of process variations has not been considered at this optimization step.

Figure 7 shows the progressive fulfillment of the initially violated specifications (e.g., delays < 85 ps, leakage < 25 nW, and total power $< 6\,\mu$W) due to worst-case conditions in temperature, supply voltage, and NBTI degradation, obtained through the optimization iterations. The green area represents the specification bounds. The green and sky-blue iterations represent the optimization at 'nominal' and 'worst-case' operating conditions, respectively.

6.3 Yield optimization results

Table 4 displays the performance data obtained after yield optimization as well as WCD (in sigma units) values including process variations for the complete range of worst-case operating conditions for the 12 different specification bounds. The WCD values are reported in brackets. Table 5 reports the estimated yield (in %), respectively, for the 12 specification bounds of targeted performance figures of power and delays.

Figure 8 shows the iteration-wise progressive total yield improvement from 41.2 % (initial) to 99.71 % in the full adder for the specification bounds of delays < 85 ps, leakage < 25 nW, and total power $< 6\,\mu$W. The figure also represents the yield improvement in some performance figures (initially very low yield), e.g., *delay_HL_nodeACo* and *delay_HL_nodeBCo*. At this estimated yield, the full adder will be robust against process variations (local and global), operating variations, and NBTI degradation.

Table 6 depicts the initial sizing of each transistor in the full adder, and the final sizing obtained yield optimizations at which the circuit will be fully robust against all statistical variations, fully functional against operating fluctuations in temperature and supply voltage and operational for intended life time. It is very important to note that the resulting optimal sizing is absolutely not intuitive with respect to by-hand cell design optimization.

7 Validation through Monte Carlo analysis

Monte Carlo analysis is one of the standard methods for estimating the distributions of performance measures. We used Monte Carlo analysis in order to verify the correctness of the estimated yield. In Monte Carlo analysis, process parameters varied in random manner and the design is simulated for many different values of process parameters. The Monte Carlo analysis has been performed with 1000 random samples and operating condition set to worst case. The results of the yield optimization estimated through worst-case distance are summarized in Table 7, along with the postoptimization Monte Carlo yield prediction for validation.

Figure 9 shows a graphical view of the Monte Carlo results by means of scatter plots for the full 1000 sample data and the corresponding performance distributions for the leakage and delay performance figures. For the obvious reason of space, only the worst-case combinations of leakage (011),

Table 7 Yield optimization results and verification through Monte Carlo simulation

Specification bound [delay, leakage, power]	Initialyield	Estimated yield after optimization	Predicted yield through Monte Carlo simulation
[65 ps, 15 nW, 6 μW]	3.66	46.32	41.67
[65 ps, 20 nW, 6 μW]	5.62	69.55	65.78
[65 ps, 25 nW, 6 μW]	13.3	78.24	75.44
[75 ps, 15 nW, 6 μW]	10.19	80.62	79.91
[75 ps, 20 nW, 6 μW]	18.99	81.88	79.48
[75 ps, 25 nW, 6 μW]	20.78	90.19	92.71
[85 ps, 15 nW, 6 μW]	43.18	97.99	97.66
[85 ps, 20 nW, 6 μW]	43.32	99.69	99.31
[85 ps, 25 nW, 6 μW]	43.47	99.81	99.82
[90 ps, 15 nW, 6 μW]	46.64	99.04	98.86
[90 ps, 20 nW, 6 μW]	48.11	99.79	99.84
[90 ps, 25 nW, 6 μW]	46.41	99.92	99.94

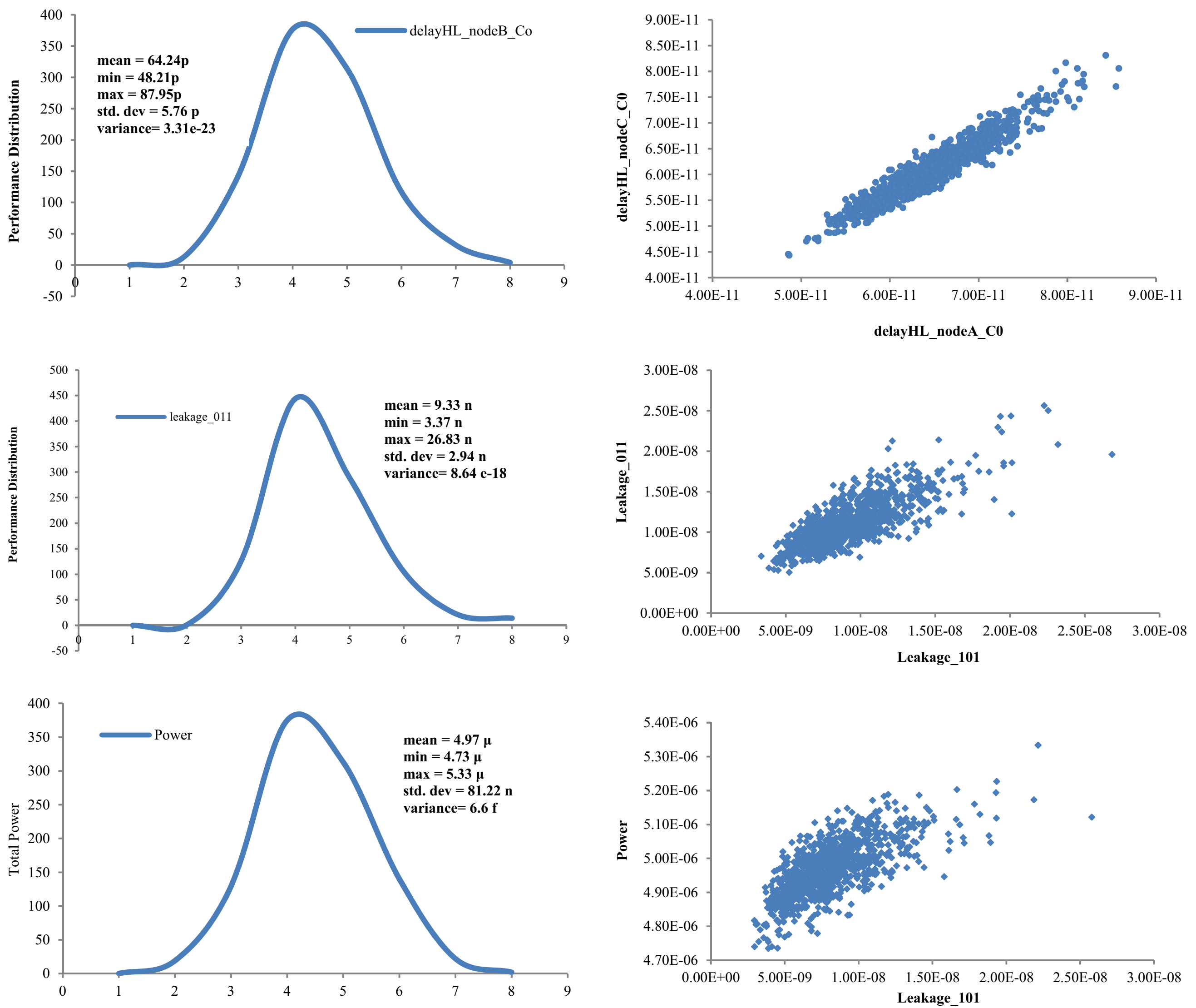


Fig. 9 Performance distribution and scatter plots for initially violated performances

delay (*delayHL_nodeB_Co*), and power have been shown. The plots refer to the leakage and delay combinations which were initially violated, for the specification case [delays < 85ps, leakage < 25 nW, and total power < 6 µW]. We can see all performances are in bounds for random variations in process parameters, while operating conditions are set to worst case. Very few samples may actually lie out of bound as the yield is not 100 % for all performances; since we are reporting a 99.8 % yield design, therefore, 2 out of 1000 samples may be out of bound.

8 Conclusion

The application of a mathematical optimization methodology to the circuit design of a full-adder cell for automotive application specifications proved to be an effective way of improving the expected yield for 12 different cases of specification bounds. The obtained circuit sizing cannot be figured out by conventional manual optimization of digital cell design. Future work will focus on the application of the methodology to even more extensive performance figure set like noise margins and robustness to cross-talk phenomena.

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