TOPOLOGIES AND DESIGN METHODOLOGIES FOR HIGH PRECISION ANALOG PROCESSING BLOCKS IN SHORT-CHANNEL TECHNOLOGIES

by

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Summary

Introduction

The research I carried out as a candidate for the Research Doctorate in Electronic Engineering (PhD) at the University of Rome "La Sapienza" has been focused on the "Topologies and design methodologies for high precision analog processing blocks in short-channel technologies" .

With the explosive growth of battery-powered portable devices, power reduction in integrated circuits has become a major problem. In many of these portable systems the signal is processed in the digital domain by limiting the role of the analog part to interface circuits between analogous physical quantities and digital processing.

Having analog circuits operating at the same voltage as the digital ones means that I can integrate on the same chip front-end and digital processing functions without the need for additional interface circuits, reducing the overall cost of the system. Another reason that pushes to low supply voltages is given by technological considerations, for sub micrometric channel lengths the thickness of gate oxide becomes so slim that it has been forced to reduce the supply voltage to avoid effects like breakdown of the oxide of gate. With the reduction of the supply voltage there is a consequent reduction in the dynamic of the input signal. To maintain the same dynamic range with a lower power supply voltage, the thermal noise in the circuit must also be proportionally reduced. Therefore capacitors used in the circuit must be increased to lower the KT/C noise. Therefore, for operational amplifiers that have the task of driving larger loads and for high resolution applications, doing it becomes even more difficult. There is, however, a compromise between noise and energy consumption. Because of this strong compromise, under certain conditions, energy consumption will actually increase in proportion to the decrease in power supply [1].

Another aspect that poses a significant problem to the reduction of consumption is the fact that battery technology is currently progressing at a much slower pace than that of electronic circuits. Nowadays, many electronic systems work with the power supplied by batteries alone, in some cases this problem is the most critical feature of the device, just think of networks of wireless sensors or implantable devices in the human body.

There are also many switched-capacitor applications that require fast signal transitions and certain performance in given times. If I use a class A amplifier it would always be on even in the times when it is not necessary, which leads to considerable consumption. In this context, a possible solution can be represented by class AB transconductance amplifiers (OTA), which have the advantage of consuming a small current in quiescent condition and providing a large peak current when a large signal is applied. This peculiarity can be exploited to achieve fast settling times with low average power consumption. In many applications, such as active filters, Sample and Hold Amplifiers (SHA), pipeline ADCs, the use of fully differential amplifiers is required to exploit the advantages offered by differential signals, such as doubled dynamic range compared with that provided by a given voltage generator, low sensitivity to common mode disturbances and even order harmonics suppression. Various ways of achieving class AB OTAs are proposed in the literature. In all fully differential type implementations, there is a need for auxiliary circuits for controlling common mode output voltage (CMFB). These additional circuits introduce into the project additional constraints and static power consumption compared to the basic topologies of class AB amplifiers.

This line of research has driven me to focus on two main topics, closely related to the aforementioned issues:

- Low-voltage and Very-low-voltage design of Class AB OTAs blocks for S/H;
- Study of a behavioral modeling of Class AB OTAs;

This work is divided into five chapters.

Chapter 1 is an introduction to the state of the art of Class-AB OTAs. From the assessment of the state of the art there will emerge various ways to realize class-AB "OTAs" but only those that comply with certain constraints will be taken into consideration. The topologies chosen and on which the studies will be conducted will be those that will show the best performance in terms of power consumption, and that are implemented in according to the symmetrical current mirror OTAs.

Chapter 2 is an introduction to figures of merit (FOMs) that will be used to characterize OTAs from a performance point of view. Also in chapter 2 the study and comparison of four topologies emerged from the state of the art evaluation will be conducted. These topologies will be compared from the point of view of consumption and performance of both small and large signal using the FOMs. From the comparison the one will be selected that has the best performances from the point of view of power consumption, bandwidth and large signal behavior. This topology that is preferred over the other choices will be shown to have a performance limit linked to the low value of the CMRR.

Chapter 3 regards the improvement of the performance of the topology chosen to make it the most performing of the state of the art. Three possible methods will be proposed to increase the CMRR of the structure with little impact on consumption but without altering the low signal performance. The first two will be based on open loop techniques while the latter on a closed loop technique.

Chapter 4 regards the design of other topologies with the aim of improving their performance.

Chapter 5 regards behavioral modeling of a class AB OTA. Given that there are no guidelines in the literature on how to design class AB OTAs, a model will be proposed in this chapter, in its alpha phase, with the intent to understand how some parameters are linked to the settling time in similar way as to how is done for class A amplifier.

Chapter 1

Class AB architectures of Operational transconductance amplifiers

This chapter discusses some topologies chosen from the literature because they are considered useful in order to provide basic knowledge that is essential for the development of this thesis.
In literature there are various ways to make class AB stages. A first possibility is represented by a differential input stage operating in class A with the output stage in class AB.
Another possibility is represented by topologies that enhance the slew rate. These topologies work in class A and, when certain limits are exceeded, they give an extra boost in terms of current to allow fast switching overcoming the slew rate limit.
Another possibility is represented by stages completely in class AB. To realize these structures an input transconductor in class AB is needed. Can be exploited the nonlinear current mirrors (NLCMs) or local common mode feedback (LCMFB) to have the nonlinear link between input voltage and gain.
From the literature three possible ways have emerged to realize the input transconductor:
1-With cross-coupled pair (Castello [2]) and its variants.
2-With a differential pair in which the tail current generator is variable (Klinkee [3], Degruwe [4], Ramirez FVF [5], Baswa WTA [6])
3- The third way I call it "buffered" because it uses a buffer to apply a signal opposite the gate to the source (Peluso [7], Baswa [8]).
Once chosen how to make the input transconductor, there are several ways to complete the OTA.
I can complete it by doing a symmetrical OTA where the lower part is made up of constant current sources or variable current sources (see Fig.2.1).
I can complete it either by making a two-stage OTA (Local CMFB, Non Linear Current Mirror), or a folded-cascode.
The class AB stage can greatly improve the speed and dissipation trade off in analog circuits, especially those made with the SC (switched capacitor) technique.
As seen above there are various ways of achieving class AB OTAs, and in this chapter I illustrate and examine it from the point of view of the operating principle. First, however, I will illustrate the operation of some nonlinear current mirrors (NLCM) needed in some topologies to increase the output current in nonlinear manner than the one that would provide a simple mirror.

1 Not Linear Current Mirror (NLCM) [9]

A fundamental element, which is used by different authors, to obtain a class-AB behavior of the input transconductor consists of a non-linear current mirror (NLCM). The most common ways to do a NLCM are represented in "Fig.1.1" also because given their topology they are better suited for use in low voltage applications. In this section will be conducted the study of NLCM proposed in "Fig.1.1".

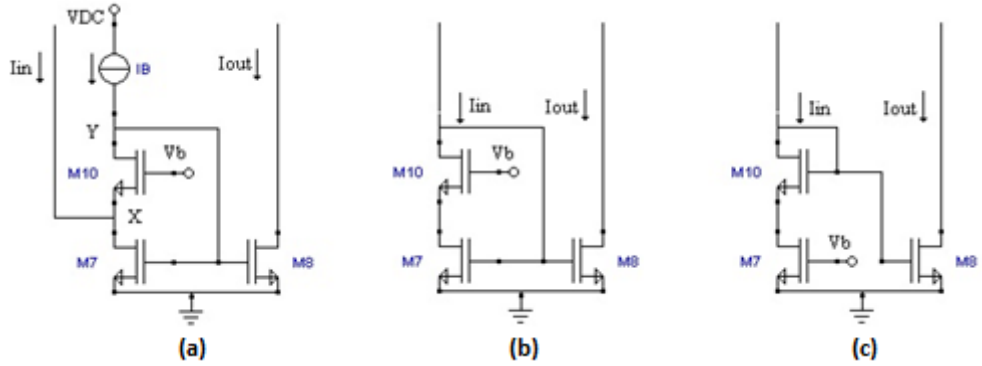


Fig.1. 1: (a) First nonlinear current mirror proposal, (b) second nonlinear current mirror proposal, (c) third proposed current mirror not linear

1.1 Not Linear Current Mirror based on Flipped Voltage Follower Current Source (FVFCS)

Current mirrors can be implemented using the scheme called FVF current sensor (FVFCS) [10], [11]. Considering node X in Fig.1.1(a) as the current detection node of input and that all transistors work in the saturation region. Because of the feedback, the impedance at node X is very low and in this way the current flowing through this node does not substantially change the voltage to node X, which is therefore able to absorb large input current variations and FVF translates them into compression voltage variations at the output node Y. This voltage can be used to generate scaled upstream input replicas via the M_8 transistor.

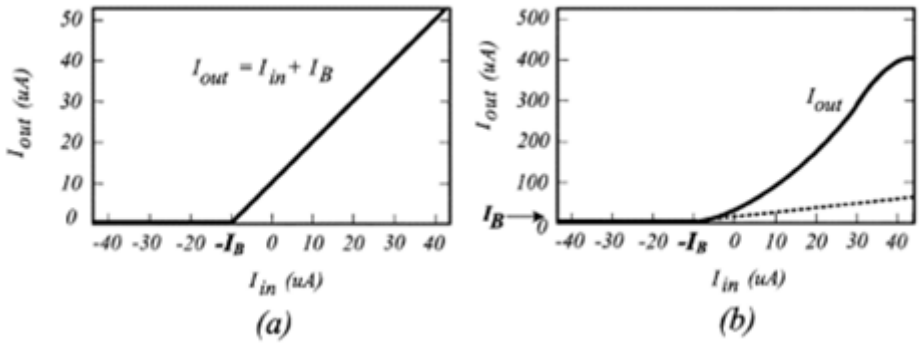


Fig.1. 2: FVFCS, (a) continuous response of the circuit of Fig.1.1 (a), (b) continuous response of the same circuit when M7 is biased near the linear region

Fig.1.2(a) shows the dc response of the circuit of Fig.1.1(a), the output and input currents are linked by the expression $I_{OUT} = I_{IN} + I_B$. The continuous DC current can be easily removed from the output node using circuits that mirror the currents if this is needed in specific applications. A special condition of FVFCS occurs when transistor M_7 is biased near the linear region and M_8 is

maintained in the saturation region. In this case, the output current may increase more than the input current Fig.1.2 (b). When a MOS operates in triode region the current-voltage link is given by:

$$I_D = K(V_{GS} - V_{TH}) \cdot V_{DS} \quad (1.1)$$

where the quadratic term has been neglected on the hypothesis that VDS is small. When the transistor operates in strong inversion and saturation, the drain current is about

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \quad (1.2)$$

where λ is the modulation parameter.

Using the formulas (1.1) and (1.2), the current through M_8, neglecting the modulation effect of the channel length, is given by

$$I_8 = \frac{K_8}{2}\left(\frac{I_{in}+I_B}{K_7 V_{DS7}}\right)^2 \quad (1.3)$$

where V_{DS7} is set to

$$V_{DS7} = V_b - \sqrt{\frac{2I_B}{K_{10}}} - V_{TH} \quad (1.4)$$

therefore achieving a nonlinear relationship between I_{in} and I_8.

1.2 Not Linear Current Mirror based on FVF

In the schematic of Fig.1.1(b), the current mirror is implemented using a classical FVF where the input transistor M_7 is biased near the ohmic region [12]. In quiescent condition, the current I_{in} (generated by the input differential transconductor) is very low and is given by I_B. In this situation, the M_7 and M_{10} transistors operate in saturation but near the boundary with the triode region, with V_{DS} slightly higher than V_{DSsat}, and the overall strength of the active load is small. However, if I_{IN} increases, this causes an increase in the gate-source voltage of M_{10} that decreases the drain-source voltage of transistor M_7, then drives it to the ohmic region. Thus, the input resistance increases, and the M_7 transistor follows (1.1) and has a large variation in the gate-source voltage. This increases the output current of the active load transistor M_8 as long as it remains in the saturation region (1.2) with the same behavior as that shown in Fig.1.2 (b). This output current, neglecting the channel length modulation, is given by

$$I_8 = \frac{K_8}{2}\left(\frac{I_{in}}{K_7 V_{DS7}}\right)^2 \quad (1.5)$$

where V_{DS7} is given by

$$V_{DS7} = V_b - \sqrt{\frac{2I_{in}}{K_{10}}} - V_{TH} \quad (1.6)$$

Note that V_{DS7} is now dependent on I_{IN}. If I_{IN} increases, V_{DS7} decreases and current I_8 can be larger for OTA than previous (a) case with the same I_{IN}.

1.3 Not Linear Current Source based on degeneration resistors of sorce

The third non linear current mirror scheme is shown in Fig.1.1(c). It is a topology that is based on current mirrors with source degeneration used to delete offsets in amplifiers [13]. In these applications, the transistors only operate in the ohmic region, thus carring out a voltage-controlled linear resistance. However, in this case, the degeneration transistor is introduced into the saturation region for large input currents. Hence, we get a strongly nonlinear equivalent resistor that produces

a large increase in the output current. When I have to eliminate the offset, I have the resistance under both transistors.

The difference from the previous current mirrors of Fig.1.1(a) and (b) is the transistor M_7 which is biased in the ohmic region with a constant gate voltage but near the limit of the saturation region, and M_{10} is in the saturation region.

Since V_{GS7} is constant, when the drain current I_{IN} of M_7 increases, M_7 enters in saturation and develops a large drain-source saturation voltage. This causes a large increase in the gate-source voltage of M_8 given by

$$V_{GS8} = V_{DS7} + V_{GS10} \quad (1.7)$$

which brings a large increase in output current similar to that of Fig.1.2(b). The current through M_8 is

$$I_8 = \frac{K_8}{2}\left[\sqrt{\frac{2I_{in}}{K_{10}}} + \frac{2I_{in}}{\lambda_7 K_7 (V_b - V_{TH})^2} - \frac{1}{\lambda_7}\right]^2 \quad (1.8)$$

where $\lambda_7 \neq 0$ e $V_B > V_{TH}$.

1.2 Castello and Gray [6]

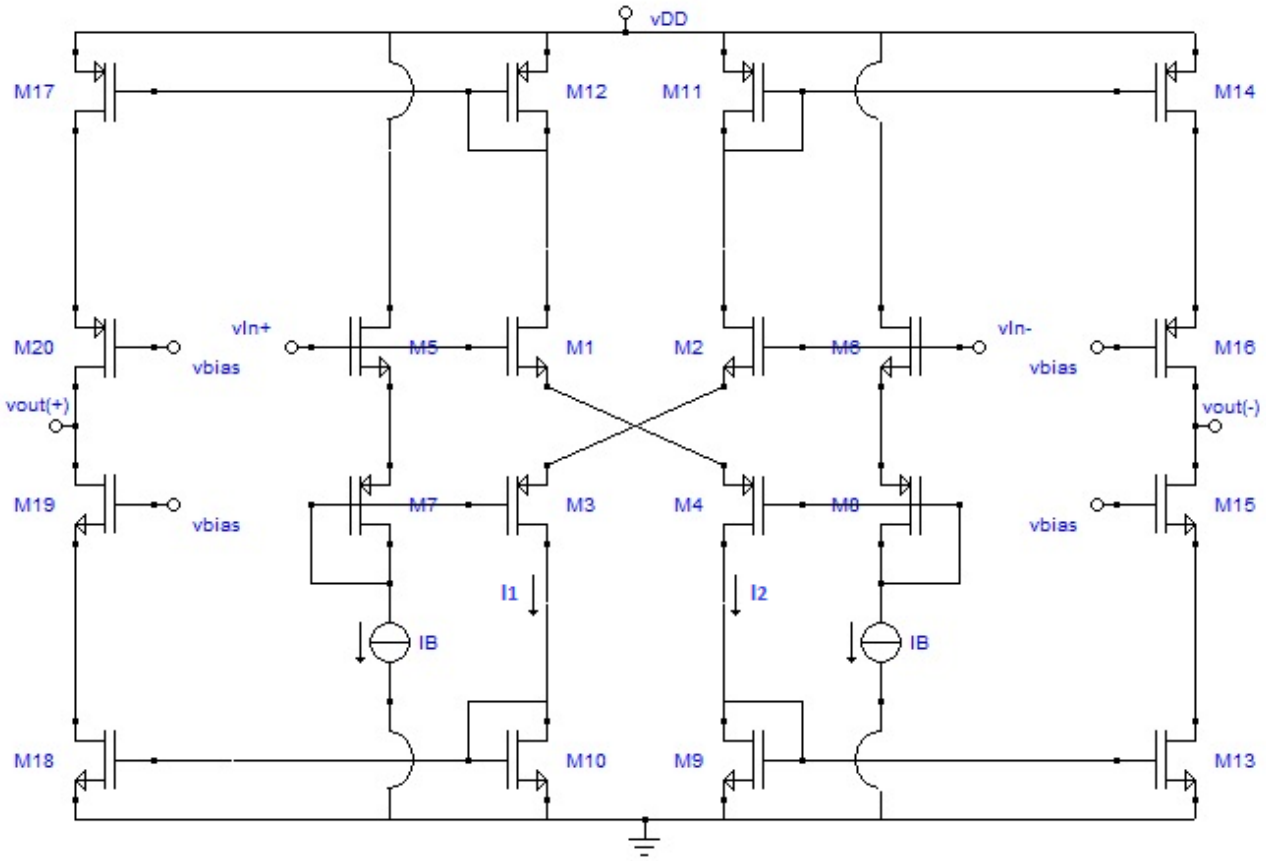


Fig.1. 3: A simplified schematic of the class AB amplifier used by Castello R.

The first examined topology, shown in Fig.1.3, bases its operating principle on a double transconductor (cross-coupled pair) input stage and I will call it "topology by Castello". This topology implements a class AB amplifier used in filter or switched capacitor circuits. If a differential input signal equal to zero is applied, the two matched current sources I_B uniquely define the circuit quiescent current level. For simplicity it is assumed that the four NMOS input devices are identical, and the same is true for the four PMOS devices, then $I_1 = I_2 = I_B$. Furthermore, since all current mirrors have a gain equal to 1, the quiescent current in the output branches is also equal to I_B. It follows, therefore, that the quiescent power consumption in the circuit is precisely controlled by the two matched current sources in the input stage.

Applying a large positive differential input signal, the current I_1 goes to zero and half of the devices in the circuit become cut off and have not been shown on Fig.1.4. Current I_2, on the other hand, increases to a peak value which, in principle, is only limited by the value of the input voltage applied. The same current is mirrored to the outputs and can quickly charge and discharge the load capacitance.

Although in the above consideration it was assumed that the peak value for current I_2 in the class AB circuit of Fig.1.4 is only a function of the applied input voltage, in practice another limiting factor is the total supply voltage. In fact as the current level increases, the sum of the voltage drops across devices M_l, M_4, M_9, and M_{13} in Fig.1.4 also increases, until it is equal to the total supply voltage. At this point, some of the devices (M_l,M_4 or both) enter the linear region of operation, and the current level becomes practically constant independently on the value of the input voltage. This

problem becomes more and more severe as the supply voltage is reduced, and represents the limiting factor to the maximum achievable peak current for a total supply voltage. The achievable value for the peak current is also strongly dependent on the value of the input common-mode voltage V_{cmi}. An optimum choice of the value of V_{cmi} is important in order to obtain the best possible performance in the opamp. In fact, increasing V_{cmi} by one n-channel threshold voltage above the middle-point between the two supplies, as allowed by the fully differential configuration, gives more than a threefold increase on the achievable peak current level.

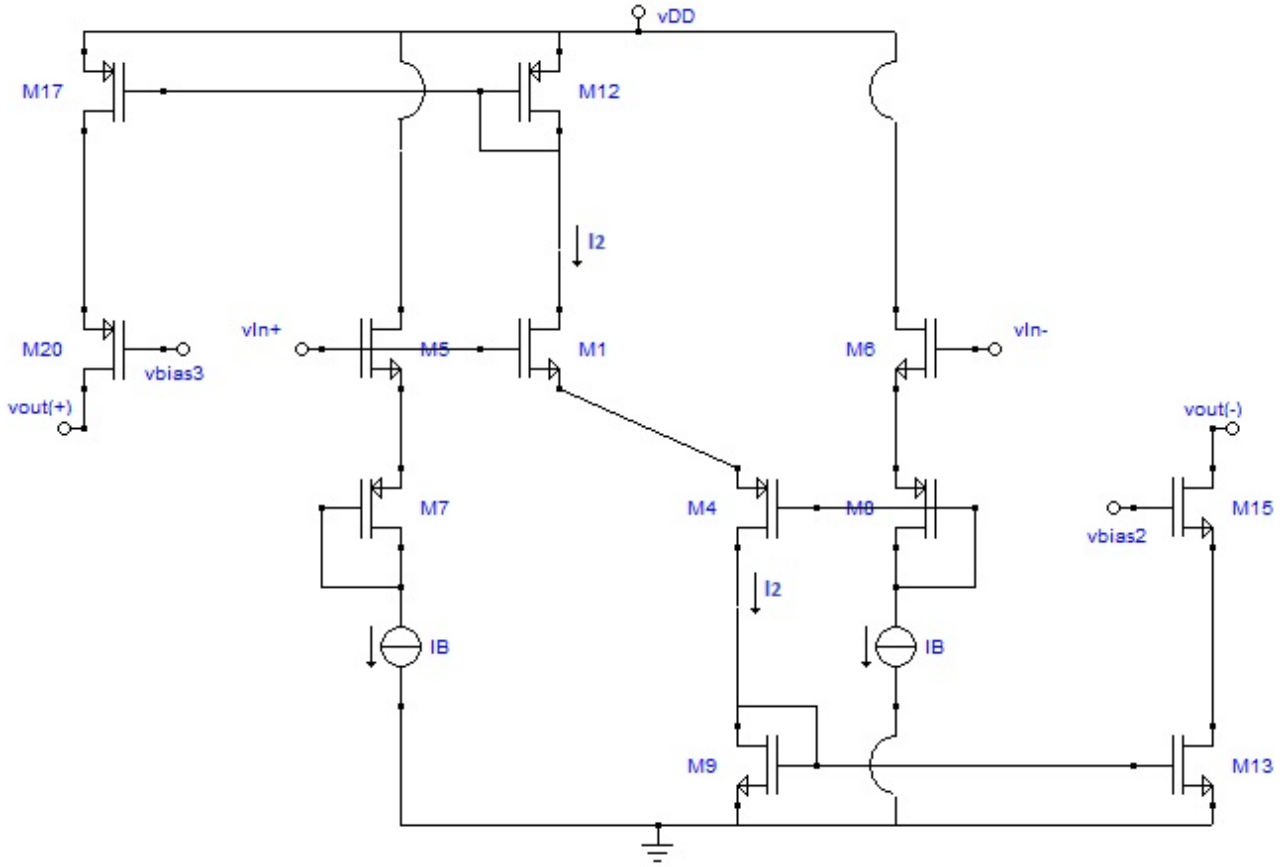


Fig.1. 4: Simplified schematic of the circuit by Peluso for large differential input (cut off devices not shown)

By utilizing a class AB configuration, a saving on the quiescent power dissipation for a given speed can therefore be achieved. Furthermore, the low quiescent current level on the output devices improves the voltage swing, and gives a larger dc gain. The class AB structure, however, has also some disadvantages. In particular it tends to be more complicated, and makes the problem of designing the CMFB circuit more difficult.

A single-stage configuration is particularly suitable for class AB operation. Also it has good power-supply rejection at high frequencies (beyond the dominant pole) and gives no high-frequency second-stage noise contribution, an effect which can greatly reduce the dynamic range of a sampled data system due to aliasing effects. Furthermore, in a single stage opamp the load capacitance is enough to guarantee stable closed-loop response, so that no extra compensation is required. The main drawback of the single-stage topology, particularly for low-voltage applications, is the reduced output swing due to the cascade devices. In order to take full advantage of the class AB structure the amplifier must be able to deliver all of the peak input current to the load, without unacceptably compromising the output voltage swing. This requires use of a novel biasing scheme for the cascode devices.

1.3 Sen and Leung [15]

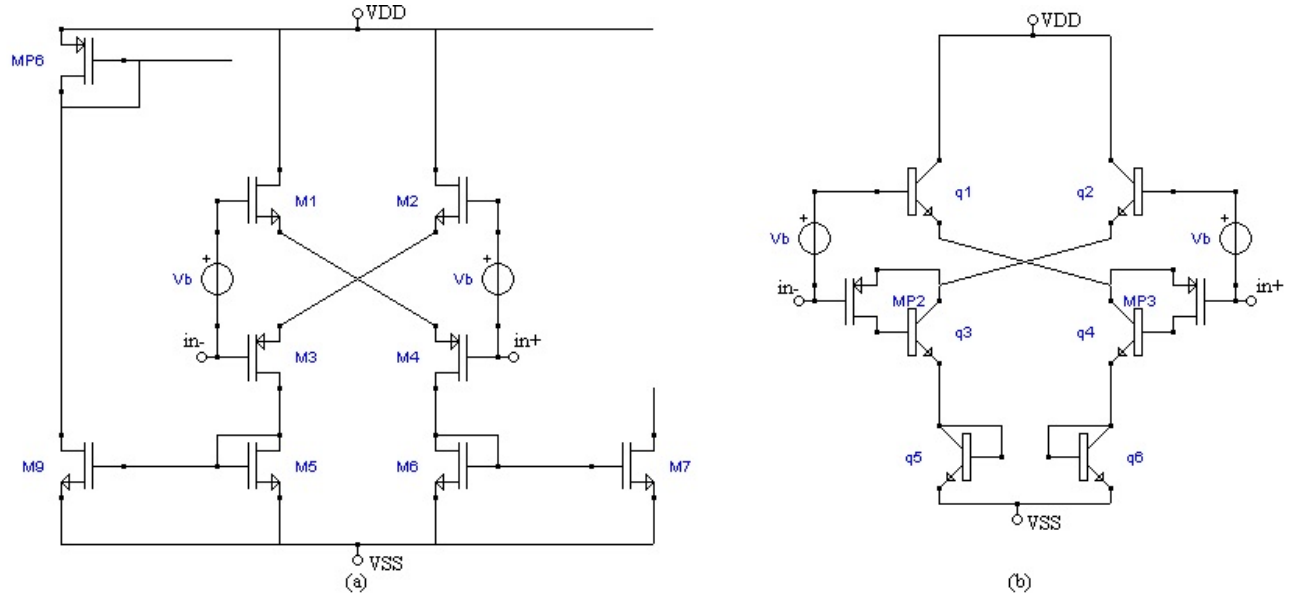


Fig.1. 5: Input stages CMOS (a) e BiCMOS (b)

A single-ended version of the topology by Castello was proposed in 1996 by S.Sen and Leung and it is shown in Fig.1.5. In addition to considering the single-ended version, S.Sen et al. propose the benefits that can be obtained by making the cross-coupled pair in BiCMOS technology.

Taking Fig.1.5(a) into consideration, in the absence of differential input signal, the voltage generator V_b biases the devices so that they have a small current in quiescent condition. When an input differential voltage is applied to the gates of M_3 and M_4, the sum of V_{GS} of M_1 (M_2) and M_4 (M_3) increases (decreases) and the drain current increases (decreases) according to the quadratic law and finally, that current is mirrored to the output stage. In Fig.1.5(b), the input stage of the BiCMOS operational amplifier is shown. The transistors M_1 (M_2) of Fig.1.5(a) are replaced by bipolar transistors npn Q_1-Q_2 in Fig.1.5(b), M_4 (M_3) is replaced by a Q_4 and MP_3 structure (Q_3 and MP_2) .

To bias the input stage with a small quiescent current, a level translator is used to shift the voltage by a value equal to that between the gate-source of MP_3 (MP_2) and the Q_1 (Q_2) base-emitter voltage drop. The combination of Q_4 and MP_3 in the structure actually behaves like an equivalent PNP transistor, which is why this structure is called "pseudo-PNP" (PS-PNP).

Its transconductance is given by $\beta_{Q4}gm_{Mp3}$ and its advantages are that the transconductance of the PMOS transistor MP_3 is exalted by β of Q_4 without increasing the input gate capacitance of the same factor and without requiring a base input current.

Fig.1.6 shows the graphs of the respective currents in the two branches of the circuit for the two cases. The BiCMOS input stage shows a significant improvement in currents' management compared to the CMOS version. Fig.1.7 shows the complete opamp without the adaptive polarization circuit of the output stage cascode transistors [14]. The output pull-up current is derived by mirroring the Q_5 collector currents to the drain of the MP_6 transistor through Q_7, Q_8, and MP_6.

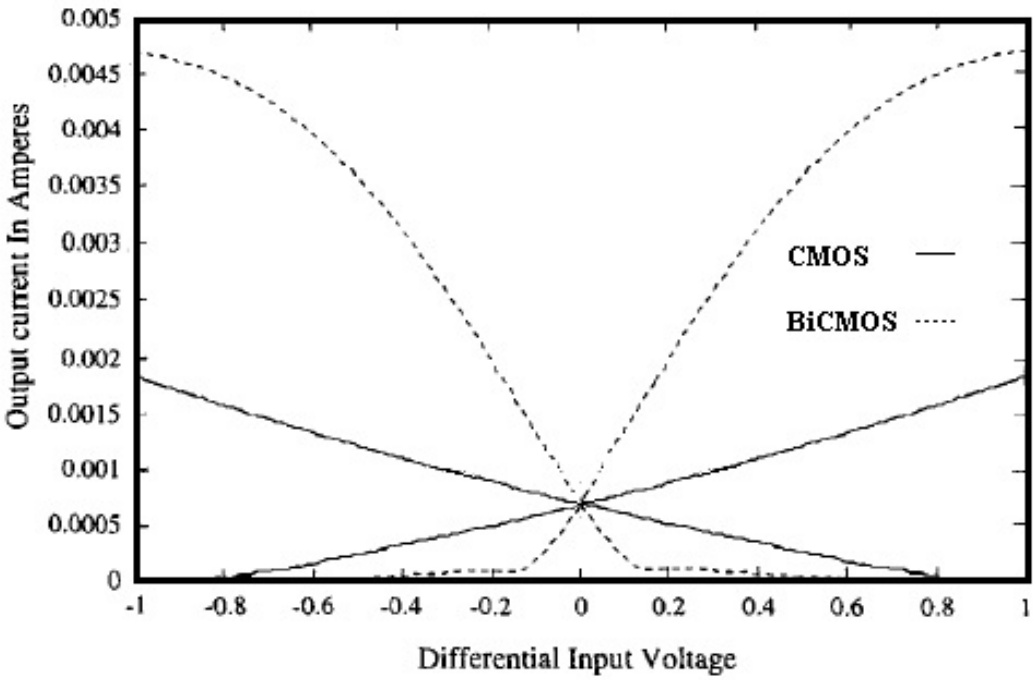


Fig.1. 6: Comparison between the output currents of the CMOS input stage and BiCMOS

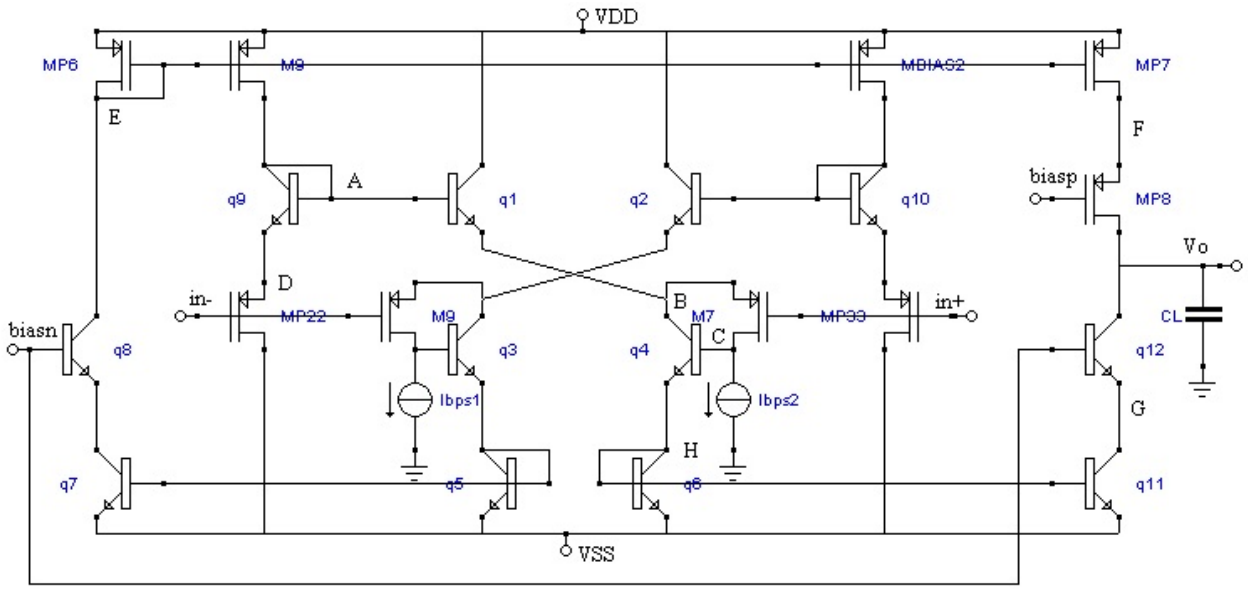


Fig.1. 7: Basic Structure of a class-AB BiCMOS amplifier

1.4 Shulman and Yang [16]

The third topology considered is shown in Fig.1.8 and also uses a double transconductor cell as input stage. Respect to the previous case, it presents the cross-coupled pair formed only by MOS device and the manner used to mirrors the current to the output branches is different and this saves a current branch.

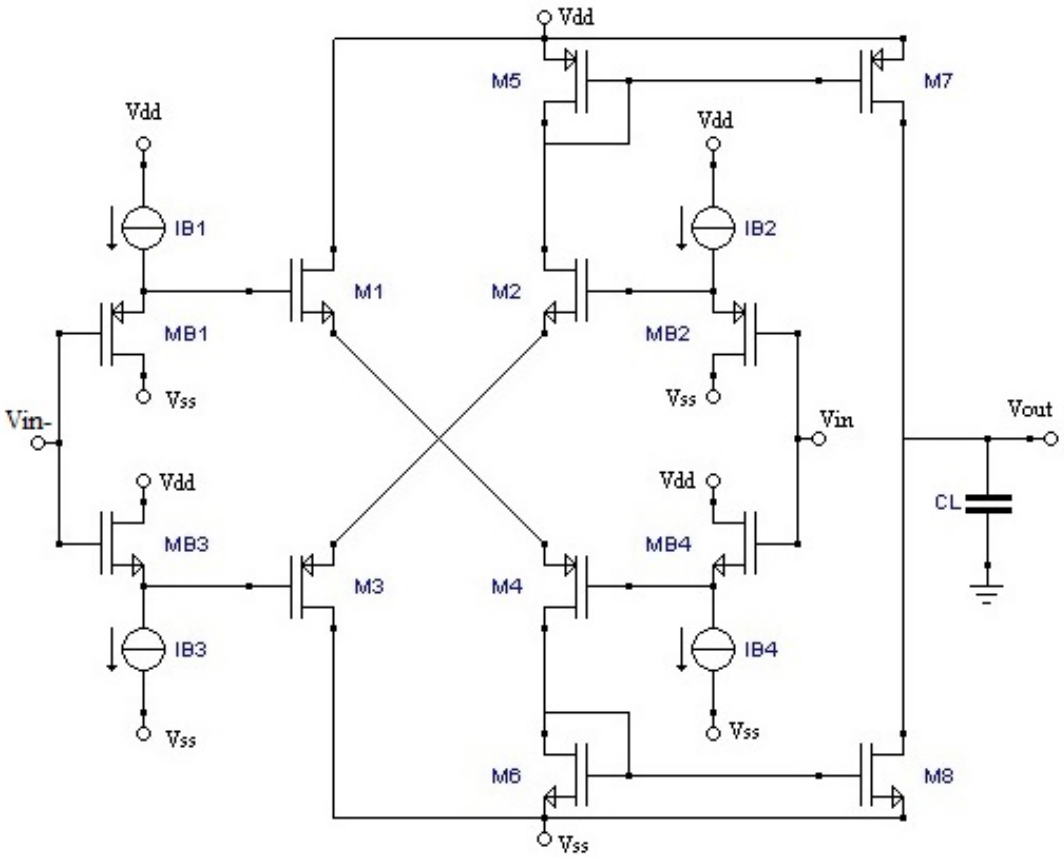


Fig.1. 8: Schematic of a CMOS class AB opamp

Under stationary conditions, the crossover pair of transistors is normally biased with a voltage slightly above the threshold, so that the current of the input stage is small. By applying a positive input voltage step, the current in M_2-M_3 increases dramatically due to the nonlinear characteristic of the MOS transistors and is transferred to the output by the current mirrors.

1.5 Peluso and Vancorenland [17]

The simple current mirror with diode connection has the disadvantage that it cannot be used for low supply voltages. This is due to the fact that the difference in potential of a V_{GS} is required for the diode connection. Now I'll consider the circuit in Fig.1.9 (a), (that's equivalent to that shown in Fig.1.1(a)). As seen in section 1.1, if the current $i_{IN,2}$ is a biasing one, this circuit acts as a mirror for the $i_{IN,1}$ current which is injected into node n1.

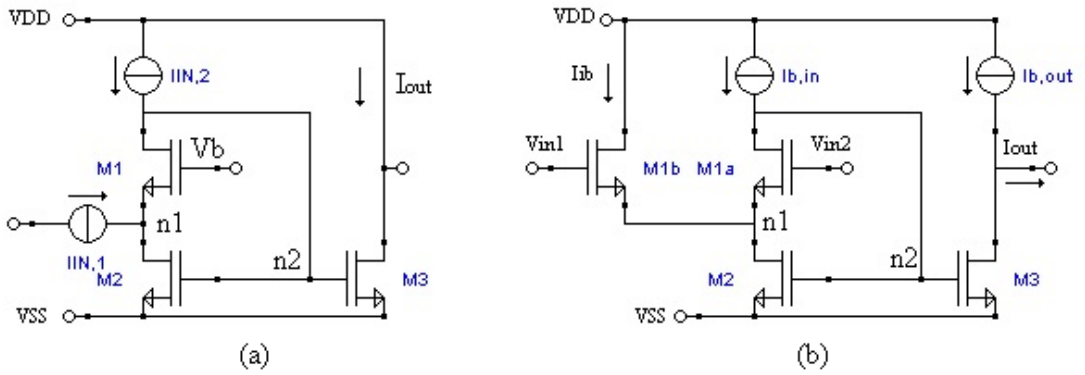


Fig.1. 9: (a) Low voltage current mirror, (b) Input differential structure based on low voltage current mirrors.

By using such a device in this way, you will gain a benefit in terms of the input potential difference, which is approximately equal to the M_2 V_{DSsat}. Parallel-parallel feedback is implemented, an output voltage is measured, and a current is reported to the input node. This configuration makes the input resistance very low.

In the current mirror configuration of Fig.1.9 (a), a voltage V_b is used to set the potential drop at the input node n_2. If an additional transistor is connected and the source is connected to the input of the mirror (node n_1), as shown in Fig.1.9 (b), the source potential is set. If in such conditions a signal is applied to the gate of the additional transistor (M_{1b}), a current is generated which is injected into the current mirror and copied to the output. It is not necessary to bias M_{1a} with a constant voltage as its gate can be used for an auxiliary signal (V_{in2}).

Fig.1.10 shows the schematic of a class-AB OTA operating at low supply voltages [18], [19]. It consists of two types of differential input structures based on the operating principle of the current mirrors shown in Fig.1.9, one of the n-type and the other of the p-type. If V_{in1}-V_{in2} is a positive quantity, a large current is generated in the input stage and mirrored in one of the two output branches.

In the other half of input stage, the current through it goes down to zero. The amplifier is single-stage and offers sufficient gain to find employment in single loop delta-sigma modulators.

The OTA transfer characteristic is typical of a class-AB amplifier. For a small signal applied to the input, the output current is linear, while for large signal, the output current increases rapidly to saturation. In the next sections I will refer to this topology by calling it “Peluso topology”.

Transistors M1a and M2a (M1d and M2b) with the current source IB form a flipped voltage follower (FVF) that copies the input signal to the source of M1b (M1c). In this way the transistors of the input pair M1b-M1c have a gate-source voltage VGS=VGSQ±(in1-in2), where VGSQ is the quiescent component. This doubles the signal component at the input of the pair of devices M1b and M1c. For large differential inputs one of them cuts off whereas the other carries a current that is not limited by a fixed current source.

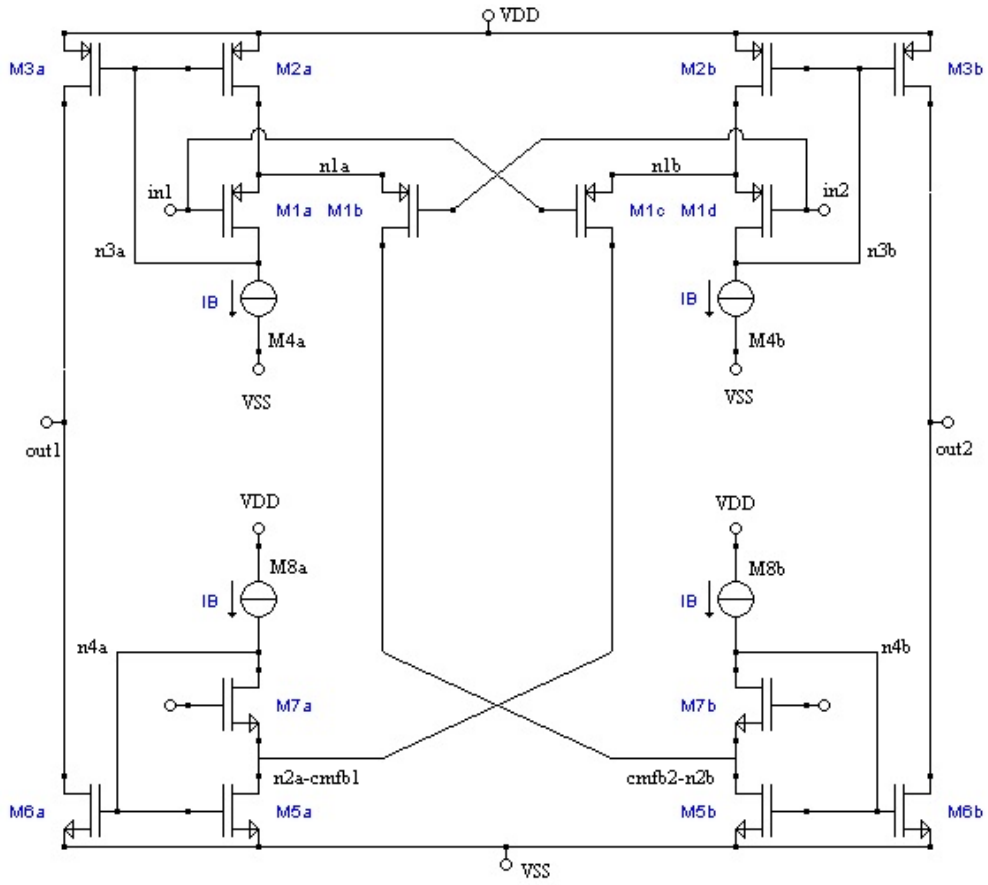


Fig.1. 10: Fully differential class AB OTA.

1.6 Elwan and Gao [20]

Compared to the previously treated cases in which it was more intuitive to understand the operation in class AB, in the following cases, to get the current variations desired, the dependence of the tail current on the input signal is utilized.

Fig.1.11 (a) and Fig.11 (b) show, respectively, an input stage consisting of a standard differential pair and a basic class AB stage. For the differential pair, the transconductance can be increased by increasing the aspect ratio of transistors M_1 and M_2 and increasing the tail current. However, the maximum current available from a differential pair cannot exceed that of the tail current. Power consumption in quiescent condition is related to the load capacity and the desired slew rate:

$$P = V_{dd}(SR)(C_L)(n) \quad (1.9)$$

where SR is the slew rate, C_L is the load capacitance and n is a factor related to the type of OTA used.

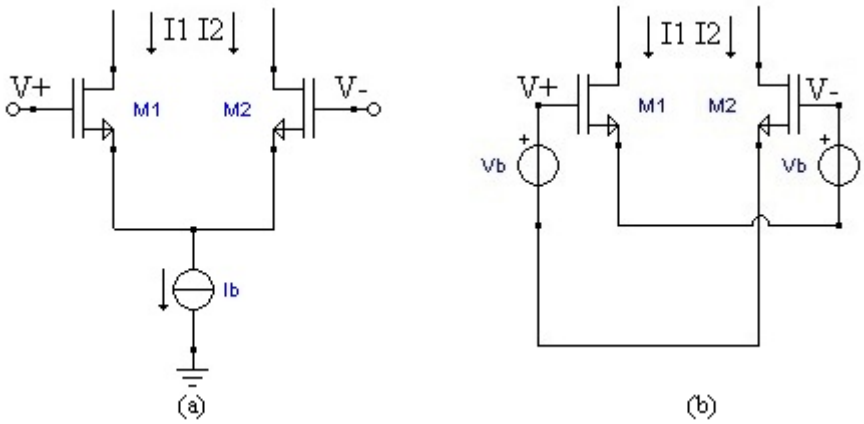


Fig.1. 11: (a) Differential pair as input stage (b) Class AB input stage

A standard OTA dissipates a large power in quiescent condition, especially when driving a large load capacitor. The class AB stage shown in Fig.1.11 (b) consists of two identical transistors M_1 and M_2 coupled by two constant voltage sources. In quiescent condition, the two gate voltages of the transistors are maintained at the same common mode level. The transistors M_1 and M_2 have the same V_b voltage and thus carry the same current given by:

$$I_{dc} = \frac{k_1}{2}(V_b - V_T)^2 \qquad (1.10)$$

By choosing V_b slightly above the threshold voltage, the quiescent current can be kept low. The circuit shown in Fig.1.12 represents a possible implementation of the ideal scheme of Fig.1.11b. Looking at Fig.1.12, when the gate voltage of M_1 increases, the circuit performing the level translation will cause the M_2 source voltage to increase. The source voltage of M_1 remains fixed by the level translator circuit connected to the gate of M_2. Therefore, the current through M_1 will increase while the one through M_2 will decrease. By choosing a large enough shape ratio for the M_1 and M_2 transistors, a high driving current can be obtained.

The maximum output current is not limited by the tail current and can reach high values not depending on of current consumption in quiescent condition. Hence, you can drive high currents with low power consumption in standby mode. To effectively implement the class-AB input stage, an efficient level translator circuit must be implemented.

The main problem is that the level translator circuit is required to drive the source of the two transistors M_1 and M_2.

The CMOS transistor pair strongly limits the input signal excursion that hinders the circuit use in many low power supply applications. Additionally, the CMOS transistor pair of the input stage increases the number of noise inputs and thus increases the overall noise generated by the OTA circuit. Low noise and power supply requirements force the use of only two transistors to achieve the input class AB. This leads to the following restrictions on the biasing circuit:

1) To keep an accurate voltage level in level shifters, which can provide a well-controlled standby current and robustness with respect to temperature and process variations.
2) To provide a low-impedance terminal that can biase the source of the input stage transistors.
3) To provide a reasonably fast response with a minimum contribution of noise to the OTA.
4) To have a low consumption in quiescent condition
5) To be powered by low voltage supply without limiting the signal dynamic range of the input stage.

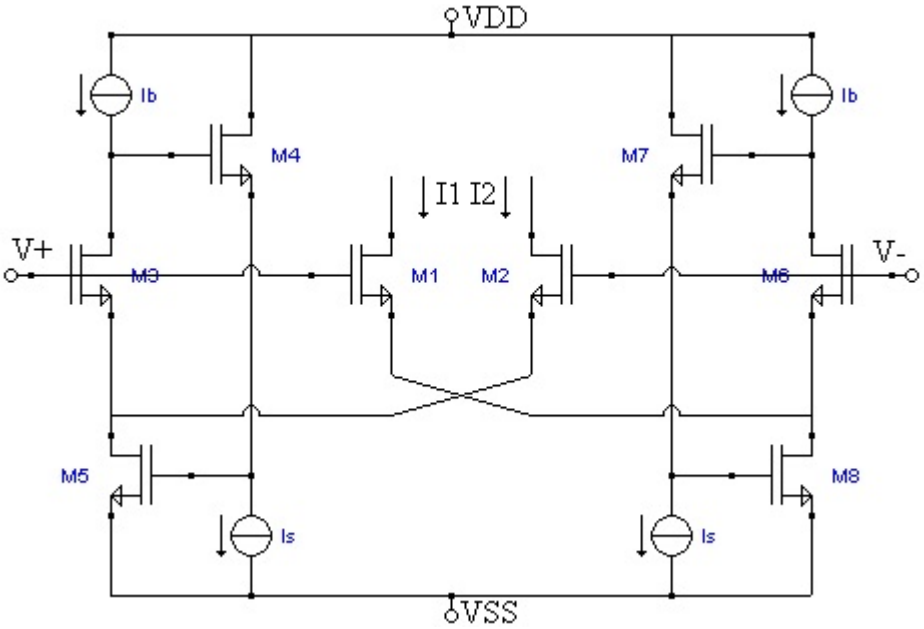


Fig.1. 12: The main part of class AB OTA.

In order to satisfy all these requirements, the circuit shown in Fig.1.12 is proposed. Transistors M_1 and M_2 form the input transconductance stage operating in class AB. The level shifter circuit consists of transistors M_3, M_4, M_5 and M_6, M_7, M_8. A constant current I_b is forced through the transistors M_3 and M_6. Assuming that both transistors operate in the saturation region, the gate and source voltage between transistors M_3 and M_6 is thus fixed and can be expressed by:

$$V_{GS} = V_b = V_T + \sqrt{\frac{2I_b}{k_3}} \qquad (1.11)$$

The source terminal of the transistor M_3 is kept to a low impedance by the negative feedback circuit formed by M_4, M_5, and the current source I_S. The gate voltage of the transistor M_5 is automatically adjusted, since Ib is fixed, the variable current is from the transistor M_2. In quiescent condition, both V+ and V- inputs are held at the same V_{cm} common mode level. Since the sources of the transistors M_1 and M_2 are at the same voltage level as described above, the V_{GS} voltages of the transistors M_1, M_2, M_3 and M_6 are all equal. Therefore, the quiescent current of the transistors M_1 and M_2 is given by:

$$I_{sb} = \frac{k_1}{k_3} I_b \qquad (1.12)$$

The quiescent current is therefore well controlled by I_b and is independent of process parameters such as VT and K. It is clear that the main contribution to the noise is given by the input stage transistors M_1, M_2, M_3 and M_6. Even the transistors that mirror the output current will make a contribution in terms of noise, but the latter is divided by the transconductance of the input stage. If a completely differential topology is used, the input voltage is further divided by a factor of 2 [6]. There are two possible ways to mirror the current to the output. One way is to use current mirrors to copy the drain currents of M_1 and M_2 to the two output terminals.

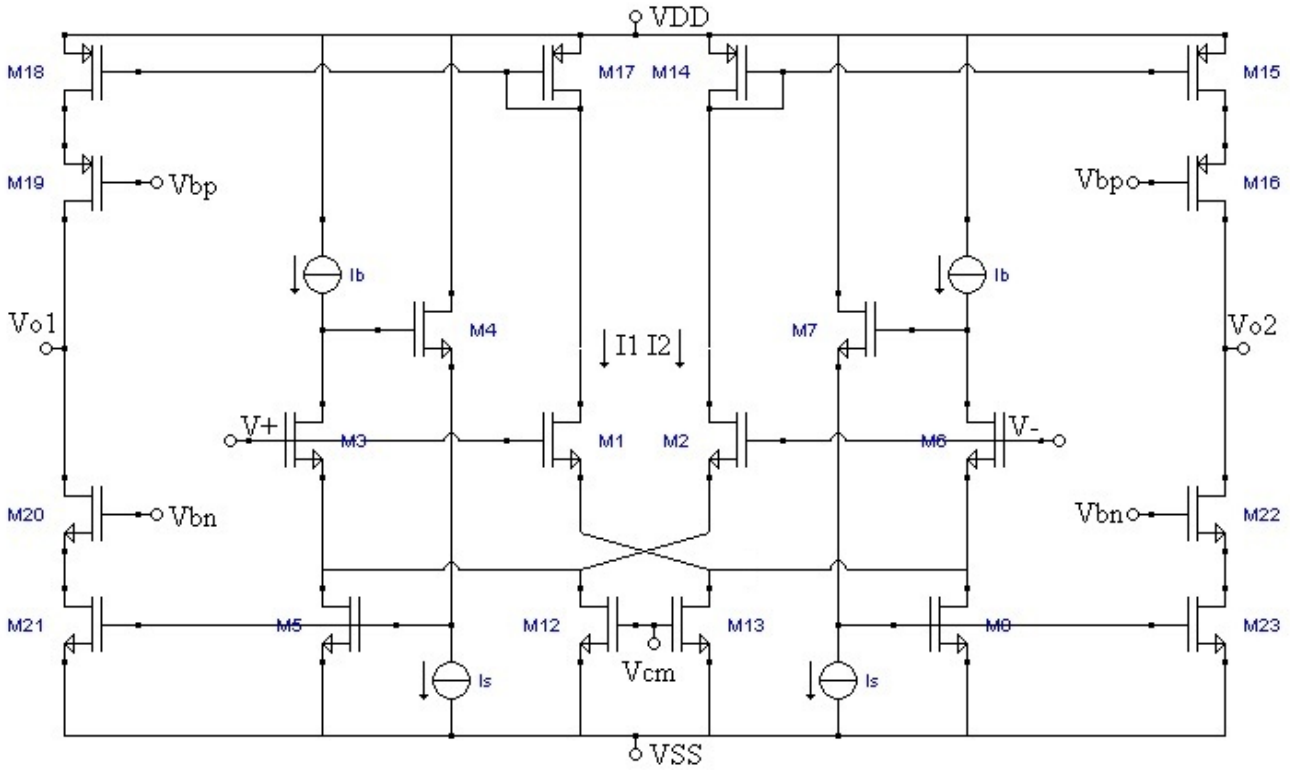


Fig.1. 13: Class AB OTA

The other less obvious way is to exploit the fact that the M_5 and M_8 feedback transistors carry an inverted version of the M_1 and M_2 drain currents. As shown in Fig.1.13 these currents can be copied directly to the output from transistors M_{21} and M_{23}. Common mode control transistors (CMFBs) can be added without introducing additional power dissipation. The CMFB, consisting of the M_{12} and M_{13} transistors, controls the amount of current from the M_3 and M_6 transistors of the feedback loop. Therefore, they influence the output current bidirectionally. In quiescent condition, both transistors M_{12} and M_{13} carry an amount of current equal to I_b. If the current through M_{12} and M_{13} decreases, an additional continuous current flows through transistors M_{21} and M_{23}. If the current through M_{12} and M_{13} increases, the current through M_{21} and M_{23} decreases, producing as an effect a continuous current flowing from the output terminals to the OTA. The CMFB network uses M_{12} and M_{13} gates to control the common output mode level. The total quiescent current of the fully differential OTA is given by:

$$I_{sb} = 2I_b + 2I_s + 4\frac{k_1}{k_3}I_b \qquad (1.13)$$

The maximum OTA current is controlled by the aspect ratio of the transistors M_1, M_2, M_3 and M_6. This current value can then be adjusted without affecting power consumption under quiescent condition. The transconductance of the OTA is given by:

$$G = 2k\sqrt{\frac{2I_b}{k_{LS}}} \qquad (1.14)$$

1.7 Yavari and Shoaci [21]

The OTA topology of Fig.1.14 uses two identical transistors M_1 and M_2 that are coupled crosswise through two constant voltage sources made of flipped voltage follower (FVF) acting as level shifters. The FVF cell consists of the $M_{c1} \div M_{c6}$ transistors that realize the floating voltage source.

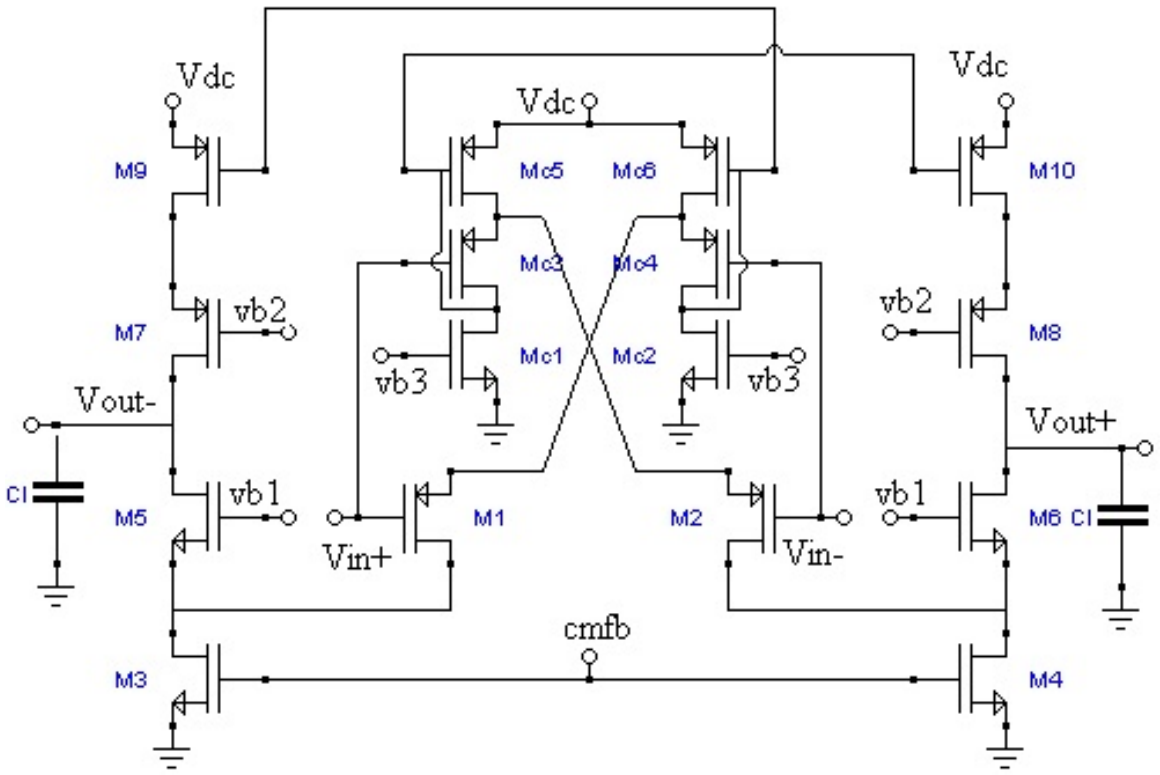


Fig.1. 14: Class AB OTA

In quiescent condition, the gate voltages of the input transistors M_1 and M_2 are the same. In this case, $V_{SG1}=V_{SG2}=V_b$, and both transistors carry the same current that is controlled by V_b. This tension is chosen slightly above the threshold value so as to obtain a small quiescent current.

When an input signal is applied, a large current is generated in one of the two input transistors. For example, if $V_{in}+$ increases and $V_{in}-$ decreases, the M_2 source voltage increases while the voltage at the M_1 source decreases by the same amount. In this way, the M_1 drain current decreases as M_2 current increases. When a signal is applied at the input, the maximum current that can flow in M_1 or M_2 is independent on the quiescent current.

To enable class AB operation of output devices that act as current sources, the gates of M_9 and M_{10} are respectively connected to M_{c6} and M_{c5}. During the slew-rate period in one of the two branches of the cascode, there is an increase of current. If $V_{in}+$ is larger than $V_{in}-$, the M_1 drain current will be reduced by the same amount as M_2 is increased. M_{c5} drain current will be increased, and even in M_{10}, as long as the M_{c6} and M_9 drain current is reduced.

The M_2 drain voltage increases considerably due to the improvement of the current passing through it which results in an increase in voltage at the gate of M_3 and M_4 through the gate-drain capacitance of M_4. Then, the M10 current will be forced to the positive output node, $V_{out}+$, and the negative output node will be discharged by the current of M_3. The increase in the M_4 drain current

will be provided by M_2 because, due to the sudden increase in the M_2 drain voltage, the transistor M_6 will be forced to cut off. When a large negative input signal is applied to the OTA, a similar improvement in the slew value is obtained. Therefore, a large slew-rate is obtained during both positive and negative slew phases of the OTA.

If the gate of M_9 and M_{10} are connected to a fixed biasing voltage, their currents will be blocked during the OTA slew phase. In this case, when a large positive input signal is applied to the OTA, the positive output node will be loaded only by the M_{10} polarization current. Thus, the response speed of the OTA being examined will be much greater than that of an OTA consisting of a folded-cascode that employs class-AB operation only in the input transistors.

Class AB operation of the M_9 and M_{10} output transistors acting as current sources also improves the OTA small signal DC gain and the unitary gain bandwidth. When a small signal is applied to the input of the OTA, this appears through the gate-source of the output transistors M_9 and M_{10} that operate as current generators and through the FVF buffer cells. The effective transconductance of the input transistors is increased from $gm_{l,2}$ to about $gm_{l,2}+gm_{9,10}$, which improves the OTA unitary gain bandwith of the same amount.

Therefore, the class AB operation of the input stage leads doubling the actual transconductance of the input transistors, and doubling the unit gain bandwith and DC gain.

The minimum voltage to be applied to the OTA under test, for proper operation is approximately equal to $V_{GS}+V_{DS\ sat}$ where $V_{DS\ sat}$ is the drain-source saturation voltage of a MOS transistor. To achieve a large output signal excursion, a two-stage topology can be used where the first one is constituted by the proposed OTA and the second one a classical common source topology with class AB operation.

1.8 Galan and Lopez-Martin [22]

The following topologies illustrate adaptive polarization techniques to make the tail current, signal dependent. In [23], a Class A OTA, such as that shown in Fig.1.15 (a), has been transformed into a circuit called "super-class AB OTA" Fig.1.15 (b) using a different adaptive polarization of the input stage and an active load with resistance acting as a common local mode feedback (LCMFB) to provide additional boost current [24]. In Fig.1.15 (b), an imbalance in I_1 and I_2 causes a non-zero current in the R_1 and R_2 resistors, which unbalances the gate voltage of M_5 and M_8, producing a large output current. In this section, a technique that uses double current boosting is used, but in this case, it is proposed to use a different active load based on current mirrors whose gain is dependent on their input current. The idea is shown in Fig.1.15 (c).

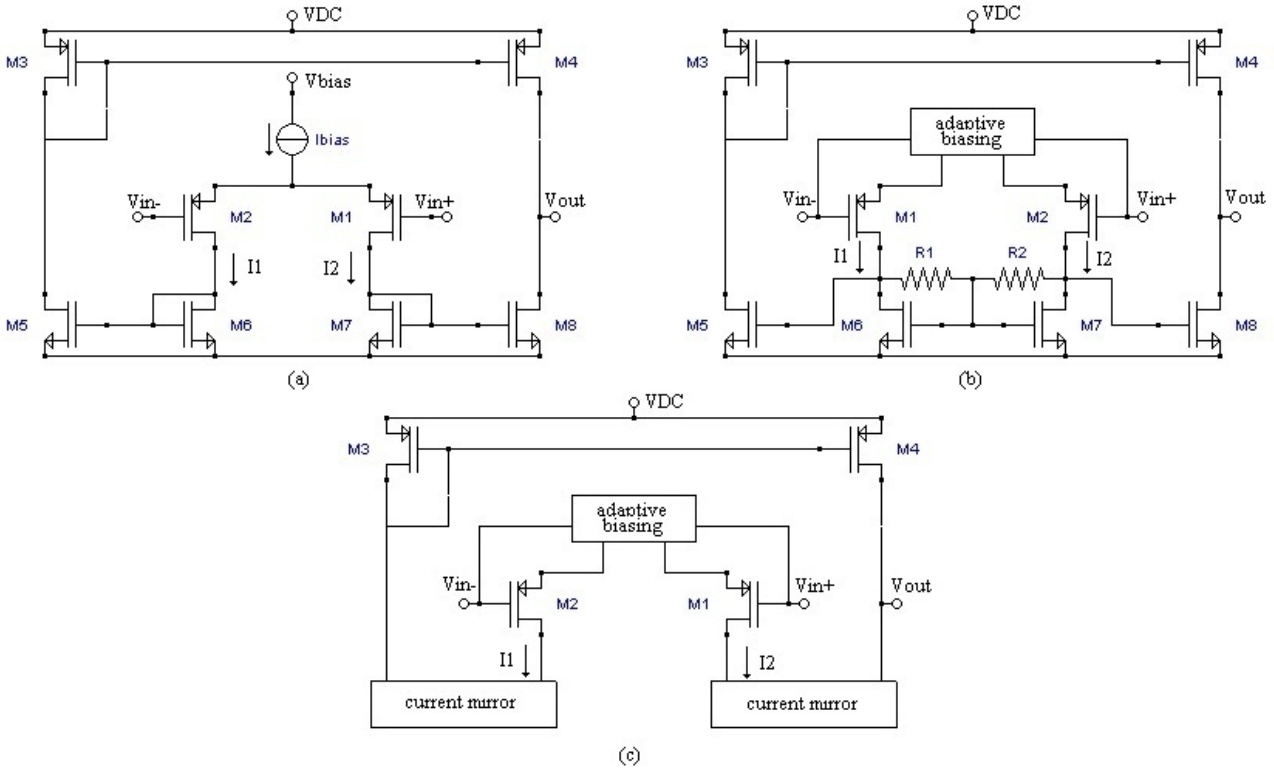


Fig.1. 15: (a) Class A OTA, (b) super-class AB OTA which uses LCMFB, (c) super-class AB OTA alternative.

The current mirror gain is ideally $G(I_{in})$ equal to 1 when the input current is low (of the quiescent current order or lower). Thus, the quiescent current in the output branches is simply and carefully controlled, and can be very low.

However, $G(I_{in})$ increases as I_{in} increases for large voltage signals V_{in}, resulting in large output currents. To achieve this behavior two topologies of current mirrors operating in the saturation region for low currents are used, but for high currents their input transistors enter the ohmic region. In the third topology current mirrors with degeneration source transistors are used that for low currents operate in the ohmic region and enter in saturation region for high currents. In order to realize the adaptive polarization technique of the input stage shown in Fig.1.15 (c), the topology depicted in Fig.1.16 (a) has been used.

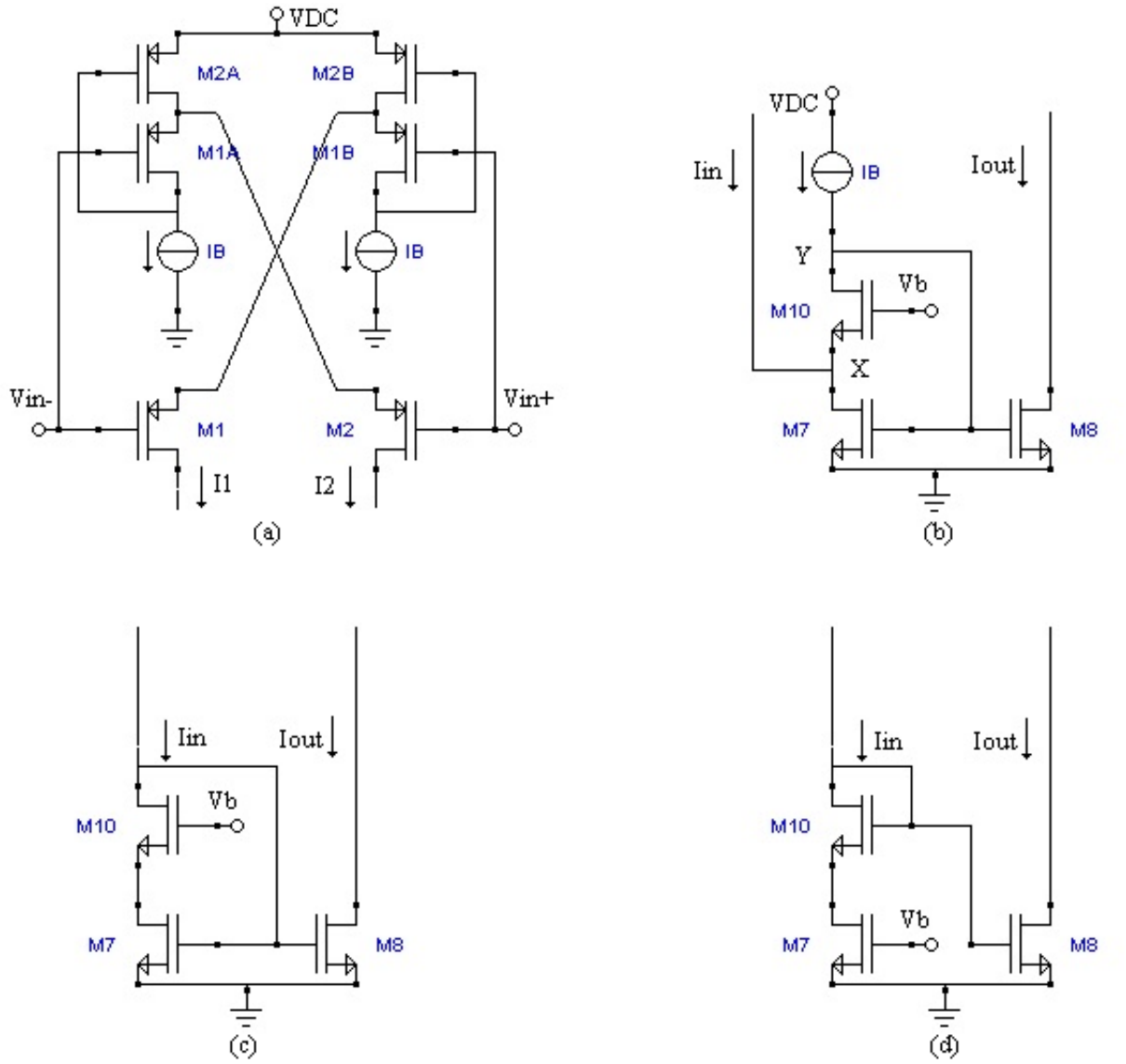


Fig.1. 16: (a) AB input class differential torque with adaptive polarization, (b) first nonlinear current mirror proposal, (c) second nonlinear current mirror proposal, (d) third proposed current mirror not linear.

This circuit is proposed in [10] and consists of two identical transistors M_1 and M_2 coupled crosswise with two level shifters. Each level translator is based on two flipped voltage followers [11], which employ two transistors (M_{1a}, M_{2a} and M_{1b}, M_{2b}) and a current source. This input stage constitutes an adaptive polarization circuit because, when a large input differential signal is applied, the current output may be much greater than the quiescent current I_b supplied by the current generators.

Therefore, it operates in class AB and this makes it very attractive for low power applications. For $V_{id} = (V_{in+}) - V_{in-} < 0$, the current through M_2 increases while the current passing through M_1 falls below the quiescent current I_b and eventually becomes zero. Consequently, when $V_{id} > 0$, the current through M_1 increases without being limited by I_b and the current through M_2 drops below I_b. The input stage can operate with a minimum supply voltage of $V_{DDmin} = | V_{TT} | + 2V_{SDsat}$, where V_{TT} is the transistor threshold voltage and V_{SDsat} is the minimum voltage between the source-drain needed to maintain a saturated transistor.

Therefore, the circuit is suitable for low voltage applications. For large V_{id} and assuming that the transistors M_1, M_2, M_{1A} and M_{1B} are identical, the currents I_1 and I_2 are given by

$$I_1 = \frac{K_{1,2}}{2}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + V_{id}\right)^2, \qquad I_2 < I_B \;;\; V_{id} > 0 \tag{1.15}$$

$$I_2 = \frac{K_{1,2}}{2}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + V_{id}\right)^2, \qquad I_1 < I_B \;;\; V_{id} < 0 \tag{1.16}$$

Where $K_{1,2} = \mu_n C_{OX}$ (W/L) is the transconductance of transistors M_1 and M_2, and μ_p, C_{OX}, W and L have the usual meaning. Since the AC input signal is applied both to the gate and to the source terminal of M_1 and M_2, the differential signal V_{id} coincides in AC with the small V_{gs} signal of each input transistor so that the transconductance of this input stage is doubled compared to a conventional differential pair.

Using different implementations for the nonlinear current mirror, it is possible to obtain several superclass-AB OTA topologies as it can be seen in the general scheme of Fig.1.15 (c).

Fig.1.16 (b) - (d) illustrates three possible alternatives for making these blocks. The resulting OTA circuits are shown in Fig.1.17. In all cases, the non-linearity of the current mirrors increases the desired output current. Non-linearity is due to the transition from the ohmic region to that of the saturation of some of the current mirror transistors.

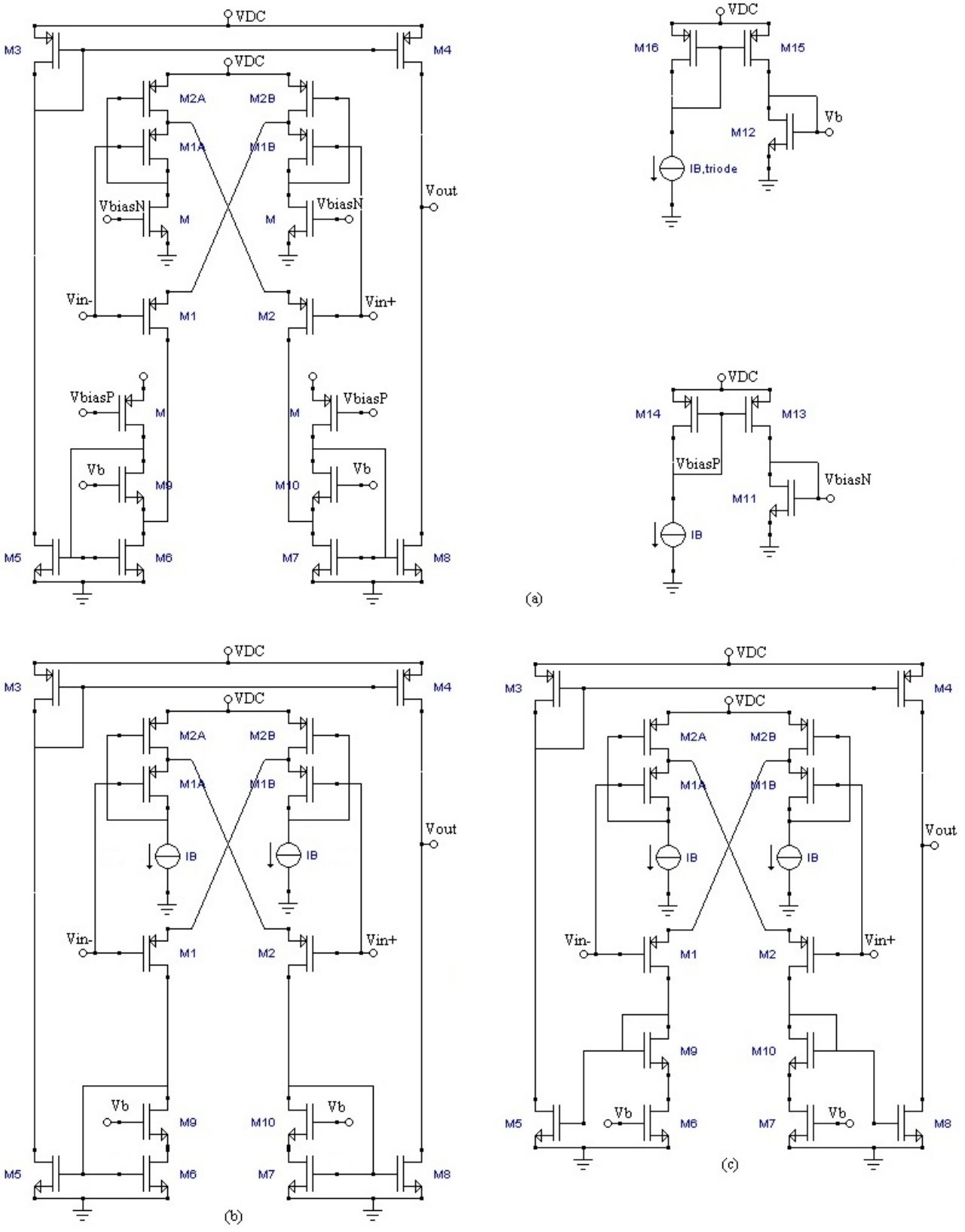


Fig.1. 17: Super-OTA class AB topologies, (a) OTA with FVFCS-based current mirror, (b) OTA with FVF-based current mirror, (c) OTA with current mirror based on source degeneration.

To describe the operation, an approximate expression is used for the drain current of a MOSFET operating in a region of strong inversion and in an ohmic region

$$I_D = K(V_{GS} - V_{TH}) \cdot V_{DS} \quad (1.17)$$

where the quadratic term has been neglected under the hypothesis that VDS is small. When the transistor operates in strong inversion and saturation, the drain current is about

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \quad (1.18)$$

where λ is the modulation parameter.

1.8.1 OTA with NLCS based on FVFCS

The OTA shown in Fig.1.17(a) used a NLCM based on FVFCS presented in section 1.1 to get super-class AB behavior.

In quiescent condition, the current generated by the differential input pair of the class-AB is given by I_B. In this situation, the transistors M_6 and M_7 operate in saturation, but near the boundary with the triode region. For V_{ID} <0, the current through M_2 increases while the one through M_1 drops below the quiescent current IB. In this case, using (1.7) and (1.10), the current through M_8 is

$$I_8 = \frac{K_8}{2}\left[\frac{K_{1,2}}{2K_7 V_{DS7}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} - V_{id}\right)^2 + \frac{I_B}{K_7 V_{DS7}}\right]^2 \quad (1.19)$$

and the current I_5 <I_B, and the output differential current is $I_{OUT} = I_5 - I_8 \approx -I_8$. Such an expression is obtained when V_{ID} <0 for the current flowing through M_5

$$I_5 = \frac{K_5}{2}\left[\frac{K_{1,2}}{2K_6 V_{DS6}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + V_{id}\right)^2 + \frac{I_B}{K_6 V_{DS6}}\right]^2 \quad (1.20)$$

and current I_8 <I_B. Now, the output current is $I_{OUT} = I_5 - I_8 \approx I_5$. Thus, the differential output current is given by the general expression

$$I_{out} = I_5 - I_8 = \pm\frac{K_{5,8}}{2}\left[\frac{K_{1,2}}{2K_{6,7} V_{DS6,7}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + |V_{id}|\right)^2 + \frac{I_B}{K_{6,7} V_{DS6,7}}\right]^2 \quad (1.21)$$

For a large V_{ID}, the differential current generated by the input stage is much larger than I_B and (1.14) can be simplified as

$$I_{out} = I_5 - I_8 \approx \pm\frac{K_{5,8}}{2}\left[\frac{K_{1,2}}{2K_{6,7} V_{DS6,7}}(V_{id})^2\right]^2 \quad (1.22)$$

Note that for a large V_{ID}, the current output increases with V_{ID}^4, improving quadratically the current boost provided by the input stage in class-AB. If the $M_{6,7}$ transistors are in saturation region, the output current of the mirrors should have the same behavior as the OTA in class A in Fig.1.15 (a). But when $M_{6,7}$ enters in the triode region, their transconductance decreases and the total transconduttance of the OTA increases. Therefore, the gain-bandwidth product (GBW) and the slew rate increase accordingly. In addition, the circuit is suitable for low voltage operation because the minimum required supply voltage is $|V_{TH}| + 2|V_{DS,sat}|$.

1.8.2 OTA with NLCS based on FVF

The OTA in Fig.1.17 (b) is implemented by using such adaptive load, also called FVF [26], explained in section 1.2. When V_{IN+} decreases (V_{ID} <0), the class-AB input stage generates a current through the transistor M_2 much larger than the biasing current I_B. Using (1.15-1.16) and (1.5), the current through M_8 turns out to be

$$I_8 = \frac{K_8}{2}\left[\frac{K_{1,2}}{2K_7 V_{DS7}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} - V_{id}\right)^2\right]^2 \quad (1.23)$$

with current $I_5 < I_B$. Then, the output current is $I_{OUT} = I_5 - I_8 \approx -I_8$. Such an expression is obtained when $V_{ID} > 0$ for the current through M_5

$$I_5 = \frac{K_5}{2}\left[\frac{K_{1,2}}{2K_6 V_{DS6}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + V_{id}\right)^2\right]^2 \quad (1.24)$$

And current $I_8 < I_B$. Now, the output current is $I_{OUT} = I_5 - I_8 \approx I_5$. The output differential current is given by the general expression

$$I_{out} = I_5 - I_8 = \pm\frac{K_{5,8}}{2}\left[\frac{K_{1,2}}{2K_{6,7} V_{min}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + |V_{id}|\right)^2\right]^2 \quad (1.25)$$

where V_{MIN} is the minimum of V_{DS6} and V_{DS7}. For a large V_{ID}, the current generated by the input stage is greater than I_B and (1.25) can be simplified, so it has

$$I_{out} = I_5 - I_8 \approx \pm\frac{K_{5,8}}{2}\left[\frac{K_{1,2}}{2K_{6,7} V_{DS6,7}}(V_{id})^2\right]^2 \quad (1.26)$$

Note that for a large input differential voltage, it increases the output current with V_{ID}^4, improving quadratically the current supplied by the class-AB input stage. However, this increase in output current is higher for the previous OTA (Case A) due to the dependence of $V_{DS6,7}$ on the current generated by the input stage. As with the previous OTA, the GBW and the slew rate are improved when $M_{6,7}$ enters in the ohmic region. However, in the OTA of this section, the decrease in $M_{6,7}$ transconductance is greater due to the decrease in $V_{DS6,7}$ when $V_{ID} < 0$. This results in a higher increase in GBW and slew rate. For this OTA, the minimum supply voltage is $|V_{TH}| + 3|V_{DSsat}|$.

1.8.3 OTA with NLCS based on degeneration resistors of source

The third adaptive load scheme is shown in Fig.1.16 (d) and was explained in section 1.3. The OTA in Fig.1.17 (c) is constructed using the adaptive load of Fig.1.16 (d). When V_{IN+} decreases so that ($V_{ID} < 0$), the class-AB input stage generates a current through the M_2 transistor much higher than the bias current I_B. From (1.15-1.16) and (1.7), the current flowing through M_8 is given by

$$I_8 = \frac{K_8}{2}\left[\sqrt{\frac{K_{1,2}}{2K_{10}}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} - V_{id}\right) + \frac{K_{1,2}}{\lambda_7 K_7 (V_b - V_{TH})^2}\left(\sqrt{\frac{2I_B}{K_{1,2}}} - V_{id}\right)^2 - \frac{1}{\lambda_7}\right]^2 \quad (1.27)$$

The output current is $I_{OUT} = I_5 - I_8 \approx -I_8$ and current $I_5 < I_B$. Such an expression is obtained when $V_{ID} > 0$ for current through M_5

$$I_5 = \frac{K_5}{2}\left[\sqrt{\frac{K_{1,2}}{2K_9}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + V_{id}\right) + \frac{K_{1,2}}{\lambda_6 K_6 (V_6 - V_{TH})^2}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + V_{id}\right)^2 - \frac{1}{\lambda_6}\right]^2 \quad (1.28)$$

Now, the output current is $I_{OUT} = I_5 - I_8 \approx I_5$ and current $I_8 < I_B$. The output differential current is given by the general expression

$$I_{out} = I_5 - I_8 = \pm\frac{K_{5,8}}{2}\left[\sqrt{\frac{K_{1,2}}{2K_{9,10}}}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + |V_{id}|\right) + \frac{K_{1,2}}{\lambda_{6,7} K_{6,7} (V_b - V_{TH})^2}\left(\sqrt{\frac{2I_B}{K_{1,2}}} + |V_{id}|\right)^2 - \frac{1}{\lambda_7}\right]^2 \quad (1.29)$$

For a large V_{ID} (1.29) it can be simplified with

$$I_{out} = I_5 - I_8 = \pm\frac{K_{5,8}}{2}\left[\frac{K_{1,2}}{\lambda_{6,7} K_{6,7} (V_b - V_{TH})^2}(V_{id})^2\right]^2 \quad (1.30)$$

Note that for a large V_{ID} the output current increases with V_{ID}^4, by improving a square factor for the current provided by the class-AB input stage. Theoretically, this OTA should reach both the maximum current and the maximum GBW.
However, in order to design this OTA under the same OTA conditions as in the previous cases, the quiescent current in the output transistors must be adjusted to be equal to I_B: this requires $K_{5,8} \approx K_{9,10} \| K_{6,7}$. This $gm_{5,8}$ reduction decreases the maximum value of slew rate and GBW. For this OTA, the minimum supply voltage value is $|V_{TH}| + 4|V_{DSsat}|$.

1.8.4 Comparison of super-class AB OTAs

As shown in section 1, current mirrors modify their current gain in dynamic conditions and generate large output currents that are proportional to V_{ID}^4.
In all topologies, the current mirrors must be carefully designed and biased in order to make the circuits suitable for low voltage operation because large variations in the gate voltage of M_6 and M_7 can switch off the input transistors M_1 and M_2 in Fig.1.17 (c) and (d) or the current source I_B in the FVFCS scheme in Fig.1.17 (a).
The voltage V_B that bias M_6 and M_7 near the boundary with the triode region in Fig.1.17 (b) and (c), or near the boundary with the saturation region in Fig.1.17 (c), is easily generated using bias replica bias technique.
V_B can be generated using a diode-connected transistor with a I_B current and with dimensions $\left(W/\left(1+\sqrt{2}\right)^2 L\right)$, $(W/4L)$,$(W/2L)$ in the case of Fig.1.17 (a) - (c), respectively, where in this case, (W/L) corresponds to the size of M_6-M_7-M_9-M_{10}.
The current mirror shown in Fig.1.17 (b) has the advantage over that of Fig.1.17 (a), that, when the input stage generates an increase of current, the $V_{DS6,7}$ voltage decreases and the excursion of the voltage at the gate of M_6 and M_7 is greater, resulting in increased current.
The OTA in Fig.1.17 (b) has a higher slew rate and GBW than the OTA in Fig.1.17 (a).
However, in the OTA of Fig.1.17 (a), when the gate voltage of M_6 and M_7 is pulled on, it does not force M_1 and M_2 out of saturation. Although the OTA in Fig.1.17 (c) has the best behavior in dynamic conditions, it is necessary to establish a comparison between OTAs at equal conditions in terms of quiescent current in the output branches.
This is obtained with $\beta_{5,8} = \beta_{9,10} \| \beta_{6,7}$ which reduces the maximum boost current. For all OTAs in Fig.1.17, the current yeld, defined as the percentage of power supply current that reaches the output, is close to the optimal value of 100%. The reason is that the high output current dynamics is generated directly in the output transistors, without internal replica. In conventional class A or class AB OTA with a unit ratio of the mirror output current, is 50% or less [17].

1.8.5 Stability of the OTA Super Class-AB

The general expression for the DC gain of the OTAs in Fig.1.17 is

$$A_{dc} = 2gm_1 gm_8 (r_{08} \,||\, r_{04}) \setminus G_{in}, \quad (1.31)$$

where G_{in} is the input conductance of the nonlinear current mirrors used. The 3dB cutting frequency is

$$f_{-3dB} = \frac{1}{[2\pi(r_{08}||r_{04})C_L]} \quad (1.32)$$

with C_L load capacitance (which includes the parasitic capacitances at the output node).

$$GBW = \frac{gm_1 gm_8}{\pi G_{in} C_L} \quad (1.33)$$

The poles introduced to the input nodes of nonlinear current mirrors are

$$f_p = \frac{G_{in}}{2\pi C_p} \quad (1.34)$$

C_P being the capacitance of these nodes (eg $C_P = C_{GS7} + C_{GS8}$, in Fig.1.17b). Thus, the phase margin PM of the OTAs in Fig.1.17 is approximately given by

$$PM \approx 90^\circ - arctg\frac{GBW}{f_p} \approx 90^\circ - arctg\left[\frac{2gm_1 gm_8}{G_{in}^2}\frac{C_p}{C_L}\right] \quad (1.35)$$

This formula allows to estimate the minimum value for G_{IN} that can be used for a given capacitive load (CL) in order to maintain stability. A low G_{IN} increases output current, but also lowers stability margin.

For small V_{ID}, the current mirror outputs are linear and $G_{IN} = G_{M8}$ so that the above parameters are similar to those of a conventional current mirror OTA. However, for large V_{ID} mirrors become nonlinear and G_{IN} decreases, reducing the phase margin.

1.9 Ramirez-Angulo and Baswa [5]

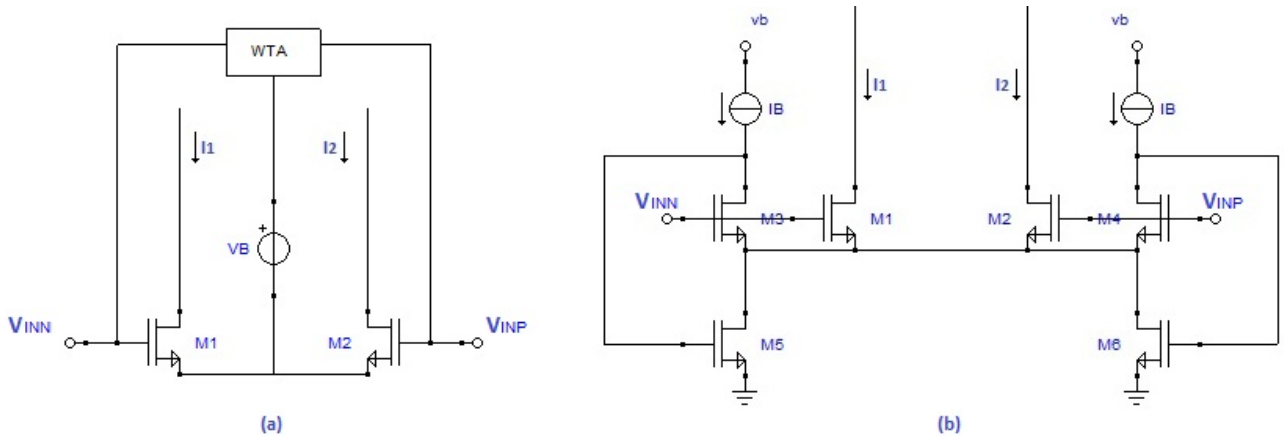


Fig.1. 18: (a) Basic diagram; (b) Implementation of WTA

Fig.1.18(a) shows a basic diagram of the class AB input stage proposed by Baswa. In Fig.1.18(b) the WTA (Winner Take All) block is replaced by double floating battery, used to set the voltage at the common source node of the input differential amplifier.

A Winner-Take- All (WTA) circuit generates the maximum value of the input voltages. Therefore, the voltage at the common source node is the maximum input voltage shifted by the constant voltage V_B. Under quiescent conditions, input voltages are equal, so that the maximum value corresponds to the common mode input voltage. Thus $V_{GS1}=V_{GS2}=V_B$, and quiescent currents are well controlled and determined by V_B.

If the input voltage V_{INP} decreases so than it is lower that V_{INN}, the common source node tracks the maximum input voltage, i.e., V_{INN}, and not the common-mode voltage of the inputs. Therefore, the resulting V_{GS2} is larger and therefore a larger transient current level is obtained.

Fig.1.18(b) shows a very efficient implementation of the WTA circuit. The basic cell employed is again a FVF cell, thus benefiting from its large sourcing capability and low voltage operation. Two FVFs, formed by transistors M_3- M_5 and M_4-M_6 and two current sources, are employed to generate a very low impedance node at the common source of M_1 and M_2. In this case, again $V_B = V_{GS3}$ and

the quiescent current is I_{BIAS}, assuming that transistors M_1, M_2, and M_3, M_4 are matched. Under application of a large differential voltage, dynamic currents I_1 and I_2 are generated, where one of them may be significantly larger than I_{BIAS}. Another advantage of the circuit in Fig.1.18(b) is that transistors are not driven in the cutoff region when an input signal is applied.

1.10 Ramirez-Angulo and Gonzalez-Carvajal [6]

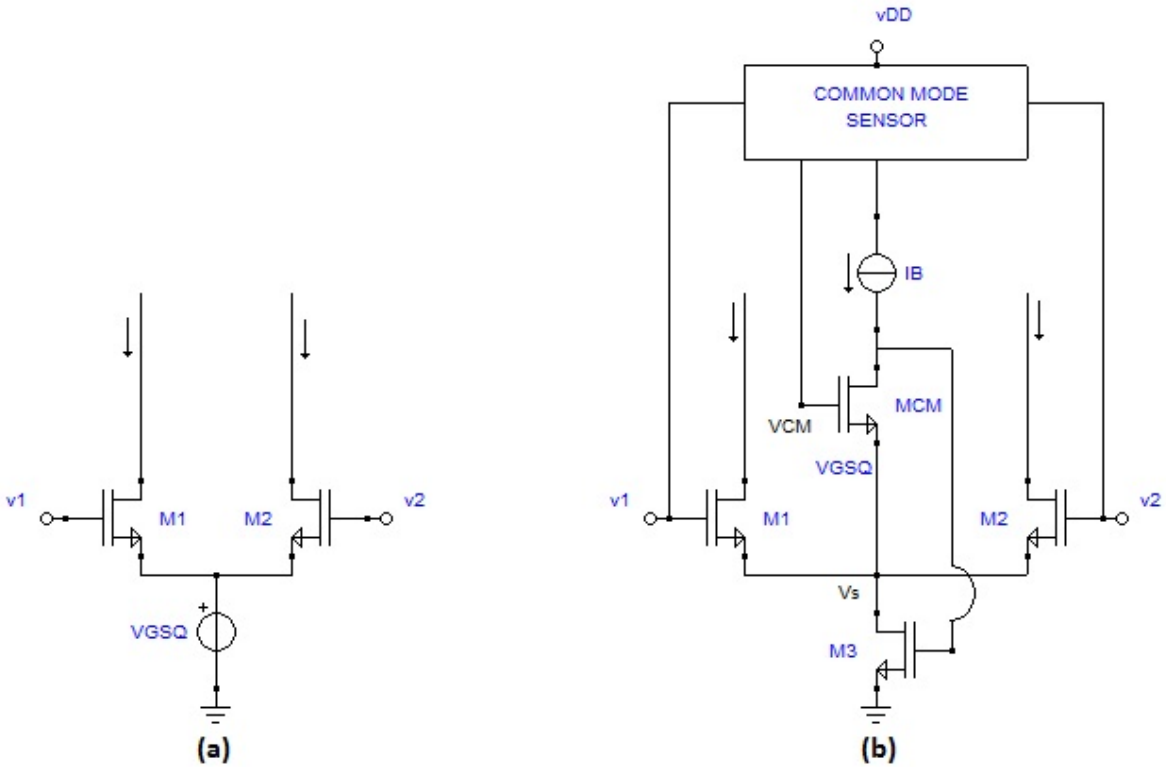


Fig.1. 19: class AB input differential stage: a) conceptual circuit; b) implementation

The conceptual scheme of the structure proposed by Ramirez-Angulo et al. is shown in Fig. 1.19(a), and its implementation in Fig. l.19(b). It operates also based on a gain enhanced (flipped) voltage follower formed by MCM and M_3. This circuit generates a very low impedance node at the common source node of M_1,M_2 and MCM. A common mode signal detector (shown as a black box in Fig.1.l9(b)) provides a signal VCM=$(V_1+V_2)/2$ at the gate of MCM. This signal represents the common mode component of the input voltages V_1 and V_2. The most important characteristic of this circuit is that only one half of the differential input signal Vd appears as a signal across each of the input transistors (V_{GSMl}=VGSQ-Vd/2 and V_{GSM2}=VGSQ+Vd/2). This results in lower supply voltage requirements VGSQ+V_{DSsat3}+$V_{dMAX/2}$ where V_{DSsat3}=V_{DSsatQ}+$V_{dMAX/2}$. In case the linearity is of concern (for example for high resolution delta sigma converters and for implementation of linear transconductors) cutoff of M_1 and M_2 must be avoided. In this case the minimum quiescent gate-source voltage of the input devices (M_l, M_2 and M_3) equals the maximum expected signal VSGS=V_{th}+V_{dMAX}.

An advantage of the structure in Fig.l.19(b) is that the quiescent voltage required to keep both input transistors active over the whole input differential range is reduced to VGSQ=$V_{dMAX/2}$+V_{Th}. This allows the use of lower bias currents. The implementation of the common mode signal detector of Fig.1.19(b) is shown in Fig.1.20. An even simpler implementation of the input common mode

sensor uses two equal valued resistors RCM connected between both opamp input terminals and the gate of MCM. This resistive implementation can be used only for continuous-time applications.

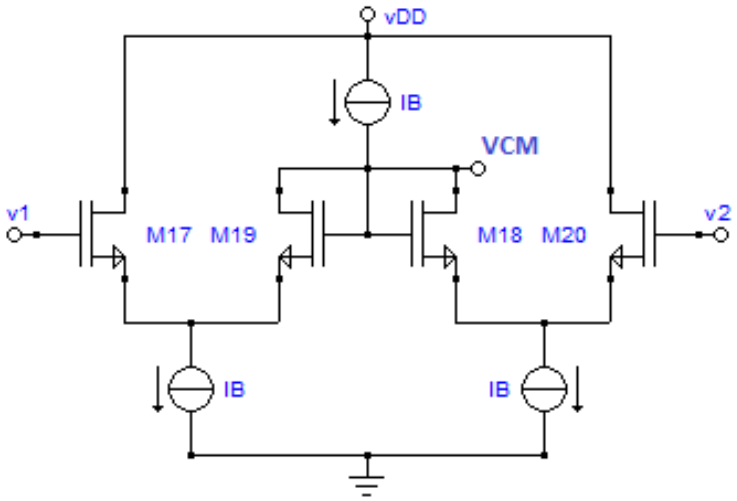


Fig.1. 20: Implementation of common mode sensing network

1.11 M. Yavari [25]

In this section, a single-stage class AB and a three path operational amplifier is illustrated, using a folded-cascode amplifier (FCA) in the signal path and a flipped voltage follower cell to achieve operation in class AB. This structure entails greater bandwidth, unit gain, DC gain, and large slew rate, all with the same power consumption of the folded cascode amplifier. The structure greatly improves the performance both at high signal and small signal of the traditional FCA.

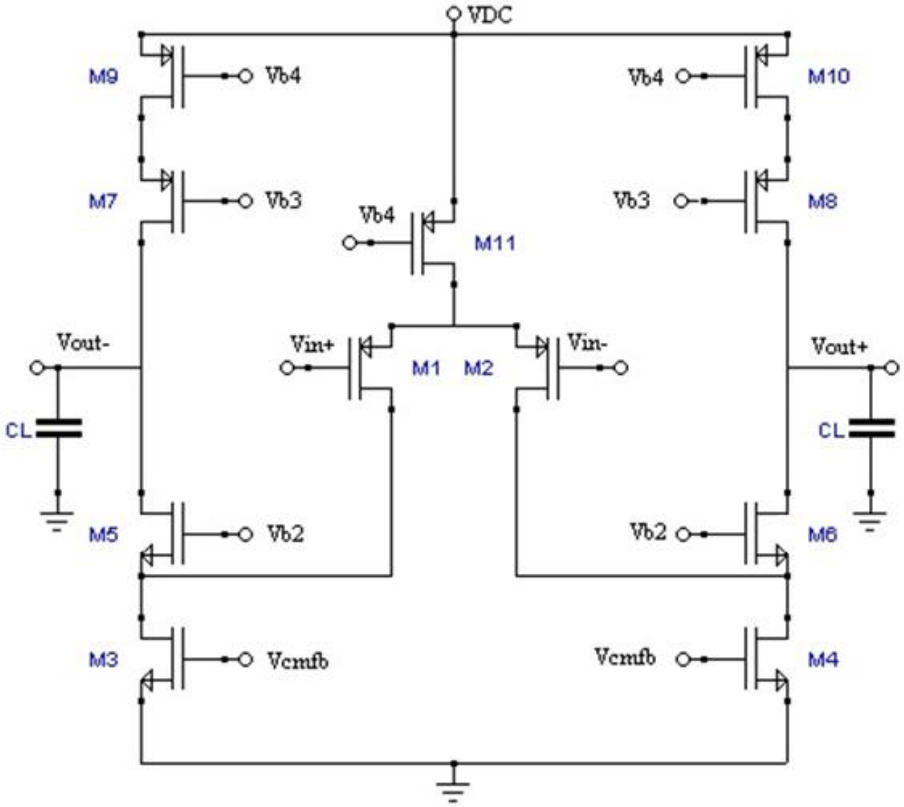


Fig.1. 21: Traditional folded-cascode amplifier

The folded-cascode amplifier (FCA) is tipically in low voltage applications either as a single stage or as the first stage of multistage amplifiers, as it achieves a high DC gain and a relatively large signal swing.

Furthermore, the pMOS input pair is preferable to nMOS for its lower flicker noise, higher non-dominant pole, and lower common input mode voltage [26].

However, as shown in Fig.1.21, in order to obtain a symmetric behavior in the slewing phase, the biasing current used in the input transistors and the cascode must be the same. As a result, the M_3 and M_4 devices must support the sum of the two currents.

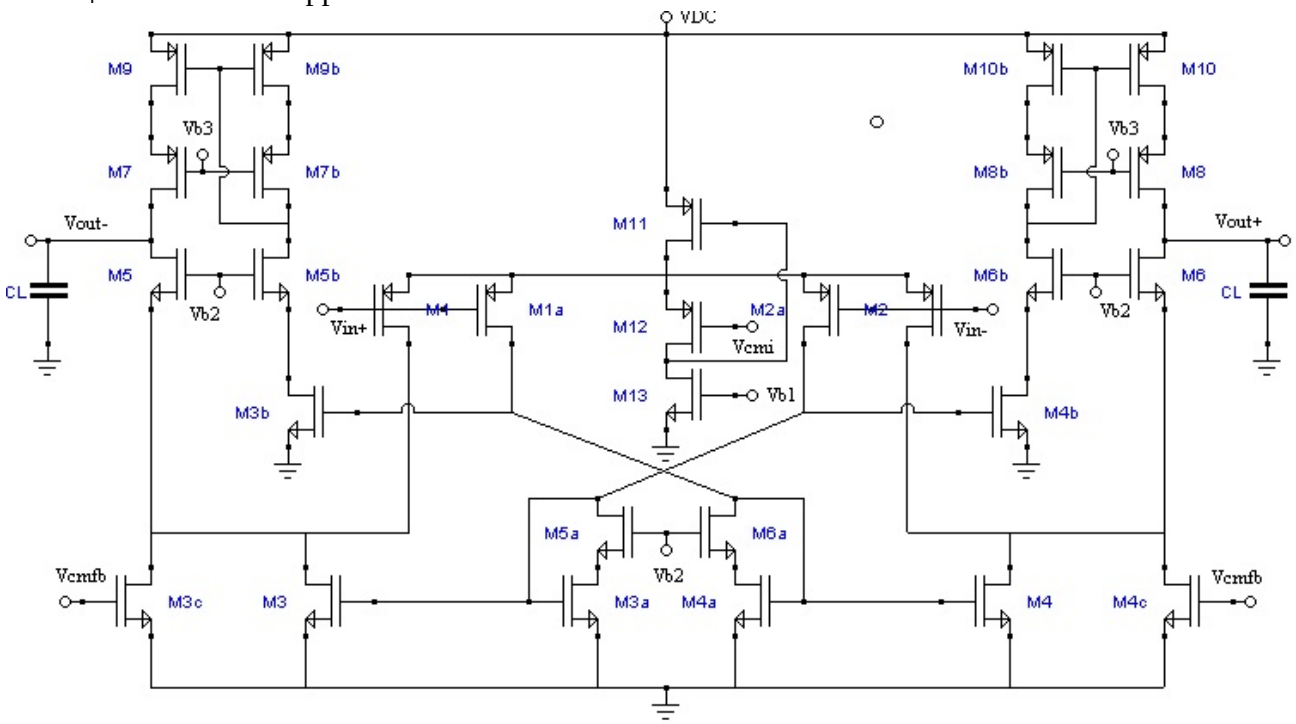


Fig.1. 22: Proposed structure of a single stage class AB amplifier

Fig.1.22 shows the amplifier being tested, the MOS M_1-M_{11} realizing the conventional FCA. The input transistors and nMOS of the current source are subdivided as M_1, M_{1a}, M_2, M_{2a}, M_3, M_{3a}, M_4 and M_{4a} to achieve a dual path amplifier as in [27]. M_{5a} and M_{6a} are used to form high-swing cascode current mirrors for better matching.

Another path is used to drive the gate of M_9 and M_{10}, this is realized by high-swing current mirrors made up of M_{3b}-M_{10b}. A flipped voltage follower (FVF) comprising the M_{11}-M_{13} transistors [28] is used to construct operation in class AB for both input transistors and cascode transistors. M_{3c} and M_{4C} devices are used to control common mode output voltage. V_{cmi} and V_{cmfb} respectively denote the common mode input voltage of the amplifier and the control voltage of the common mode output of the circuit. In fact, the proposed amplifier is constructed as the combination of three different amplifiers: a folded cascode amplifier and two different current mirror amplifiers.

Because of the class AB operation of the amplifier under test, a large slew rate independent of the biasing current can be obtained. If, for example, V_{in}+ is much larger than V_{in}-, M_1 and M_{1a} enter the cut-off region and the M_{2a} drain current is increased by a large factor depending on the input step amplitude.

This is because the source voltage of the input transistors is fixed by the FVF cell because the M_{12} drain current is constant and during the slewing phase the gate-source voltage of the input transistors is changed depending on their gate voltage variation.
Then, the M_{4A}, M_4, M_{3b}, M_{9b}, M_9 transistors turn off, while the M_{3a}, M_3, M_{4b}, M_{10b}, M_{10} drain current is increased. On the other hand, as M_4 goes out, the M_2 drain voltage increases, turning M_6 off. Therefore, the load capacitor on the positive output is charged by M_{10} and the load capacitor on the negative output is discharged by M_3. Therefore, you have:

$$SR^+ = \frac{mnI_{D2a}}{C_L}, \qquad SR^- = \frac{kI_{D2a}+I_{D3c}}{C_L} \tag{1.36}$$

where I_{D2a} is the M_{2a} drain current during the slew phase, and k, m and n are the aspect ratios of the current mirrors. Usually $I_{D2a}>>I_{D3c}$, mn = k is chosen for symmetric slew behavior. So the differential slew rate is given by:

$$SR \cong \frac{2kI_{D2a}}{C_L} \tag{1.37}$$

Moreover, during the negative slew you get a similar improvement in the value of the slew rate. The DC gain and the unit gain bandwidth of the amplifier in question are, respectively, given by:

$$A_{DC} = (gm_1 + kgm_{2a} + mngm_{1a})R_{out} = (1 + k + mn)gm_1R_{out} \tag{1.38}$$

$$\omega_1 \cong \frac{(gm_1+kgm_{2a}+mngm_{1a})}{C_L} = \frac{(1+k+mn)}{C_L}gm_1 \tag{1.39}$$

The total polarization current of the amplifier proposed is as follows:

$$I_{total} = 4I_a + I_{D12} + 2mI_a + 2mnI_a \cong (4 + 2m + 2mn)I_a \tag{1.40}$$

It is assumed that the input transistors of the amplifier and conventional FCA have the same aspect ratio and therefore have the same input parasitic capacitance and thus the same feedback factor in the closed loop configuration. With the same power consumption, the transconductance of their input transistors is given by:

$$gm_1 = \sqrt{\frac{1}{2+m+mmn}}gm_{1,fc} \tag{1.41}$$

where $gm_{1,fc}$ is the transconductance of the input transistors in the conventional FCA. Thus, the unit gain bandwidth and the DC gain of the amplifier in question are:

$$A_{DC} = A_{DC,fc}\frac{(1+k+mn)}{\sqrt{(2+m+mn)}}\frac{R_{out}}{R_{out,fc}} \tag{1.42}$$

$$A_{DC} = \omega_{t,fc}\frac{(1+k+mn)}{\sqrt{(2+m+mn)}} \tag{1.43}$$

However, the phase margin of the amplifier under exam is degraded compared to the FCA since it has more non-dominant poles introduced by the current mirrors. For high-speed applications, you must move the non-dominant poles at higher frequencies. This can be achieved by choosing ratios to get small currents. For example, considering m = 1, n = k = 2, both the DC gain and the unit gain bandwidth of the amplifier in question are improved by a factor $\sqrt{5}$ with respect to the conventional FCA.

1.12 J. Liang and D. A. Johns [29]

The circuit shown in Fig.1.23 was conceived by authors for applications requiring the use of over-sampled ADCs (delta-sigma). Since the latter require relatively high resolution and small bandwidth, the amplifier must provide a high gain.

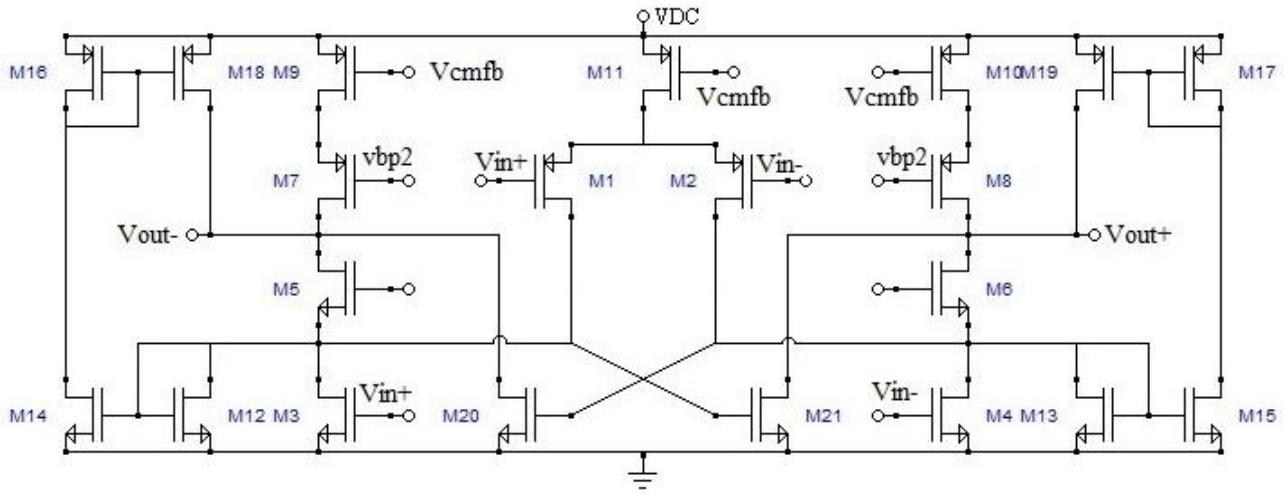


Fig.1. 23: Class AB pseudo operational amplifier.

To minimize power and noise, it was chosen to maximize the transconductance of the input of the operational amplifier. This can be achieved using class AB [30], [31] techniques combining the gm of complementary MOS devices. However, such circuits often require additional polarization networks such as level translators, or complicated networks for common mode control. To avoid this, a solution was chosen that fulfills most of the benefits of class AB project performance (see Fig.1.23).

The topology consists of a folded-cascode amplifier where the input differential pair ($M_1\backslash M_2$) and the current generators ($M_3\backslash M_4$) are driven by the applied input signal. The topology makes it possible to combine the gm of both pairs of devices. By assigning more current to the differential pair than to the folded network, the improvement of gm is significant. To improve the slew rate of the amplifier, a current mirror network was added that is turned on to provide additional current.

The network is controlled by devices connected to diode M_{12} and M_{13}, which only turn on when there is a large signal. An increase in slew rate reduces the duration of the settling time of the amplifier output.

This can relax the opamp bandwidth requirements as it has more time for linear settling.

1.13 H. A. Aslanzadeh and S. Mehrmanesh [32]

In this section, a new technique called "Slew Boost" is introduced to improve the large signal behavior in terms of settling time of the low voltage and low power class AB operating amplifier, more useful in switching capacitor circuits, in ADC pipeline converters and sigma delta modulators, etc.

The opamp in question is an improved version of the high-speed and low-voltage class AB amplifier topology proposed by the authors in [33], where the pole introduced by the mirror of the previous architecture has been eliminated using the configuration described in Fig.1.24. The input stage is replicated to provide two input-dependent signals for the two outputs of the amplifiers. The results in [33] show a fast settling for a small input step, but when applying a larger one, the settling time increases considerably.

To drive a large capacitive load, the output stage transistors (M_{18}, M_{19}, M_{28} and M_{29}) are designed with a great aspect ratio, which imposes a large capacitive load seen from the previous stage. The overall slew rate is limited by the slew rate of the previous stage. To counteract the degradation of settling time due to a large signal [33], a new technique called "Slew Boost" is applied to improve the step response time of the amplifier.

By employing the "Slew Boost" technique, there is an improvement of settling time in both the small signal phase and the large signal phase. The output transistors (M_{21} , M_{22}, M_{23} and M_{24}) are chosen in small size to improve the step response due to bandwidth limitation and expand the bandwidth of the opamp. Another stage called "Auxiliary" is made up of two large transistors that will be used by the opamp when it is necessary to increase the speed. In this technique, input signals are controlled. As long as the input signal remains small enough, no slew-boosting circuit is needed, so the auxiliary stage is off. When the input signal becomes large, the opamp should be able to operate the slew-boost circuit, the auxiliary stage consisting of large transistors added to the main amplifier.

The part of step response limited by small signal bandwidth will be improved due to the smaller size of the output transistors and the large signal behavior with slew limitation will be greatly improved due to the large pilot added to the opamp. Since output transistors (M_{21}, M_{22}, M_{23} and M_{24}) are small, the previous stage has a lower load and the slew-rate of the latter will not limit the overall slew-rate of the opamp.

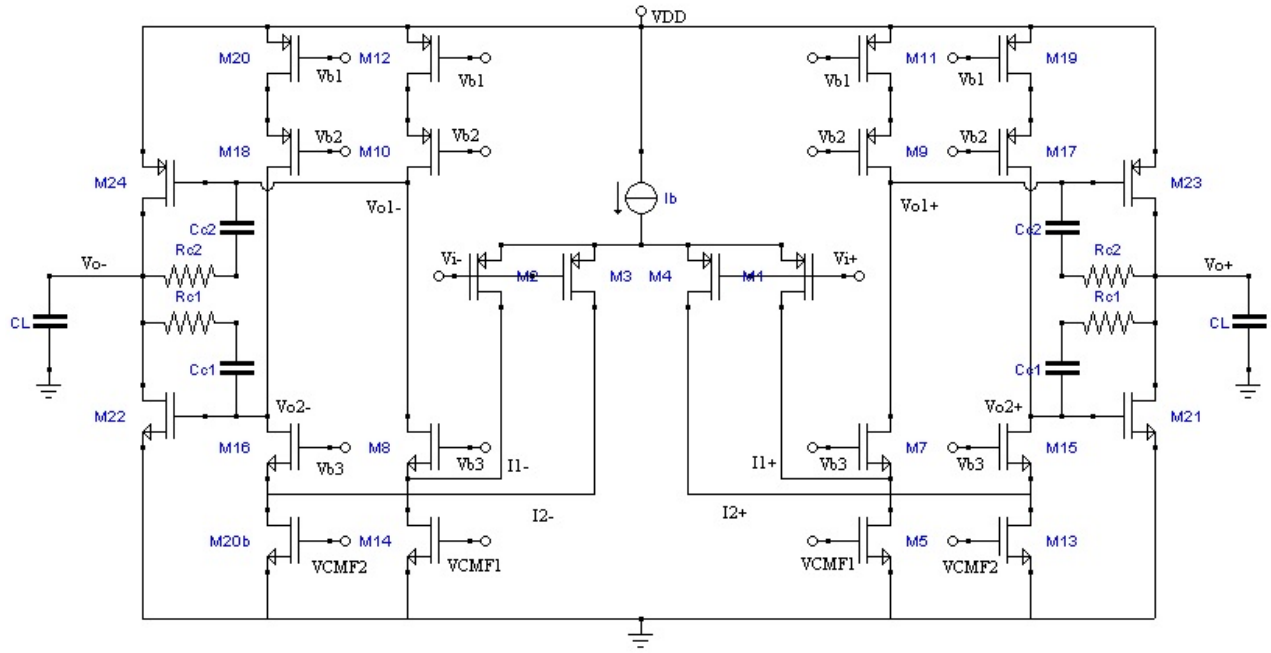


Fig.1. 24: Class AB operational amplifier used in [33] .

The common mode control circuit (CMFB) and the circuit to control the quiescent current are similar to those used in [33].

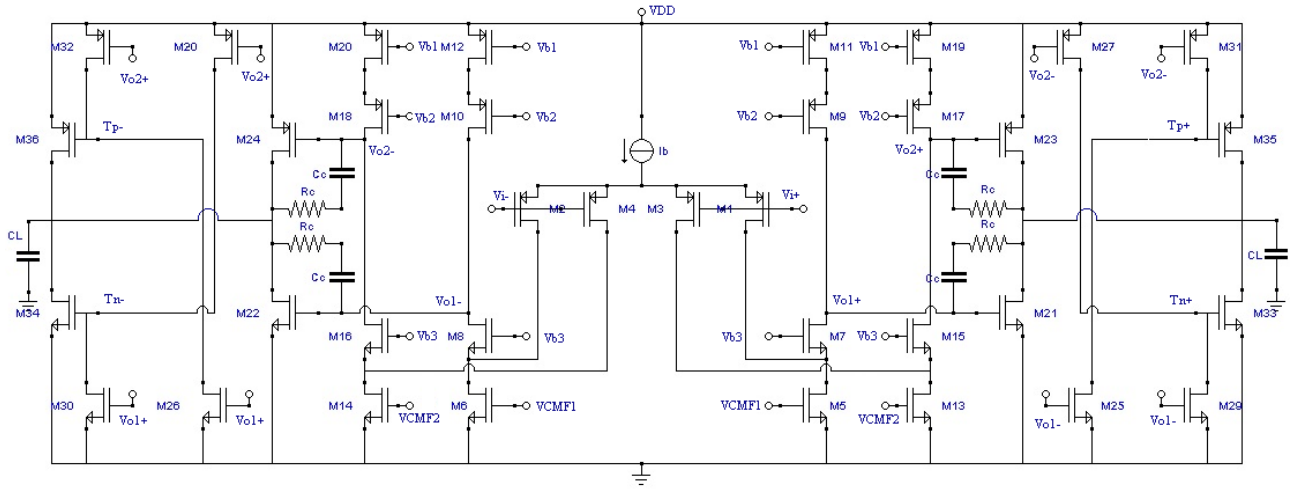


Fig.1. 25: Class AB operational amplifier that use “Slew Boost” technique

Fig.1.25 shows the full circuit of the opamp in question. The auxiliary stage consists of two current comparators controlling the outputs of auxiliary transistors. The devices, M_{29}, M_{30}, M_{31} and M_{32} (said threshold current generators) are dimensioned n times larger than their corresponding transistors M_{27}, M_{28}, M_{25} and M_{26} (so-called current source comparators), so that when opamp is in its normal polarization or when a small signal is applied, they act as two different current sources connected in series, forcing a V_{DD} voltage to the T_{p+} and T_{p-} nodes and a voltage equal to the negative node power supply to T_{n+} and T_{n-}.

Therefore in this state, the transistors PMOS M_{35} e M_{36} e M_{33} and the NMOS M_{34} are both off, and the auxiliary stage is transparent to the main circuit excluding a small capacitive load. The V_{0l}+ and V_{02}+ nodes "hear" a small capacitive load, and so can be high-speed nodes.
Furthermore, the signal received at the V_{0l}+ e V_{02}+ nodes passes through a cascode configuration to be amplified.
Since the cascode amplifier is a very suitable configuration for high-speed applications, this amplifier can be intrinsically fast [34]. When a large step is applied to the opamp, the devices for supplying an additional current will come into operation. By applying a positive voltage step between the nodes V_{i+} and V_{i-} and following the signal on the right side of the circuit, when the voltage of the V_{i+} node increases, the one at the V_{02}+,V_{0l}+ nodes decreases.
When the input signal becomes small, the auxiliary block will be turned off. Intermediate auxiliary nodes (T_p+, T_n+), as needed may vary from V_{eff} to V_{dd}-V_{eff} and provide a large output current so that the slew rate is greatly improved.

1.14 M. Fan and J. Ren [35]

The structure proposed in this section and illustrated in Fig.1.26 implements a new two-stage opamp type that works in class AB for both the input stage, for high gain, low power consumption and design simplicity respect to [36] and [37], and for the output stage to get a large dynamic range. With this structure, the gm transconductance of the two stages is doubled if compared to a "normal" configuration without class AB behavior with the same power consumption. The quiescent current can be small, and the one required for proper operation is dynamically increased [38], [39].

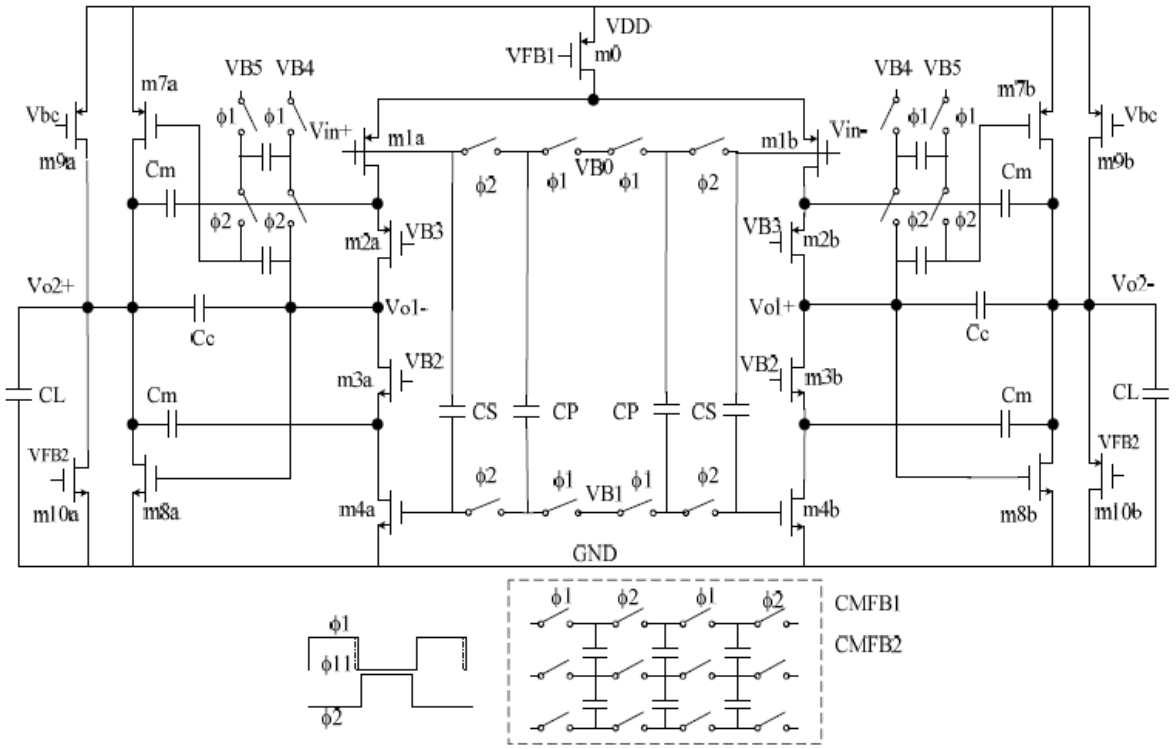


Fig.1. 26: Class AB operational amplifier.

The polarization principle that is exploited to achieve class AB behavior can be better understood if we consider the structure of Fig.1.27. V_{in1} and V_{in2} are set differently to obtain small saturation voltages ($V_{DS,sat}$) and to obtain a small quiescent current.

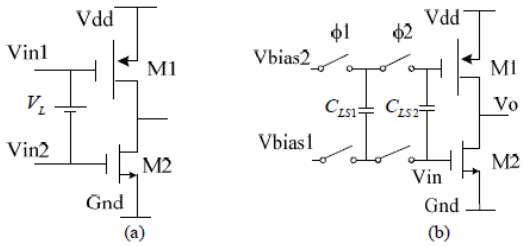


Fig.1. 27: (a) Polarization principle of a Class AB, (b) Polarization of a class AB using switched capacitor technique.

If V_{in1} is in direct relation with V_{in2}, for example, $V_{in1}=V_{in2}+V_L$, where V_L is the level shifter voltage, this voltage can be generated using a switching capacitor network with two not overlapping clocks ϕ_1 and ϕ_2, shown In Fig.1.18 (b); The voltage value V_L is the same for C_{LS1} and C_{LS2}:

$$V_L = V_{bias2} - V_{bias1} \quad (1.44)$$

To reduce the effects of parasitic capacitiance on the PMOS transistor node in Fig.1.18 (b), large capacitance must be chosen. In this structure, the equivalent transconductance is given by:

$$g_{in} = gm_1 + gm_2 \quad (1.45)$$

If theV_{GS}-V_{th} of M_1 is equal to that of M_2, the input transconductance is twice the same as the configuration of a class A amplifier that consumes the same current. Coming back to the structure of Fig.1.17, the CP, CS capacitors have such values as to minimize the effect of parasitic capacitor on the gates of M_{4a}, M_{4b}, M_{1a} and M_{1b}. By making overdrive voltages of M_{4a}, M_{4b}, M_{1a} and M_{1b} equal and the overdrive voltages of M_{8a}, M_{8b}, M_{7a}, M_{7b} equal, the input transconductance (gm_{input}) becomes:

$$gm_{input} = gm_1 + gm_4 = 2gm_1 \quad (1.46)$$

The output transconduttance (gm_{output}) becomes:

$$gm_{output} = gm_8 + gm_7 = 2gm_8 \quad (1.47)$$

gm_1, gm_4, gm_7, gm_8, gm_3, are the transconductances of M_{1a}, M_{4a}, M_{7a}, M_{8a}, M_{3a}, respectively. In this way, the transconductance is doubled without any increase in current. Since there is a large ratio between the dynamic current and the quiescent current, when it is in class AB operation, the transconductance of the stage varies over a wide range.

Therefore, the use of normal Miller compensation or the cascode Miller compensation is not enough to keep the opamp stable.

A nested cascode Miller compensation is employed here to cope with the headache problem and a very good frequency response is reach by this method [40].

Compared to a traditional two-stage low voltage amplifier in which Miller cascode compensation is used, the architecture under consideration saves current tanks to the elimination of two cascode circuits [41]. In the following, poles and zeros of the amplifier in question will be presented. The dominant P_1 pole is given by:

$$p_1 = -\frac{1}{r_{01}r_{02}gm_2gm_8r_{08}(C_m+C_c)} \quad (1.48)$$

where r_{01}, r_{02}, r_{08}, are the resistances of M_{1a}, M_{2a}, M_{8a}, respectively. The site of the first non dominant pole P_2 is:

$$p_2 = -\frac{gm_8}{(C_\pi+C_L)+\left(1+\frac{C_{g8}}{C_c}\right)}\left(\frac{C_m+C_c}{C_c}\right) \quad (1.49)$$

C_{gs} represents the total parasitic capacitance of the gate of transistor M_{8a}, which is the same as the transistor M_{8b}. C_m and C_c are Miller's capacitance, C_L is the load capacitance. The second non-dominant pole P_3 is:

$$p_2 = -gm_3\left(\frac{C_m+C_L}{C_L}\right) \quad (1.50)$$

The unit gain frequency, which is equal to the gain bandwidth product (GBW), should be fixed at 1/3 P_2 to have a good phase margin [38] so that:

$$\mathrm{GBW} = \frac{2gm_1}{C_m+C_c} = \frac{1}{3}P_2 \quad (1.51)$$

An additional zero is at a frequency:

$$Z = -\left(\frac{gm_3}{C_m}+\frac{gm_3}{C_c}\right) \quad (1.52)$$

The minimum damping of the system is given by:

$$\xi_{min} \cong \sqrt{\frac{C_M}{C_M+C_c}} \quad (1.53)$$

From expression (1.53), the damping of the poles is always greater than 0.7 when the value of C_m is greater than that of C_c, which means that the peak will never occur [40]. Another important aspect to consider is the common mode feedback of the opamp under consideration. As the two-stage common mode output modes of the proposed operational amplifier are set independently, two independent common mode feedback loops (CMFBs) are needed to determine common mode voltages for the first and second stage outputs. The CMFB circuit adopted consists of a symmetric switching capacitor network [42], which has several benefits, such as faster settling time, low charge and dispersion error, than the simple and traditional switched capacitors network [41].

In the second stage, the output common mode voltage is used to control two additional common source amplifiers M_{9a}, M_{10a} e M_{9b}, M_{10b}, which drive output nodes to maintain stable common mode voltage. There are usually two ways to control the common output voltage [37], [41], which are shown in Fig.1.28.

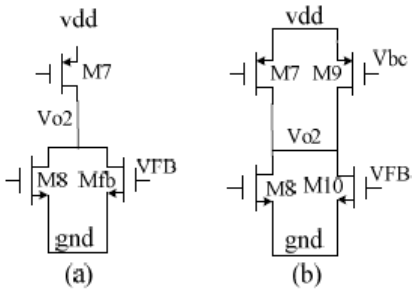


Fig.1. 28: Two ways to realize the CMFB of the class AB output stage.

In the way shown in Fig.1.28(a), the transconductance of M_7 is greater than that of M_8 with the same V_{DSsat} because the current in M_{fb} has to pass through M_7. However, in the circuit of Fig.1.28(b), the current through the feedback transistor M_{10} is generated mainly by the transistor M_9 which is biased with an appropriate voltage V_{bc}. In order to have good stability and fast feedback operation, the common source add-on for the second CMFB stage should consume at least one fifth of the current through the second stage. Even if it turns out to be a great amount, to get great bandwidth and high speed, it's worth it.

Chapter 2

Analysis and comparison of class AB current mirror OTAs

From the study carried out in the previous chapter, we have seen several ways to implement a class AB OTA. Of all the topologies seen in Chapter 1, I want to narrow the field of action to single stage fully-differential OTAs of symmetric type, as they are suitable for operation at low supply voltages and with low power consumption. It provides a simpler way to cope with variable currents, and are therefore composed of a differential transconductor whose output currents are not limited and are mirrored to the output branches. As seen in Chapter 1, Castello in [1] proposed a transconductor topology based on four transistors with cross-coupled source terminals, but most of the topologies in the literature are based on a differential pair with an adaptive bias current that is a function of the input differential signal [2]-[3], or on a pair of transistors whose source terminals are fed with a copy of the input signal with a polarity opposed to the one on the gate [4]-[5].
In order to compare the class AB OTA topologies, I need figures of merit (FOMs) and in literature I have found some definite ones. Harjani et al. in [6] and Pennisi et al. in [7] have proposed some figures of merit to compare these topologies in the case of a single-ended output OTA. Centurelli et al. in [8] have extended the FOMs to the case of differential output.
In this Chapter I analytically compare class AB single stage OTAs using the FOMs which take into account small signal parameters and large signal parameters. From the choice criterion stated at the beginning and from what has been seen in Chapter 1, four ways have emerged to obtain a single-stage amplifier that operates completely in class AB, which is fully-differential and of symmetrical type, and which is suitable to operate at low supply voltages and with low supply power consumption.
Therefore, four class AB Current Mirror OTAs will be analytically compared in terms, of power consumption, speed, bandwidth and CMRR.

2.1 Fully differential symmetrical OTAs

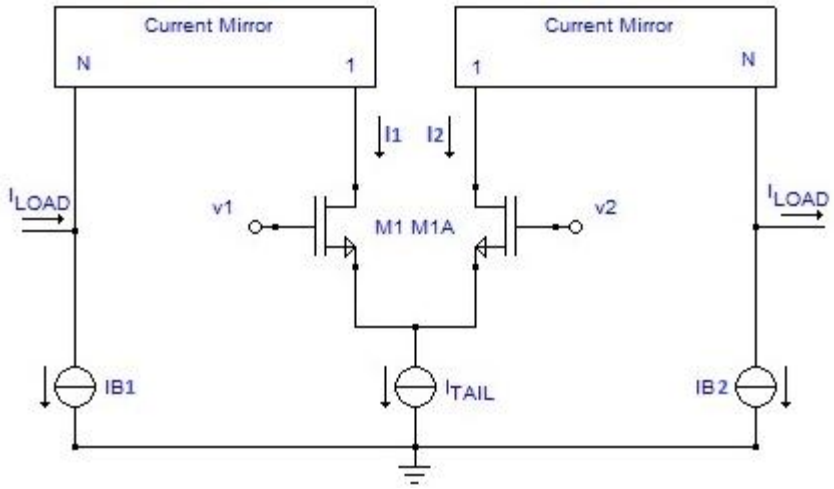


Fig.2. 1: General model of a fully differential symmetrical OTA

The simplest way to realize a fully differential symmetrical OTA is represented in Fig.2.1. In the fully differential implementation, the current sources I_{B1} and I_{B2} can be controlled by a common-mode feedback (CMFB) loop Fig.2.2, or can be obtained by a suitable mirroring of signal currents, as shown in Fig.2.3.

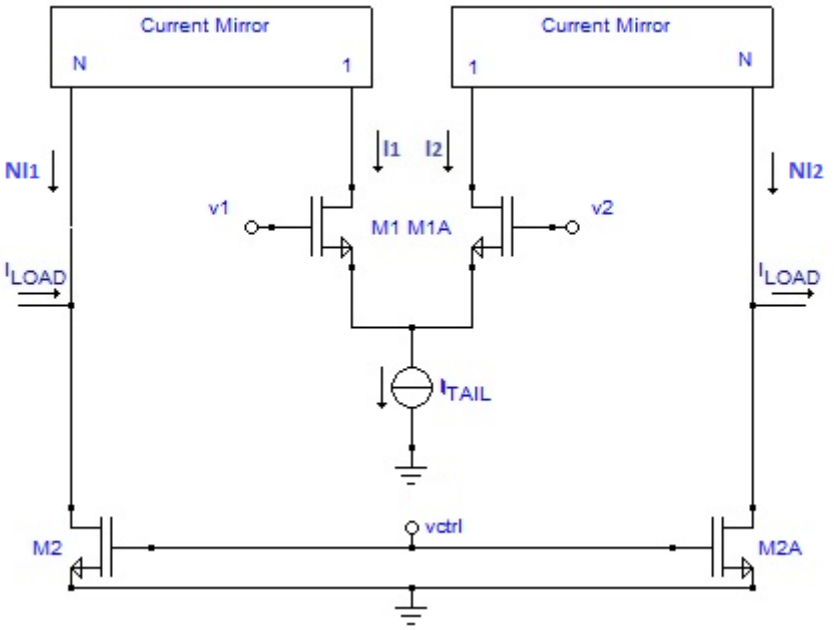


Fig.2. 2: Fully differential class A symmetrical OTA

In a single-ended implementation, I_{B1} and I_{B2} can be substituted by a current mirror to provide a single output. In the single stage OTAs the class of work A or AB is established by the manner to realize the input transconductor and in particular its tail current source.

If I choose the use of the differential pair as input transconductor, as shown in Fig.2.1,Fig.2.2 and Fig.2.3, I can decide to make the tail current source as fixed or variable. If I decide that the tail current source has to provide a fixed current, it means that the OTA works in class A, otherwise in class-AB if I decide to make the tail current source variable.

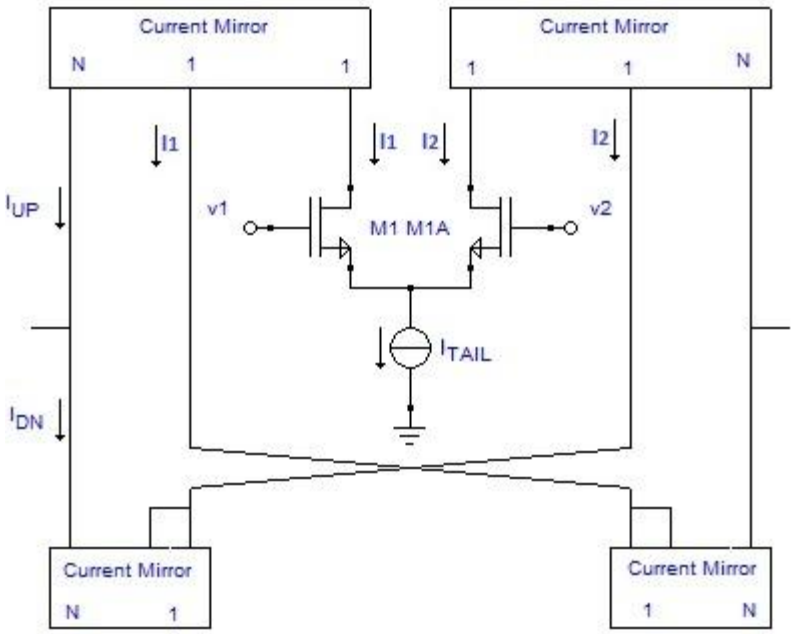


Fig.2. 3: Enhanced fully differential symmetrical OTA

2.1.1 Symmetrical class A OTA

As seen in the previous section, the choice of how to make the tail current source determines the work's class of the differential transconductor. Then, if in Fig.2.2, Fig.2.3 the bias current I_{TAIL} is constant I have two possible ways to realize a fully differential class-A OTA. I assumed that I_{TAIL} value is equal to I_B.

The static current that flows in the input branches is:

$$I_1 = I_2 = \frac{I_B}{2}, \quad (2.1)$$

while the static current that flows in the output branches is:

$$I_{Qout} = N\frac{I_B}{2} + N\frac{I_B}{2} = NI_B$$

where N is current mirrors gain. (2.2)

The total current that flows in the OTA will be given by the sum of all current contributions due to each branch. From the scheme in Fig.2.2, the total current is given by:

$$I_{Qtot} = I_1 + I_2 + I_{LOAD1} + I_{LOAD2} = \frac{I_B}{2} + \frac{I_B}{2} + N\frac{I_B}{2} + N\frac{I_B}{2} = I_B + NI_B = (1+N)I_B \quad (2.3)$$

From the scheme in Fig.2.3, I have two additional branches and then the quiescent total current of the OTA is given by:

$$I_{Qtot} = 2I_1 + 2I_2 + I_{LOAD1} + I_{LOAD2} = 2\frac{I_B}{2} + 2\frac{I_B}{2} + N\frac{I_B}{2} + N\frac{I_B}{2} =$$

$$= 2I_B + NI_B = (2+N)I_B \quad (2.4)$$

where I assumed that the mirrors' gain for the additional branches is equal to α=1.

The peak output differential current, for the circuit of Fig.2.2, is:

$$I_{loadMAX} = N\frac{I_{TAIL}}{2} = N\frac{I_B}{2} \quad (2.5)$$

The peak output differential current, for the circuit of Fig.2.3, is:

$$I_{loadMAX} = 2N\frac{I_{TAIL}}{2} = NI_B \quad (2.6)$$

The OTA in the fully differential implementation needs a CMFB circuit to fix the output common-mode voltage and then I suppose that the static quiescent currente in the CMFB circuit is equal to γI_B for normalization reasons. In virtue of these considerations, in the calculations of the total

current (I_{Qtot}) I must take into account the latter contribution due to the CMFB circuit. The equations (2.3) and (2.4) become respectively:

$$I_{Qtot} = I_1 + I_2 + I_{LOAD1} + I_{LOAD2} + I_{CMFB} = I_B + NI_B + \gamma I_B = (1 + N + \gamma)I_B \quad (2.7)$$

$$I_{Qtot} = 2I_1 + 2I_2 + I_{LOAD1} + I_{LOAD2} + I_{CMFB} = 2I_B + NI_B + \gamma I_B = (2 + N + \gamma)I_B \quad (2.8)$$

2.1.2 Symmetrical class AB OTA

As for the class A OTA in the previous section, the differential transconductor can be thought in its simplest form as a differential pair (Fig.2.1-2.3) but in this case the tail current source is function of the input signal. In this manner I have a class AB architecture that presents a low static current, that however has to be compatible with the required small-signal ac performance, that is mirrored N times larger in the output branches. When a large differential input signal is applied, an output current much larger than the quiescent current of the output branches is provided to the load, thus allowing fast transients.

For a class AB OTA, the formulas (2.1) and (2.2) defined in the previous section are still valid. For a class AB OTA there is additional static current in the circuit used for adaptive biasing of the input transconductor: I define this current as βI_{TAIL}. I must take into account the latter contribution due to the adaptive polarization circuit. The equations (2.7) and (2.8) become respectively:

$$I_{Qtot} = I_1 + I_2 + I_{LOAD1} + I_{LOAD2} + I_{CMFB} = I_B + NI_B + \gamma I_B = (1 + N + \gamma + \beta)I_B \quad (2.9)$$

$$I_{Qtot} = 2I_1 + 2I_2 + I_{LOAD1} + I_{LOAD2} + I_{CMFB} = 2I_B + NI_B + \gamma I_B = (2 + N + \gamma + \beta)I_B \quad (2.10)$$

The peak output differential current for a class AB OTA is not limited as its class A counterpart. I can write, that:

$$I_{loadMAX\_AB} > I_{loadMAX\_A} \quad (2.11)$$

Suitable (FOMs) for a class AB OTA therefore have to take into account the ratio between peak and quiescent current, that relates transient response and power consumption, the small signal bandwidth and dc gain. The fraction of total current that flows in the output stage is also of interest to allow a comparison of total power consumption. In case of fully differential OTAs, common-mode gain or common-mode rejection ratio (CMRR) are further parameters that have to be taken into account, still more in a class AB implementation where differential to common-mode conversion is likely to happen.

2.2 Figures of merit (FOMs)

In this section the FOMs for class A-AB symmetrical OTAs in the fully differential case are presented. On the basis of these FOMs, I will compare the selected topologies.

The FOMs are nothing more than metrics that allow to objectively measure the performance of different topologies of OTA. Then, the metrics represent the tools necessary for the objective application to the performance verification. The specific ways of using each metric are determined from time to time depending on the type of performance that I want to evaluate. In the following, general FOMs will be defined such as efficiency factors (F_C) and slew rate factor (F_R) and subsequently I will define the related quality factors (Q) where these FOMs are compared to the ones of a class A case. The FOMs are more generic and they can be applied to all topologies while the quality factors are related to particular types of structures . In particular to use quality factors will be established a reference topology, for example of a symmetrical class-A OTA in its simplest form.

Then, below I will introduce the FOMs and related quality factors and for both I will consider the topology shown in Fig.2.3.

2.2.1 Quiescent current efficiency factor (F_C)

To compare different class AB Current Mirror OTAs in terms of power consumption, I need a figure of merit that will consider the fraction of the total quiescent current supplied by the power supply delivered to the output branch I_{Qout}, and the total quiescent current provided by the power supply I_{Qtotal}. Then I define the quiescent current efficiency factor (F_C) as:

$F_C = I_{Qout} / I_{Qtotal}$ (2.12)

It is apparent that the higher the value of F_C, the better is the performance of the circuit, since for a given quiescent current I_{Qout}, a circuit with higher F_C requires lower I_{Qtotal}.

Also for a class A Current Mirror OTA, the quiescent current efficiency factor, $F_{C,A}$ is defined, which is always higher than in a generic class AB current mirror OTA. Taking into account that I_{Qout} (2.2) and I_{Qtotal} (2.8) have been calculated in section 2.1.1, I can write:

$$F_{C,A} = \frac{N}{(2+N+\alpha+\gamma)} \quad (2.13)$$

whereas for the case where I_{B1} and I_{B2} are constant currents controlled by the CMFB, in the scheme of Fig.2.3 I would have α=0 (where α is the static current in the CMFB circuit). In this case F_C is given by:

$$F_{C,A} = \frac{N}{(1+N+\gamma)} \quad (2.14)$$

2.2.2 Slew Rate Factor

The purpose of using OTAs in class AB is to provide much current when it is needed and much less in quiescent condition.

Slew Rate Factor (F_{SR}) is a parameter related to the ability of class AB stages to cope with large input signals, and is given by the ratio

$F_{SR} = I_{loadMAX} / I_{Qout}$ (2.15)

between the peak current on the load and the quiescent current of the output branches. For a class A symmetrical OTA, the quiescent current in the output branches is $N \cdot I_{TAIL}$, where I_{TAIL} is the tail current of the input differential pair, N is the current mirrors gain, and the peak output differential current is $N \cdot I_{TAIL}/2$ if I_{B1} and I_{B2} are constant, or NI_{TAIL} if they are signal dependent as for example in Fig. 2.3. We consider just this latter case in the following, since it reflects what is usually done in the class AB case, so we can write for the class A fully differential OTA:

$F_{SR,A} = 1$ (2.16)

2.2.3 Quiescent power quality factor (Q_C)

To compare class AB Current Mirror OTAs in terms of the quiescent current efficiency, which also allows to compare the topology with the more simple class A OTA having the same transistor aspect ratios and equal I_{Qout}, we define the quality factor, Q_C, as the ratio between F_C and $F_{C,A}$. From (2.12) and (2.13), we get

$$Q_C = \frac{F_C}{F_{C,A}} = \frac{(2+N+\gamma)I_{TAIL}}{I_{Qtotal}}. \quad (2.17)$$

Q_C is always less than unity since class AB topologies are supplied by a total current greater than that of the class A counterpart.

2.2.4 Quality Factor for Slew Rate

The quality factor for the slew rate (Q_{SR}) is given by the ratio of F_{SR} that refer to a class AB (2.15) and the F_{SR} that refer to a class A (2.16).

$$Q_{SR} = F_{SR} / F_{SR,A} = F_{SR} . \quad (2.18)$$

2.2.5 Bandwidth quality factor (Q_{BW})

Since dynamic performance of a class AB OTA is affected by both slew rate and small signal behavior, [7] introduces a further quality factor as the ratio between the bandwidth of the OTA and that of its class A counterpart, for the same dc gain.

$$Q_{BW} = BW_{AB} / BW_{A} . \quad (2.19)$$

2.2.6 Common mode quality factor (Q_{CM})

In a fully differential implementation, a further parameter to be taken into account is the common mode gain, both in the light of differential to common-mode conversion, and for the fact that a feedback that is negative for the differential mode could be positive for the common mode (it is the case of the symmetrical OTA, if a further inverting stage is not used). Common-mode quality factor is defined as the ratio of the common mode gain of the class AB and class A OTAs, or equivalently as the ratio of their CMRRs, since we are assuming the same differential gain:

$$Q_{CM} = A_{cmAB} / A_{cmA} = CMRR_{AB} / CMRR_{A} . \quad (2.20)$$

It has to be noted that the common mode gain of the fully differential OTA is affected by the CMFB, that reduces its value improving the CMRR; however, for simplicity we will use the open loop (i.e. without CMFB) common mode gain to define the FOM.

2.3 Comparison of selected class AB topologies

In this Section, we analyze some class AB fully differential OTAs presented in Chapter 1, with a particular focus on topologies that have been implemented in recent years in low voltage short channel technologies. The topologies we consider are representative of a wide class of class AB current mirror OTAs: in particular, we consider the topology by Peluso [4] where flipped voltage followers (FVFs) are used to apply the signal also to the source of the input transistors, the topology by Ramirez-Angulo [9] that exploits a FVF to achieve adaptive biasing of the differential pair, and the topology by Baswa [10] that achieves adaptive biasing through a winner-take-all (WTA) circuit. We take also into account the topology presented by Castello in [1], since it presents interesting properties for fully differential applications.

In all cases, FVF current mirrors are used in branches with three or more stacked devices, to allow low voltage operation and maximize dynamic range, and current reuse techniques with floating current generators are exploited to minimize power consumption. Current sources I_{B1} and I_{B2} are made signal dependent, by using additional current mirror branches as in Fig. 2.3, or by exploiting features in the adaptive biasing techniques.

2.3.1 A. **Castello et al. class AB topology [1]**

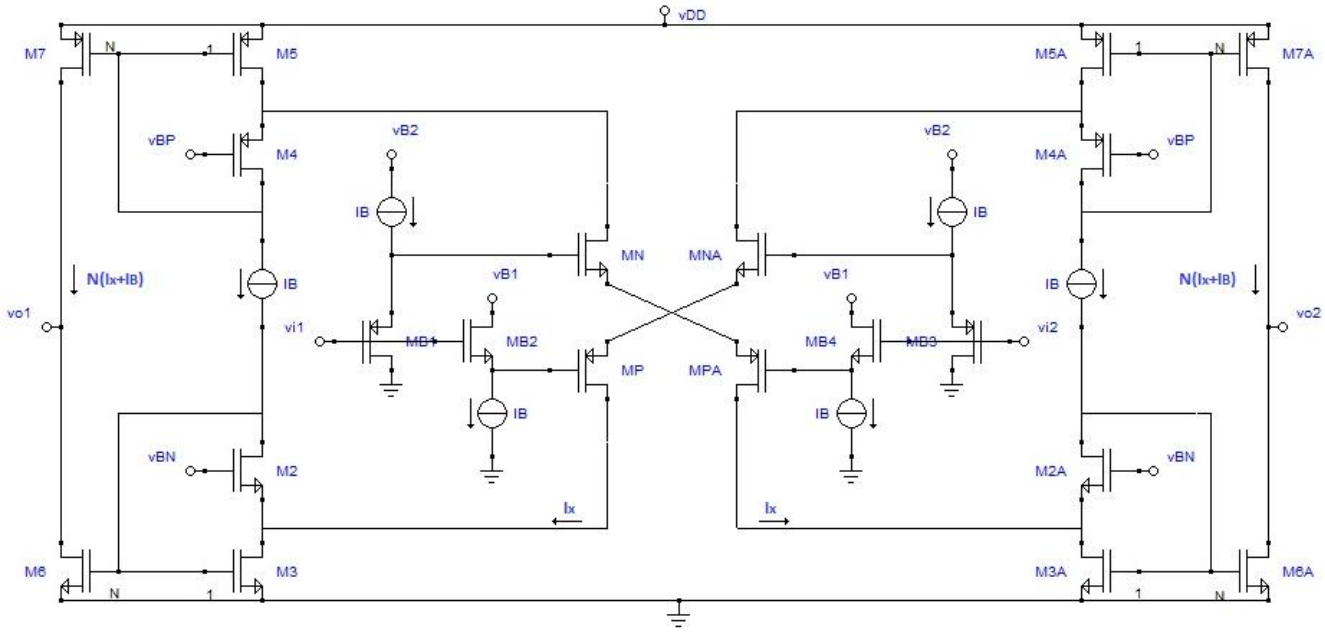


Fig.2. 4: Fully differential class AB OTA based on topology by Castello

The class AB input stage introduced by Castello et al. in [1] is based on four transistors with cross-coupled source terminals. Input level shifters are needed to drive the transistors, and they can be implemented as shown in Fig. 2.4 or by switched-capacitor structures, for applications where this is suitable. The four drain currents are mirrored to the output branches, thus easily making current sources I_{B1} and I_{B2} of Fig.2.1 signal dependent. This doubles the differential gain and improves CMRR, but a CMFB (not shown in Fig.2.4) is still required to set the correct output common mode voltage.

FVF current mirrors are mandatory in low-voltage applications due to the four stacked devices in the input branches.

The quiescent current of the cross-coupled devices is calculated in Appendix (A.2) and so I can write:

$$I_Q = k_{eff}(V_{GN} - V_{GP} - V_{Tn} + V_{Tp})^2 \quad (2.21)$$

where V_{GN} and V_{GP} are the dc voltages on the gates of MN and MP respectively, and

$$k_{eff} = \left(\frac{\sqrt{k_n k_p}}{\sqrt{k_n}+\sqrt{k_p}}\right)^2 \quad (2.22)$$

To calculate F_C I need to know the quiescent current flowing in the output branches and the total quiescent current flowing into the OTA as seen in section 2.2.1. With reference to Fig.2.4 I can write:

$$I_{QOUT} = 2N(I_B + I_x) \quad (2.23)$$

$$I_{QTOT} = 2N(I_B + I_x) + 2I_B + 2I_x + 2\beta I_B + 2\gamma I_B \quad (2.24)$$

where the current of the input level shifters has been expressed as $2\beta I_B$ (β=2 in Fig.2.4) and the current contribution of the CMFB has been expressed as $2\gamma I_B$.

By assuming for simplicity that I_Q and I_x are chosen equal to I_B, the quiescent current efficiency factor can be calculated using (2.12) as seen in section 2.2.1. Then I can write:

$$F_C = \frac{2N}{2N+2+\beta+\gamma} \quad (2.25)$$

When the circuit is unbalanced, two of the cross-coupled devices are off, and the other two draw a current which depends on the square of the input differential voltage V_{id}:

$$I_1 = k_{eff}(V_{id} + V_{GN} - V_{GP} - V_{Tn} + V_{Tp})^2. \quad (2.26)$$

The maximum current is limited by the maximum input voltage: the level shifters limit the input dynamic range, and assuming an input common mode level of $V_{DD}/2$, from the calculations carried out in the Appendix (A.3), I get

$$F_{SR} = \frac{k_{eff}\left(V_{DD} + \sqrt{\frac{I_B}{k_{eff}}} - V_{LS}\right)^2}{4I_B} \quad (2.27)$$

where

$$V_{LS} = (V_{GN} - V_{GP})/2 \quad (2.28)$$

is the voltage shift imposed by the input level shifter. The quality factor for slew rate defined by (2.18), for the previous choices, is equal to the slew rate factor (F_{SR}). A small signal analysis of the circuit in Fig.2.4 shows that, for the same bias current of the input stage and the same mirroring factor N, the differential gain is the same as the one of the class A OTA in Fig.2.4 if

$$g_{meff} = \frac{g_{mn}g_{mp}}{g_{mn} + g_{mp}} \quad (2.29)$$

is equal to g_{m1}. The FOM defined by (2.19), that is the ratio of the unity-gain bandwidths of this stage and of a class A stage, is therefore

$$Q_{BW} = 1 . \quad (2.30)$$

It has to be noted that the input level shifter adds a pole to the transfer function, that could lower the phase margin of the OTA.

The Common Mode Rejection Ratio (CMRR) calculated in Appendix (A.3) is equal to:

$$\frac{g_{m3}g_{m7} + g_{m5}g_{m6}}{g_{m3}g_{m7} - g_{m5}g_{m6}} \frac{1}{1/A_{0n} - 1/A_{0p}} \quad (2.31)$$

where A_{0n} and A_{0p} are $gm_N r_{oN}$ and $gm_{PA} r_{oPA}$ respectively.

2.3.2 B. Peluso et al. class AB topology [4]

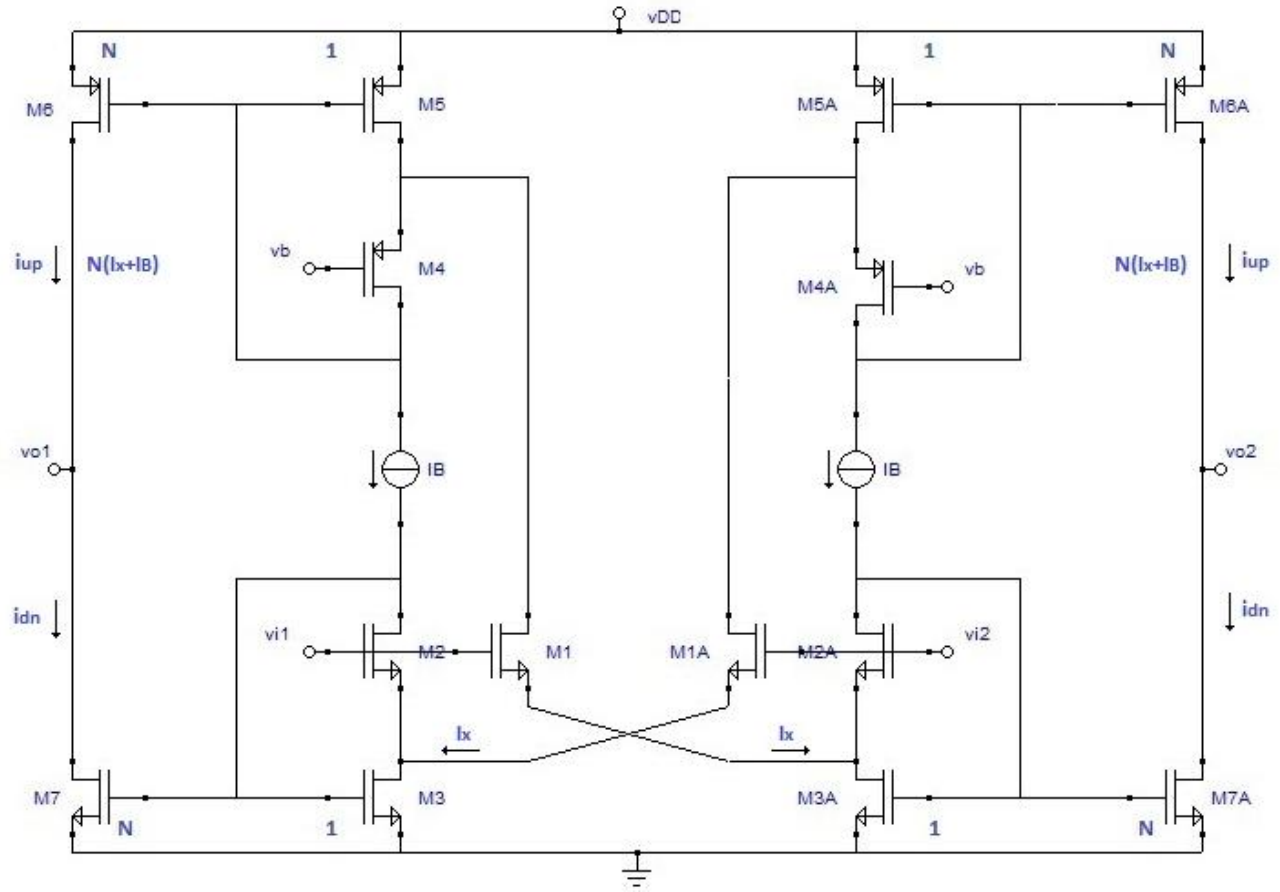


Fig.2. 5: Fully differential class AB OTA based on the topology by Peluso

The class AB topology by Peluso et al. presented in [4] exploits level shifters to apply signals to the sources of the input devices with opposite polarity with respect to that applied to the gates. This arrangement and the use of FVFs allow to provide large currents to the load when the circuit is unbalanced, achieving class AB behavior.

To calculate F_C, defined by (2.12), I need to know the quiescent current flowing in the output branches and the total quiescent current flowing into the OTA.

$$I_{QOUT} = 2N(I_B + I_x) \quad (2.32)$$

$$I_{QTOT} = 2N(I_B + I_x) + 2I_B + 2I_x + 2\gamma I_B \quad (2.33)$$

As in previous section, the current contribution of the CMFB has been expressed as $2\gamma I_B$ for normalization reasons.

The topology is shown in Fig.2.5 and I assume that M_1 and M_2 have the same dimensions, so that in the limit that channel length modulation is negligible the quiescent current of the input devices is set to I_B.

As in previous section, I assume for simplicity that I_x is chosen equal to I_B, and so quiescent current efficiency factor can be calculated using the (2.12) as seen in section 2.2.1. Then I can write:

$$F_C = \frac{2N}{2N+2+\gamma} \quad (2.34)$$

When the circuit is unbalanced, for example by setting Vid >> 0, M1A is turned off and M1 draws a current

$$I_1 = k_1(V_{id} + \sqrt{I_B/k_2})^2. \quad (2.35)$$

By assuming an input common mode level of $V_{DD}/2$, the maximum differential input signal is equal to V_{DD}, and from the calculations carried out in the Appendix (A.6), I get

$$F_{SR} = \frac{k_1(V_{DD}+\sqrt{I_B/k_2})^2}{4I_B}. \quad (2.36)$$

A small signal analysis of the circuit carried out in Appendix (A.6) shows that, for the same bias current of the input stage and the same mirroring factor N, the differential gain is twice that of the class A OTA in Fig. 2.3 since the input devices see twice the input signal. In this case therefore I have

$$Q_{BW} = 2 \quad (2.37)$$

The Common Mode Rejection Ratio (CMRR) calculated in Appendix (A.6) is equal to:

$$\frac{A_{01}}{2}\frac{r_{o3}}{r_{o1}}\left(1+\frac{g_{m3}}{g_{m5}}\right) \quad (2.38)$$

where A_{01} is equal to $gm \cdot r_o$.

2.3.3 C. Ramirez-Angulo et al. class AB topology [9]

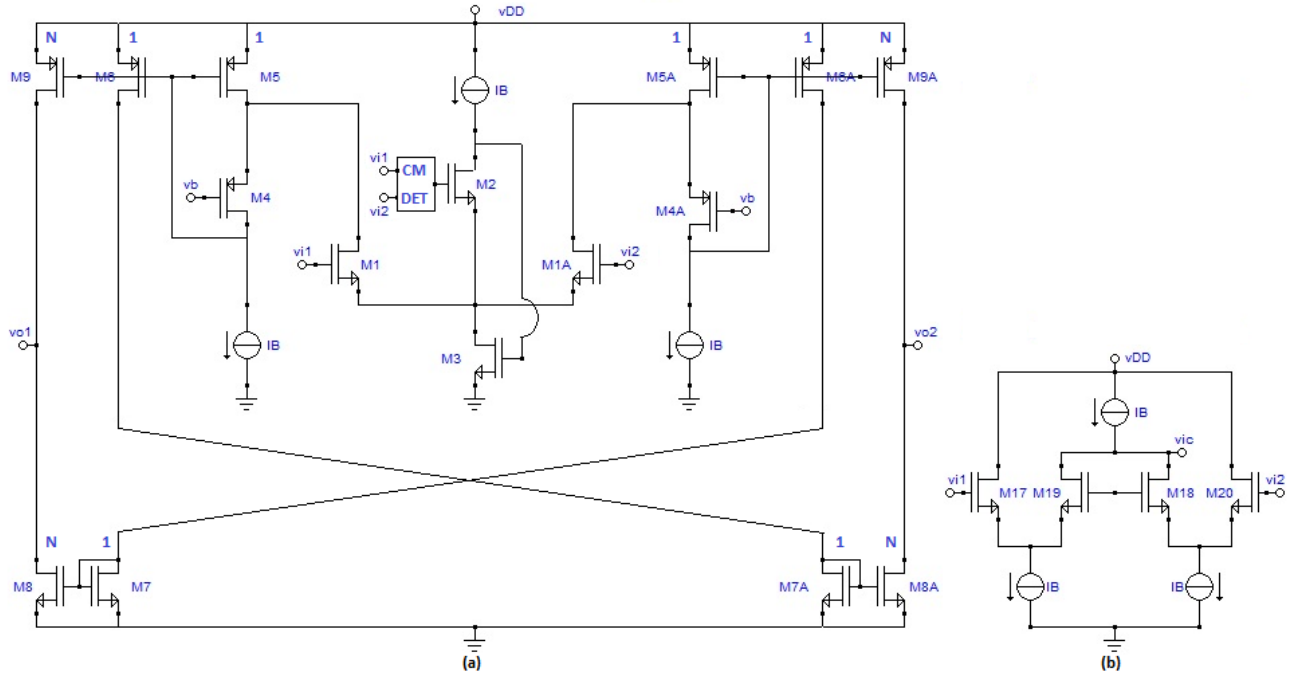


Fig.2. 6: Fully differential class AB OTA based on the topology by Ramirez-Angulo and (b) a possible implementation of the input common mode voltage detector

The class-AB input stage proposed by Ramirez-Angulo et al. in [9] exploits a flipped voltage follower driven by the input common-mode signal to provide adaptive biasing of a differential pair, as shown in Fig.2.6a. A common-mode detector is needed, and a possible implementation is shown in Fig.2.6b. Transistors M_6 and M_{6A} and current mirrors M_7-M_8 and M_{7A}-M_{8A} are needed to make currents I_{B1} and I_{B2} in Fig.2.1 dependent on the input signal, as in Fig.2.3.

We assume that M_1 and M_2 have the same dimensions, so that in the limit that channel length modulation is negligible, the quiescent current of the input devices is set to I_B. To calculate F_C I need to know the quiescent current flowing in the output branches and the total quiescent current flowing into the OTA as seen in section 2.2.1. With reference to Fig.2.6 I can write:

$$I_{QOUT} = 2N(I_B + I_x) \quad (2.39)$$

$$I_{QTOT} = 2N(I_B + I_x) + 2(I_B + I_x) + 2I_x + 2I_B + I_B + 2\beta I_B + 2\gamma I_B \quad (2.40)$$

By (2.12), the quiescent current efficiency can therefore be calculated as

$$F_C = \frac{4N}{4N+9+2\beta+2\gamma} \quad (2.41)$$

where the current of the common-mode detector CMDET has been expressed as $2\beta I_B$ (β=1 for the circuit in Fig.2.6b) and the current contribution of the CMFB has been expressed as $2\gamma I_B$.

When the circuit is unbalanced, for example by setting Vid >> 0, M_{1A} is turned off and M_1 draws a current

$$I_1 = k_1\left(\frac{V_{id}}{2} + \sqrt{I_B/k_2}\right)^2. \quad (2.42)$$

By assuming an input common mode level of $V_{DD}/2$, the maximum differential input signal is equal to V_{DD}, and from the calculations carried out in the Appendix (A.4), I get

$$F_{SR} = \frac{k_1\left(\frac{V_{id}}{2}+\sqrt{I_B/k_2}\right)^2}{4I_B}. \quad (2.43)$$

The small signal analysis of the circuit in Fig.2.6 shows that the circuit presents the same gain and bandwidth than its class A counterpart, since the source node of M_1 and M_{1A} is grounded for differential signals.The FOM defined by (2.19), that is the ratio of the unity-gain bandwidths of this stage and of a class A stage, is therefore

$$Q_{BW} = 1 . \quad (2.44)$$

The Common Mode Rejection Ratio (CMRR) calculated in Appendix (A.4) is equal to:

$$\frac{g_{m7}g_{m9}+g_{m6}g_{m8}}{g_{m7}g_{m9}-g_{m6}g_{m8}}\frac{A_{02}A_{03}}{2} \quad (2.45)$$

where A_{02} and A_{03} are $gm \cdot r_o$.

2.3.4 D. Baswa et al. class AB topology [10]

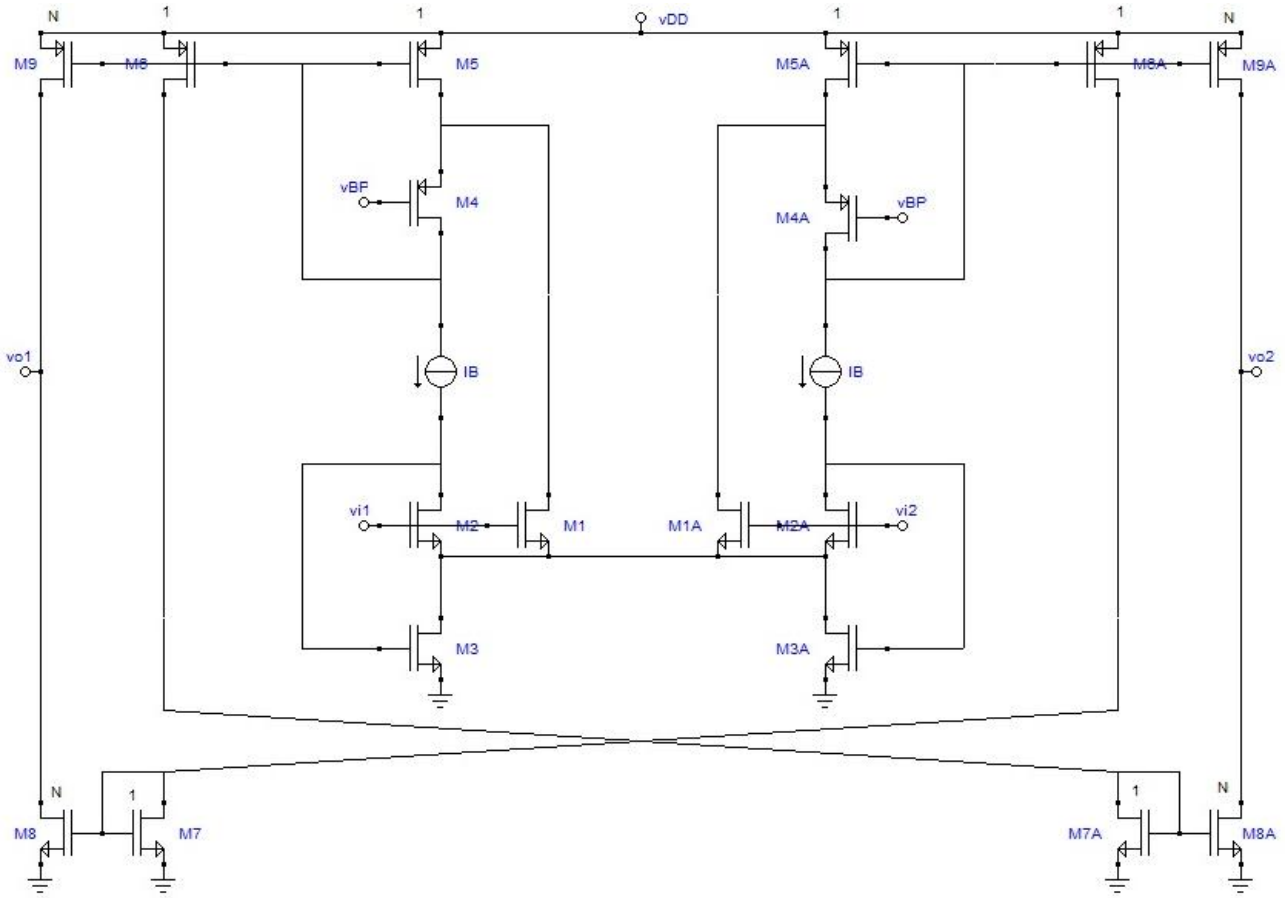


Fig.2. 7: Fully differential class AB OTA based on the topology by Baswa.

The class AB input stage exploits a winner-take-all (WTA) approach to set the adaptive biasing of the differential pair; the WTA circuitry is composed by two FVFs driven by the input signals, with their output nodes shorted together, as shown in Fig.2.7. The circuit is similar to that in Fig.2.5, but the sources of M_1 and M_{1A} are shorted together, and the FVFs driven by the input signals cannot be used to make currents I_{B1} and I_{B2} of Fig.2.1 dependent on the input signal, so that the approach of Fig.2.3 is needed.

Under the same hypotheses used to analyze the topology by Peluso, the output quiescent current (I_{QOUT}) and the total quiescent current (I_{QTOT}) can be calculated as

$$I_{QOUT} = 2N(I_B + I_x) \quad (2.46)$$

$$I_{QTOT} = 2N(I_B + I_x) + 2(I_B + I_x) + 2I_x + 2I_B + 2\beta I_B + 2\gamma I_B \quad (2.47)$$

By (2.12), the quiescent current efficiency can therefore be calculated as

$$F_C = \frac{2N}{2N+4+\beta+\gamma} \quad (2.48)$$

where the current contribution of the CMFB has been expressed as $2\gamma I_B$.

When the circuit is unbalanced, for example by setting Vid >> 0, the current in M_{1A} is set to I_B (equal to that in M_{2A}) whereas M_1 draws a current

$$I_1 = k_1(V_{id} + \sqrt{I_B/k_2})^2. \quad (2.49)$$

By assuming an input common mode level of $V_{DD}/2$, the maximum differential input signal is equal to V_{DD}, and from the calculations carried out in the appendix (A.5), I can calculate

$$F_{SR} = \frac{k_1\left(V_{DD}+\sqrt{\frac{I_B}{k_2}}\right)-I_B}{4I_B}. \quad (2.50)$$

The small signal analysis of the circuit of Fig.2.7 shows that the circuit presents the same gain and bandwidth than its class A counterpart, since the source node of M_1 and M_{1A} is grounded for differential signals.

The FOM defined by (2.19), that is the ratio of the unity-gain bandwidths of this stage and of a class A stage, is therefore

$Q_{BW} = 1$.

The Common Mode Rejection Ratio (CMRR) calculated in Appendix (A.5) is equal to:

$$\frac{g_{m7}g_{m9}+g_{m6}g_{m8}}{g_{m7}g_{m9}-g_{m6}g_{m8}}\frac{A_{02}A_{03}}{2} \quad (2.45)$$

where A_{02} and A_{03} are $g_m \cdot r_o$.

2.4 Comparison of selected topologies

Table 2.1

Comparison of class AB fully differential symmetrical OTAs

Topology	F_C	Q_{SR}	Q_{BW}	CMRR
Castello[1] 1985	$\frac{2N}{2N+2+\beta+\gamma}$ $\beta = 2$	$\frac{1}{4}\left(1+\frac{V_{DD}-V_{LS}}{2V_{ov1}}\right)^2$	1	$\frac{g_{m3}g_{m7}+g_{m5}g_{m6}}{g_{m3}g_{m7}-g_{m5}g_{m6}}\frac{1}{1/A_{0n}-1/A_{0p}}$
Peluso[4] 1997	$\frac{2N}{2N+2+\gamma}$	$\frac{1}{4}\left(1+\frac{V_{DD}}{V_{ov1}}\right)^2$	2	$\frac{A_{01}}{2}\frac{r_{o3}}{r_{o1}}\left(1+\frac{g_{m3}}{g_{m5}}\right)$
Ramirez-Angulo[9] 2001	$\frac{2N}{2N+4.5+\beta+\gamma}$ $\beta = 1$	$\frac{1}{4}\left(1+\frac{V_{DD}}{2V_{ov1}}\right)^2$	1	$\frac{g_{m7}g_{m9}+g_{m6}g_{m8}}{g_{m7}g_{m9}-g_{m6}g_{m8}}\frac{A_{02}A_{03}}{2}$
Baswa[10] 2006	$\frac{2N}{2N+4+\beta+\gamma}$	$\frac{1}{4}\left[\left(1+\frac{V_{DD}}{2V_{ov1}}\right)^2-1\right]$	1	$\frac{g_{m7}g_{m9}+g_{m6}g_{m8}}{g_{m7}g_{m9}-g_{m6}g_{m8}}\frac{A_{02}A_{03}}{2}$

Table.2.1 synthesizes the results for the class AB topologies we have considered. The quiescent current efficiency (2.12) and the CMRR are reported instead of the respective quality factors for ease of comparison. V_{ov1} is the quiescent overdrive voltage of M_1, The values reported for the CMRR are the dc values without CMFB, and we have considered

$\mu = g_m r_o$ (2.45)

for the intrinsic gain of the devices. The table shows that the topology by Peluso presents the best quiescent current quality factor and quality factor for slew rate, but the worst CMRR, since it cannot become infinite by suitable sizing of the devices. The best CMRR is provided by the topology by Castello, whose main drawbacks are the need for the input level shifter, that limits the input dynamic range, increases quiescent current consumption, and degrades the phase margin, and the four stacked devices in the input branch, that limit the minimum supply voltage.

Chapter 3

Improvement of the CMRR of the topology by Peluso

In Chapter 2 I compared four topologies of class AB fully differential OTAs from the point of view of the consumption, slew rate, bandwidth, and common mode rejection ratio (CMRR).
The topology proposed by Peluso [1] shows the best differential-mode performance among symmetrical OTA topologies, providing the highest efficiency and doubled small-signal unity-gain frequency. This is achieved by applying the same signal with opposite polarity to the gates and the sources of the input transistors through source followers. However non idealities of such source followers make the common-mode behavior of this topology very poor. Common-mode gain is high, thus requiring a high-gain power consuming CMFB amplifier to enhance the CMRR. Moreover, it has to be noted that a fully differential amplifier closed in a (negative) feedback loop could result in positive feedback for the common-mode, thus a common-mode gain larger than 1 would make it unusable.
If I could improve the CMRR of Peluso's topology and at the same time keep the other performance unchanged, I would have a very good topology by all points of view and a broad range of applications.
In this chapter I will explain why the common mode gain of Peluso topology is particularly high and I will propose some solutions to increase the CMRR of Peluso's topology with a slight increase in consumption.
The proposed solutions, in the following paragraphs, will be explained analytically and later on the results obtained will be reported from their implementation in "Virtuoso CADENCE", which is a CAD tool for the simulation of microelectronic circuits.
The technology used for amplifier design is provided by STMicroelettronics with 40nm production process. This short channel technology is designed for digital applications because it has some advantages: primarily, the triode region MOSFETs lets the current flow better because they have a smaller resistance. Secondly, they have smaller Gate capacitance. These two factors contribute to reducing the switch-on and switch-off times of the transistors themselves, and in addition allow for higher switching speeds because the cutting frequency increases. A third reason is to have greater computing power for the same occupied area.
However, with the reduction of the dimensions I have a reduction of oxide thickness and the voltage that can be applied to the gate must be reduced to avoid gate oxide breakdown. In analog design, at low power supply voltages, the threshold voltage has to be reduced so that multiple stacked devices can operate properly, moreover, a low threshold allows to have more dynamic. With reduced threshold voltages, the transistor cannot turn off completely, forming a layer with a weak reverse voltage that generates a subthreshold current that dissipates power. In digital design having a too low threshold involves leakage problems and therefore I prefer to have high threshold devices.

Other issues are related to the saturation of carrier speed, so the current varies almost linearly with the overdrive voltage and not quadratically assuming a value lower than that it would have in normal saturation. The used technology provides transistors with three different threshold voltages.

LVT (Low VTh)	SVT (Standard VTh)	HVT (High VTh)

Since the amplifier is designed for Low Voltage applications with multiple stacked devices as the Cascode, the transistors chosen are the LVTs. These transistors are also the ones where the product between transconductance and resistance of output at low signal is the largest of the three.

3.1 Evaluation of the problem of Peluso's original topology

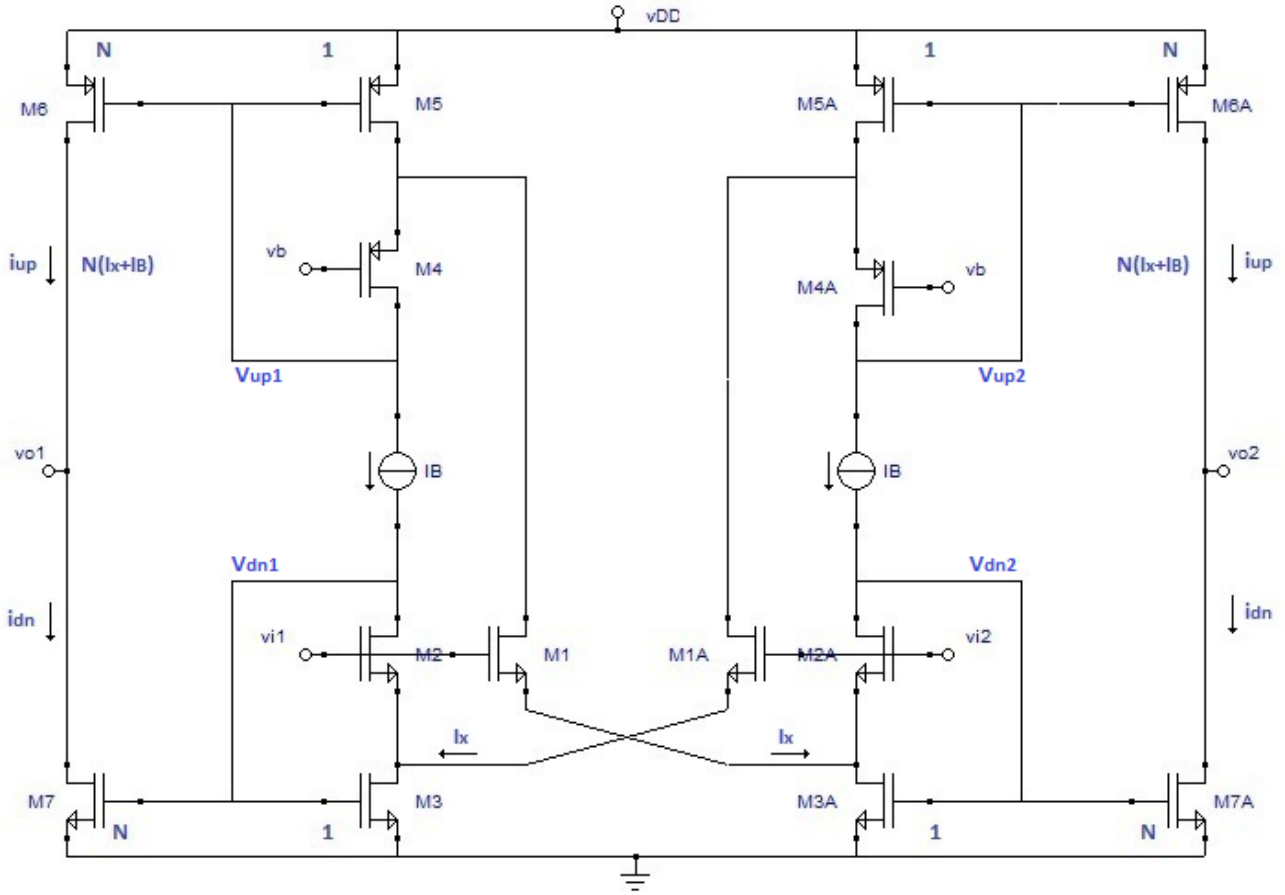


Fig.3. 1: Fully-differential class-AB OTA topology by Peluso.

The class-AB OTA topology by Peluso is shown in Fig.3.1. Transistors M2 and M3 (M2A and M3A) with the floating current source IB form a flipped voltage follower (FVF) that copies the input signal to the source of M1A (M1). In this way the transistors of the input pair M1-M1A have a gate-source voltage VGS=VGSQ±(vi1-vi2), where VGSQ is the quiescent component. For large differential inputs one of them cuts off whereas the other carries a current that is not limited by a fixed current source, and is larger than in other class AB symmetrical OTA topologies for the same input swing. Drain currents of M1 and M1A are mirrored to the output branches; FVF current mirrors (M4-M6 and M4A-M6A) are used to maximize dynamic range in a low voltage environment, and the output branch can be cascoded to increase the differential gain. Active loads M7 and M7A on the output branches should provide a variable current to minimize differential to

common-mode conversion, since in a class-AB OTA the common-mode current is not constant. For this reason, and also to double the differential gain, they are made signal dependent, and to minimize power consumption they are driven by the same FVFs used for input buffering.
This allows maximizing efficiency, but it is the source of poor common-mode behavior. When a common-mode input is applied (vi1=vi2=vic), the gate-source signal voltage of input transistors M1 and M1A goes to zero, thus keeping iup constant (the signal component of Iup is zero). However to achieve this result the FVF M2-M3 makes vdn, and therefore idn, dependent on the input signal, providing a common-mode signal component at the output. To understand what happens, we can note that the signal current in M1 and M1A is zero; the current in M3 is therefore constant and equal to the quiescent current, but its drain-source voltage changes with the input signal.

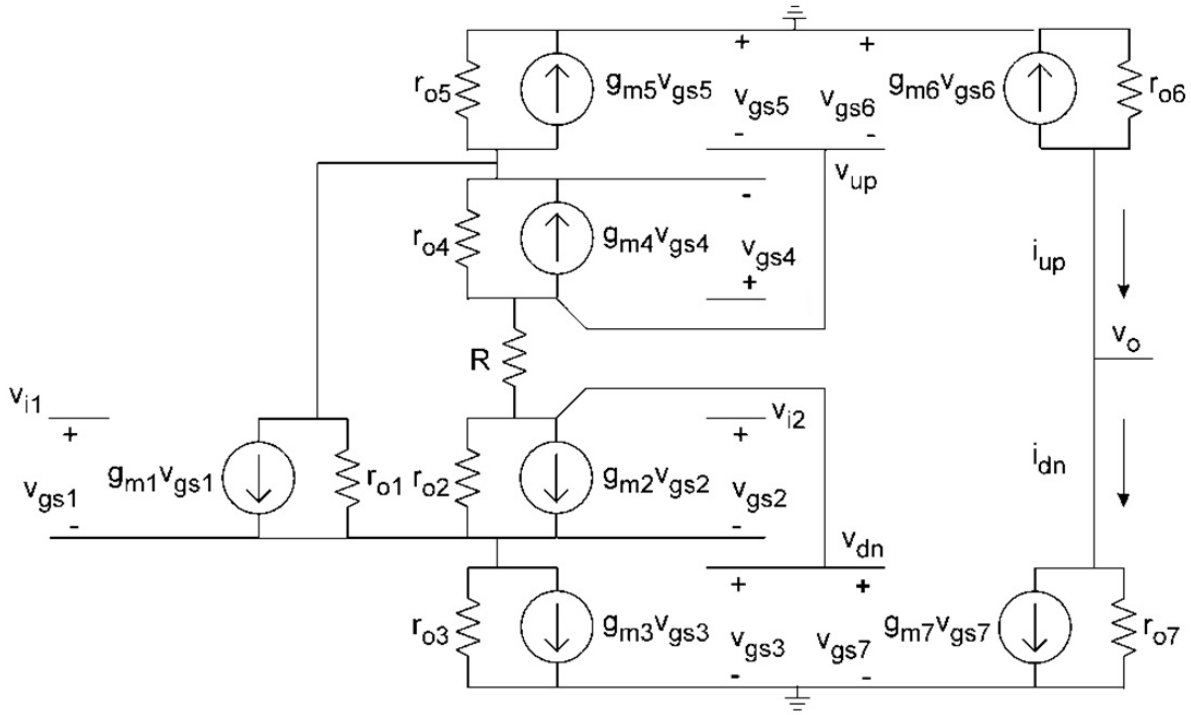


Fig.3. 2: Simplified small-signal common-mode half-circuit

The gate-source voltage of M3 has therefore to change to compensate the variation in the drain-source voltage, the more the lower is the transistor output resistance, thus generating a signal component vdn.
A simplified analysis of the common-mode behavior can be performed exploiting the half-circuit in Fig.3.2, and neglecting the output resistances of M_1, M_2 and M_7; R is the resistance of the current source I_B. The gate-source voltage of M_1 results

$$V_{gs1} = \frac{g_{m2}r_{o3}(g_{m3}R+1)(V_{i1}-V_{i2})+V_{i1}}{g_{m2}g_{m3}r_{o3}R+(g_{m1}+g_{m2})r_{o3}+1} \quad (3.1)$$

that is practically zero for $v_{i1}=v_{i2}=v_{ic}$, therefore $i_{up}=0$, whereas v_{dn} is given by

$$V_{dn} = \frac{-g_{m2}RV_{i2}}{g_{m2}g_{m3}r_{o3}R+(g_{m1}+g_{m2})r_{o3}+1} \approx \frac{-V_{i2}}{g_{m3}r_{o3}} \quad (3.2)$$

providing an output current $i_{dn}=g_{m7}v_{dn}$. A more detailed analysis provides a differential gain

$$A_d \approx g_{m1}R_{LOAD}\left(\frac{g_{m7}}{g_{m3}}+\frac{g_{m6}}{g_{m5}}\right) \quad (3.3)$$

where RLOAD=ro6||ro7 is the output resistance of the amplifier, and for the common-mode gain

$$A_c \approx \frac{R_{LOAD}}{r_{o1}A_{02}A_{03}}\left\{g_{m7}[r_{o1}A_{02} - (A_{01} - A_{02})r_{o3}] + \frac{g_{m6}}{g_{m5}R}[A_{01}(r_{o2} + R) + (A_{01} - A_{02})r_{o3}]\right\} \quad (3.4)$$

where A0x=gmxrox is the intrinsic gain of the transistor Mx and R is the resistance of the current source IB. For A01=A02, Eq. (3.4) becomes

$$A_c \approx \frac{R_{LOAD}}{A_{03}}\left(g_{m7} + \frac{g_{m6}}{g_{m5}}\frac{r_{o2}+R}{r_{o2}R}\right) \approx R_{LOAD}\frac{g_{m7}}{A_{03}} \quad (3.5)$$

and cannot be reduced to zero by exploiting matching between the devices; CMRR is given by

$$CMRR = 2g_{m1}r_{o3}\left(1 + \frac{g_{m7}g_{m3}}{g_{m6}g_{m5}}\right) \quad (3.6)$$

Eq. (3.5) shows that the common-mode input propagates to the output through the NMOS path, whereas the gain of the path through PMOS devices is negligible.

3.2 Peluso topology with CMFB in triode

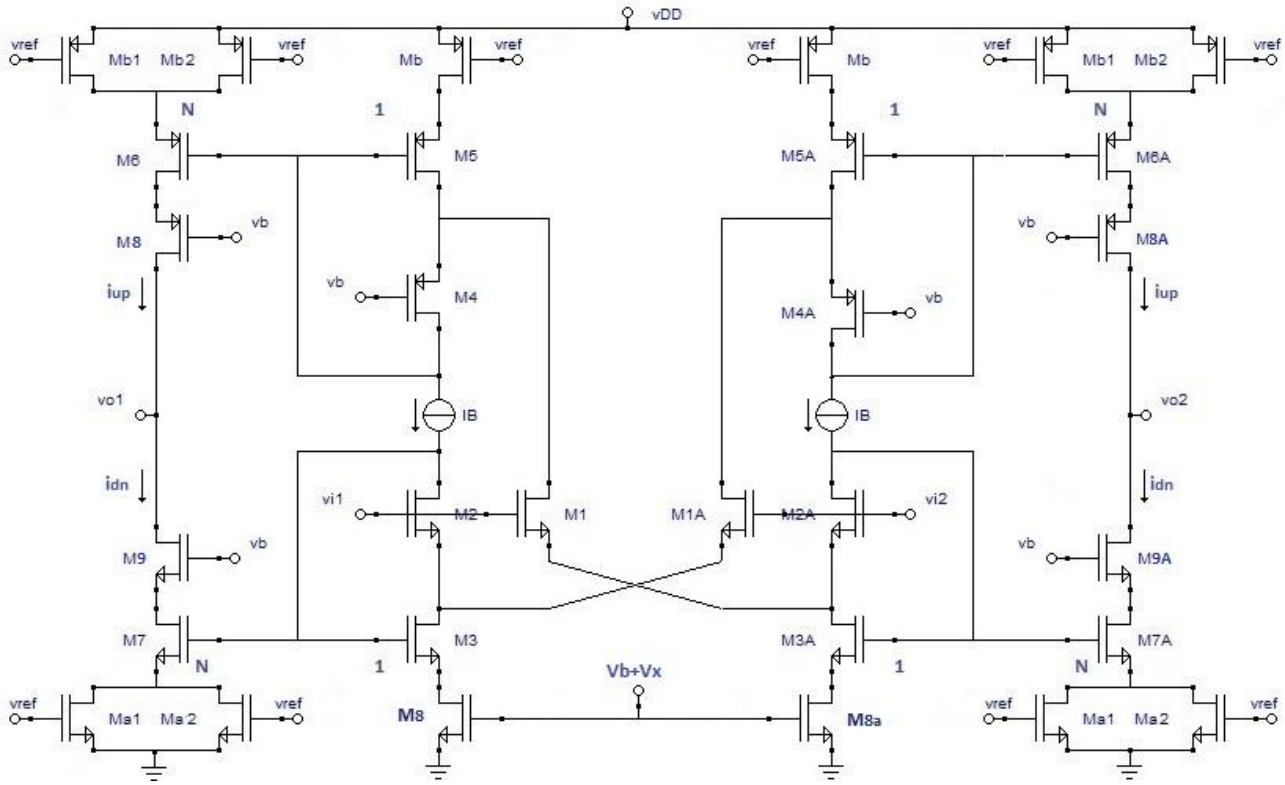


Fig.3. 3: Fully-differential class-AB OTA topology by Peluso with CMFB in triode

In the previous section I have explained intuitively why Peluso's topology has a high common mode gain. Since any fully differential amplifier requires a common mode feedback loop (CMFB) in order to operate properly, this section introduces the CMFB used for Peluso topology.

As seen in chapter 2, in the input stage a very low quiescent current is used, and therefore consumption in the CMFB could contribute significatively to the global power consumption.

In general, the CMFB requires a common mode sensor and a loop amplifier, and both these blocks usually dissipate power. Class AB amplifiers used in switched-capacitor applications often use a switched-capacitor CMFB [2], [3], that however dissipates dynamic power, and could require an additional error amplifier. A CMFB architecture that does not require additional power exists, is the triode CMFB [4], where MOS transistors operating in the triode region are used to sense the output common mode voltage and control the current flowing in a branch of the circuit, and in this way the

output common mode voltage. The drawback of this approach is the limited loop gain, due to the MOS devices biased in triode region.

In general a class AB amplifier with the fully differential symmetrical OTA requires a CMFB with very low power consumption, the triode CMFB architecture is very well suited for this application.

Figure 3.3 shows the original Peluso topology with a loop for controlling the output common mode voltage (CMFB). The CMFB is implemented by the MOS Ma-Ma1,2, M3A, M7A for the N-channel part and the Mb-Mb1,2, M5A, M6A for the P-channel part, as shown in Fig.3.3. We can call this kind of CMFB as complementary triode CMFB. As the name suggests, the transistors Ma-Ma1,2 and Mb-Mb1,2, that make part of it, operate in the triode region while M3A, M7A, M5A and M6A operate in the saturation region. The CMFB can also work by only implementing the part with "N" devices or only the part with "P" devices. To increase gain without increasing consumption, I decide to use both the "N" and "P" parts.

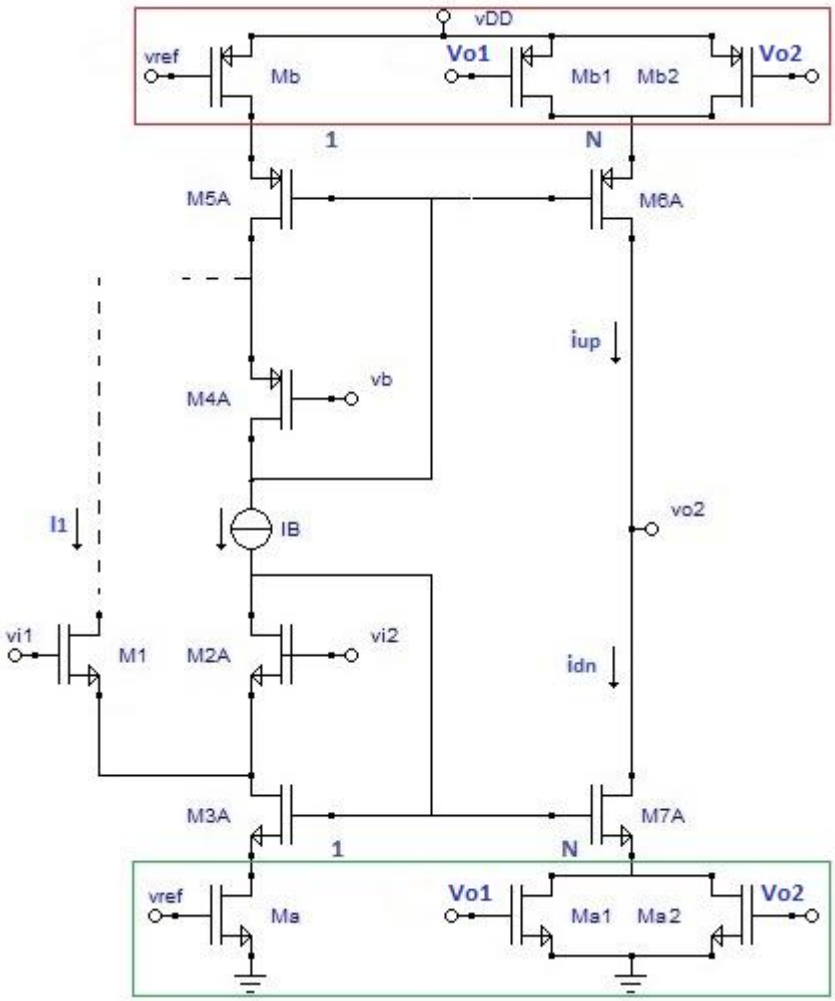


Fig.3.4: Half circuit of Fully-differential class-AB OTA topology by Peluso with CMFB in triode

Figure 3.4 shows the half circuit in which the new MOSs, $M_{a,b}$, $M_{a1,b1}$, $M_{a2,b2}$, are added that, together with the present transistors, compose the complementary triode CMFB.

For simplicity in Fig.3.5, only the CMFB made with N type MOS is represented. The output voltage (V_{o1},V_{o2}) is connected to the gates of Ma1,2 (Vref=VCM). To simplify the description of this circuit, assume that Ma, M3A, M7A, Ma1 and Ma2 are matched and ignore body effect.

Before this CMFB approach is mathematically analyzed, its operation will be explained intuitively. At first, let's assume that the OTA outputs in Fig.3.3 have only a common mode (CM) component; that is, Vo1=Vo2=Voc. Then the gate voltages of Ma1 and Ma2 equal Voc. Also I assume that the mirror gain is equal to 1.

Transistors Mb1, Mb2, Ma1 and Ma2 read the output voltage directly, without loading the amplifier and without requiring a power consuming buffer, and the feedback loop keeps the output common mode voltage constant and equal to Vref. This arrangement is inherently wideband, since there is no buffer that adds further poles to the transfer function, and is able to cope with output signals swinging over the whole supply rail voltage range.

This CMFB architecture is based on a nonlinear feedback loop: the transistors operating in triode region act as resistors whose value depends on the voltage applied to the gate. At the equilibrium, for matched devices, an output common mode voltage equal to Vref is required to make currents I_{dn} and I_{up} equal; if the output voltage increases, the resistance given by Ma1 and Ma2 decreases and that given by Mb1 and Mb2 increases. This results in a current I_{dn} larger than Iup, thus opposing the increase of the output voltage. The circuit can also be designed without using Ma and Mb: in this case, the dimensions of M3A and M5A (M3 and M5) have to be different, and this difference implicitly sets the reference voltage Vref. This however makes this approach less robust to mismatches.

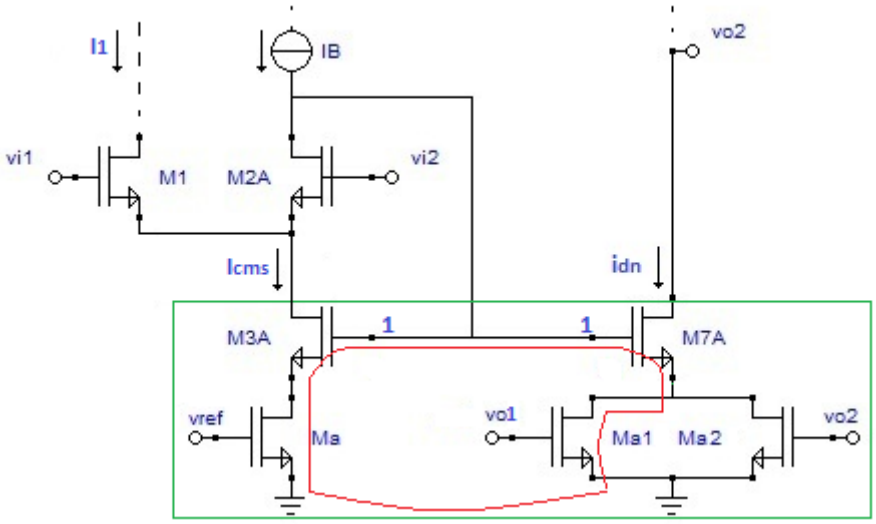


Fig.3. 5: Complementary triode CMFB, part N

Transistors shown in Fig.3.4 form a degenerated differential flipped voltage follower current mirror. Differential signals do not affect the operation of this feedback loop, as shown by the following analysis.

Since Ma1 and Ma2 are matched and operate in the triode region, the sum of their drain currents, considering that $I_{d7A}=I_{dn}$, and using the equation for the triode region is

$$I_{d7A} = I_{dn} = I_{da1} + I_{da2} = k_n' \left(\frac{W}{L}\right)_{a1} \left((V_{o1} - V_{ta1})V_{dsa1} - \frac{V_{dsa1}^2}{2}\right) +$$

$$+k_n' \left(\frac{W}{L}\right)_{a2} \left((V_{o2} - V_{ta2})V_{dsa2} - \frac{V_{dsa2}^2}{2}\right)$$

putting in evidence $V_{dsa1,2,}$ I get

$$= 2k_n' \left(\frac{W}{L}\right)_{a1} \left(\left(V_{oc} - V_{tn} - \frac{V_{dsa1}}{2}\right) V_{dsa1}\right) \quad (3.7)$$

since Vdsa1=Vdsa2, Vta1=Vta2=Vtn, and (W/L)a1=(W/L)a2. This equation shows that Idn is dependent on the common mode (CM) output voltage and not dependent on the differential output voltage because changes in the drain currents in Ma1 and Ma2 due to nonzero Vod are equal in magnitude and opposite in sign. Therefore, these changes cancel when the drain currents are summed in (3.7).

Applying KVL around the lower transistor M3A, M7A, Ma, Ma1 gives

$$V_{dsa1} = V_{dsa} + V_{gs3A} - V_{gs7A} \quad (3.8)$$

Assuming that $I_{d7A} \approx I_{d3A}$, we have $V_{gs7A} \approx V_{gs3A}$, and (3.8) reduces to

$$V_{dsa1} \approx V_{dsa} \quad (3.9)$$

Since Ma operate in the triode region with Ida=Icms=Idn, rearranging gives

$$V_{dsa} = \frac{I_{cms}}{k_n'\left(\frac{W}{L}\right)_a \left(\left(V_{CM} - V_{tn} - \frac{V_{dsa}}{2}\right)\right)} \quad (3.10)$$

Using (3.9) and (3.10) in (3.7) with (W/L)a1=(W/L) a gives

$$I_{dn} = 2k_n' \left(\frac{W}{L}\right)_{a1} \left(\left(V_{oc} - V_{tn} - \frac{V_{dsa1}}{2}\right) V_{dsa1}\right) =$$

$$= 2k_n' \left(\frac{W}{L}\right)_{a1} \left(V_{oc} - V_{tn} - \frac{V_{dsa}}{2}\right) V_{dsa} \quad (3.7)$$

I replace Vdsa with the equation (3.10) and I get

$$= \left(\frac{I_{cms} 2k_n'\left(\frac{W}{L}\right)_{a1}\left(V_{oc} - V_{tn} - \frac{V_{dsa}}{2}\right)}{k_n'\left(\frac{W}{L}\right)_a \left(\left(V_{CM} - V_{tn} - \frac{V_{dsa}}{2}\right)\right)}\right) = 2I_{cms} \frac{\left(V_{oc} - V_{tn} - \frac{V_{dsa}}{2}\right)}{\left(V_{CM} - V_{tn} - \frac{V_{dsa}}{2}\right)}$$

$$I_{dn} = 2I_{cms} \frac{\left(V_{oc} - V_{tn} - \frac{V_{dsa}}{2}\right)}{\left(V_{CM} - V_{tn} - \frac{V_{dsa}}{2}\right)} =$$

$$= 2I_{cms} \frac{V_{CM} - V_{tn} - \frac{V_{dsa}}{2}}{V_{CM} - V_{tn} - \frac{V_{dsa}}{2}} + 2I_{cms} \frac{V_{oc} - V_{CM}}{V_{CM} - V_{tn} - \frac{V_{dsa}}{2}} =$$

$$= 2I_{cms} + 2I_{cms} \frac{V_{oc} - V_{CM}}{V_{CM} + V_{SS} - V_{tn} - \frac{V_{dsa}}{2}} \quad (3.11)$$

3.3 First method to improve the performance of Peluso's topology [5]

The analysis in Section 3.1 shows that the CMRR can be enhanced by making also i_{up} (and therefore V_{up}) dependent on the input common-mode signal V_{ic}, or by making the gate-source voltage of M7 not dependent on V_{ic}. The latter can be obtained by adding at the source of M7 a MOS biased in triode region with a suitable signal proportional to V_{ic} on its gate. However this arrangement would interfere with the use of a triode-based CMFB. Since the triode-based CMFB requires a MOS in triode region also at the source of M3, the solution is to use this latter device, whose gate would normally be connected to a constant voltage, to apply a signal v_x proportional to V_{ic} and cancel the dependence of idn on the output common-mode voltage without affecting differential-mode performance. Fig. 3.2 shows the resulting topology where at the V_b terminal is applied a v_x signal proportional to V_{ic}; a cascode or regulated cascode topology can be exploited for the output branches to increase the output resistance and thus gain, however this will not be taken into account in the following analysis.

Let's consider $V_{i1}=V_{i2}=V_{ic}$; the output voltage when the CMFB loop is open can be written as

$$V_{o1} = V_{o2} = V_{oc} = -(g_{m6}^* V_{up} + g_{m7} V_{dn}) R_{LOAD} \quad (3.12)$$

where $R_{LOAD} = r_{o6}^* || r_{o7}^*$, and $g_m^*$and r_o^*take into account the effect of the triode degeneration:

$$r_o^* = g_m r_o r_T + r_o + r_T \quad (3.13)$$

$$g_m^* = g_m r_o / r_o^* \approx 1/r_T \quad (3.14)$$

with r_T the resistance provided by the triode-biased degeneration transistor. The transfer functions from the common-mode input to V_{dn} and V_{up} are respectively

$$\frac{V_{dn}}{V_{ic}} \approx -\frac{1}{A_{03}} \quad (3.15)$$

$$\frac{V_{up}}{V_{ic}} \approx \frac{g_{m1}}{g_{m5}^*} \frac{1}{A_{03} g_{m2} (r_{o2} || R)} \quad (3.16)$$

where I am assuming A_{01}=A_{02}, showing that the input common mode propagates to the output mostly through the lower (NMOS) path, since (3.15) is much larger than (3.16). The transfer functions from the auxiliary input v_x=kV_{ic} are respectively

$$\frac{V_{dn}}{V_x} \approx -\frac{g_{T8}}{g_{m3}^*} \quad (3.17)$$

$$\frac{V_{up}}{V_x} \approx -\frac{g_{m1}}{g_{m5}^*} \frac{1}{g_{m2} (r_{o2} || R)} \frac{g_{T8}}{g_{m3}^*} \quad (3.18)$$

Also in this case we have (3.17) much larger than (3.18), so the auxiliary input mostly acts on the lower signal path, and the output common mode is cancelled when

$$k \approx \frac{1}{g_{T8} r_{o3}^*} \approx -\frac{1}{g_{T8} r_{T8} A_{03}} \quad (3.19)$$

where g_{T8} is the transconductance of transistor Q8 that is biased in triode region.

The signal v_x is generated by an auxiliary amplifier that can be obtained by a simple circuit such as that shown in Fig.3.6, therefore its impact on the OTA characteristics is minimal, apart from the desired effect of lowering the common mode gain.

The signal v_x is generated by an auxiliary amplifier (corresponding to the block AUX in Fig.3.13), that has to sense the input common-mode voltage, to apply an inverting gain (or attenuation, according to values in (3.19) and to provide the dc bias V_B. Its simplest implementation, shown in Fig. 3.6a, consists of two common-source stages with shorted drains and a diode-connected load, since the required gain is low (and can even be less than 1). To make the specifications on dc output voltage and gain independent, a dc current source I_{CTR} can be added, so that transistors M_{X1}-M_{X2} and M_Y are biased at different currents. The gain of the auxiliary amplifier can be easily calculated as

$$k = -2\frac{g_{mX}}{g_{mY}} = 2\frac{I_X}{I_Y}\frac{V_{DD} - V_B - |V_{TP}|}{V_{ic} - V_{TN}} \quad (3.20)$$

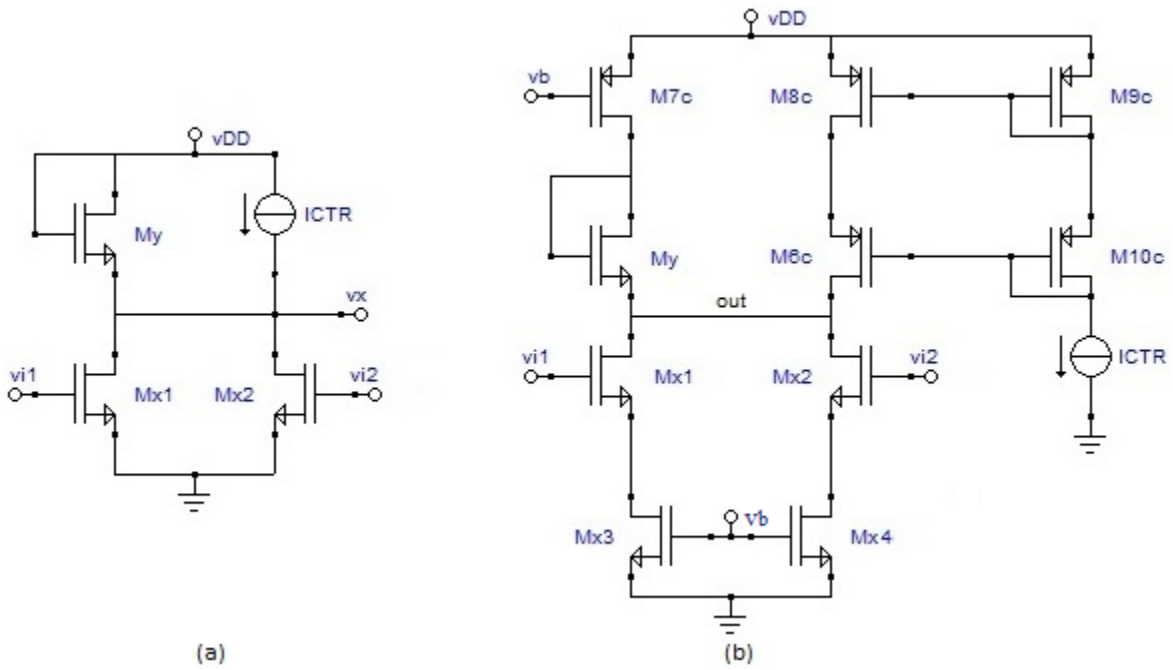


Fig.3. 6: Auxiliary amplifier topology: a) ideal; b) real implementation

where I_X and I_Y are the currents in M_{X1} (and M_{X2}) and M_Y respectively; given the values of all the voltages (threshold voltages, input common mode and bias V_B), $I_Y \neq 2I_X$ is usually required to obtain the desired gain (3.19 and 3.20), and this can be achieved through the current I_{CTR}. In deep submicron technologies with a dc bias level of $V_{DD}/2$, even using minimum size transistors this arrangement could result in a too high current for the auxiliary amplifier. A possible solution is represented in Fig.3.6b where degeneration resistors are added to the common source, a series resistor to the diode connected load, and a cascade current mirror is used to provide ICTR.
The circuit can be biased at very low current, thus not affecting the efficiency of the overall class-AB amplifier. This circuit has also to provide the reference voltage for the triode-based CMFB: to make the gain k independent from the dc output voltage, a NMOS or PMOS dc current source ICTR can be added, so that MX1-MX2 and MY are biased at different currents.

3.3.1 Simulation results

A fully differential OTA based on the proposed topology has been designed in CMOS 40-nm technology by ST Microelectronics. The OTA features cascode transistors in the output branch, in order to enhance the gain, and a complementary triode CMFB: both NMOS (M2-M3-M7) and PMOS (M4-M5-M6) current mirrors present a triode degeneration, with the triode devices in the output branch connected to the output voltage (two transistors connected to vo1 and vo2 are used to sense the common-mode voltage). The triode biased transistor at the source of M5 has its gate connected to VDD/2, whereas the triode at the source of M3 is also used to apply the correction signal, as shown in Fig.3.3. Supply voltage is 1.2 V, and 500-fF load capacitors have been added at the outputs.

Table 3.1		
Shape ratio of OTA and triode CMFB		
M	**W[µm]**	**L[µm]**
1,1A	0.47	0.1
2,2A	0.9	0.1
3,3A	0.75	0.1
4,4A	4	0.1
5,5A	2	0.1
6,6A	20	0.1
7,7A	7.5	0.1
a	1.5	0.1
a1,a2	7.5	0.1
b	4	0.1
b1,b2	20	0.1
8,8A	150	0.25
9,9A	35	0.25

In Table 3.1 and 3.2 the aspect ratios of the devices used to design the OTA are reported, together with the CMFB and the auxiliary amplifier, reported in Fig. 3.3 and Fig 3.6, respectively.

Table 3.2		
Auxiliary amplifier shape ratio		
M	**W[µm]**	**L[µm]**
x1,x2	0.2	0.1
x3,x4	0.96	0.25
y	0.41	0.1
6c,8c,9c,10c	0.35	0.04
7c	0.5	0.25

Table 3.3 reports the performance for the proposed topology by considering variation of the process corners.

By adjusting the current ICTR be, a large improvement of CMRR can be achieved in all the process corners. In reality, I will not able to get the optimum value of current, as even if I have to dimension everything perfectly, in the end I will still have to deal with uncertainty. To evaluate more realistically the performance of the proposed amplifier, the simulations have been repeated considering a ±5% variations of the nominal current in all the process corners and the results are reported in Table 3.5 and Table 3.6.

Even if the optimum situation is represented by nominal case, realistically, I can expect that the improvement I get on average will be within the "±5%" of the current (ICTR) compared to the optimum value: ± 5% is a plausible variation according to what is stated in the foundry manual.

Table 3.4 shows the results obtained by acting on the current generator ICTR. The current ICTR in the auxiliary amplifier could be controlled to compensate variations, thus improving performance.

Table 3.3								
Performance at the variations of the corner process								
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**ICTR [µA]**
TT	601.5	51.5	58.2	348	-102.1	-29.3	10.22	-
FF	179.8	23.6	80.5	1.1	-2.7	-2.7	29.9	-
FS	119.6	21.9	82	0.191	-12.8	-12.8	29.9	-
SF	638.4	51.6	63.18	322	-6.3	-6.3	10.2	-
SS	627.2	51.2	62	257.5	-12.2	-12.2	11.93	-

Table 3.4								
Correction of the performance at the variations of the corner process								
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**ICTR [µA]**
TT	601.5	51.5	58.2	348	-102.1	-29.3	10.22	-
FF	607.51	51.7	57.57	427.6	-116.45	-29.88	9.12	-3.85432
FS	612.66	49.81	55.6	339.8	-128.19	-29.35	10.86	-5.4855
SF	555.18	51.22	59.25	329.59	-93.32	-30.74	10.13	3.9926
SS	596.72	51.47	58.78	276.15	-107.29	-29.48	11.92	2.2676

Table 3.5									
Performances at the variation of +5% of the current source ICTR									
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mφ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**ICTR+5%**	**ICTR [µA]**
TT	601.5	51.5	58.2	348	-102.1	-29.3	10.22	-	-
FF	611	51.69	57.79	425.6	-23.19	-	9.12	-4.043670	-3.85432
FS	615.3	49.79	55.94	337	-22.03	-	10.86	-5.759775	-5.4855
SF	537.19	51.04	59.15	318.15	-13.5	-	10.2	4.19223	3.9926
SS	687.45	51.53	58.1	279.48	-14.43	-	11.9	2.38098	2.2676

Table 3.6									
Performances at the variation of - 5% of the current source ICTR									
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mφ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**ICTR-5%**	**ICTR [µA]**
TT	603.13	51.5	58.2	348	-102.1	-29.3	10.22	-	-
FF	607.7	51.72	57.31	429.8	-19.8	-	9.13	-3.661604	-3.85432
FS	610.1	49.86	55	344.64	-13.15	-	10.87	-5.211225	-5.4855
SF	569.24	51.33	59.52	334.06	-16.48	-	10.14	3.79297	3.9926
SS	602.75	51.43	59.29	273.5	-20.35	-	11.92	2.15422	2.2676

Table 3.7 reports differential and common-mode performance for the proposed topology, compared to the original topology (where the gate of the triode biased NMOS at the source of M3 is connected to a static voltage VDD/2), highlighting the improved CMRR of the proposed one, without degradation of differential-mode performance, and Fig.3.7 shows the common-mode gain: the improvement for typical process parameters is more than 90 dB, and reduces to 20 dB at higher frequencies.

Table 3.7			
Class-AB OTA performance			
Performance	**Proposed**	**Original**	**Unit**
Differential gain	51.56	51.56	**dB**
Unity-Gain Bandwidth	349	349	**MHz**
Phase Margin	58	58	°
Common-Mode Gain (dc)	-102.10	-9.20	**dB**
Peak Common-Mode Gain	-29.29	-9.20	**dB**
Quiescent Power	128	115	**µW**
Settling Time	10.22	10.04	**ns**

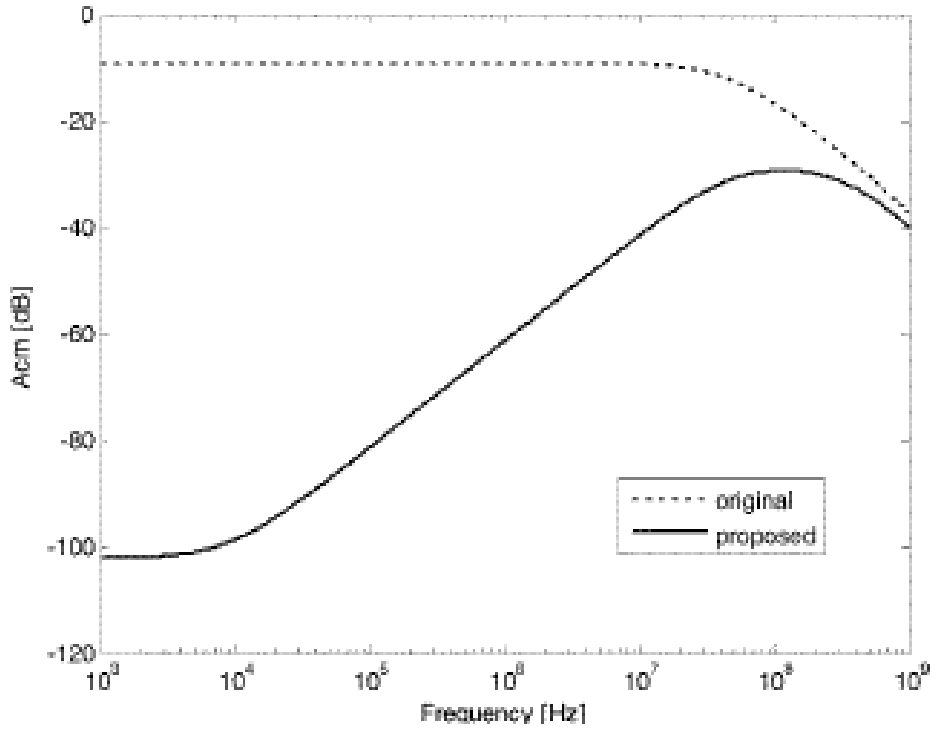


Fig.3. 7: Common-mode gain.

Fig.3.8 shows the histograms of the common-mode gain after 1000 Monte-Carlo iterations, to evaluate the effect of process and mismatch variations; to better highlight the advantage of the proposed topology, the common-mode gain without CMFB is considered.

Figs.3.9 and 3.10 present respectively the dc transfer characteristic and differential-mode gain, showing that they are not affected by the auxiliary block, and Fig.3.11 shows the transient response to a full swing input signal when the amplifier is closed in unity-gain configuration and loaded by 500-fF capacitors.

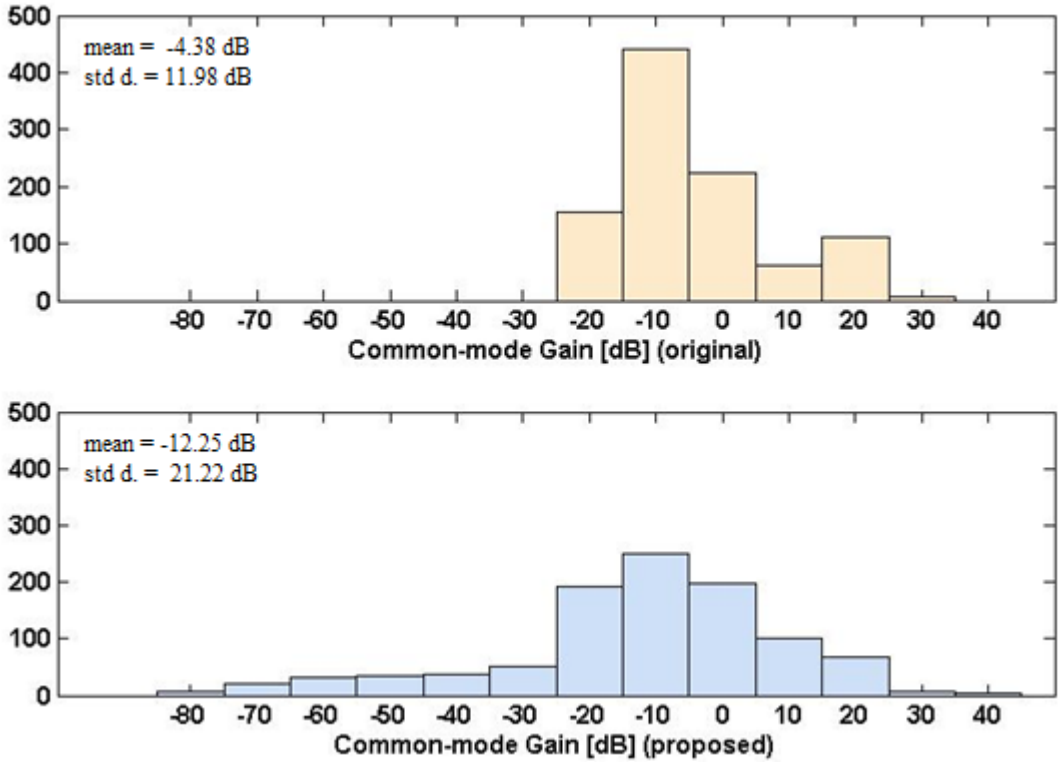


Fig.3. 8: Histogram of common-mode gain (without CMFB): a) original topology; b) proposed topology

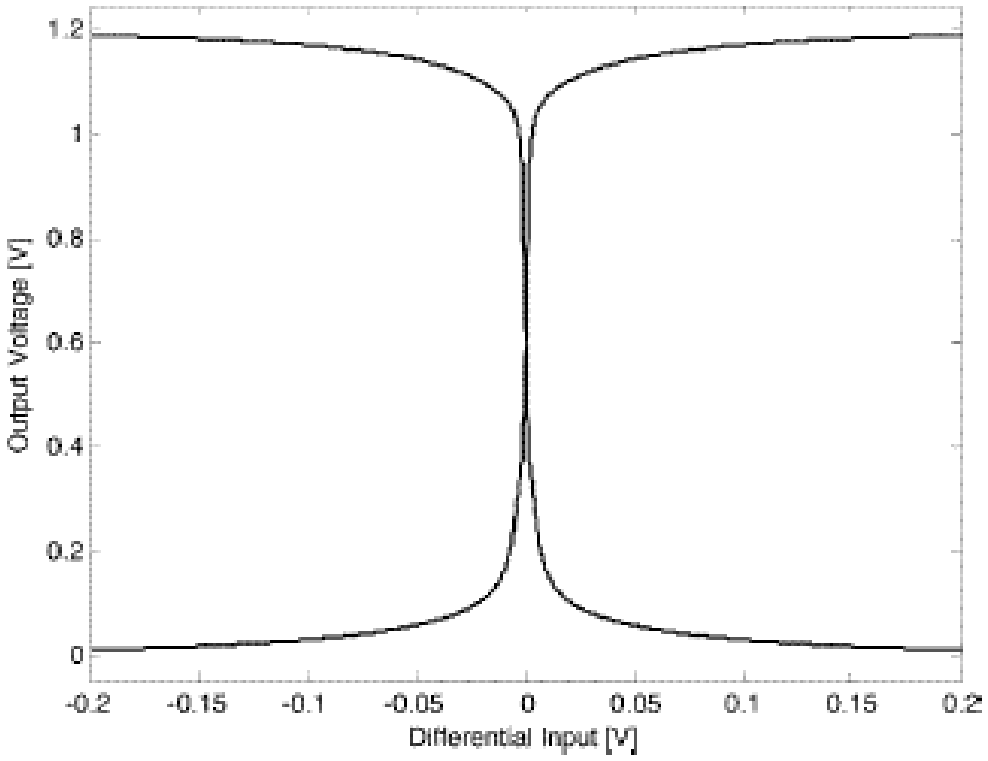


Fig.3. 9: DC transfer characteristic.

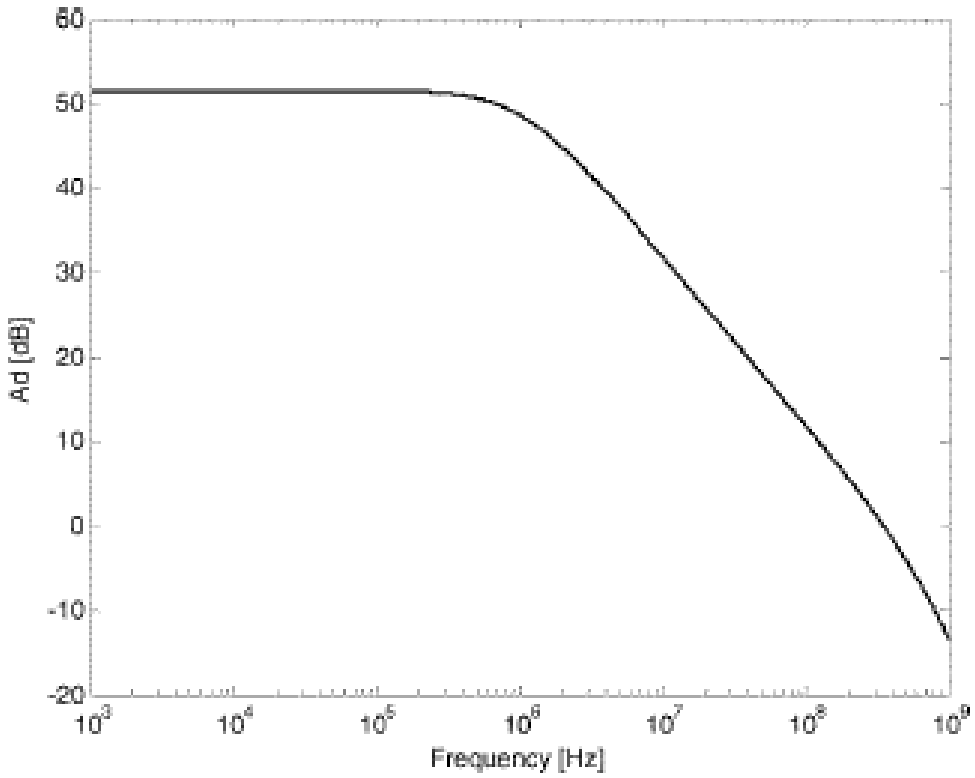


Fig.3. 10: Differential gain.

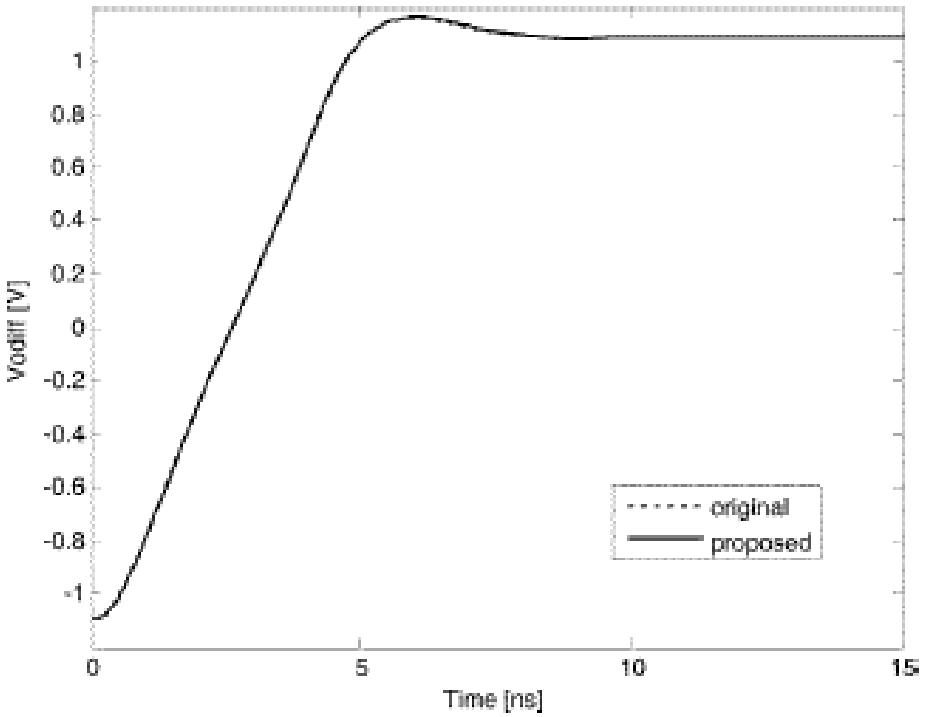


Fig.3. 11: Step response in unity-gain configuration.

3.3.2 OTA test as S/H

The proposed OTA, once the test of robustness at process variations has been passed, has been used in the implementation of a Sample and Hold Amplifier (SHA). The considered SHA bases its operating principle on switched capacitor technique, so it needs proper clock signals to work properly.

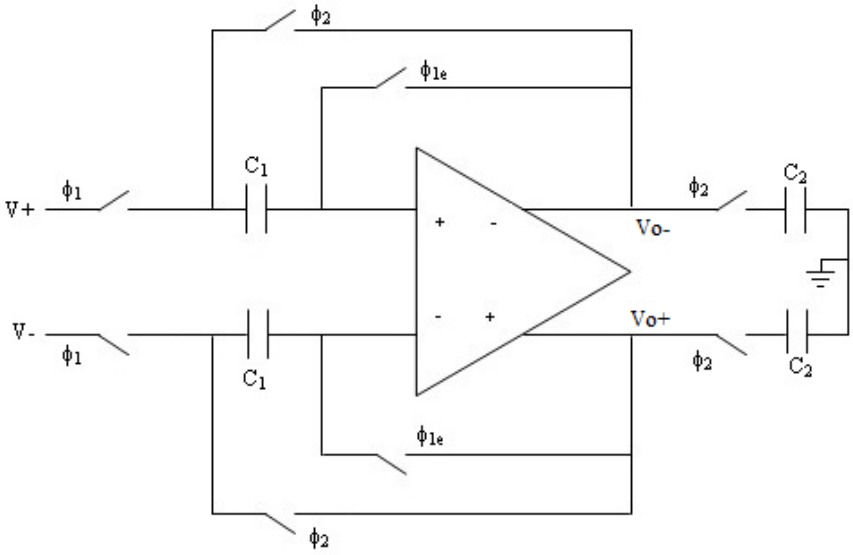


Fig.3. 12: SHA circuit

The clock signals were realized using "Vpulse" generators that were set with the parameters shown in Table 3.9.

Table 3.8

Parametri	Ck1	Ck1e	Ck2	Ck2e
V1 [V]	0	0	0	0
V2 [V]	Vdd	Vdd	Vdd	Vdd
Period [s]	Tck	Tck	Tck	Tck
Delay time [s]	0	0	Tck/2	Tck/2
Rise time [ps]	*tr	*tr	*tr	*tr
Fall time [ps]	*tr	*tr	*tr	*tr
Pulse Width [s]	*Tck/2-tov-2tr	*Tck/2-tov-2tr-dt	*Tck/2-tov-2tr	*Tck/2-tov-2tr-dt

*tr=100p, tov=100p, dt=200p

In Table 3.8, Vdd indicates the supply voltage of the switches, Tck is equal to the sampling time, the rise time (tr) and the fall time (tf) have the same value. The "tov" and "dt" parameters are used to obtain the required pulse width, the "dt" parameter in the specified, to allow early closure of the switches that uses Ck1e and Ck2e. To get the complementary clock signals from the ones shown in Table 3.8, it is sufficient to swap V1 and V2 values. The Fig.3.13 shows the trends of the clock signals used to carry out sample and hold phases.

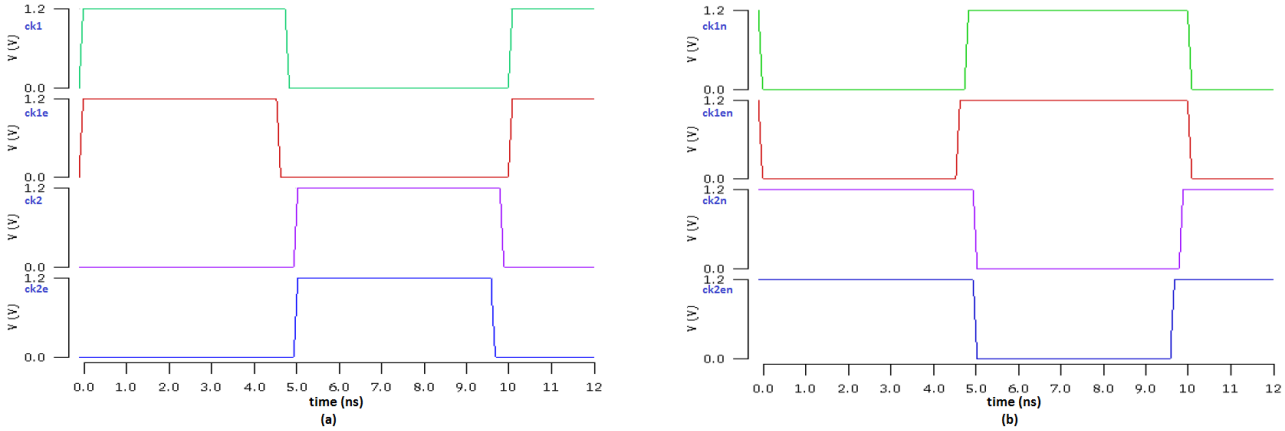


Fig.3. 13: a) Clock signals; b) Complementary clock signals

The OTA has been used to design a 100-MHz flip-around sample-and-hold with 500-fF sample capacitors, and Fig.3.14 shows the output spectrum for an input signal at fs/64 with 800 mV peak differential amplitude. Total harmonic distortion is -65.4 dB, with an average power consumption of 245µW. Table 3.9 shows the performance of the SHA for several cases of sampling frequency.

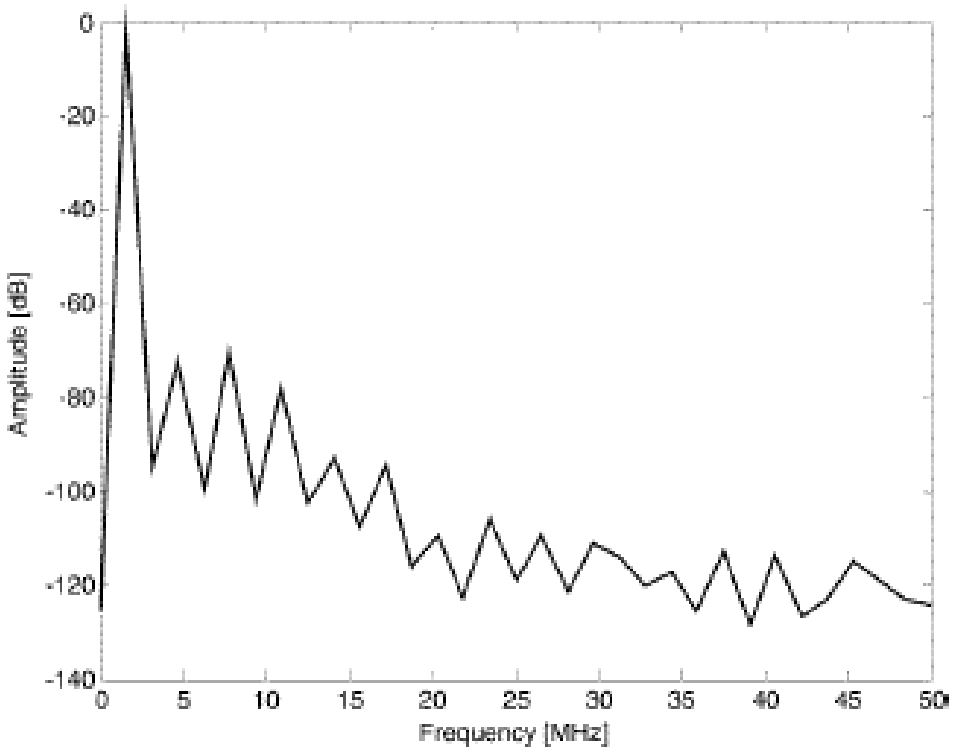


Fig.3. 14: Output spectrum of a 100-MHz sample-and-hold.

Table 3.9		
SHA Performance vs sampling frequency		
fsample (MHz)	**Tck(ns)**	**THD (dB)**
50	20	65.7
100	10	65.4
105	9.5	63.3
111	9	60.97
118	8.5	60.85
125	8	60.3
133	7.5	57.46
143	7	55.47
154	6.5	50.89
167	6	39.89

Conclusion

The class-AB fully differential OTA topology proposed by Peluso in [1] presents very good fully differential performance but low CMRR. An improvement that exploits a simple low-current auxiliary circuit is proposed: common-mode gain is reduced up to 90 dB without affecting differential-mode performance, with a net improvement in CMRR. Monte Carlo simulations show that the proposed topology is somehow sensitive to the gain of the auxiliary amplifier, and the effective CMRR improvement could result lower, however the gain can be controlled by changing the current ICTR in Fig. 3.6b to compensate process variations.

3.4 Second method to improve the performance of Peluso's topology [6]

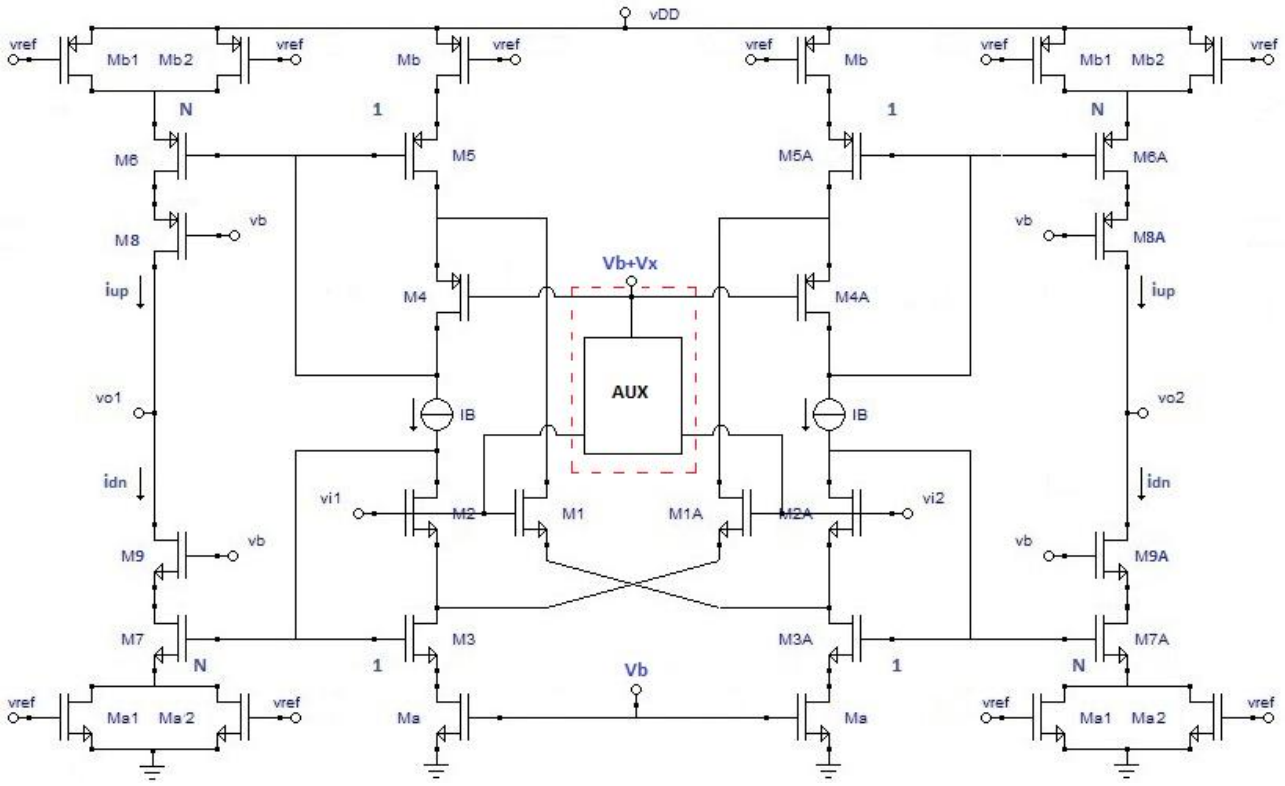


Fig.3. 15: Proposed fully differential OTA topology

The analysis in Section 3.1 shows that CMRR can be enhanced by making also I_{up} (and therefore v_{up}) dependent on the input common-mode signal v_{ic}, so to cancel the common-mode component in I_{dn}. This can be achieved by exploiting the gate terminal of M_4 in the FVF current mirror M_4-M_6: a suitable input signal v_x is superimposed on the bias voltage V_B through the auxiliary amplifier in the dashed box in Fig.3.15. The compensation signal v_x has to depend only on the input common-mode component, not to affect the differential-mode performance, with a suitable gain (or attenuation) to match the common-mode signal components of I_{up} and I_{dn}. The signal v_x has to present opposite phase with respect to the common-mode input component v_{ic}: a positive input common-mode signal v_{ic} results in a lower gate-source voltage of M_7 and a reduction of the current I_{dn}. To obtain a corresponding reduction of I_{up}, the gate voltage of M_6 has to increase, and this can be achieved if the signal v_x is negative.

Consider $v_{i1}=v_{i2}=v_{ic}$; a simplified small-signal analysis of the common-mode half-circuit of the amplifier, shown in Fig.3.2, shows that the transfer functions from the input common- mode signal v_{ic} to the currents i_{up} and i_{dn} are respectively.

$$\frac{i_{up}}{V_{ic}} = \frac{g_{m6}}{A_{o2}A_{o3}}\frac{g_{m1}}{g_{m5}}\left(1+\frac{r_{o2}}{R}\right) - \frac{g_{m6}}{g_{m5}r_{o1}}\left(1-\frac{A_{o1}}{A_{o2}}\right) \quad (3.21)$$

$$\frac{i_{dn}}{V_{ic}} = -\frac{g_{m7}}{A_{o3}} - \frac{g_{m7}}{g_{m3}r_{o1}}\left(1-\frac{A_{o1}}{A_{o2}}\right) \quad (3.22)$$

whereas the transfer functions from the control input v_x to the same currents are

$$\frac{i_{up}}{V_x} = \frac{g_{m6}}{g_{m5}(r_{o1}||r_{o5})} \quad (3.23)$$

$$\frac{i_{dn}}{V_x} = \frac{g_{m7}}{g_{m3}r_{o1}} \quad (3.24)$$

The output voltage is then given by

$$V_{o1} = V_{o2} = V_{oc} = (i_{up} - i_{dn})R_{LOAD} \quad (3.25)$$

Assuming $A_{01}=A_{02}$ we see that the input common-mode voltage affects the output mostly through i_{dn}, whereas v_x affects both i_{up} and i_{dn}. Therefore a signal $v_x=-kv_{ic}$, with

$$k = \frac{A_{o5}}{r_{o3}}\frac{g_{m7}r_{o1}}{g_{m6}g_{m3}r_{o1}+(g_{m6}g_{m3}-g_{m7}g_{m5})r_{o5}} \approx \frac{A_{o5}g_{m7}}{A_{o3}g_{m6}} \quad (3.26)$$

is required to have $i_{up}=i_{dn}$ and cancel the output common-mode component.

The signal v_x is generated by an auxiliary amplifier (corresponding to the block AUX in Fig.3.15, that has to sense the input common-mode voltage and to provide the dc bias V_B on the gate of M_4. Its simplest implementation, shown in Fig. 3.16a, consists of two common-source stages with shorted drains and a diode-connected load, since the required gain is low (and can even be less than 1). As seen in previous section, to make the specifications on dc output voltage and gain independent, a dc current source I_{CTR} can be added.

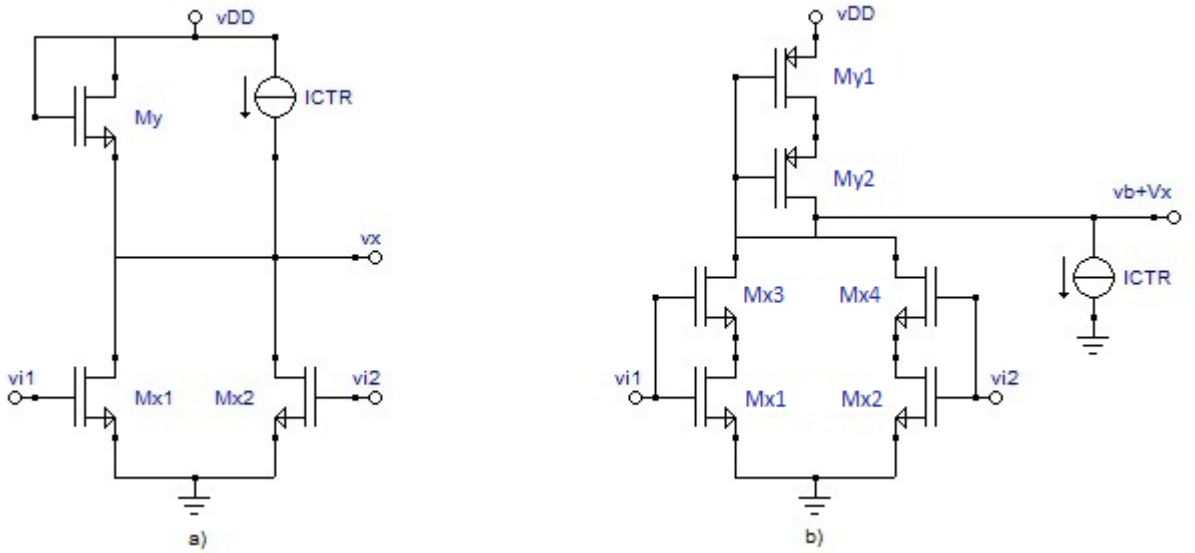


Fig.3.16: Auxiliary amplifier for the proposed topology: a) basic scheme; b) low power implementation.

As seen in previously section with a dc bias level of $V_{DD}/2$, even using minimum size transistors this arrangement could result in a too high current for the auxiliary amplifier.
For circuits biased at very low current, a possible solution is to use MOS devices with longer gates (to reduce the form factor) and exploit self-cascoding to reduce the current for a given gate-source voltage: the resulting amplifier is shown in Fig.3.16b. Obviously this solution increases area consumption and also the input capacitance of the amplifier, thus resulting in a degradation of settling time with respect to the original topology, and a trade-off between power, area and dynamic performance has to be found for the specific design.

3.4.1 Simulations results

A fully differential class-AB OTA based on the proposed topology has been designed and simulated using 40-nm CMOS technology by ST Microelectronics. Cascode transistors in the output branches have been exploited to enhance the differential gain, and a complementary triode CMFB [7] has been used. 0.1-µm gate length has been used for all devices, except the cascode transistors in the output branches, that have 0.25-µm gate length to increase gain. The auxiliary amplifier in Fig. 3.16b has been used to minimize the increase in power consumption; 0.5-µm gate length has been used for all devices, and minimum length has been chosen for the NMOS to keep bias current low. Supply voltage is 1.2V, and 500-fF load capacitors have been added at the outputs.

Table 3.10		
Auxiliary amplifier aspect ratio		
M	**W[µm]**	**L[µm]**
x1,x2,x3,x4	0.12	0.5
y1	1.92	0.5
y2	1.9	0.5

Table 3.11		
Aspect ratio of OTA with triode CMFB		
M	**W[µm]**	**L[µm]**
1,1A	0.47	0.1
2,2A	0.9	0.1
3,3A	0.75	0.1
4,4A	4	0.1
5,5A	2	0.1
6,6A	20	0.1
7,7A	7.5	0.1
a	1.5	0.1
a1,a2	7.5	0.1
b	4	0.1
b1,b2	20	0.1
8,8A	150	0.25
9,9A	35	0.25

In Table 3.10 and 3.11 the aspect ratios of the devices used to design the OTA are reported, together with the CMFB and the auxiliary amplifier, reported in Fig. 3.16 and Fig 3.13 respectively.

Table 3.12								
Performance at the variations of the corner process								
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**Icorr [nA]**
TT	602.3	51.5	58.15	349	-22.1	-	12.1	-
FF	597.3	51.7	56.9	431.8	-44.17	-26.2	10.93	-
FS	573.7	49.7	58.11	350.2	-29.3	-28.7	12.54	-
SF	617.6	51.9	56.6	349.15	-26.4	-22.3	12.27	-
SS	596.4	51.4	59.4	273.2	-43.4	-27.5	13.8	-

Table 3.13								
Correction of the performance at the variations of the corner process								
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**Icorr [nA]**
TT	597	51.5	58.8	347.5	-151.99	-26.7	12.07	358.407
FF	597.7	51.7	57.3	430.5	-164.4	-26.17	10.9	320.391
FS	576.4	49.7	58.19	350.15	-155.23	-28.9	12.5	64.7506
SF	620.46	51.8	57.3	347.42	-150.11	-22.3	12.24	229.404
SS	596.8	51.3	60.2	272	-145.46	-27.4	13.7	327.4255

Table 3.14									
Performances at the variation of +5% of the current source ICTR									
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**+5%**	**Icorr [nA]**
TT	596.8	51.5	58.8	347.4	-49.4	-26.7	12.07	376.32735	358.407
FF	597.5	51.7	57.4	430.4	-51.6	-26.2	10.92	336.41055	320.391
FS	576.4	49.7	58.19	350.15	-67.6	-28.9	12.53	67.98813	64.7506
SF	620.2	51.8	57.3	347.3	-47	-22.3	12.24	240.874725	229.404
SS	596.6	51.3	60.2	272	-48.95	-27.5	13.78	343.796775	327.4255

Table 3.15									
Performances at the variation of -5% of the current source ICTR									
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**-5%**	**Icorr [nA]**
TT	597.3	51.5	58.7	347	-49.2	-26.7	12.07	340.48665	358.407
FF	597.9	51.7	57.3	430.59	-51.5	-26.14	10.92	304.37145	320.391
FS	576.4	49.7	58.19	350.16	-67.5	-28.96	12.53	61.51307	64.7506
SF	620.7	51.8	57.3	347.5	-46.92	-22.26	12.25	217.934275	229.404
SS	597.11	51.3	60.1	272.16	-48.8	-27.45	13.78	311.054225	327.4255

Tab.3.4. reports differential and common-mode performance for the proposed topology, compared to the original topology (where the gate of M_4 is connected to a static voltage $V_{DD}/2$), highlighting the improved CMRR of the proposed one, without degradation of differential-mode performance, and Fig.3.17 shows the common-mode gain: the improvement for typical process parameters is more than 140 dB at low frequency, and reduces at higher frequencies. This is however an ideal situation, and Monte-Carlo and corner simulations have been performed to get a more realistic evaluation.

Table 3.16			
Class-AB OTA performance			
Performance	**Proposed**	**Original**	**Unit**
Differential gain	51.53	51.56	**dB**
Unity-Gain Bandwidth	347	349	**MHz**
Phase Margin	59	58	**°**
Common-Mode Gain (dc)	-151.99	-9.20	**dB**
Peak Common-Mode Gain	-26.75	-9.20	**dB**
Quiescent Power	121	115	**µW**
Settling Time	12.09	10.04	**ns**
Slew Rate	538.3	527.7	**V/µs**
Silicon Area	391	381	**μm^2**

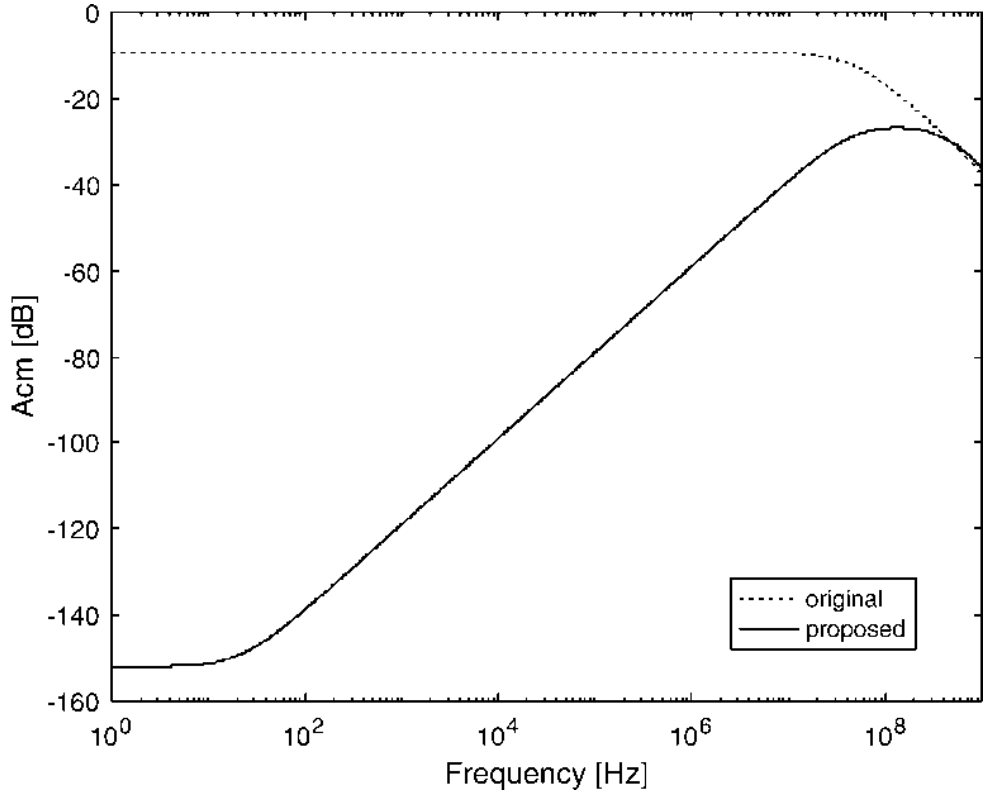


Fig.3. 17: Common-mode gain.

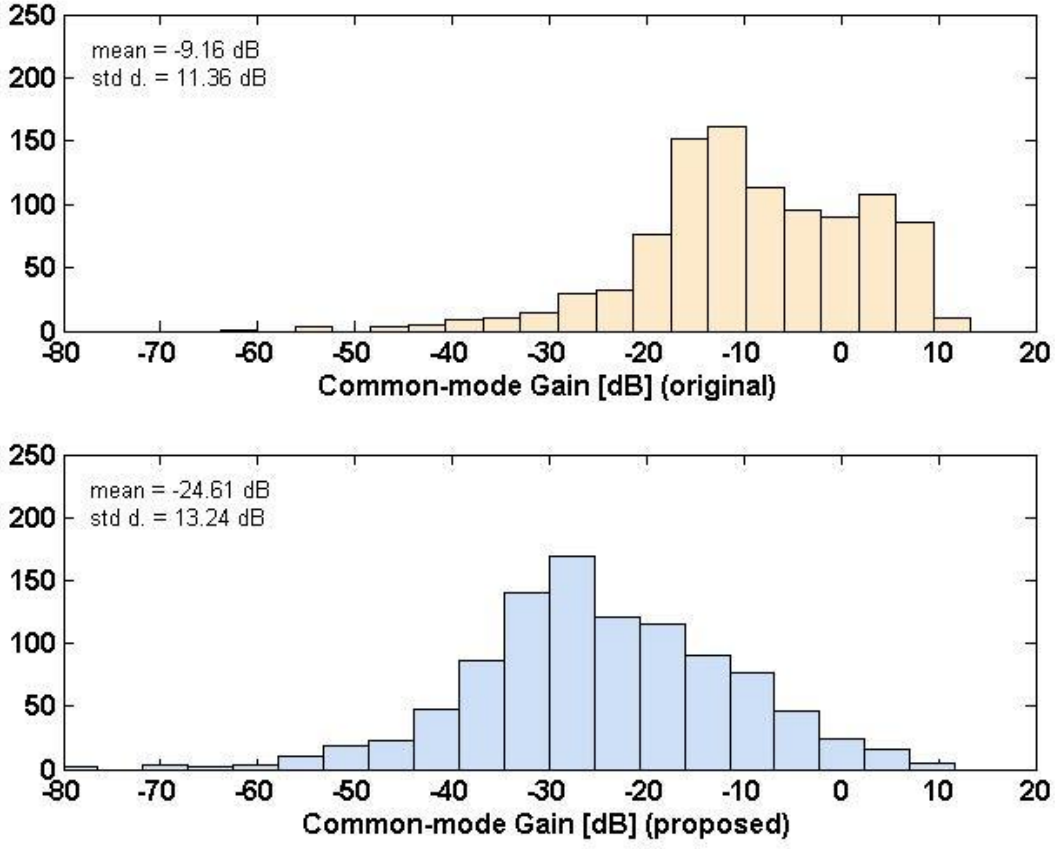


Fig.3. 18: Histogram of dc common-mode gain: a) original topology; b) proposed topology.

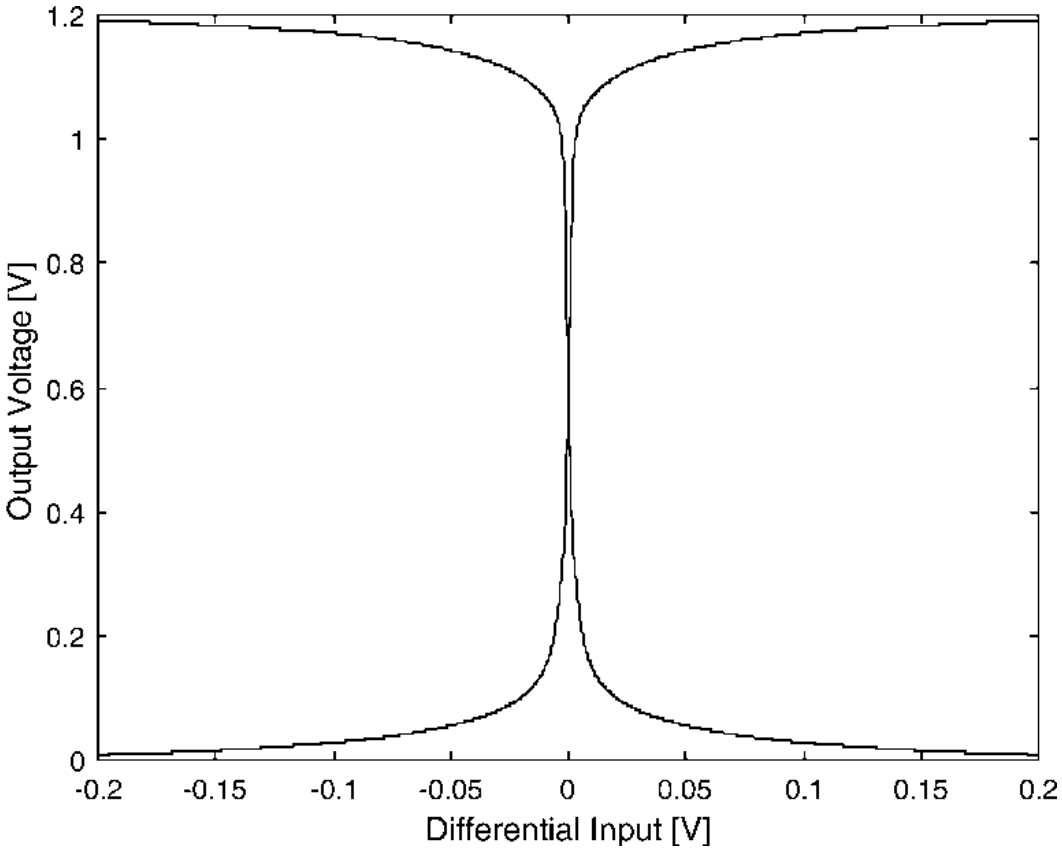


Fig.3. 19: DC transfer characteristic.

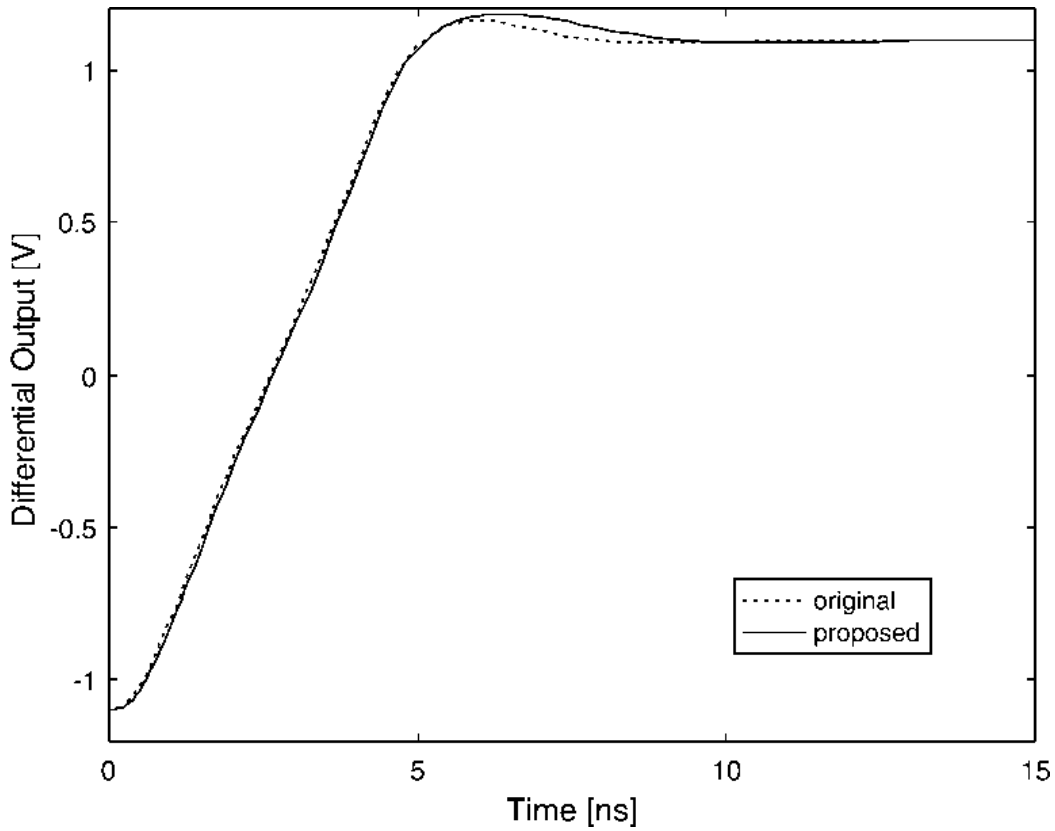


Fig.3. 20: Step response in unity-gain configuration.

Table 3.17				
DC common-mode gain vs. process corners				
Corner	**A_{CM}(dB) proposed**		**A_{CM}(dB) Original**	**I_{CTR} (nA)**
	@I_{CTR}	**@I_{CTR}±5%**		
TT	-151.99	-49	-9-20	358
FF	-164.40	-51	-8.32	320
FS	-155.23	-67	-12.70	65
SF	-150.11	-47	-5.52	229
SS	-145.46	-49	-10.21	327

Fig.3.18 shows the histograms of the common-mode gain after 1000 Monte-Carlo iterations, for both the original topology (without the auxiliary amplifier) and the proposed one, to evaluate the effect of process and mismatch variations; the average improvement of CMRR reduces to about 15 dB (mean values are -9.1 dB and -24.6 dB respectively for the original topology and the proposed one), but the proposed topology still offers an advantage. Moreover, the current I_{CTR} in the auxiliary amplifier could be controlled to compensate variations, thus improving performance. A variation in I_{CTR} changes the gain of the auxiliary amplifier and also the bias voltage V_B: the latter affects the bias point of the main amplifier, that however is controlled by the CMFB.

Table 3.17 reports the dc common-mode gain vs. process corners: by adjusting the current I_{CTR}, a large improvement of CMRR can be achieved in all the process corners, whereas a fixed I_{CTR} would result in some cases in little or no improvement. Obviously, this has to be intended as a limit case, since the current I_{CTR} can be set only within a certain error. As seen in previous paragraph, to evaluate more realistically the performance of the proposed amplifier, the simulations have been repeated considering a ±5% variations of the nominal current in all the process corners, and the results are reported in Table 3.17: the improvement of CMRR reduces to about 40 dB, but the proposed topology still presents performance improvement in all process cases.

Fig.3.19(6) presents the dc transfer characteristic of both the original and proposed topologies (curves are coincident), showing that the auxiliary block does not affect performance, and Fig.3.20(7) shows the transient response to a full swing input signal when the amplifier is closed in unity-gain configuration and loaded by 500-fF capacitors.

Table 3.18		
SHA performance vs sampling frequency		
fsample (MHz)	**Tck(ns)**	**THD (dB)**
50	20	-65.03
100	10	-64.95
105	9.5	-64.76
111	9	-64.41
118	8.5	-64.03
125	8	-63.49
133	7.5	-60.78
143	7	-57.92
154	6.5	-53.13
167	6	-50.15

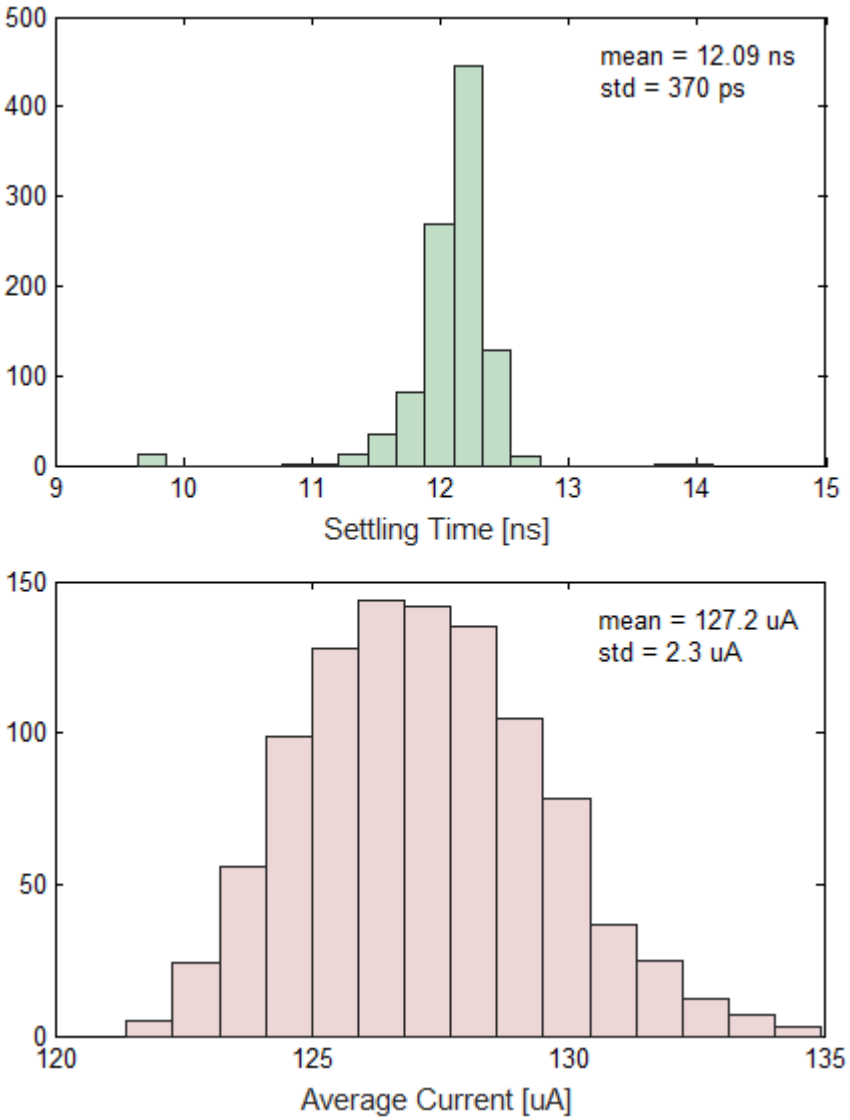


Fig.3. 21: Histogram of: a) settling time; b) Average current for step response (1000 Monte Carlo mismatch simulations).

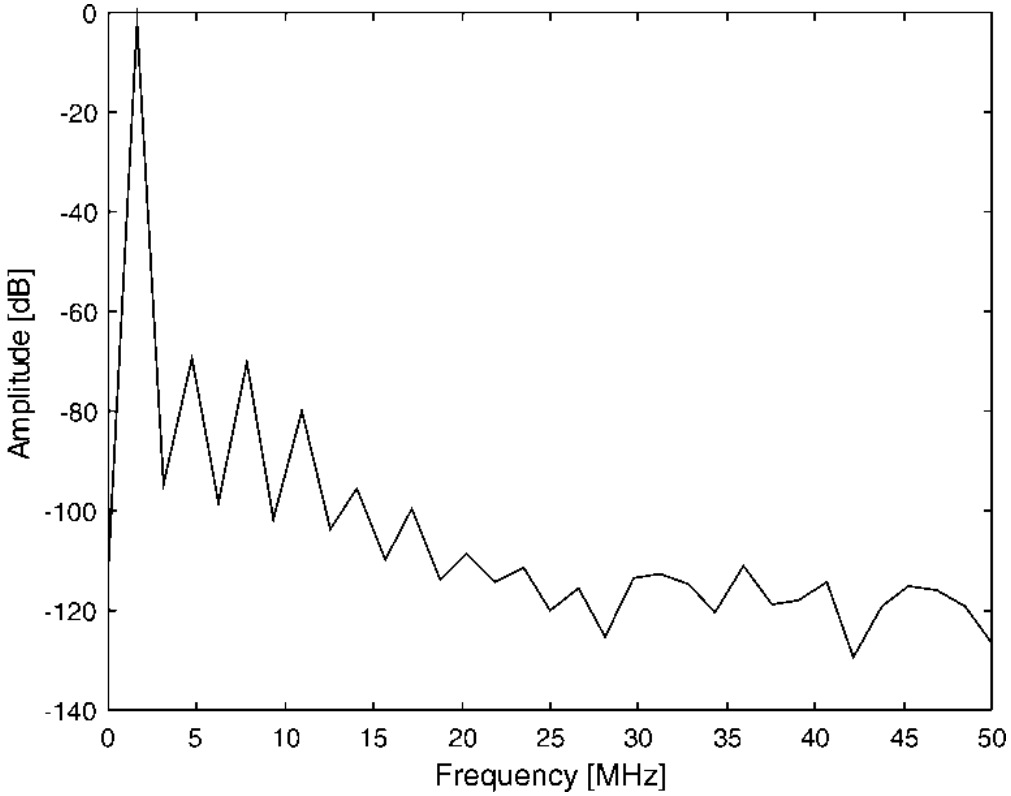


Fig.3. 22: Output spectrum of a 100-MHz sample-and-hold.

I have chosen to use large transistors in the auxiliary amplifier to minimize the excess current of the proposed topology, and this has resulted in a substantial increase in input capacitance of the overall amplifier, so leading to a longer settling time. A settling time similar to the original topology can be achieved using smaller transistors, but current consumption in the auxiliary amplifier is higher. Monte-Carlo simulations have been performed to evaluate the stability of performance under mismatch variations: Fig.3.21 shows the histograms for the settling time and the average current consumption during step response, highlighting a limited spread. The OTA has been used to design a 100-MHz flip-around SHA with 500-fF sample capacitors, and Fig.3.22 shows the output spectrum for an input signal at fs/64 with 800 mV peak differential amplitude. Total harmonic distortion is -65 dB, with an average power consumption of 127 µW. Table 3.18 shows the performance of the SHA vs. sampling frequency.

3.5 Local feedback [8]

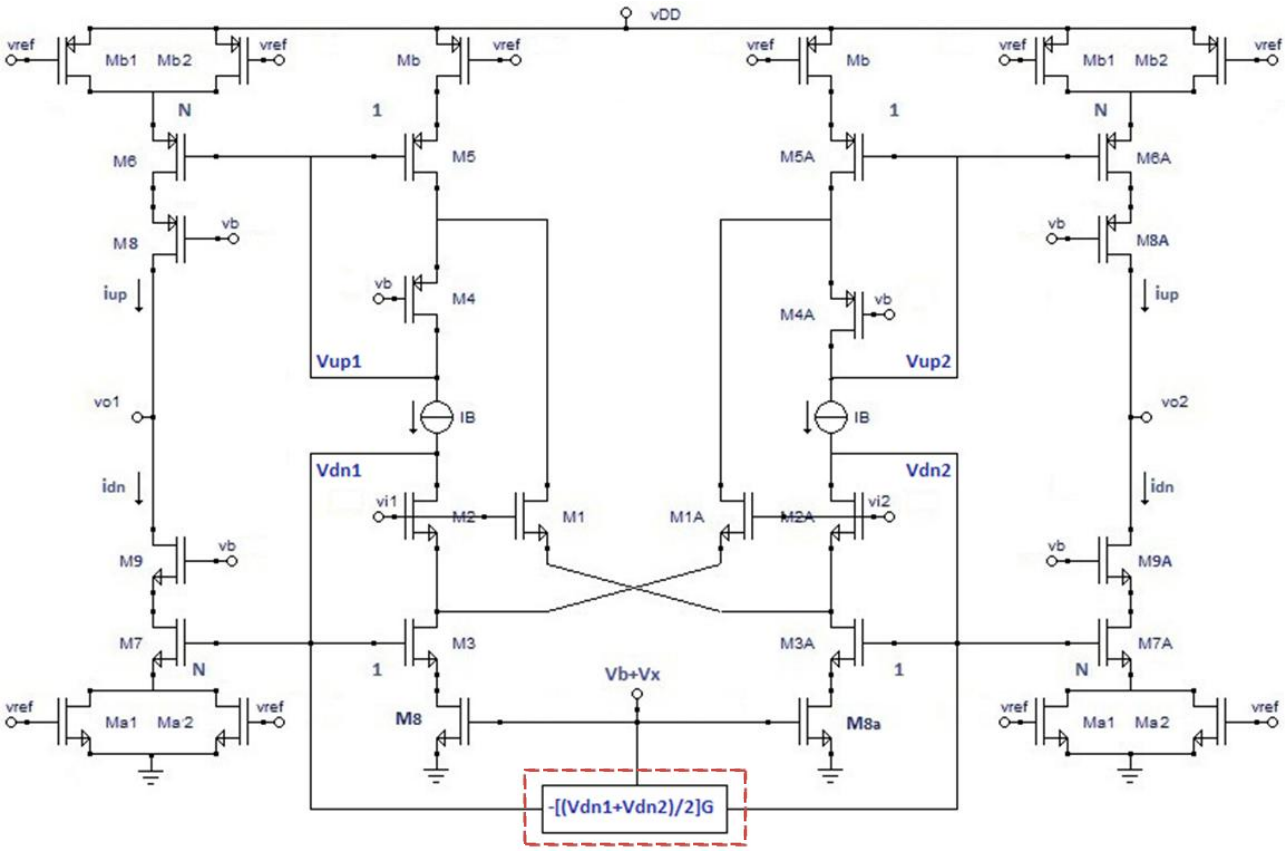


Fig.3. 23: Class-AB OTA with local feedback

In this section I propose an alternative solution that leverages the benefits of negative feedback to enhance the CMRR without affecting the differential-mode performance. The basic idea is to exploit the feedback theory to make the OTA more robust from the point of view of process variations. In the first instance I implemented a single feedback loop as shown in the Fig.3.23. Eqs. (3.30-7) and (3.31-8) show that the gain of the PMOS path is A_0 times lower than the gain of the NMOS path. A simple solution to reduce the common-mode gain would be to add a feedback loop to keep the common-mode component of voltage v_{dn} constant, thus driving A_{dn} to zero. The loop can be closed exploiting the gates of the triode-biased transistors M_8 and M_{8A}, following the approach in [5]. However in deep submicron technologies the intrinsic gain of the transistors is typically low (A_0 could be as low as 20 dB), and a feedback loop acting only on A_{dn} has a limited effect due to the non- negligible value of A_{up}. This idea was abandoned not because it did not work, but because the results were not exciting. In simulation, when I see the transfer function from Vic to Vdn and Vic to Vup, I can see that the first one is not much bigger than the one. So if I do a loop that only stabilizes Vdn, there is improvement but not so much.

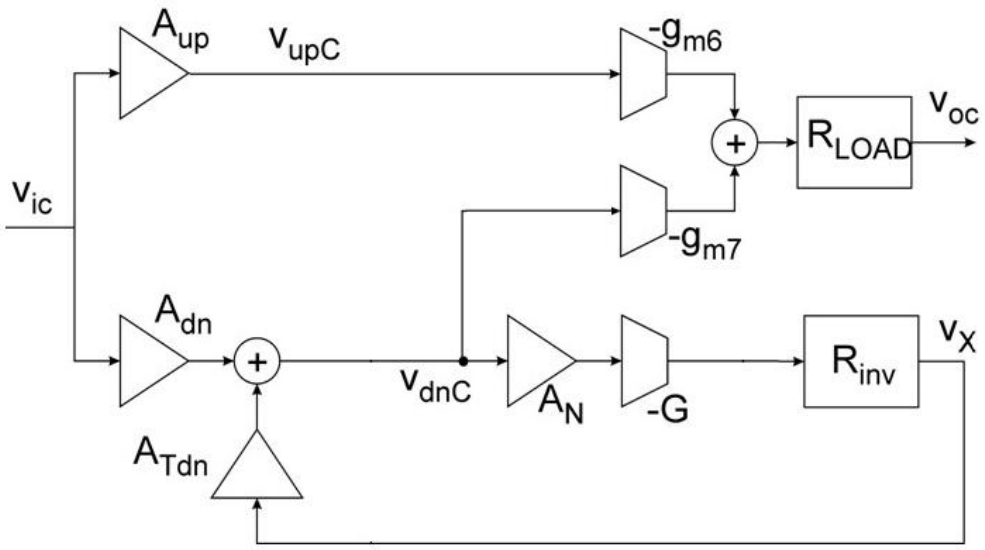


Fig.3. 24: Local feedback implementation

The gain values obtained by simulation in the "virtuoso CADENCE" environment are:

$A_{dn} = \frac{V_{dnC}}{V_{ic}} = -40.2\ dB$

$A_{up} = \frac{V_{upC}}{V_{ic}} = -37.3\ dB$

Fig. 3.25a shows the topology of the OTA by Peluso [1] with a complementary triode-based CMFB [7] to set the output dc voltage. The CMFB also allows reducing the common-mode gain, however it is not enough to have a large CMRR and a safe margin to close the amplifier in a feedback positive for the common-mode. The output voltage can be obtained as

$V_o = -\left(g_{m6}^* V_{up} + g_{m7}^* V_{dn}\right)(r_{06}^* || r_{07}^*)$ (3.27)

where

$r_0^* = g_m r_o r_T + r_o + r_T$ (3.28)

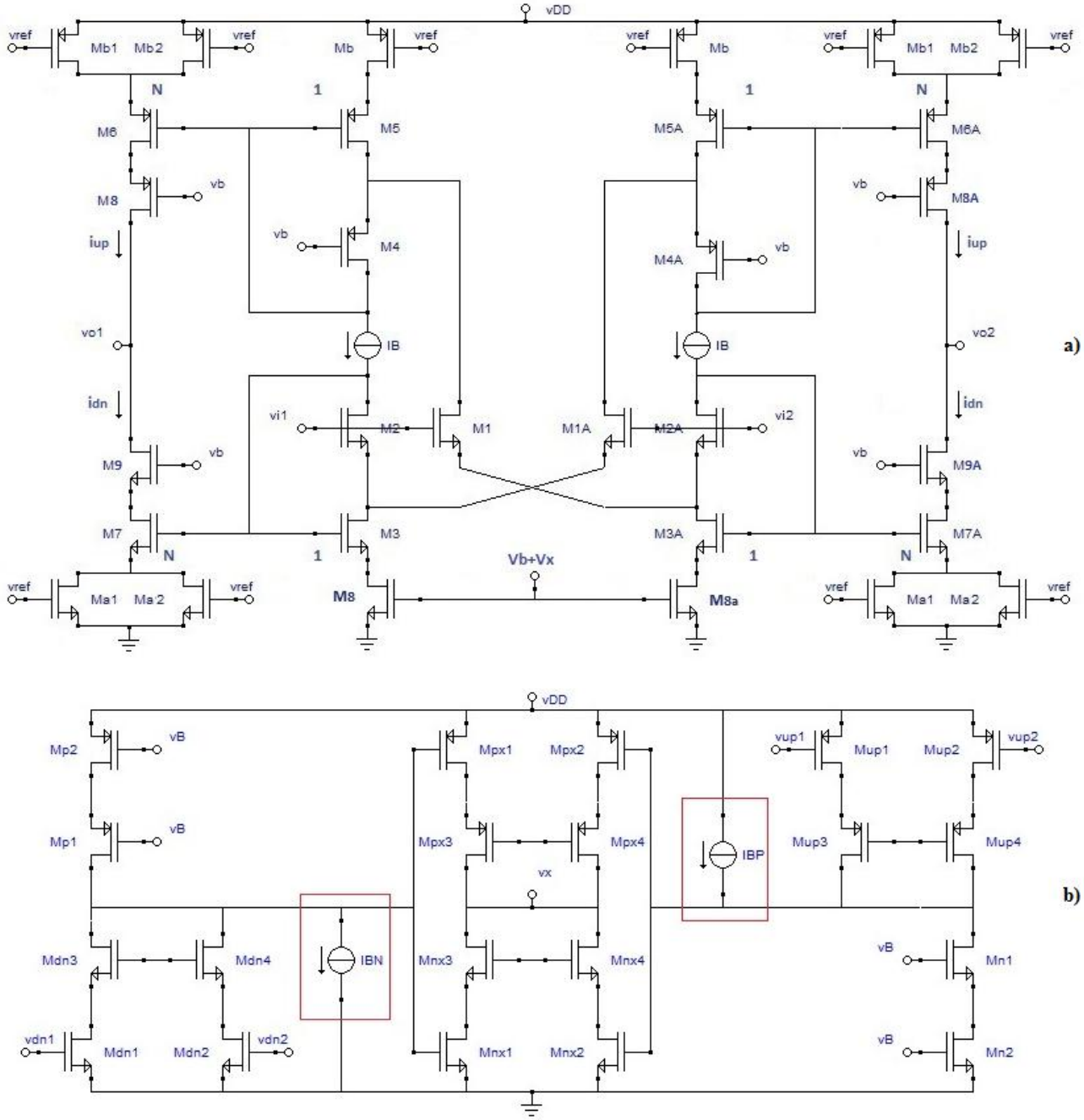


Fig.3. 25: Proposed topology: a) main amplifier; b) local feedback blocks

$$g_m^* = g_m r_o / r_0^* \approx 1/r_T \quad (3.29)$$

take into account the effect of the triode-biased devices (whose transconductance and output resistance are denoted as g_T and r_T). In the following, we will analyze the common-mode behavior of the circuit in case of open CMFB loop.

The analysis of the circuit in Fig.3.25a [9] allows to calculate the transfer functions

$$A_{up} = \frac{V_{upC}}{V_{ic}} = -\frac{1}{A_{o2}A_{o3}}\frac{g_{m1}}{g_{m5}^*}\left(1+\frac{r_{o2}}{R}\right) \quad (3.30)$$

$$A_{dn} = \frac{V_{dnC}}{V_{ic}} = -\frac{1}{A_{o3}} \quad (3.31)$$

where $A_0=g_m r_o$ is the intrinsic gain of the devices and v_{upC} and v_{dnC} denote the common-mode components of v_{up} and v_{dn}.

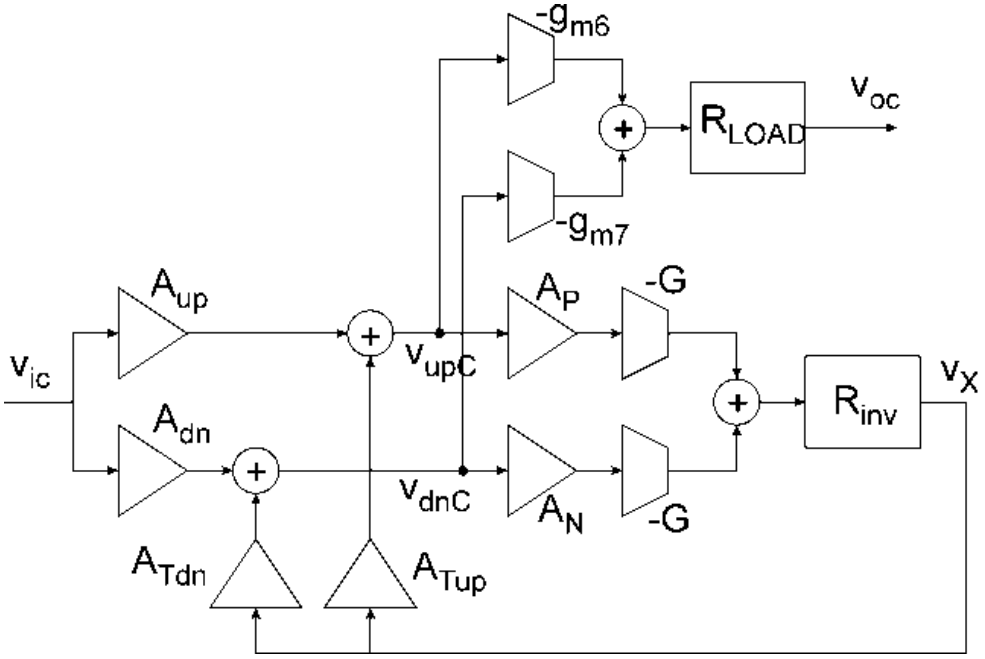


Fig.3. 26: Block scheme of the proposed local feedback loop.

To achieve better results, both gains have to be reduced by the feedback loop, and the solution we propose is shown in Fig. 3.25b. Common source stages with shorted outputs are used to read the common-mode components v_{dnC} and v_{upC}; two inverters with shorted outputs are then used to calculate the average of these voltages, providing also the necessary phase and loop gain and the dc bias to close the loop on the gates of the triode-biased NMOS devices M_8 and M_{8A} (voltage v_X in Fig. 3.25a). The current sources in the common source blocks can be adjusted to compensate process variation, allowing some control on the individual values of v_{upC} and v_{dnC} and not only their average values.

Fig.3.26 shows a block scheme of the proposed local feedback loop, where A_{up} and A_{dn} are given by (3.31-8) and (3.32-9), A_P and A_N are the voltage gains of the common-source amplifiers, the transconductance G and the resistance R_{inv} model the inverters with the shorted outputs, and the gains A_{Tdn} and A_{Tup} are given by [5]

$$A_{Tup} = \frac{V_{up}}{V_X} = -\frac{g_{T8}}{g^*_{m3}} \frac{g_{m1}}{A_{o2} g^*_{m5}} \left(1 + \frac{r_{o2}}{R}\right) \quad (3.32)$$

$$A_{Tdn} = \frac{V_{dn}}{V_X} = -\frac{g_{T8}}{g^*_{m3}} \quad (3.33)$$

From the analysis of the scheme in Fig.3.26 we get

$$V_X = -GR_{inv}\left(A_P V_{upC} + A_N V_{dnC}\right) \quad (3.34)$$

$$V_{upC} = A_{up} V_{ic} + A_{Tup} V_X \quad (3.35)$$

$$V_{dnC} = A_{dn} V_{ic} + A_{Tdn} V_X \quad (3.36)$$

and we can calculate

$$V_{upC} = \frac{A_{up} + GR_{inv} A_N \left(A_{up} A_{Tdn} - A_{dn} A_{Tup}\right)}{1 + GR_{inv}\left(A_P A_{Tup} + A_N A_{Tdn}\right)} \quad (3.37)$$

$$V_{dnC} = \frac{A_{dn} + GR_{inv} A_P \left(A_{dn} A_{Tup} - A_{up} A_{Tdn}\right)}{1 + GR_{inv}\left(A_P A_{Tup} + A_N A_{Tdn}\right)} \quad (3.38)$$

Table 3.19			
Class-AB OTA performance			
Performance	**Proposed**	**Original**	**Units**
Differential Gain	51.3	51.3	**dB**
Unity-Gain Bandwidth	201	201	**MHz**
Phase Margin	57.8	57.8	°
dc Common-Mode Gain	-71	-16	**dB**
Peak Common-mode Gain	-28.5	-16	**dB**
Quiescent Power	129.6	81.6	**µW**
Settling Time	10.2	9.49	**ns**

that show the effect of the local feedback. From (3.30)-(3.33) we also get

$$A_{dn}A_{Tup} - A_{up}A_{Tdn} \approx \frac{g_{m1}g_{T8}}{A_{o2}A_{o3}g^*_{m3}g^*_{m5}}\left(1 + \frac{r_{o2}}{R}\right) \quad (3.39)$$

3.5.1 Simulation Results

In Table 3.20 and 3.21 the aspect ratios of the devices used to design the OTA are reported, together with the CMFB and the auxiliary amplifier, reported in Fig. 3.25.

Table 3.20		
Form factors of the OTA and CMFB MOS transistors		
M	**W[µm]**	**L[µm]**
1,1A	0.17	0.04
2,2A	0.53	0.04
3,3A	0.53	0.04
4,4A	6.55	0.24
5,5A	0.51	0.12
6,6A	3.57	0.12
7,7A	3.64	0.12
8,8A	69.37	0.12
9,9A	12.67	0.12
8,8a	0.32	0.12
a1,a2	0.91	0.12
b,b1,b2	4.62	0.12
Res	48.99K	-

Table 3.21		
Form factors of the auxiliary amplifier MOS transistors		
M	**W[µm]**	**L[µm]**
dn1,dn2	0.5	0.04
dn3,dn4	1.28	0.04
p1	0.48	0.04
p2	5.74	0.04
up1,up2	0.24	0.04
up3,up4	2.87	0.04
n1	2.56	0.04
n2	5.2	0.04
nx1,nx2	0.12	0.12
nx3,nx4	3.4	0.12
px1,px2	0.68	0.12
px3,px4	17.6	0.12

Table 3.22 reports the performance for the proposed topology at the variation of the process corners.

Table 3.23 shows the results obtained by acting on the current generator ICTR that in Fig.3.25 corresponding at IBN and IBP (IBN=IBP=ICTR). The current ICTR in the auxiliary amplifier could be controlled to compensate variations, thus improving performance.

To evaluate more realistically the performance of the proposed amplifier, the simulations have been repeated considering a ±5% variations of the nominal current in all the process corners, and the results are reported in Table 3.24 and Table 3.25.

Table 3.22								
Performance at the variations of the corner process								
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**I_{CTR} [µA]**
TT	599.99	51.3	57.8	201	-71	-28.5	9.47	-
FF	638	51	57.6	248	-43	-24.5	7.6	-
FS	640	49.49	55.2	188	-20	-	12.4	-
SF	501	50.5	68.4	110.63	-41.4	-39	13.4	-
SS	575	51.6	59.4	152.69	-43.8	-24.7	13.29	-

Table 3.23								
Correction of the performance at the variations of the corner process								
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**I_{CTR} [µA]**
TT	599.99	51.3	57.8	201	-71	-28.5	9.47	-
FF	611	51.2	55.7	253.6	-72.9	-28.7	7.6	1
FS	622	49.6	52	200.5	-52.9	-25.2	12.4	6
SF	555.26	51.5	63.5	167.7	-55.2	-21.4	13.5	-5.5
SS	596.57	51.4	60.2	151.94	-54	-25.3	13.3	-0.5

Table 3.24									
Performances at the variation of +5% of the current source ICTR									
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**+5%**	**I_{CTR} [µA]**
TT	599.99	51.3	57.8	201	-71	-28.5	9.47		-
FF	609.7	51.2	55.9	259.7	-63.9	-28.7	8.19	1.05	1
FS	616.2	49.6	51.3	205.6	-52.1	-26.7	12.87	6.3	6
SF	562.2	51.5	63.6	174.6	-47	-26.8	11.63	-5.775	-5.5
SS	597.7	51.4	60.3	151.9	-55.3	-26	13.12	-0.525	-0.5

Table 3.25									
Performances at the variation of -5% of the current source ICTR									
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mϕ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**Tset [ns]**	**I_{CTR} [µA]**	**-5%**
TT	599.99	51.3	57.8	201	-71	-28.5	9.47	-	
FF	612.5	51.6	56.8	203.4	-74.8	-28.4	8.21	1	0.95
FS	629.2	49.5	53.1	199	-50.2	-23.8	13	6	5.7
SF	549	51.5	63.8	168	-65.6	-12.2	13.3	-5.5	-5.225
SS	595.4	51.4	60.2	152.3	-53.1	-25.6	13.12	-0.5	-0.475

A fully differential class-AB OTA based on the proposed topology has been designed and simulated using 40-nm technology. The output branches have been cascoded to increase the voltage gain; supply voltage is 1.2V and 500fF load capacitors have been used as loads. Tab. 3.15 reports differential and common-mode performance for the proposed topology, compared to the original topology (where v_X is connected to the static reference voltage $v_X=V_{DD}/2$), highlighting the improved CMRR of the proposed one, without degradation of differential-mode performance. Fig.3.27 shows the Bode plot of the common-mode gain: the improvement for typical process parameters is more than 50dB.

Figs.3.29 and 3.30 present the dc transfer characteristic and differential-mode gain respectively, showing that they are not affected by the auxiliary block, and Fig.3.31 shows the transient response to a full-swing input signal when the amplifier is closed in unity-gain configuration and loaded by 500fF capacitors. The OTA has been used to design a 50-MHz sample-and-hold (SHA) with 500fF sample capacitors, and Fig.3.32 shows the output spectrum for an input signal at $f_S/64$ with 0.5V peak-peak differential amplitude.

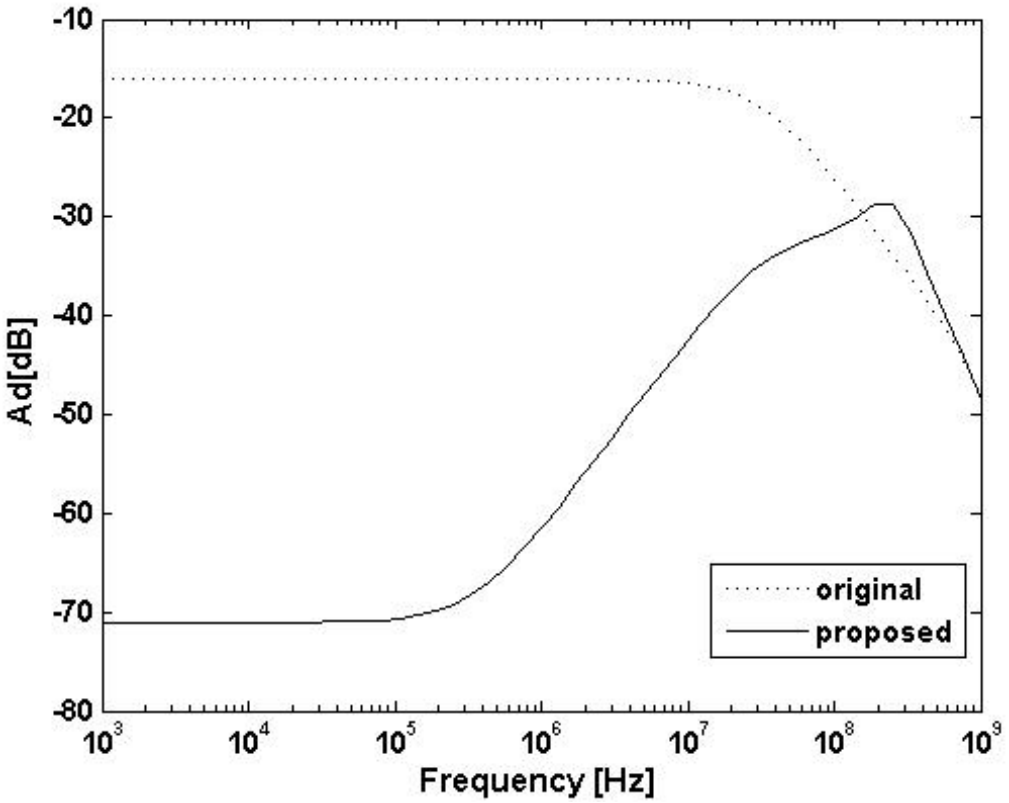


Fig.3. 27: Common-mode gain.

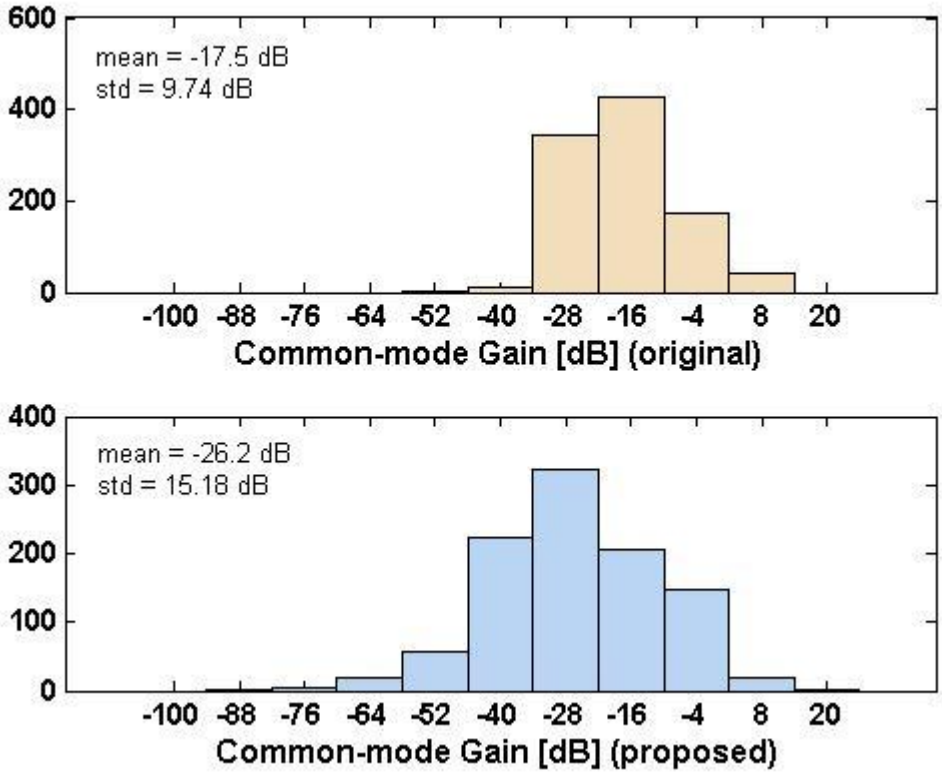


Fig.3. 28: Histogram of dc common-mode gain: a) Original topology; b) proposed topology.

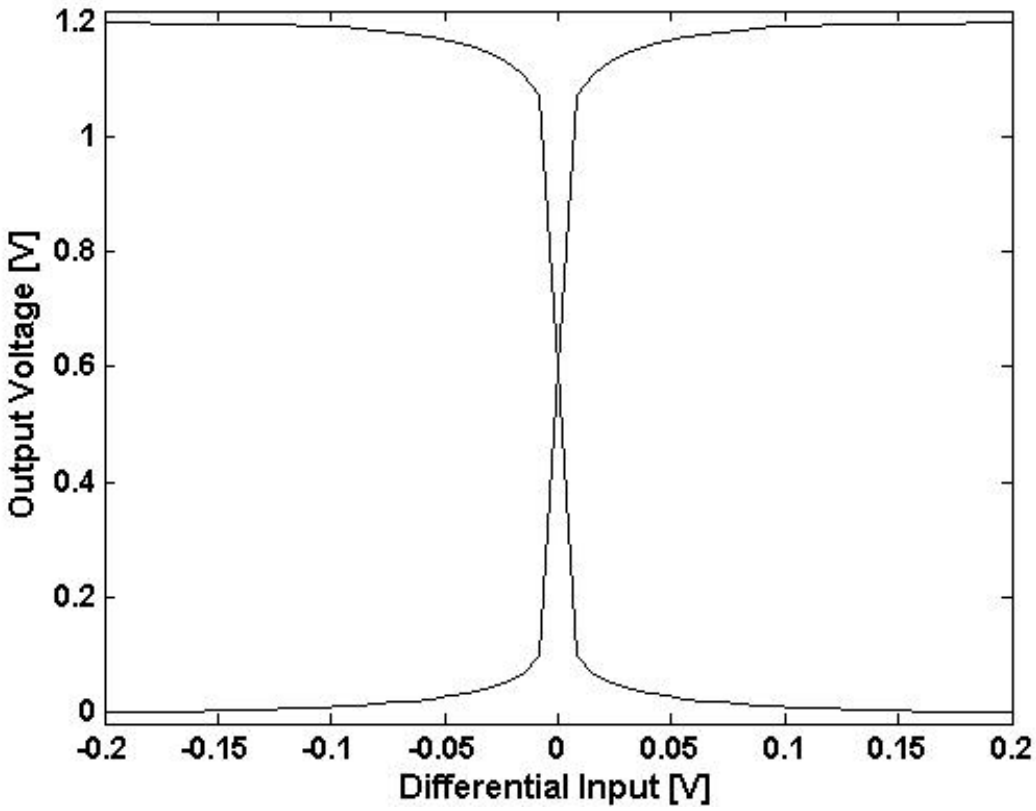


Fig.3. 29: DC transfer characteristic.

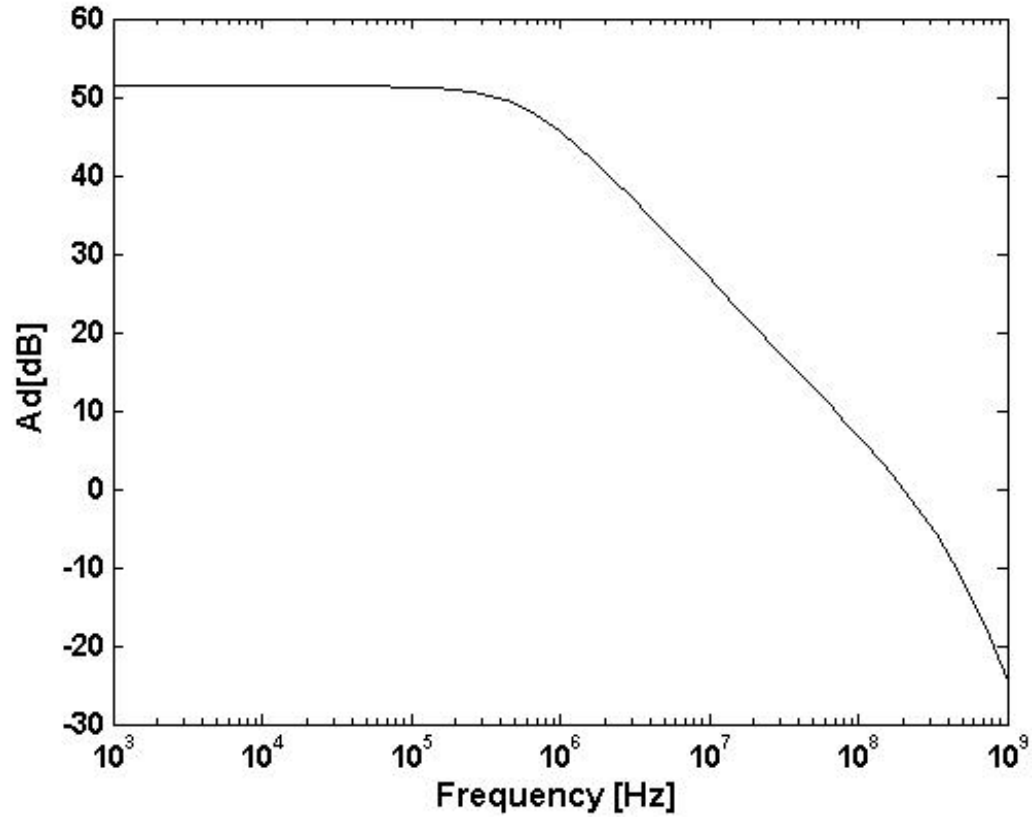


Fig.3. 30: Differential gain.

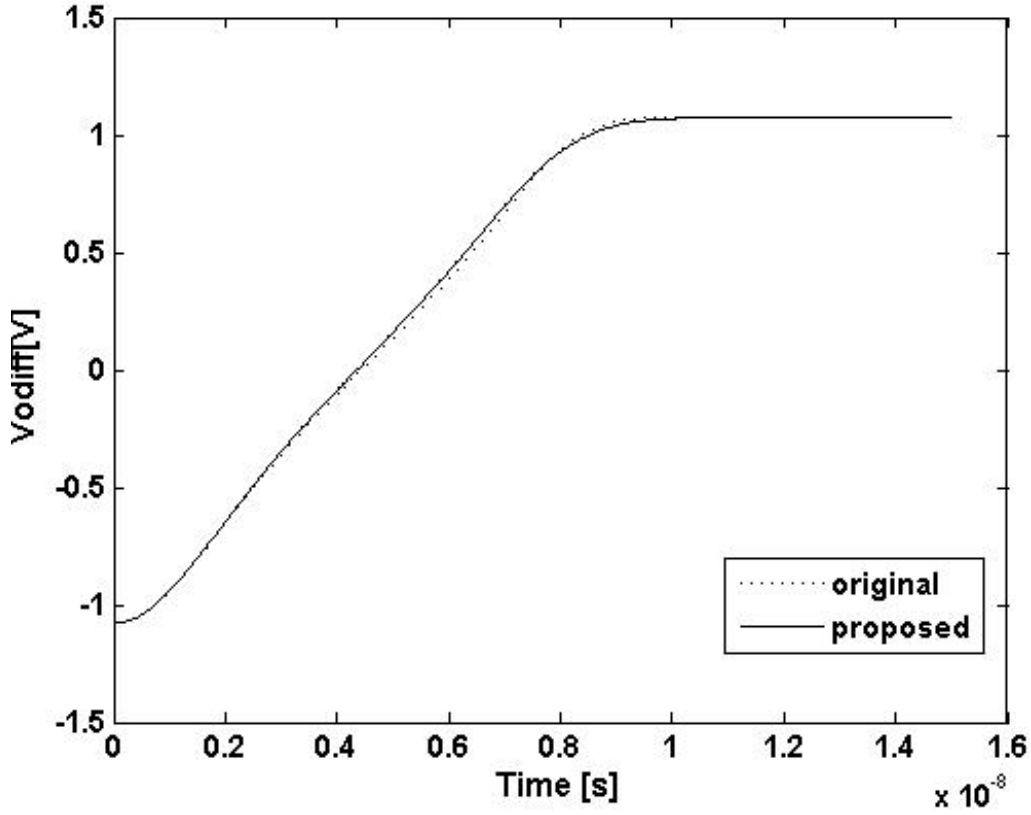


Fig.3. 31: Step response in unity-gain configuration.

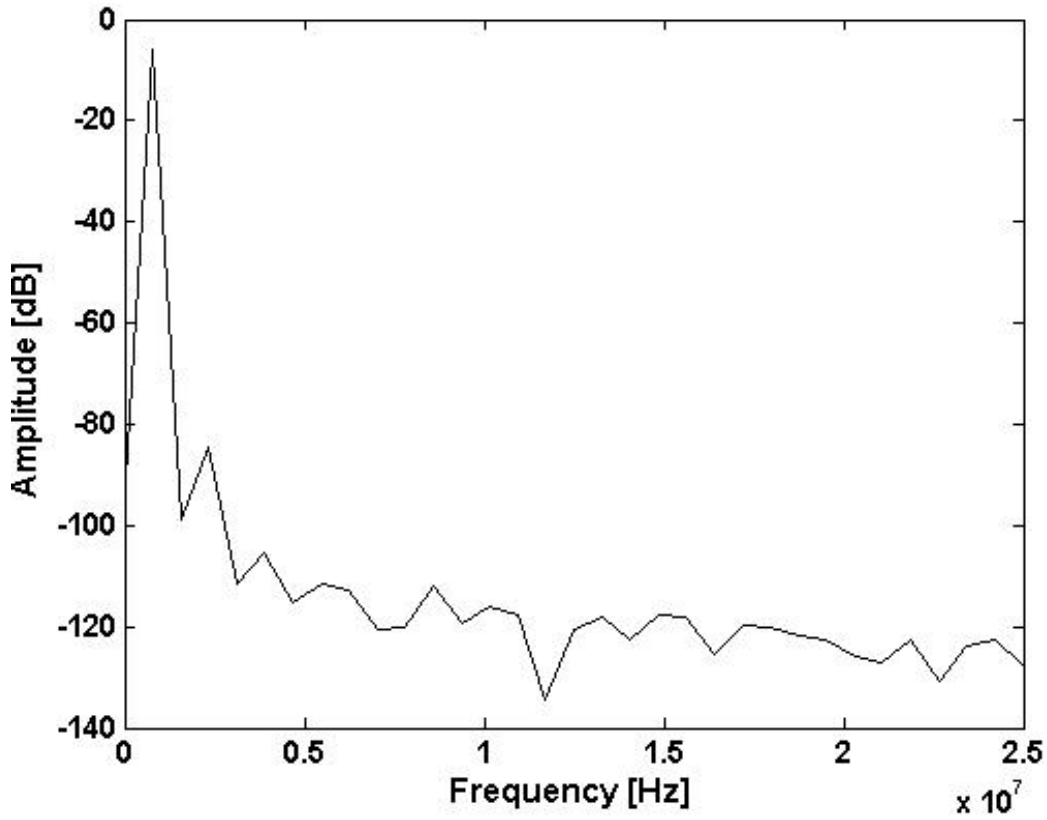


Fig.3. 32: Output spectrum of a 50-MHz sample-and-hold.

Total harmonic distortion is -73.3 dB for an input signal at $f_S/64$ with 0.5V peak-peak differential amplitude, and an average power consumption of 157.3 µW.

Table 3.26 shows the results of the class AB OTA test as Sample and Hold Amplifier (SHA) for an input signal at fs/64 with 800 mV peak differential amplitude, as in the cases discussed in the previous paragraphs.

Table 3.26		
SHA Performance vs sampling frequency		
fsample (MHz)	**Tck(ns)**	**THD (dB)**
50	20	61.9
100	10	54
105	9.5	53.6
111	9	53.3
118	8.5	53.1
125	8	52.7
133	7.5	47.2
143	7	41.5
154	6.5	39.9
167	6	38.3

Conclusions

The class-AB fully differential OTA topology proposed by Peluso in [1] presents very good fully differential performance but low CMRR. An improvement that exploits a local feedback is proposed: common-mode gain is reduced up to 71 dB without affecting differential-mode performance, with a net improvement in CMRR. Good results are obtained for a sample-and-hold exploiting the proposed amplifier.

Chapter 4

Further optimizations of class AB OTA topologies

In this chapter I will present others optimizations of class AB OTA topologies I have done in the PhD course. In the first two paragraphs, I present class AB OTA applications at very low voltage, going to optimize in one case the robustness under corners process variations of the Peluso [1] topology and in the other the input dynamics of the same topology in a single ended version used in non-inverting configuration. Even for supply voltages below the volt, Peluso topology has good performance.

In the first paragraph, as an alternative to the triode CMFB I propose another type of CMFB applicable to class AB structures that generally have no constant current generators within the original structure. Therefore, the performance of the Peluso topology will be evaluated for 0.8 volts supply voltage using a self-referenced CMFB.

In the second paragraph I went down to 0.6 Volt supply voltage and compared me to the problems that arise when working with voltages below the Volt if a single ended (SE) amplifier is used.

In the third paragraph I will consider the topology of Ramirez-Angulo [2] examined in Chapter 2, I will propose a method that reduces a bit the consumption and improves some performance.

In the fourth paragraph I will propose an alternative way of realizing a class AB starting from the Peluso topology making appropriate circuit arrangements.
As in the cases seen in Chapter 3, I will use the same technology as that provided by STMicroelectronic with a 40 nanometer production process.

4.1 Self-referenced CMFB by body

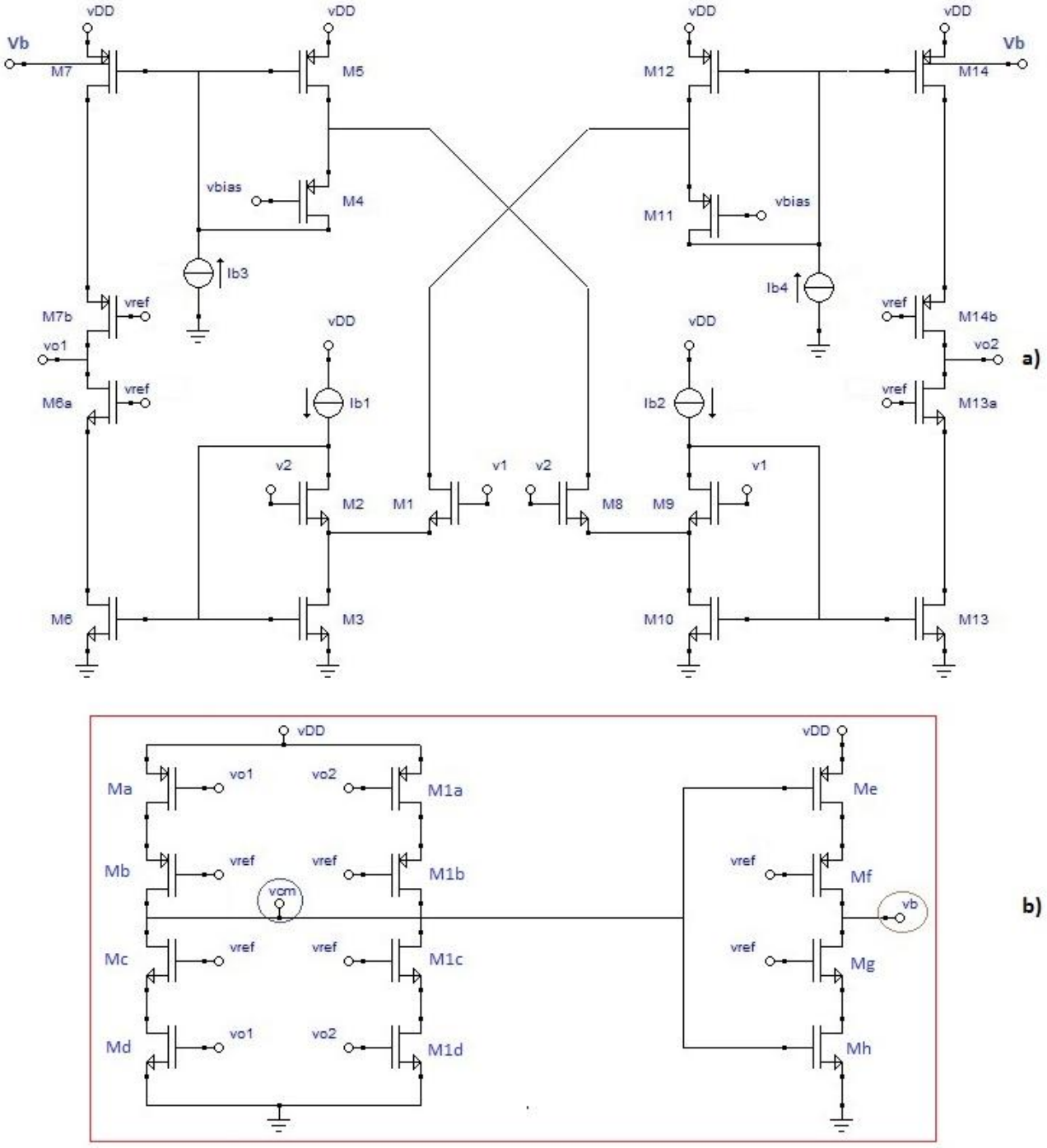


Fig.4. 1: a) Peluso topology; b) Self-referenced CMFB

In this section, I exploit another potential of the Peluso topology, that is to say that it can be used for very low power supply voltages. In this case, the supply voltage is fixed at 0.8 volts and the price to pay is to have four current generators to bias the structure instead of the two required in the topologies presented in Chapter 3. In the previous chapter, three possible methods were proposed to increase the performance of Peluso's topology from the point of view of the "CMRR". The first two methods used open loop techniques while a closed loop method was used for the last proposed method.

In this section, I propose a CMFB that is suitable for working with class AB architectures with very low power voltages. Fig.4.1b shows the proposed CMFB that allows the same performance as those obtained in the previous chapter.
In Table 4.1 and 4.2 the aspect ratios of the devices used to design the OTA are reported, together with the CMFB proposed. Table 4.3 reports the performance for the original topology (without CMFB) by considering typical case.

Table 4.1		
Aspect ratio of OTA		
M	**W[µm]**	**L[µm]**
1,8	20.52	0.04
2,9	29.6	0.04
3,10	0.3	0.12
4,11	7	0.24
5,12	1.25	0.12
6,13	0.3	0.12
6a,13a	2.25	0.12
7,14	0.5	0.12
7b,14b	11.9	0.12

Table 4.2		
CMFB aspect ratio		
M	**W[µm]**	**L[µm]**
a,1a	2.77	0.12
b,1b	2.75	0.12
c,1c	0.36	0.12
d,1d	0.4	0.12
e	2.75	0.12
f	2.75	0.12
g	0.4	0.12
h	0.4	0.12

Table 4.3 reports the performance for the original topology in typical process case. Fig.4.2 shows the voltage gain and the phase. Fig.4.3 shows the common-mode gain: the improvement for typical process parameters is more than 100 dB at low frequency, and reduces at higher frequencies.
Table 4.4 reports the performance for the proposed topology by considering variation of the process corners. A large improvement of CMRR is achieved in all the process corners. In all cases, the obtained values differ little from those obtained in the typical case, so the structure is robust. Common-mode gain is reduced without affecting differential-mode performance, with a net improvement of CMRR. Fig.4.5 show the histograms of the common-mode gain after 1000 Monte-Carlo iterations, for both the original topology and the proposed one, to evaluate the effect of process and mismatch variations, therefore the structure is robust.

Table 4.3							
Performance topology of Fig.4.1 without CMFB							
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mφ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**VDD [V]**
TT	400	50.9	81.5	43.42	18.7	-	0.8

Table 4.4							
Performance at the variations of the corner process with CMFB							
Corner	**V0_dc [mV]**	**AV_dif [dB]**	**mφ [°]**	**fu [MHz]**	**AVcm_dc [dB]**	**AVcm_pk [dB]**	**VDD [V]**
TT	400	50.9	81.5	43.42	-111.69	-29	0.8
FF	399.8	51.5	80.8	46.15	-110.7	-29.11	0.8
FS	366	49.7	79.7	51	-111.46	-29.2	0.8
SF	433	50	83	36.9	-109.3	-28.9	0.8
SS	400	49	82.3	39.86	-111.3	-29.19	0.8

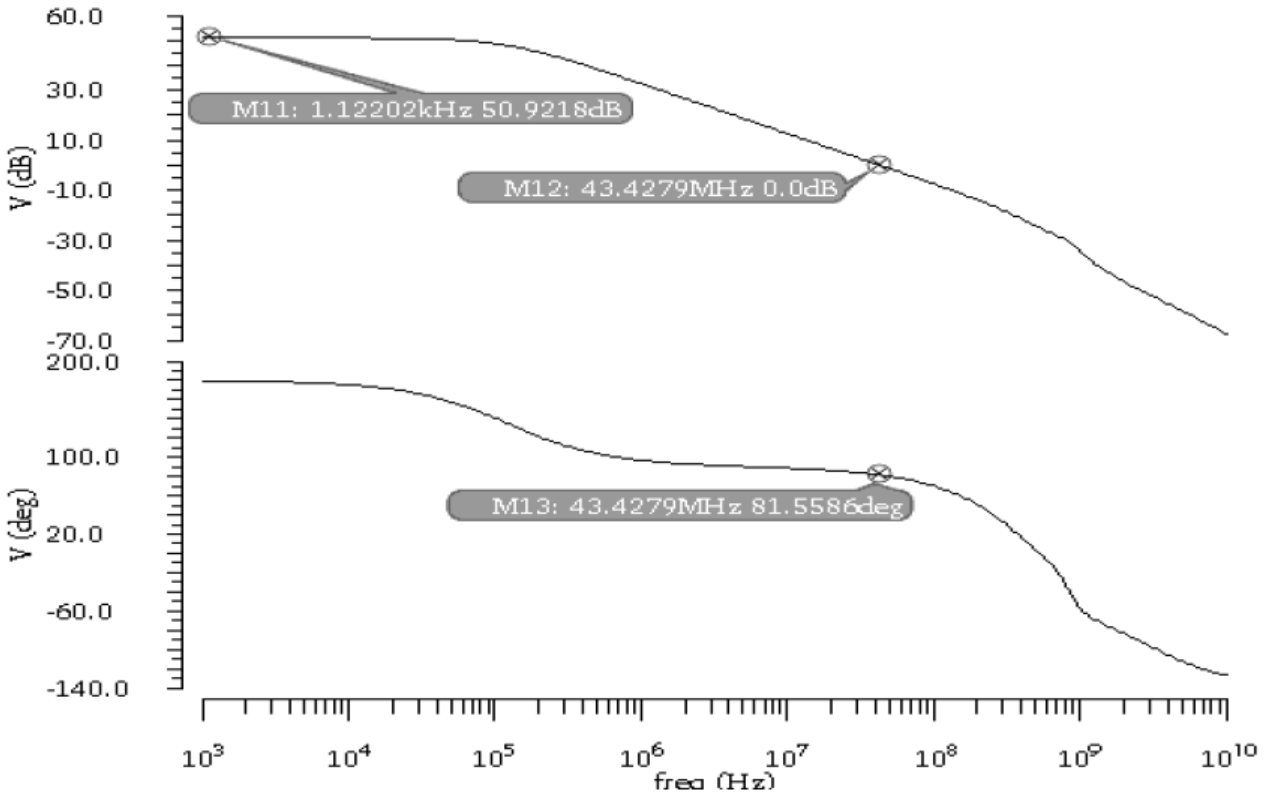


Fig.4. 2: Voltage gain and phase of class-AB OTA

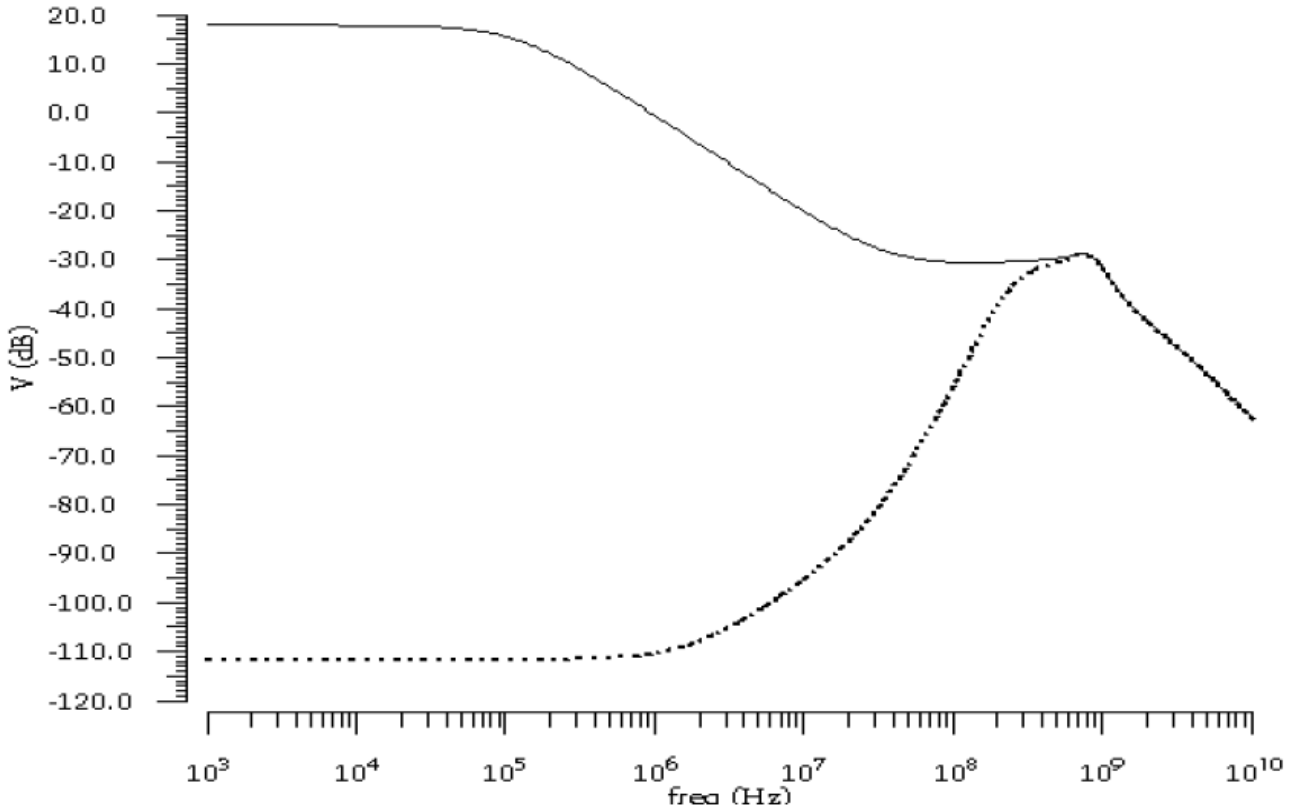


Fig.4. 3: Common mode gain without CMFB in continuous line and with CMFB in dotted line

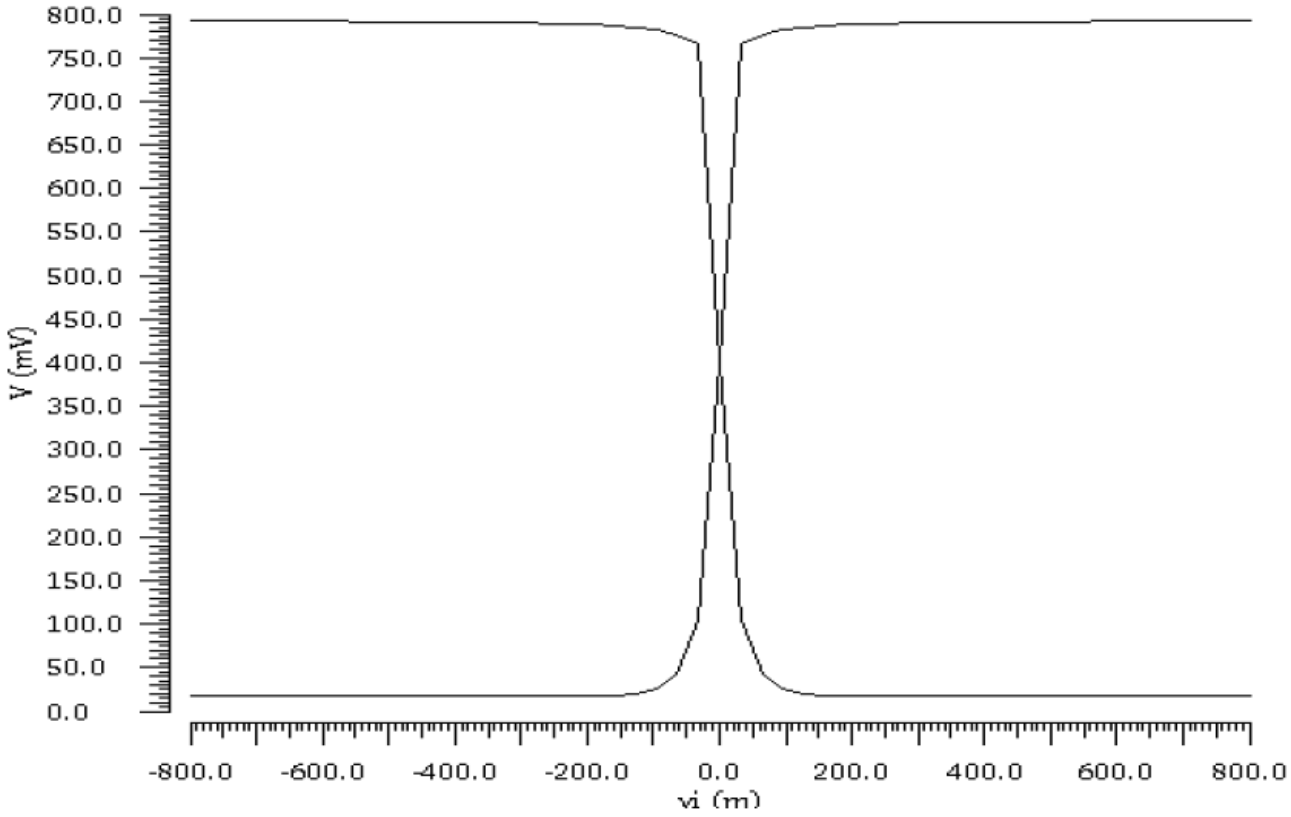


Fig.4. 4: DC transfer characterist with CMFB

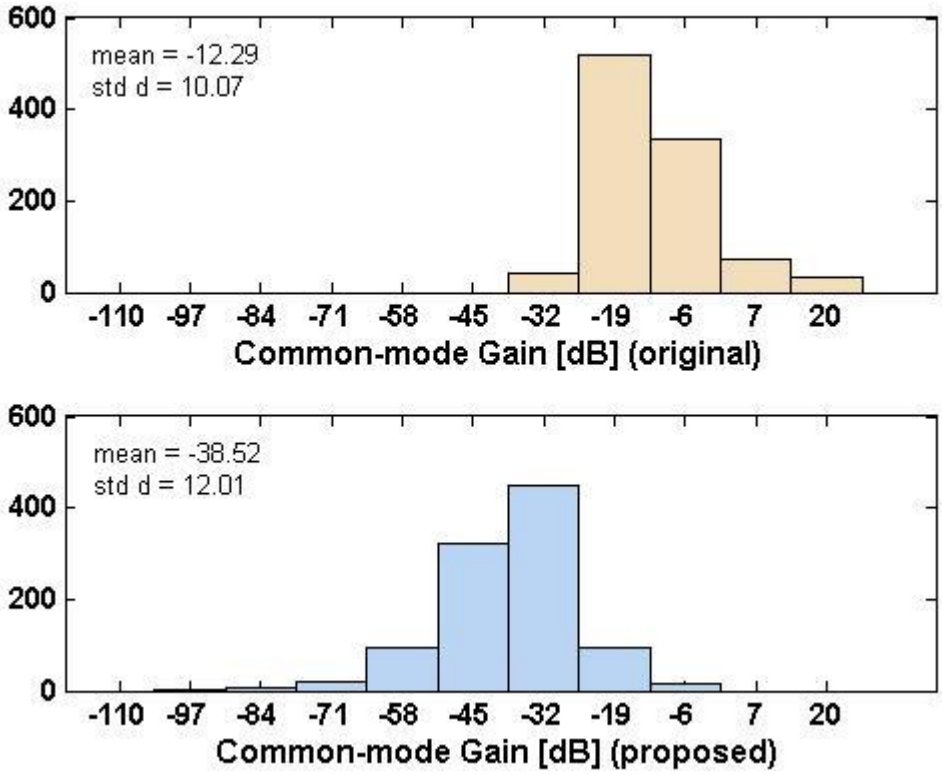


Fig.4. 5: Histogram of dc common-mode gain; a) original topology; b) proposed

4.2 Peluso N-P

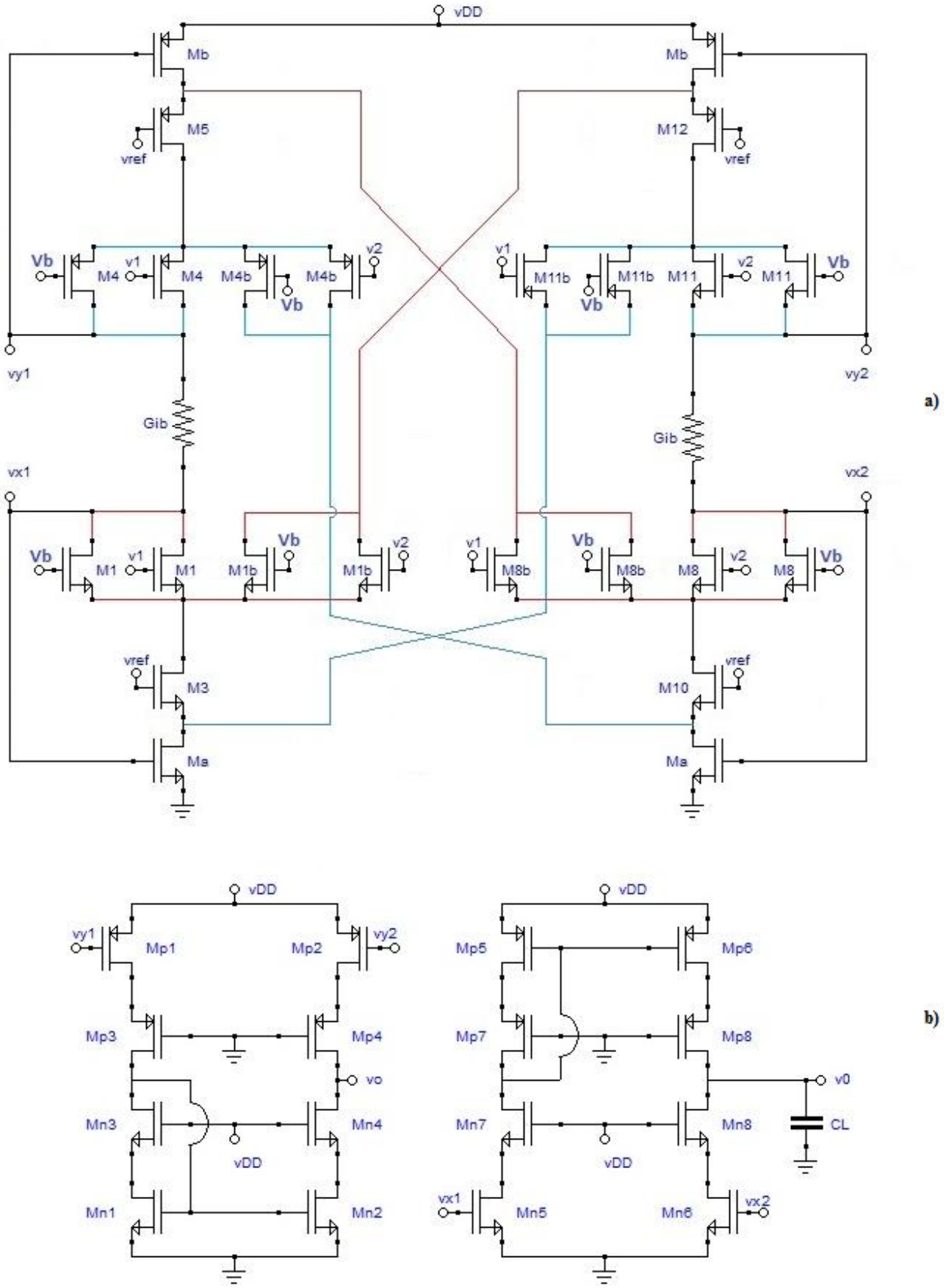


Fig.4. 6: Single ended class AB OTA proposed

In single-ended operational amplifier closed in non-inverting configuration, when voltages below the volt are used, the resulting reduction in input dynamics becomes a limit to compare with.
In single-ended operational amplifier closed in non-inverting configuration in fact the input signal I see it all as a common mode. So somehow, the input common mode dynamics tells me what the signal dynamics I can apply. In the original structure, the common mode dynamics is a crooked half, so then I find myself working on the common mode that is not centered or even less exploiting the dynamics I have. In this section I propose a possible way to increase the input dynamics of a structure based on a Peluso topology, designed to run at 0.6 Volts of power supply. In Table 4.5 are reported the MOSs shape ratio used to realize the proposed circuit. As seen in the previous chapters, Peluso's topology bases its working principle on FVF and Differential FVF (FVFD). The topology discussed in the previous chapters included the use of FVFs, implemented with P-type MOS transistors, which had the task of mirroring currents towards the output branches and FVFD, implemented with N type transistor MOS, which, in addition to mirroring currents to the output branches handled the differential input signal. The basic idea is to replace P-type FVFs with FVFD always of type P as shown in Fig.4.6. In order to obtain a double common mode dynamics compared to the originary Peluso topology is necessary adopt some circuital solutions. To make everything work properly I had to add a level to the conventional FVF, as shown in Fig.4.6. The MOS M1, M1b, M8, M8b, M4, M4b, M11, M11b transistors have all been splitted. In this way I can fix a bias on one of the two gate and the signal on the other, ensuring the correct operation of all devices. In Fig.4.7 there are three curves, the one with the dotted line is obtained from the circuit of Fig.4.6 by fixing a bias on all the MOSs of the two FVFDs of type P and leaving the N type FVFDs as in Fig.4.6. The dash dotted line represents the dual case of the one described above. The continuous line represents the case where signals and bias are set as shown in Fig.4.6. Depending on how I departs the split MOS area I can get more or less gain voltage or more or less dynamic. If I decide to make the MOS on which I apply the signal respect to that on which I apply the bias I get a gain increase and a decrease in dynamic.

Table 4.5

Aspect ratio of OTA

M	W[µm]	L[µm]
1,8	11.92	0.04
1b,8b	10.34	0.04
3,10	32	0.04
a	0.382	0.12
4,11	20.78	0.04
4b,11b	17.52	0.04
5,12	66.4	0.04
b	2.041	0.12
n1,n2	15.89	0.12
n3,n4	0.196	0.24
p1,p2	1.073	0.12
p3,p4	1.236	0.24
n5,n6	0.159	0.12
n7,n8	0.196	0.24
p5,p6	102.65	0.12
p7,p8	1.236	0.24

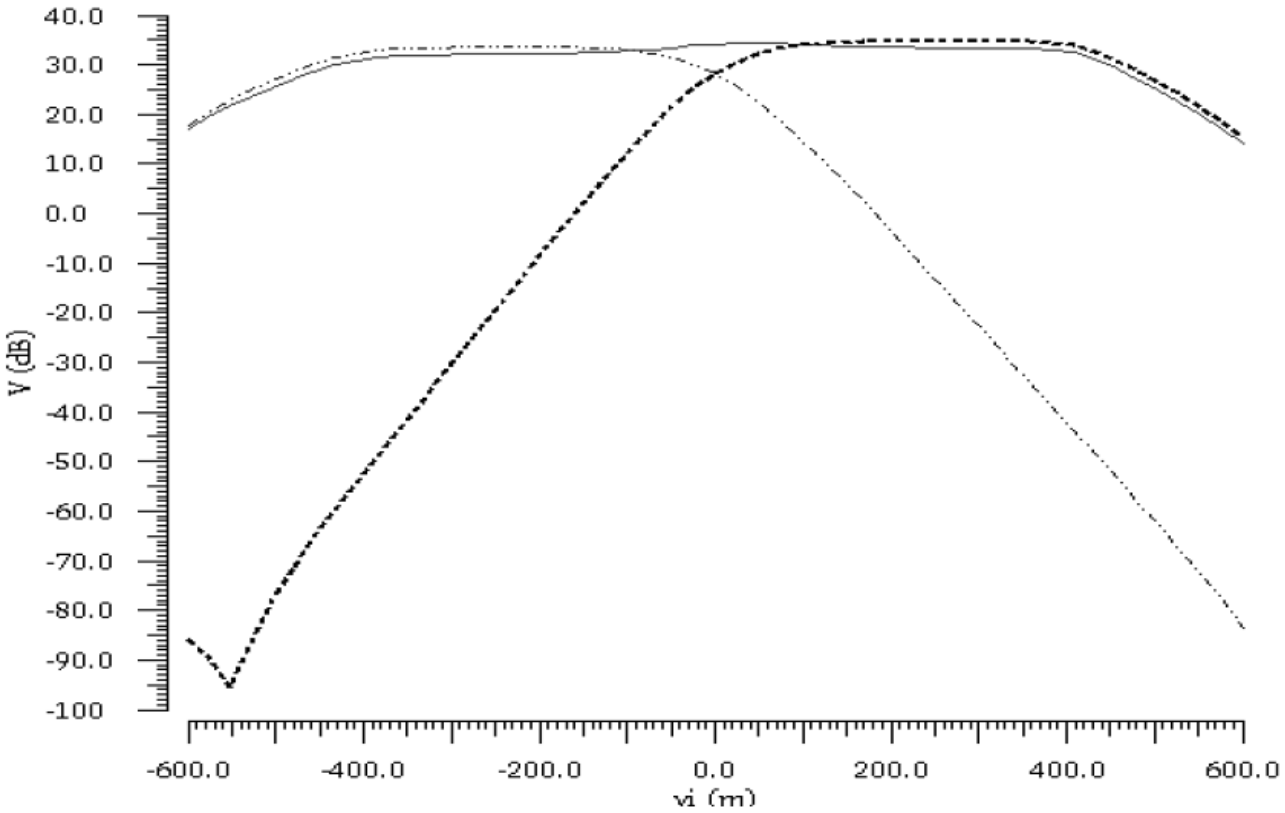


Fig.4. 7: Input common mode of proposed class-AB OTA in case described by Table 4.6

Table 4.6 shows the results of simulations in the Virtuoso CADENCE environment in case the original MOS width (W) is divided into half. In Table 4.7 shows the results obtained from the simulations in the case in which the width of the MOS in which it is applied the signal is nine times greater than that of the MOS on which to apply the bias.

From the data in Tables 4.6 and 4.7 I note that the proposed topology compared to Peluso's single-ended version leads to an increase in the voltage gain of about 6 dB, an increase of unity-gain frequency and an increase in dynamic.

Table 4.6						
MOS width divided by a ratio of 50%						
	AV_{dif}	mϕ	fu	AV_{cm_dc}	AV_{cm_pk}	VDD
N	28.29	83.9	11.2	-37	-	0.6
P	28.07	85.75	10.96	-35.7	-	0.6
N+P	34.2	76.8	21.74	-30	-	0.6

Table 4.7						
MOS width divided by a ratio of 90% signal and 10% bias						
	AV_{dif}	mϕ	fu	AV_{cm_dc}	AV_{cm_pk}	VDD
N	33.39	76.76	19.79	-32.4	-	0.6
P	33.17	79.83	19.53	-30.6	-	0.6
N+P	39.3	67.19	37.39	-25.48	-	0.6

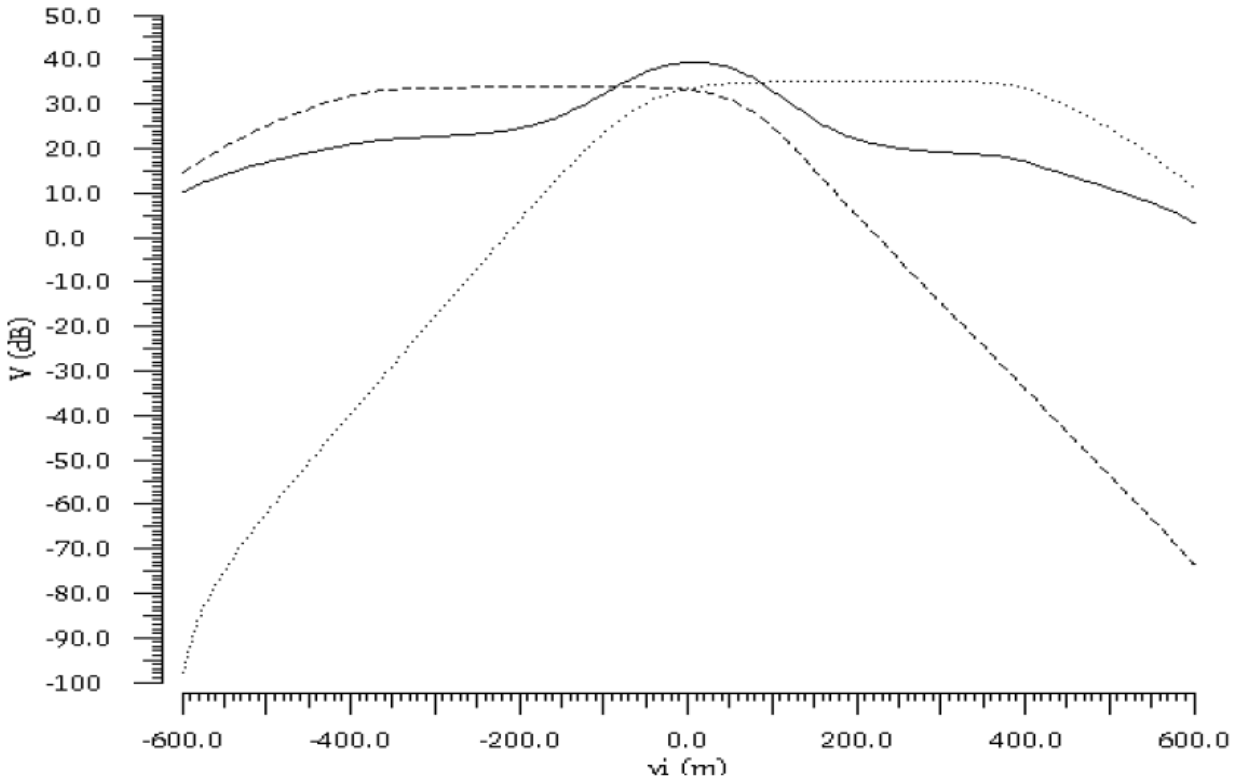


Fig.4. 8: Input common mode of proposed class-AB OTA in case described by Table 4.6

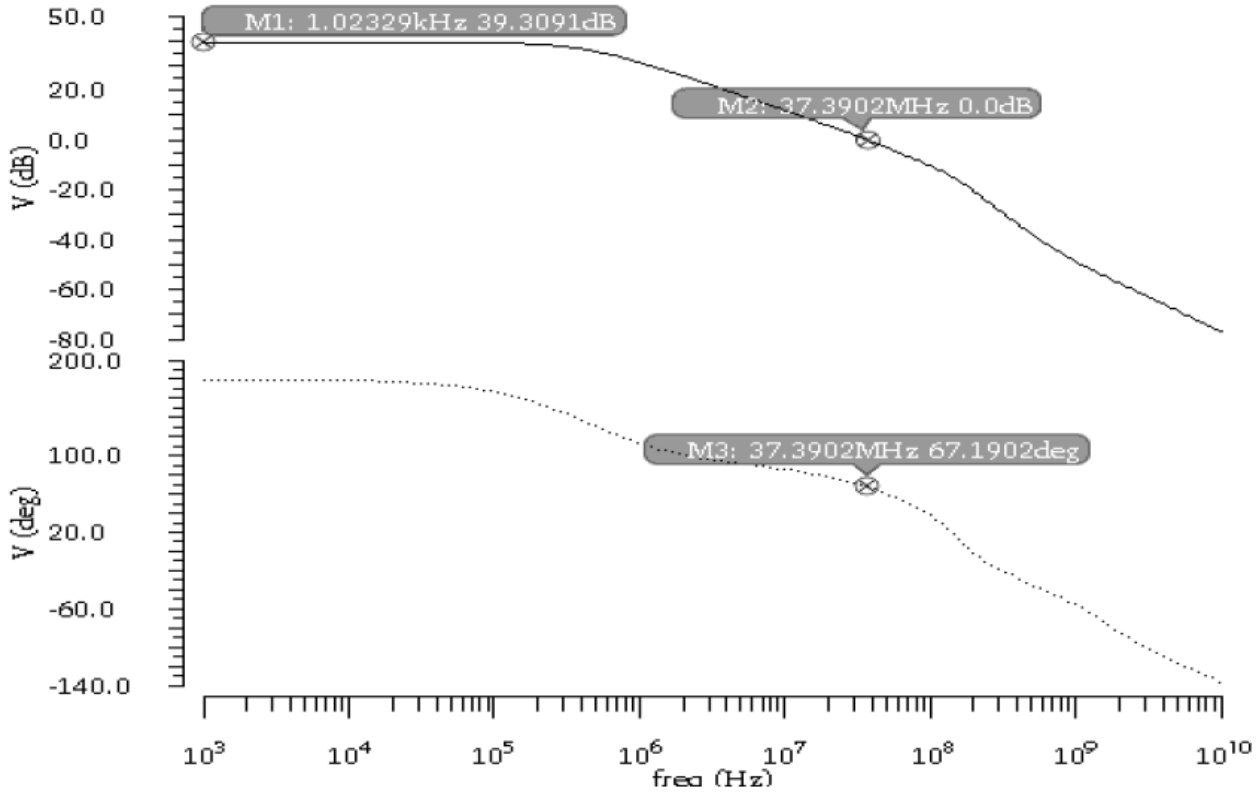


Fig.4. 9: Voltage gain and phase of proposed class-AB OTA in case described by Table 4.7

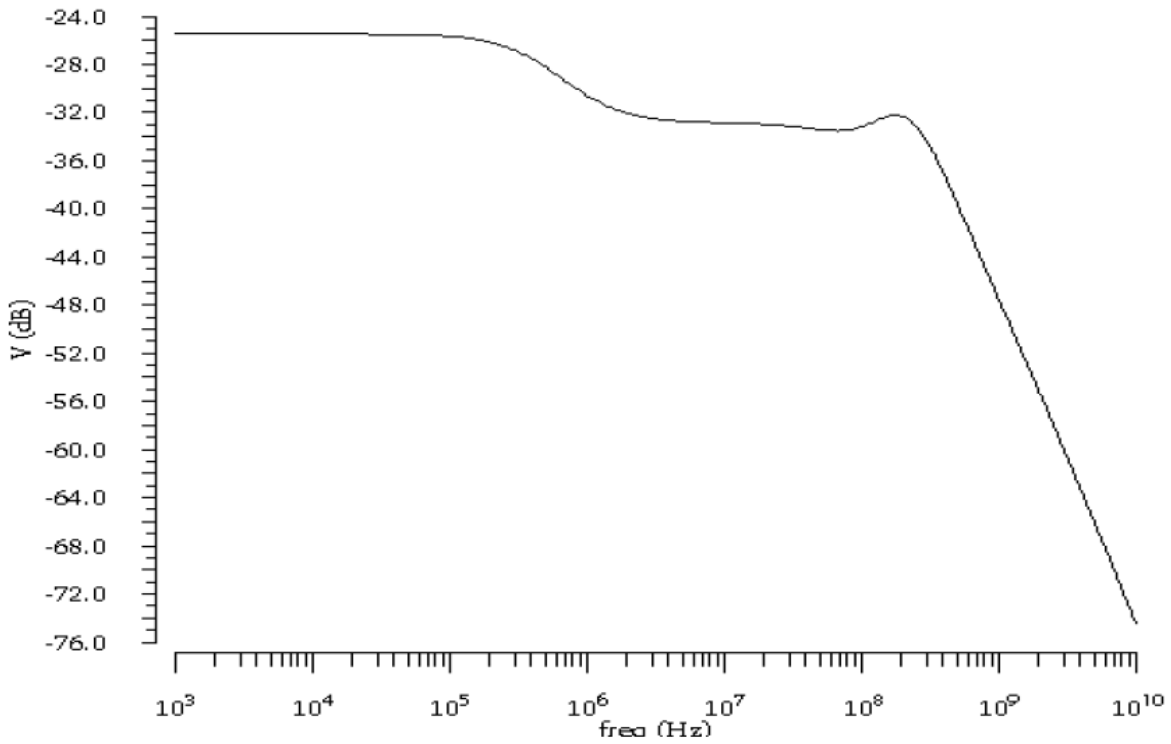


Fig.4. 10: Common mode gain of proposed class-AB OTA in case described by Table 4.7

4.3 Ramirez-Angulo improvement

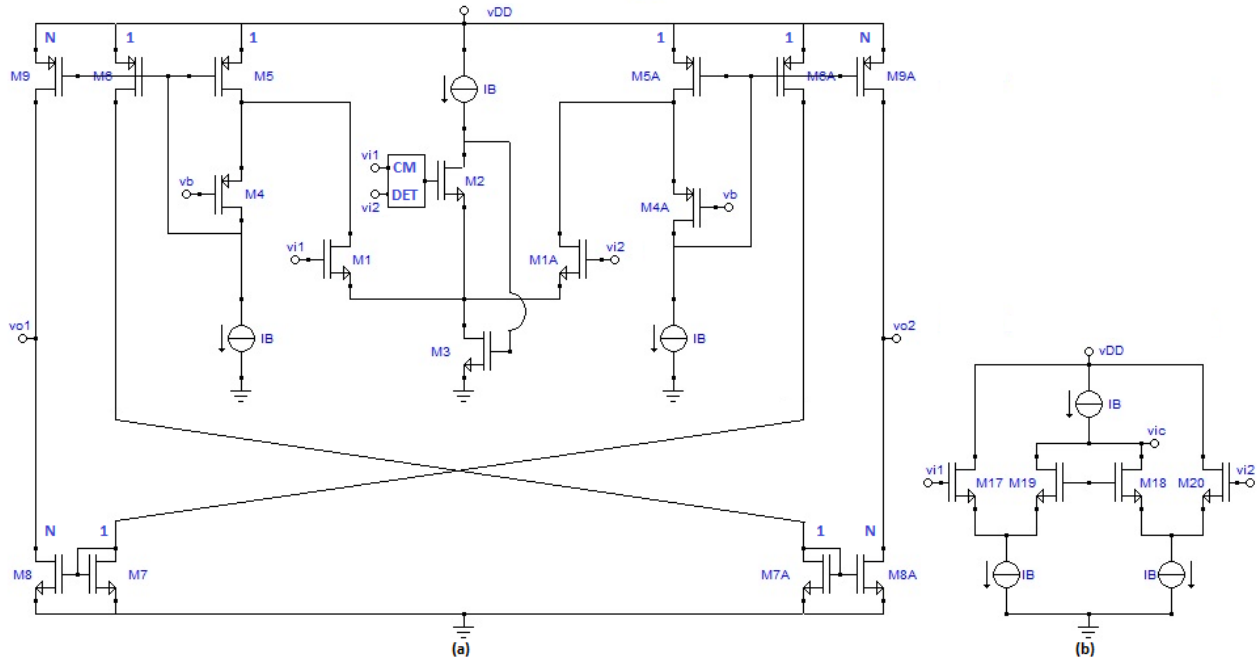


Fig.4. 11: a)Originary topology b) Common mode generation block

The Ramirez-Angulo topology was presented in Chapter 2 and is shown in Fig.4.12, from the point of view of consumption it is not preferable to the other three analyzed in Chapter 2. In order to function as class AB, it needs an auxiliary circuit, shown in Fig.4.12(b), to calculate the input common mode signal. To further reduce power consumption without affecting performance, include the common mode generation block within the cell as shown in Fig.4.12. In Table 4.8 are reported the MOSs shape ratio used to realize the originary circuit while in Table 4.10 are those of the proposed circuit. Table 4.9 summarizes the performance of Ramirez-Angulo's originary topology.

Table 4.8		
Aspect ratio of originary class AB OTA		
M	**W[µm]**	**L[µm]**
1,1A	0.175	0.04
2	0.6	0.04
3	0.32	0.12
4,4A	6.55	0.24
5,5A	0.33	0.12
6,6A	0.44	0.12
7,7A	0.155	0.2
8,8A	0.155	0.2
9,9A	0.44	0.12
17,20	0.12	0.04
18,19	0.42	0.04

Table 4.9							
Performance of the topology shown in Fig.4.11							
case	**AV_{dif} [dB]**	**mϕ [°]**	**Fu [MHz]**	**AV_{cm_dc} [dB]**	**AV_{cm_pk} [dB]**	**VDD [V]**	**I_{TOT} [µA]**
originary	26.77	90.19	39.98	-18.21	-	1.2	50

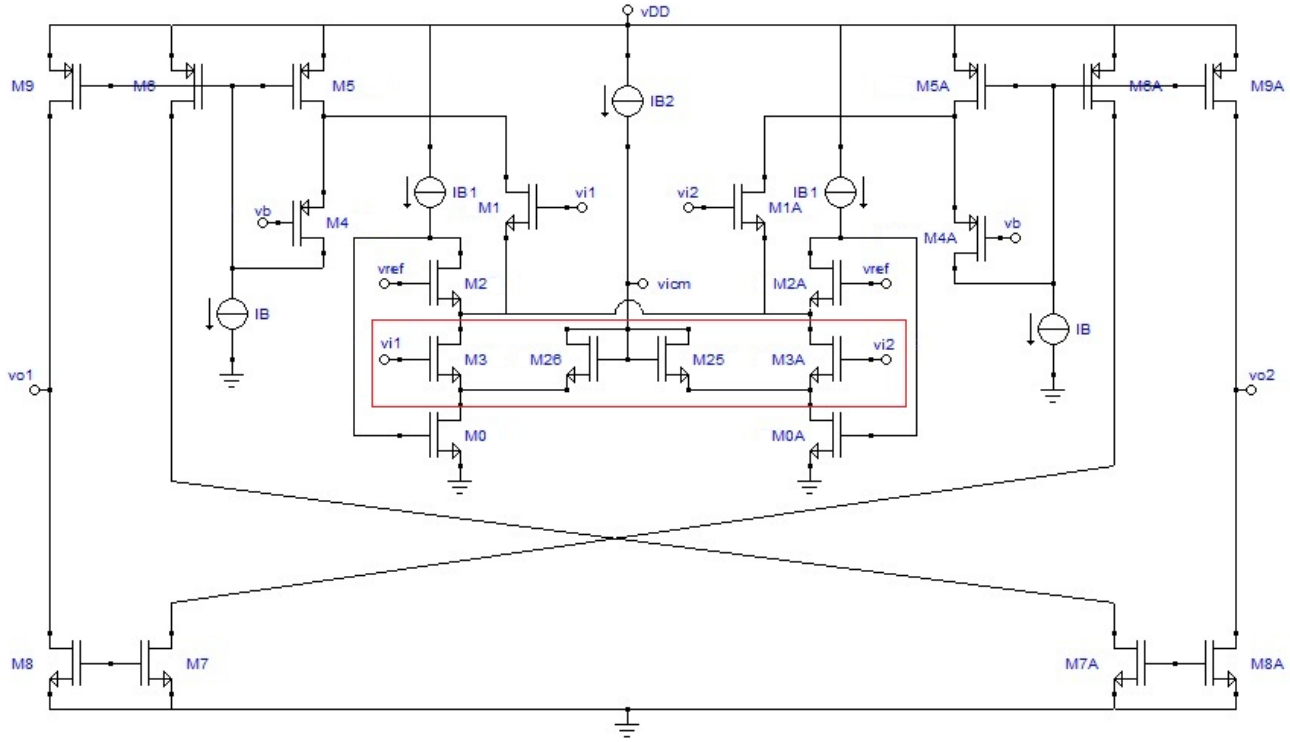


Fig.4. 12: Proposed topology

In order to insert the common mode generation block into the structure of Fig.4.11(a) I splits the FVF used in the originary structure and I adding a MOS in triode in the FVF as shown in Fig.4.12. This solution allows me to get the results summarized in Table 4.11. In Table 4.10 are reported the MOSs aspect ratio of the proposed topology. From the comparison of the results reported in Tables 4.9 and 4.11 it is noted that a noticeable improvement of the common mode gain and therefore CMRR is obtained.

Table 4.10		
Aspect ratio of OTA		
M	**W[µm]**	**L[µm]**
0,0A	0.15	0.12
1,1A	0.175	0.04
2,2A	0.315	0.12
3,3A	0.22	0.12
4,4A	6.55	0.24
5,5A	0.33	0.12
6,6A	0.68	0.12
7,7A	0.155	0.2
8,8A	0.68	0.12
9,9A	0.31	0.2
25,26	0.16	0.2

Table 4.11							
Performance of the proposed topology shown in Fig.4.12							
case	**AV_{dif}**	**mϕ**	**fu**	**AV_{cm_dc}**	**AV_{cm_pk}**	**VDD**	**I_{TOT} [µA]**
1	24.78	91.69	36.036	-1.35	-	1.2	46
2	24.78	91.69	36.025	-41.29	-	1.2	46
1-proposed without correction 2-proposed with correction							

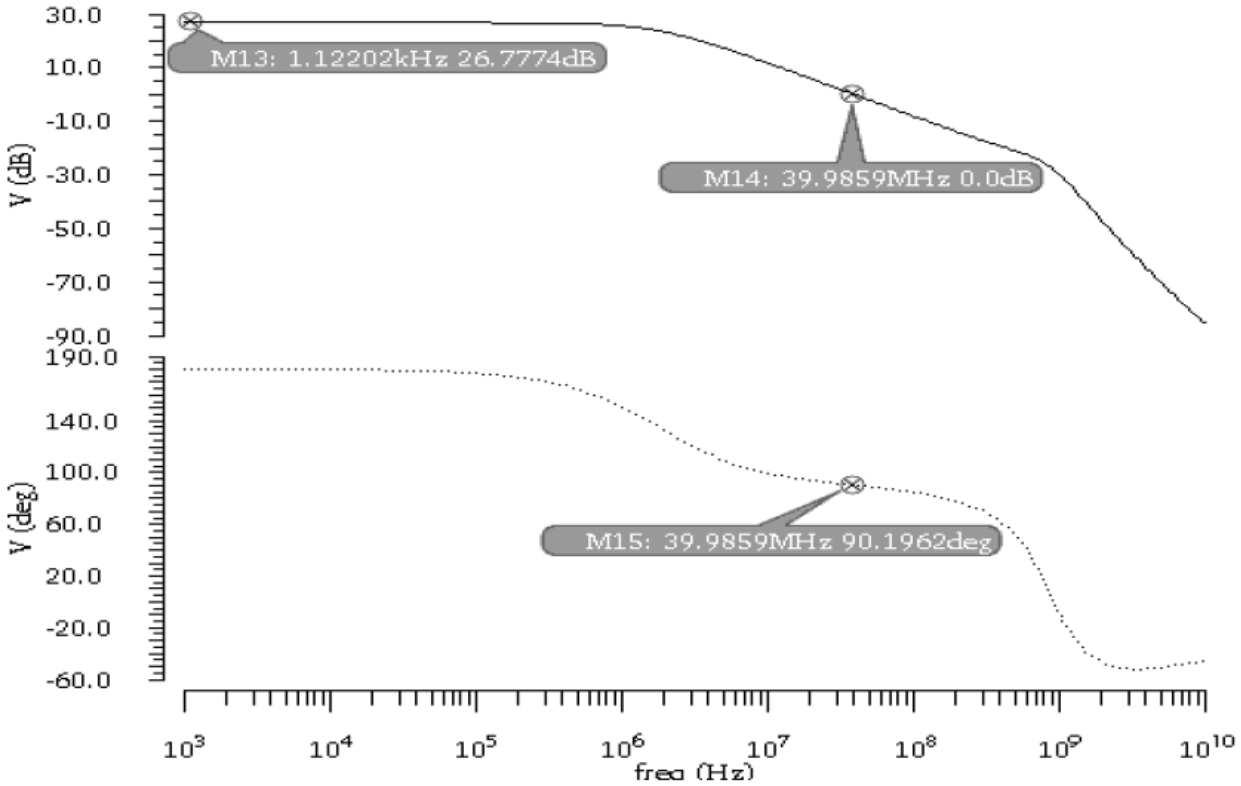


Fig.4. 13: Voltage gain and phase of the originary topology

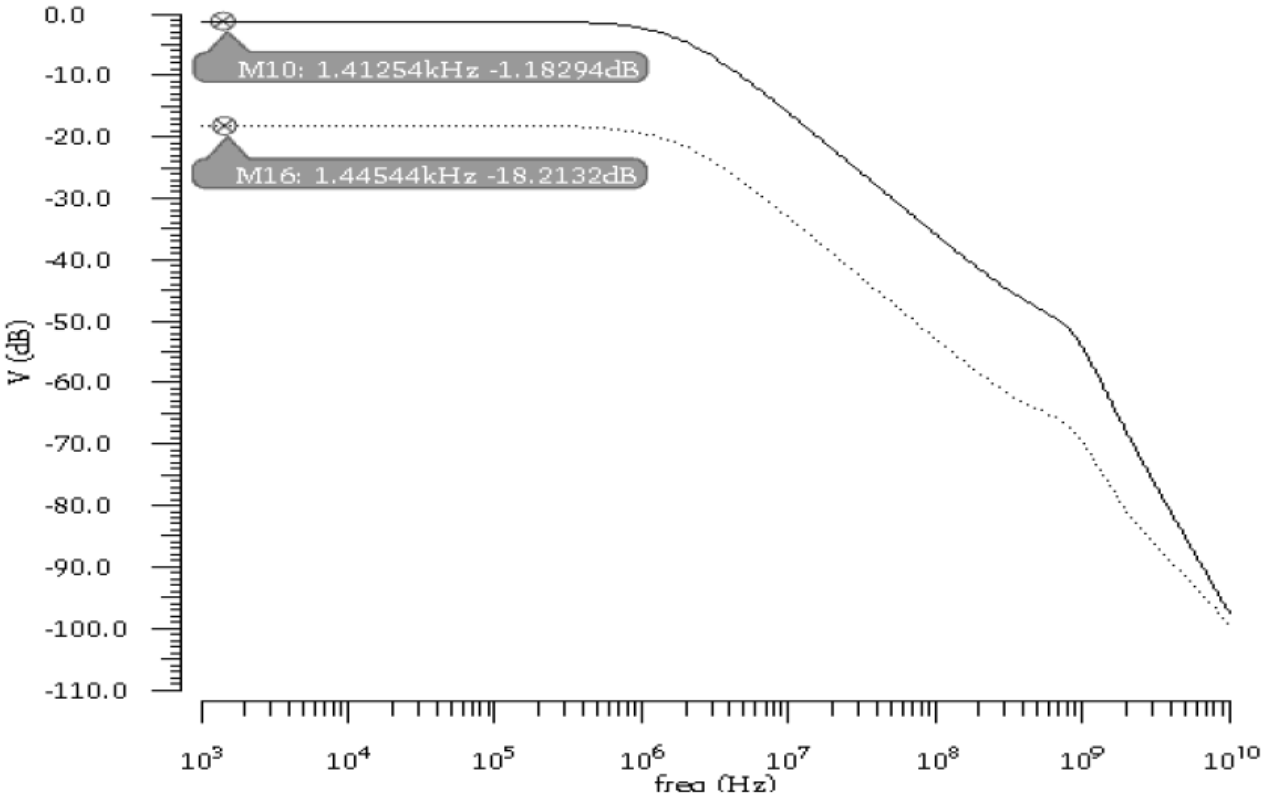


Fig.4. 14: Common-mode voltage gain for the two cases (1-2) of the originary topology

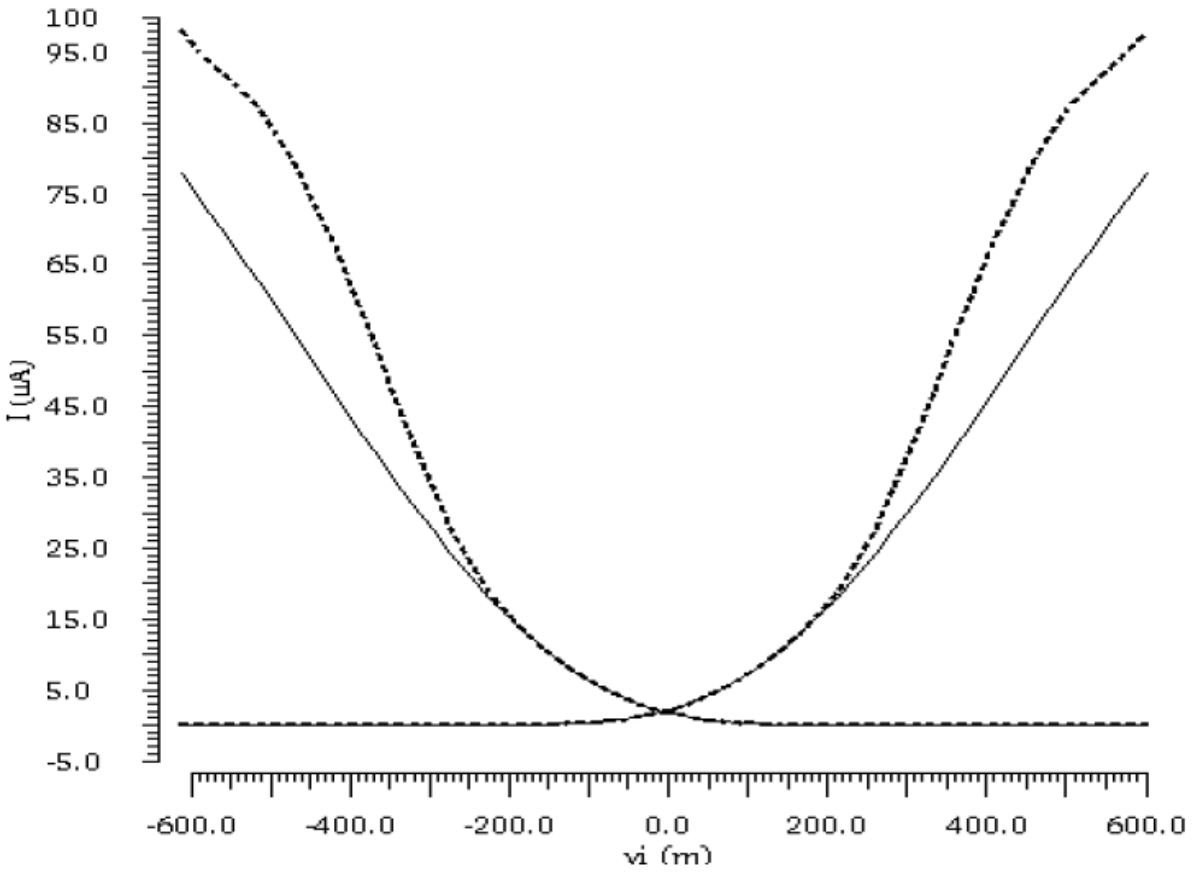


Fig.4. 15: Currents of the input differential transconductor of the originary topology

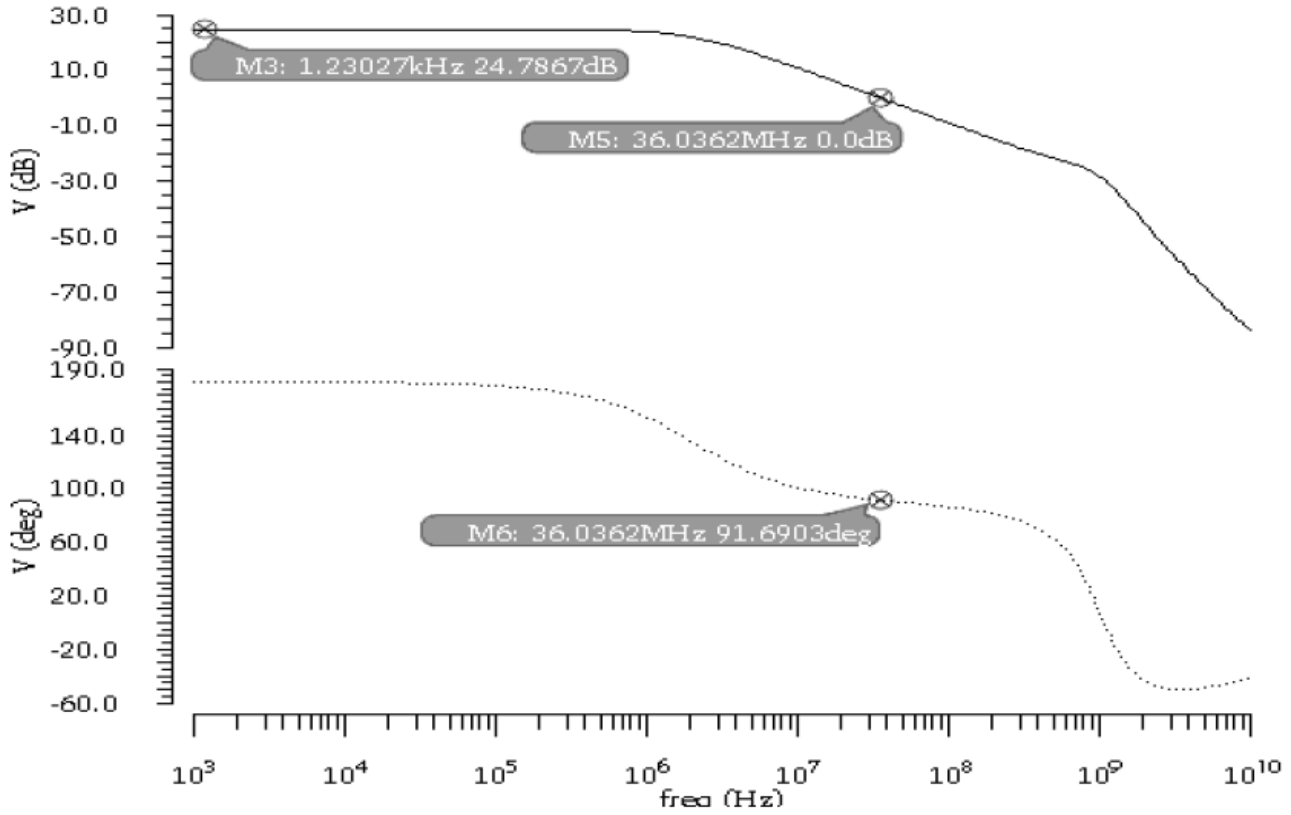


Fig.4. 16: Voltage gain and phase of the proposed topology

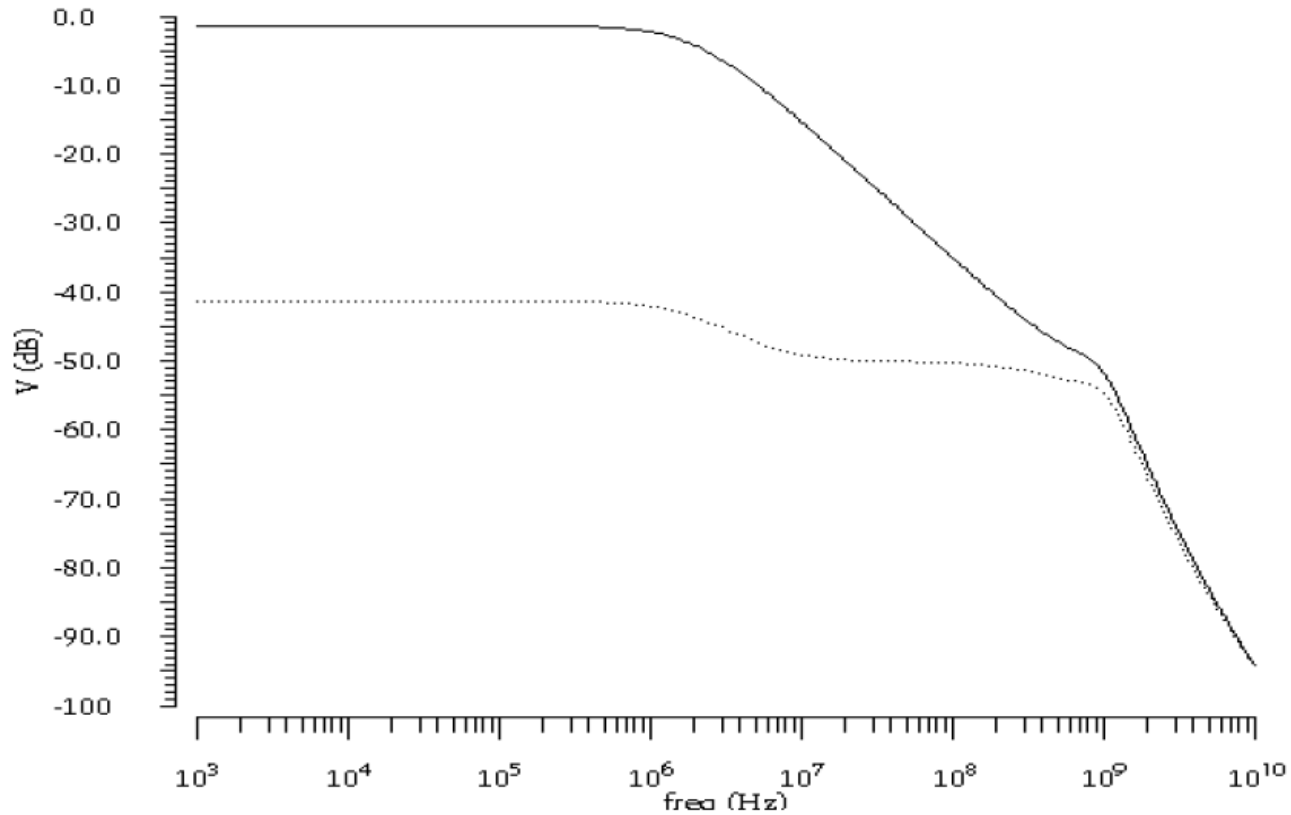


Fig.4. 17: Common-mode voltage gain for the two cases (1-2) of the proposed topology

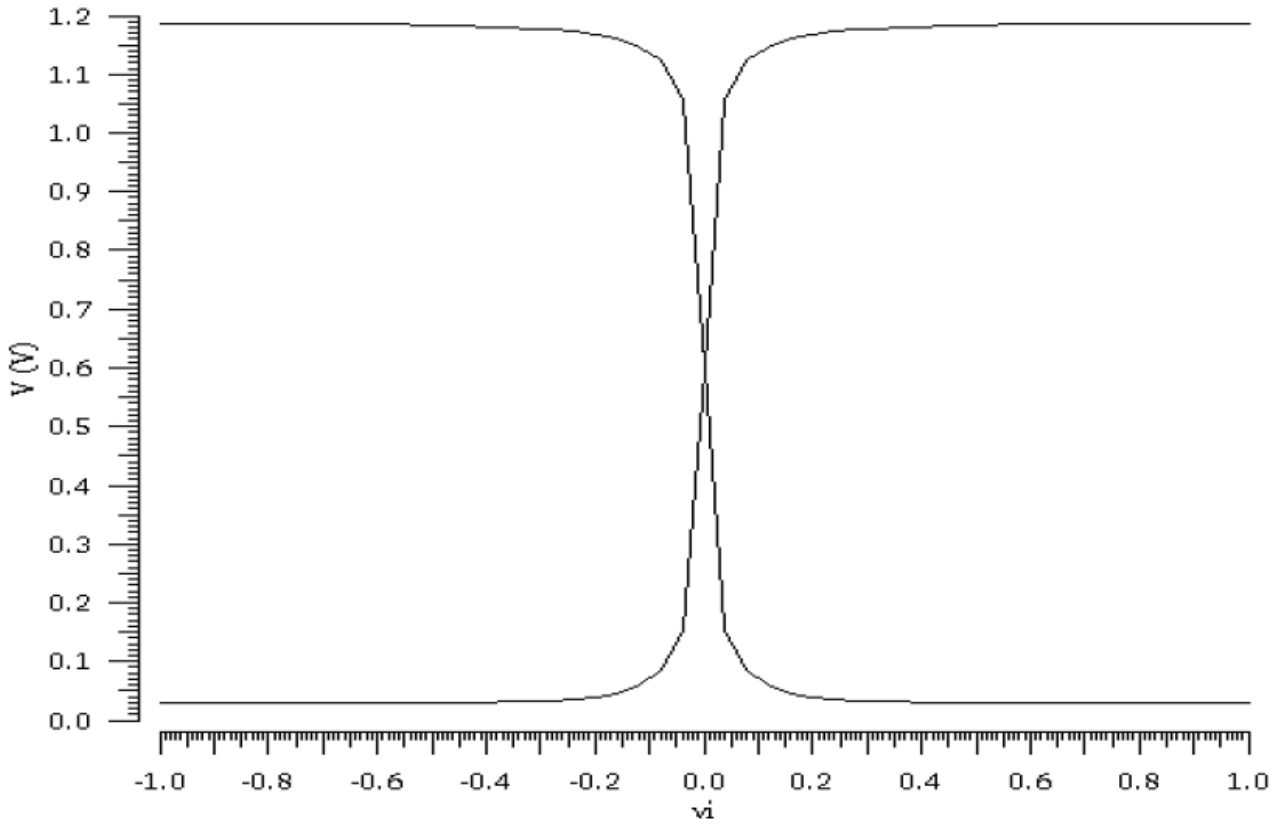


Fig.4. 18: DC transfer characteristic of the proposed topology

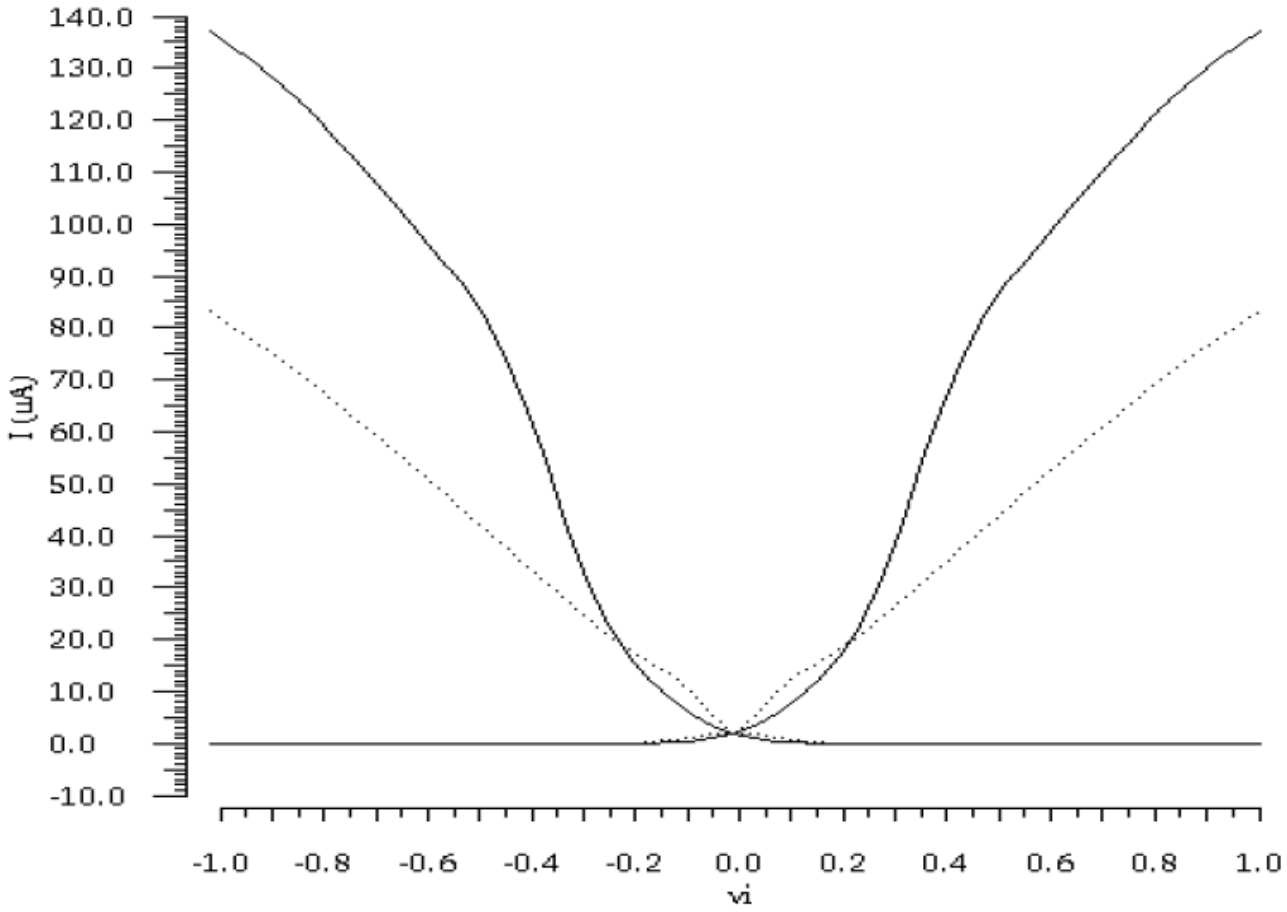


Fig.4. 19: Currents of the input differential transconductor of the proposed topology

4.4 Double Folded

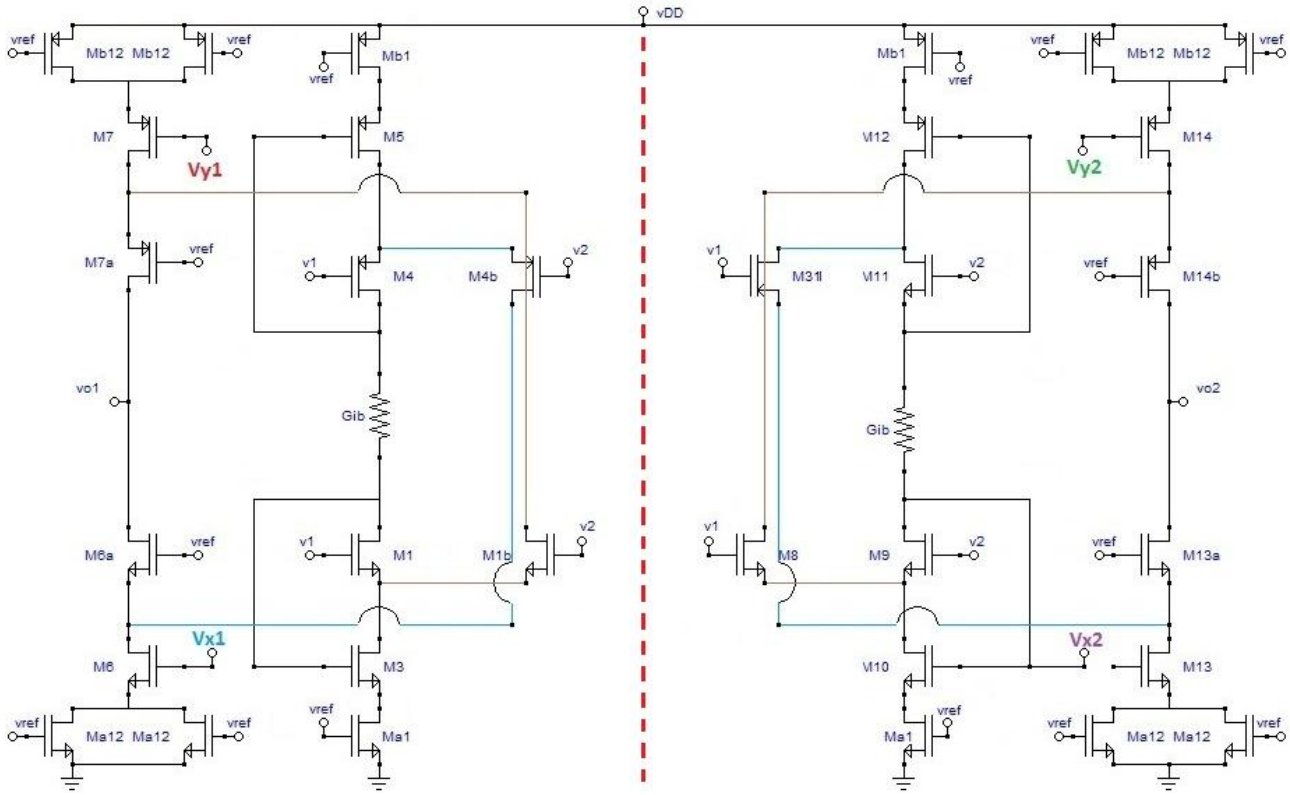


Fig.4. 20: Step 1 to obtain a class AB topology

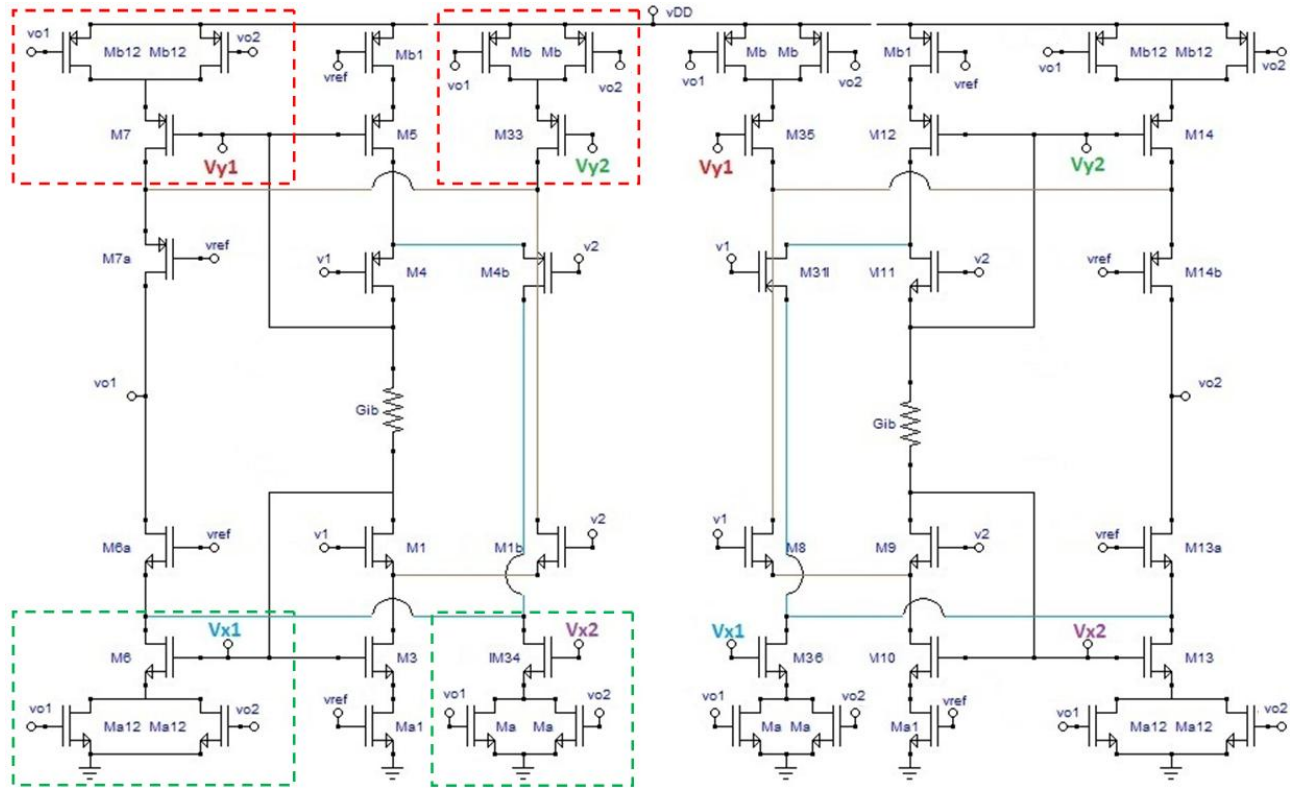


Fig.4. 21: Class AB proposed topology

Mainly I focused on symmetrical structures and tried to see if from the Peluso topology I could get a folded structure with good performance.
Considering the left-part from the dashed red line of the circuit shown in Fig.4.20, the MOS M1, M1b, M3 and M4, M4b, M5 form the FVFDs realized respectively with N type and P type MOSs. The first MOS triad will be indicated with N-FVFD and the second with P-FVFD. In the original Peluso topology, N-FVFD was used to mirror current from below and to supply current to P type FVF (P-FVF) which in turn mirrored it downwards. In the topology shown in Fig.4.20, FVFDs are not used as current mirrors but are used to exploit their ability to provide so much current that varies with the input differential signal. In this way I get two single-ended structures with performance summarized in Table 4.13. The input differential transducer delivers currents that have a typical class AB trend but then saturate. To obtain a fully differential class AB structure I changed the circuit of Fig.4.20 to that of Fig.4.21. The MOS M7,14, Mb12 are splitted respectively in the MOS M33,35, Mb while the MOS M6,13, Ma12 are splitted respectively in the MOS M34,36, Mb, with shape ratio shown in Table 4.12. MOS 33,34,35,36 have been chosen with a width (W) of approximately one third (W/3) of the starting point.

Table 4.12

Aspect ratio of OTA

M	W[µm]	L[µm]
1,9	0.525	0.04
1b,8	0.175	0.04
3,10	0.525	0.12
34,36	$W_{6,13}/3=0.175$	0.12
a	0.12	0.28
a1	0.325	0.12
4,11	6.55	0.24
4b,31	4.94	0.24
5,12	0.37	0.12
33,35	$W_{7,14}/2.7=0.185$	0.12
b	0.27	0.12
b1	1.07	0.12
b12	0.65	0.12
7,14	0.5	0.12
7a,14b	9.91	0.12
a12	0.13	0.12
6,13	0.525	0.12
6a,13a	1.82	0.12

Table 4.13

Performance of the topology shown in Fig.4.21

case	AV_{dif}	mϕ	fu	AV_{cm_dc}	AV_{cm_pk}	VDD
SE	46.5	87.5	17.7	4.4	-	1.2
SE= Single-Ended						

On the gate terminals of M7,14 where there was only one bias before, there is now a bias plus a signal that is supplied by the P-FVFD. Similarly on the gate terminals of M6,13 there is now a bias plus a signal that is supplied by the N-FVFD. The gate terminals of the MOS M33,34,35,36 are applied to the signals as shown in Fig.4.21.

Depending on how the ratio between the "W" of split MOS is unbalanced, I can get more or less gain voltage. By unbalancing the "W" ratio in favor of M33,34,35,36 I get less gain and a deterioration in the DC transfer characteristic. The shape ratio I chose was the one that gave me a good compromise between the gain and the linearity of the DC transfer characteristic. The results obtained are shown in Table 4.14.

Table 4.14

Performance of the topology shown in Fig.4.22

case	AV_{dif}	mϕ	fu	AV_{cm_dc}	AV_{cm_pk}	VDD
1	49.2	85.5	58.2	17.4	-	1.2
2	49.2	85.5	58.2	-11	-	1.2

1- without triode CMFB
2- with triode CMFB

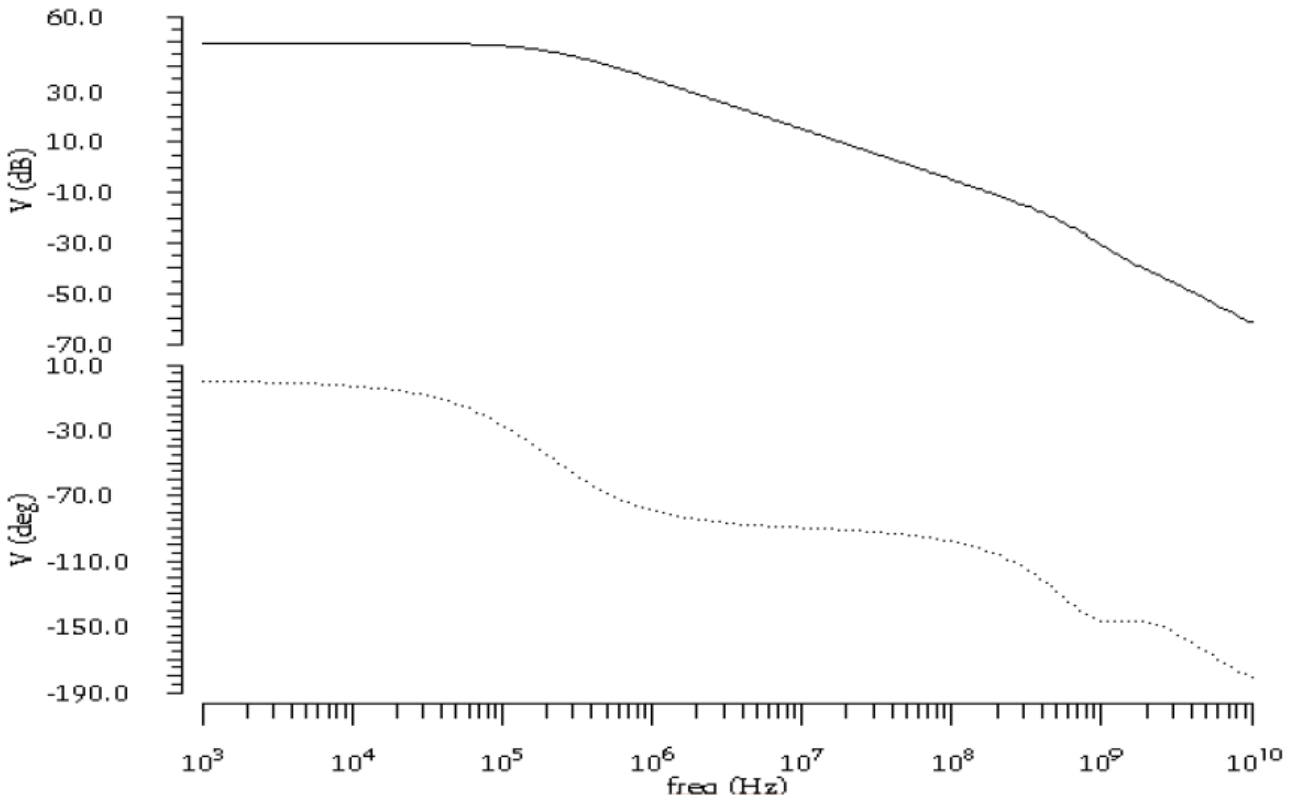


Fig.4. 22: Voltage gain and phase of the topology of Fig.4.21

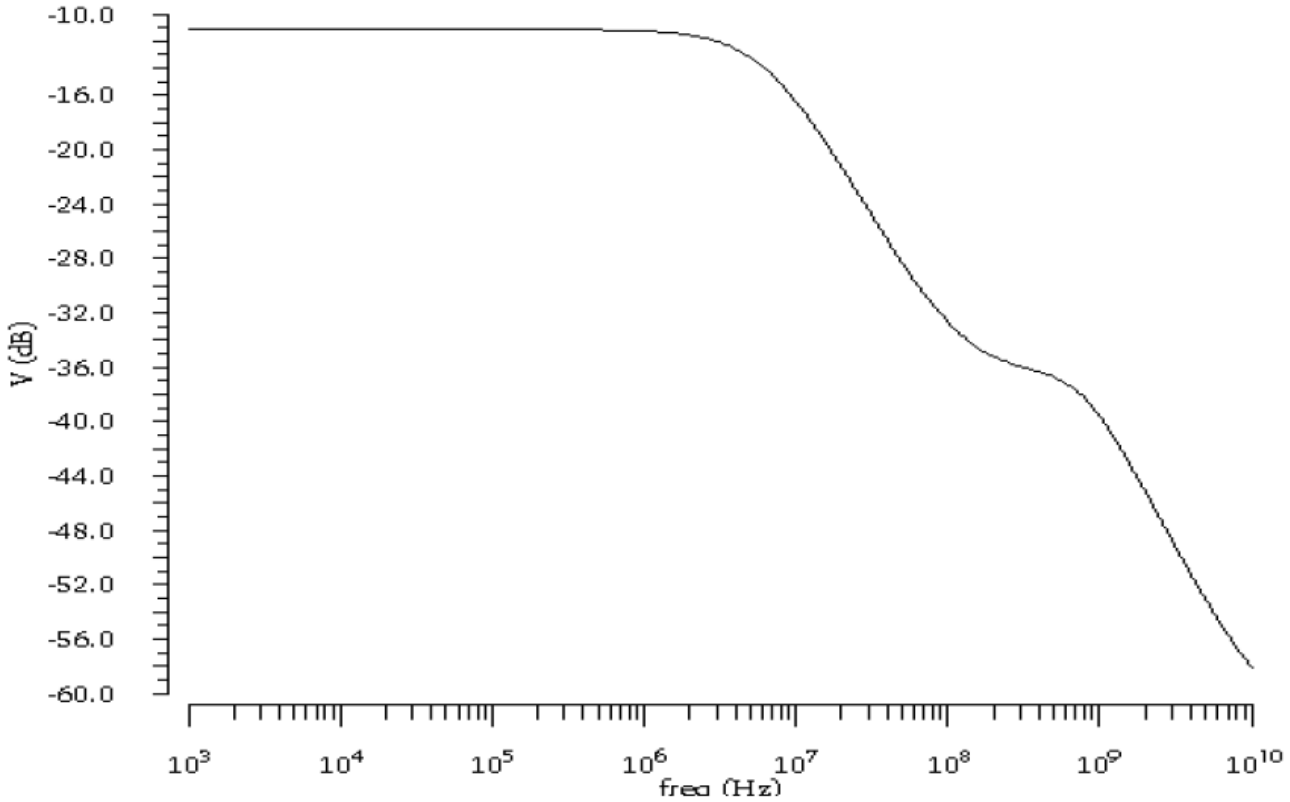


Fig.4. 23: Common-mode voltage gain for the topology of Fig.4.21

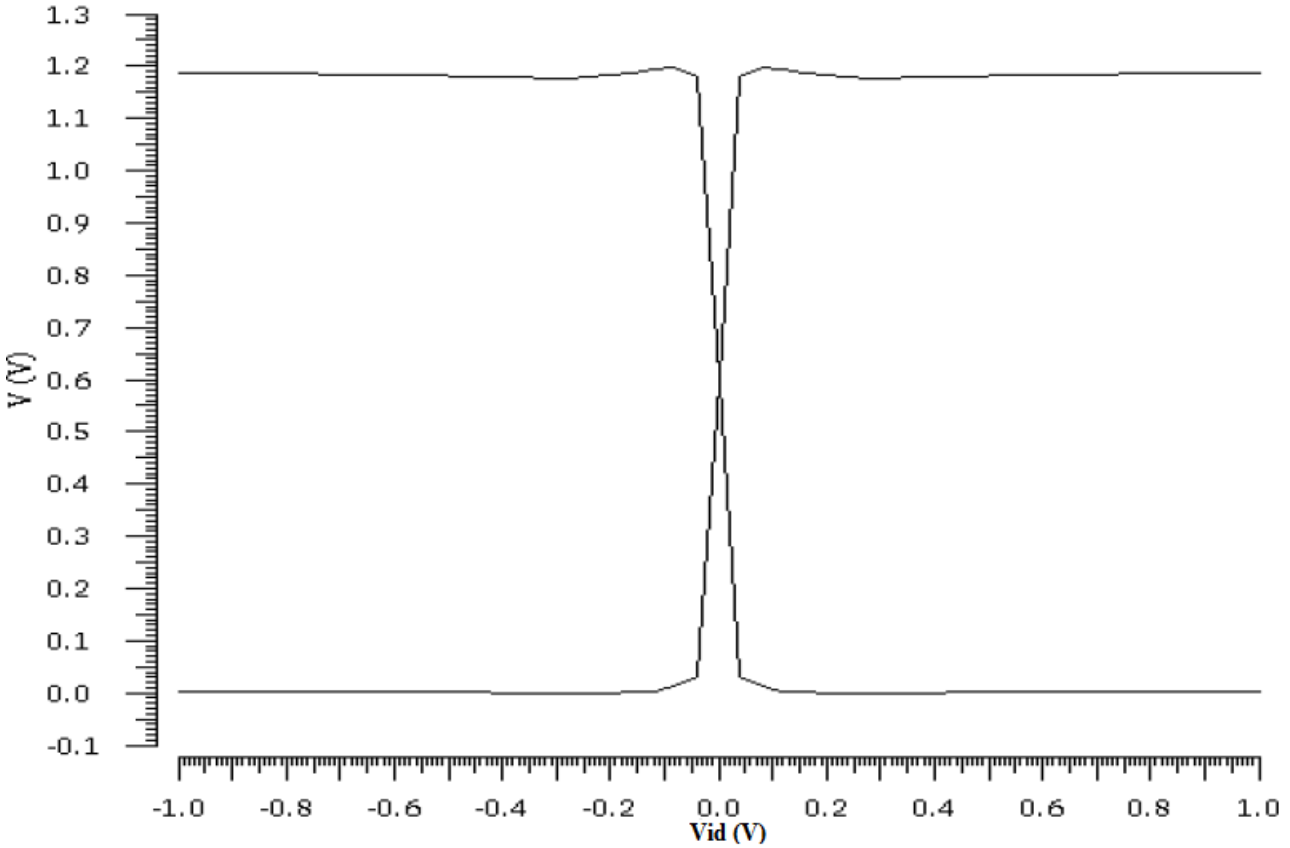


Fig.4. 24: DC transfer characteristic

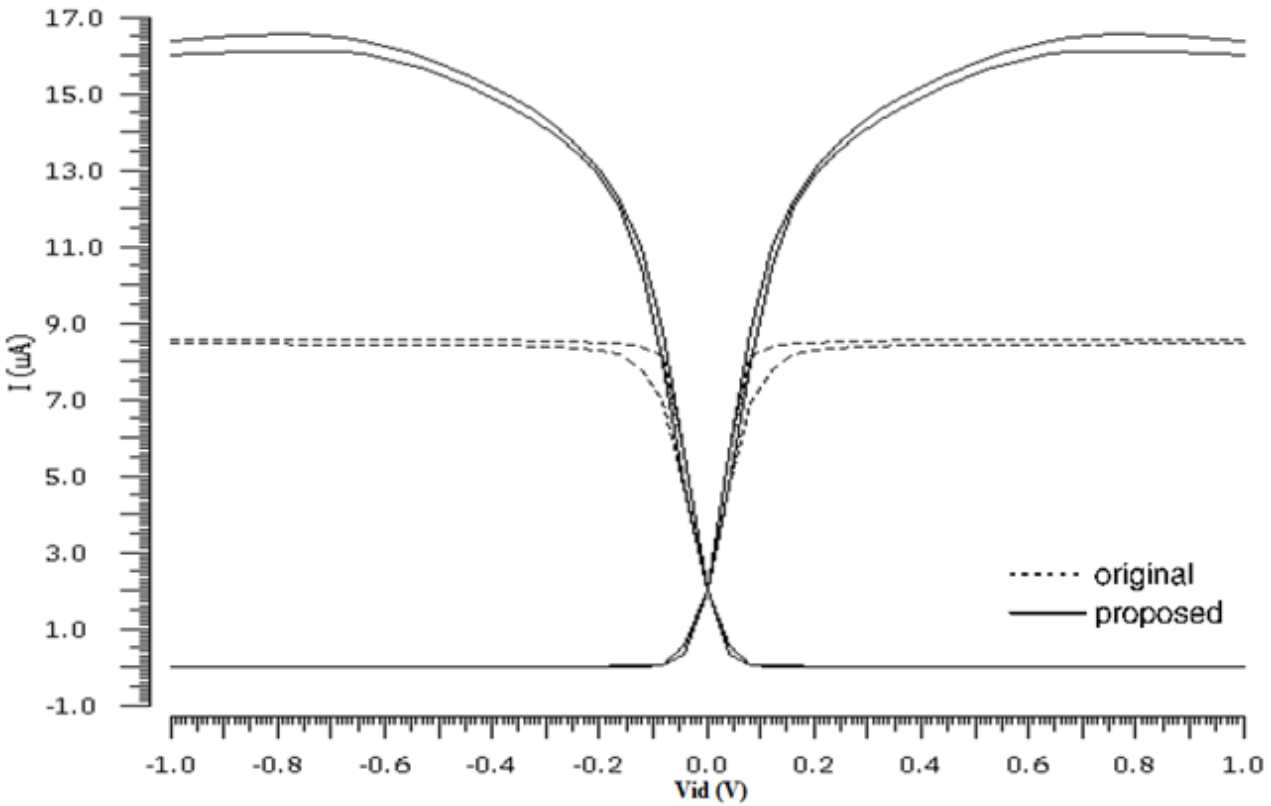


Fig.4. 25: Currents of the input differential transconductor of the original topology compared to proposed

Chapter 5

Behavioral model of a Class AB OTA

If I need to design a class AB amplifier for Switched Capacitor (SC) applications such as Sample and Hold, A/D converters or generally applications where fast transients are required and where a fundamental specification is the one of settling time, how should I proceed?
If I were to design a Class A amplifier intended for the design of a Sample and Hold, I would know how to proceed.

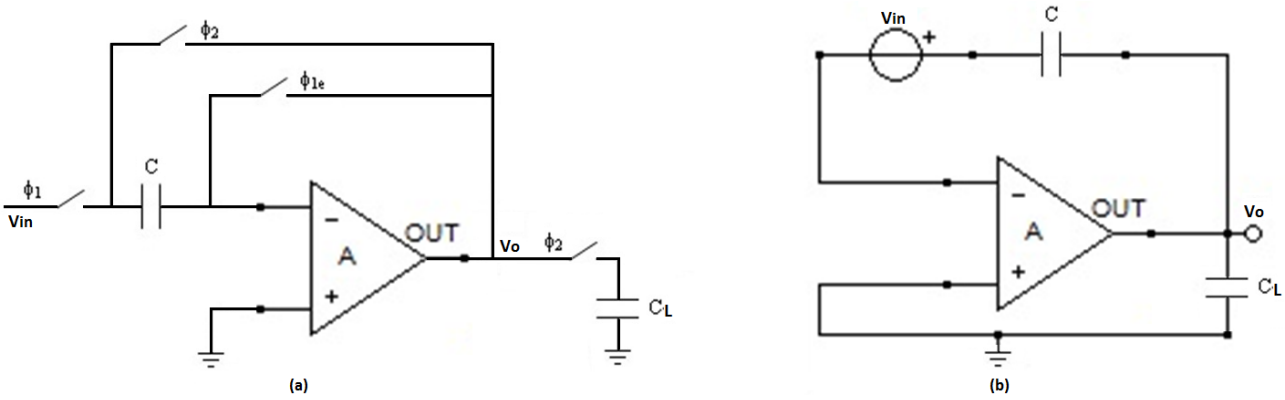


Fig.5. 1: a) Sample and Hold Amplifier; b) Sample and Hold Amplifier in sample phase

Fig. 5.1b represents a Sample and Hold Amplifier (SHA) in the hold phase (ϕ_2) with the capacitance between the input and the output. The generator V_{in} is the equivalent of the voltage value stored during the sample phase (ϕ_1).
In a class A amplifier the settling time (ts) is limited by the unit gain frequency (fu) and the slew rate of the operational amplifier.
I assumed that the amplifier is a single stage one with a dominant pole, so its transfer function will be of the following type:

$$A = -\frac{A_0}{1+s\tau} \qquad (5.1)$$

where A_0 represents dc gain. The transfer function between input and output is equal to:

$$\frac{V_o}{V_{in}} = -\frac{A}{1-A\beta} \cong -\frac{1}{1+s\frac{\tau}{A_o}} = -\frac{1}{1+\frac{s}{2\pi f_u}} \rightarrow \omega_{-3dB} = 2\pi f_u \qquad (5.2)$$

Having chosen a negative sign to express the gain "A" in 5.1, 5.2 shows a negative sign to denominator.
The system has a unitary feedback factor (β) and the bandwidth of the system coincides with the unitary gain frequency of the amplifier.
In the hold phase, the system must produce as an output a step of amplitude equal to V_{in}. In the time domain there are two phases for the output voltage: a linear phase limited by the amplifier's slew rate and a phase with exponential trend limited by the maximum time that can last the settling time.

In case both phases have the same duration, the maximum time that may last the hold phase is half of the sampling period Ts.

$$\begin{cases} V_{out}(t) = SR * t & per \quad t < t_{slew} \\ V_{out}(t) = V_{fin}(t) - [V_{fin}(t) - V(t_{slew})]e^{-(t-t_{slew})/\tau} & per \quad t_{slew} < t < \frac{T_s}{2} \end{cases} \tag{5.3}$$

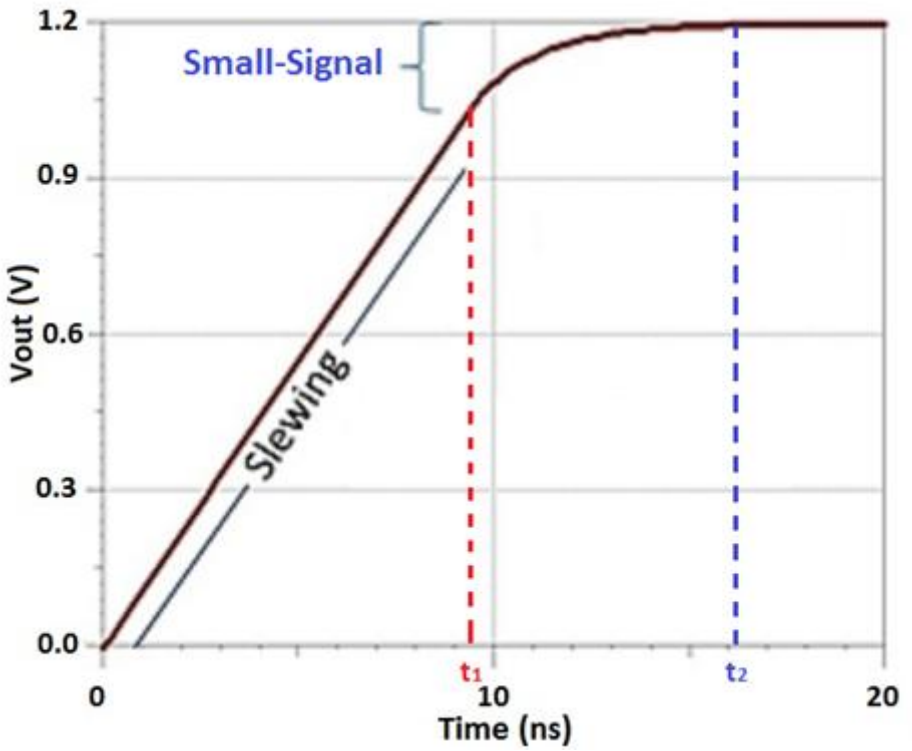


Fig.5. 2: Response to input step

The settling time (ts) is the time that the output (Vout(t)) settles down within a time interval ± ε. If I have a single pole function, the output voltage stabilizes exponentially (ideal case). In a real case the slew rate has to be considered, as shown in Fig.5.2; for a class A operational amplifier the response behaves as a ramp in the first part of the curve and in the second part of the curve as an exponential. The exponential term represents the error between the input voltage and the output voltage. The choice of a high slew rate leads to less restrictive constraints on the minimum polarization current of the amplifier, useful for Low Power applications.

From the definition of slew rate I get a relationship that links the polarization current of the amplifier to the settling time (ts).

$$SR = \frac{I}{C} = \frac{2V_{ref}}{t_{slew}} \rightarrow I \geq C\frac{2V_{ref}}{t_{slew}} \tag{5.4}$$

where 2Vref is the input range, and *I* is the output amplifier current that flows in a capacitive load (C). I can use higher currents value to improve the slew rate performance and so the settling time. So in the design of the amplifier I must reach a compromise between: the unitary frequency that limits the settling time and the current which, in addition to limiting the slew rate, is the direct cause of power consumption increase.

For example, in a Class A design, I can decide to be in Slew Rate (SR) for 20% of the time (ts) and, given the load capacitance and, using the first of the equations (5.3) and equation (5.4), I can derive the bias current. Depending on the residual time (80%), using the second of the equations (5.3), I

obtain the value of unit gain frequency (f_u) needed to carry out the design of the operational amplifier.

Given a specification on settling time, is it possible for class AB amplifier to use the same procedure as its class-A counterpart? The answer is no, because in the part of the curve in which for a class A the response is in slewing region as shown in Fig.5.2, for a class AB the relation between time and current is unknown. I have no idea what the link between the size of the amplifier and the settling time is.

I'm looking for a formula that relates the setting time to the parameters of the circuit, and another one that connects the consumption to the circuit parameters. In the end, I will look for the sizing that produces a settling time less than or equal to a given specified value.

If the operational amplifier is operating in class AB, the part of curve that in the class A is linear (constant current), in a class AB becomes more complicated.

If I have to design a class AB operational amplifier, how do I do it?

1) I choose how to make the basic cell

2) I choose an operational structure in which to use it

The baseline cell modes are:

1-double transconductor (cross-coupled pair)

2-adaptive biasing (differential cell where the current generator is not constant and, however, the two transistors have in common the emitters.

3-the Peluso topology, that does not have the emitters in common (it is not a variable current differential cell): it is a differential structure where, by properly applying the signals, the behavior resemble the one of the differential pair but does not have a limit on current.

The most efficient way to make the basic cell (OTA) for differential mode, is the one proposed by Peluso. The simplest way to build the operational amplifier is the one that makes use of the current mirror. Nobody forbids to choose Peluso topology but with a folded cascode (as long as we manage the complications that come out from this choice).

In this chapter, a study will be presented on the relation between the output current and the input voltage of a class AB OTA. Expressions will be derived for the Peluso single ended topology, but results can be easily extended to fully differential structures and to all symmetrical OPAs that follow a law of the type:

$$I_{1,2} = K(V_B \pm v_i)^2$$

specifically to all the topologies discussed in Chapter 2. A single pole model will be proposed that is a valid approximation for large phase margin in real cases.

5.1 Peluso single ended (SE) topology

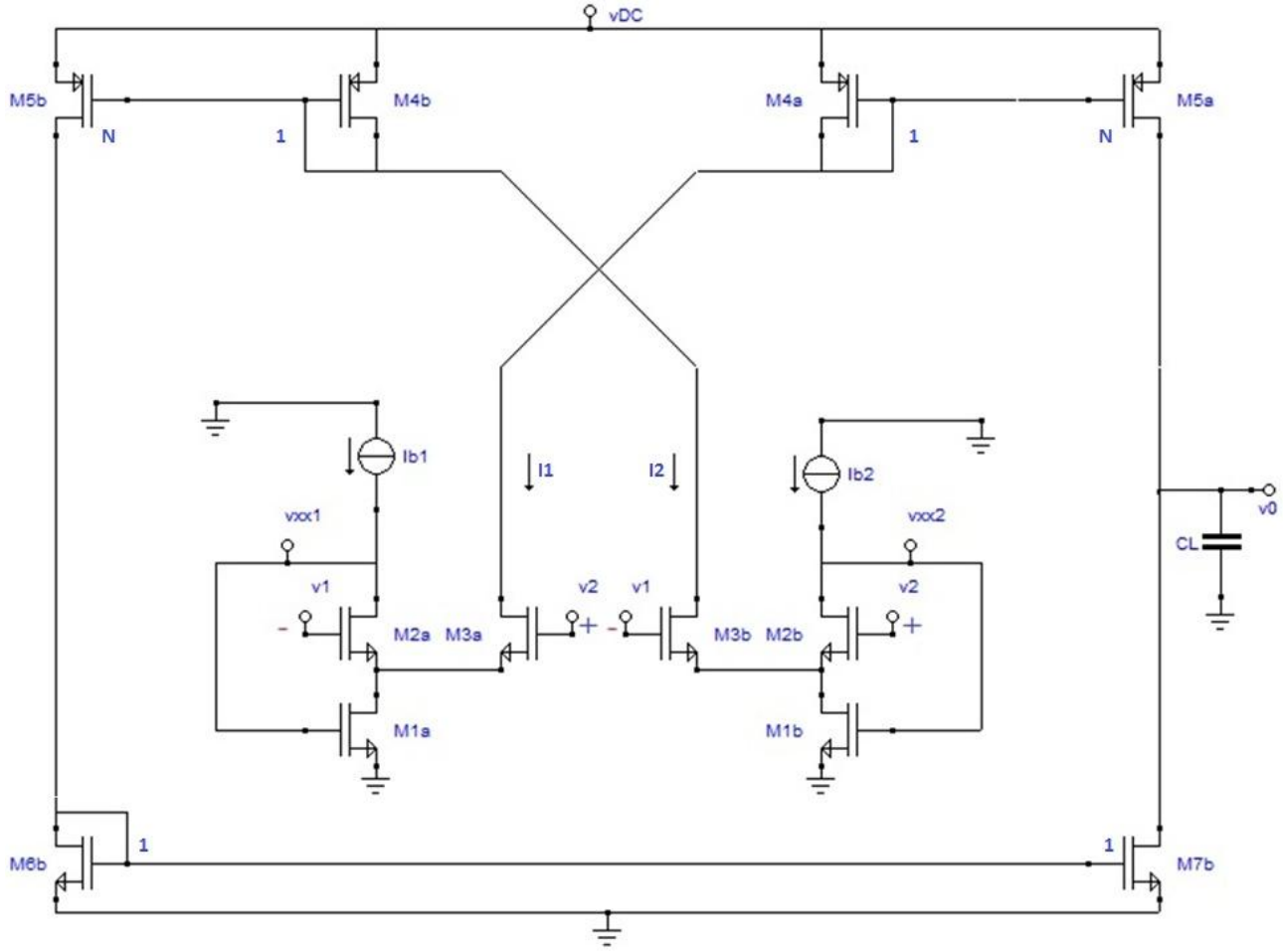


Fig.5. 3: Class AB OTA single ended based on Peluso topology

As a case study, the Peluso topology in the single ended version, shown in Fig.5.3, will be considered. Terminal V_1 is the inverting one while V_2 is the non-inverting one. The circuit of Fig.5.3 was characterized by the point of view of the large signal, taking into account that the MOS behaves as a voltage controlled current source.

The equation that describes its large signal behavior is:

$$I_D^{sat} = k(V_{GS} - V_T)^2 \quad (5.5)$$

The model describing the operation of a n-type MOS in the saturation zone is illustrated in Fig.5.4.

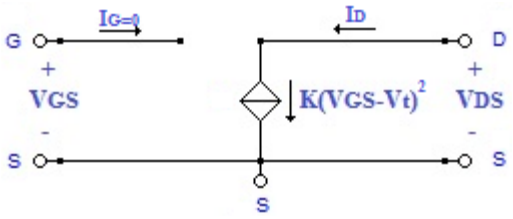


Fig.5. 4: Large-signal model of saturated n-MOS

The characteristic curve of the drain current I_D as a function of the V_{GS} input voltage is shown in Fig.5.5.

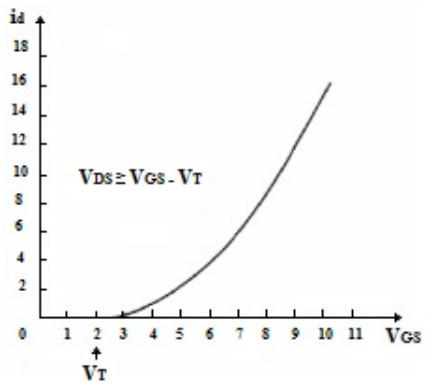


Fig.5. 5: Large-signal I_D-V_{GS} characteristic curve in saturation region

5.2 Large signal modeling

For large signal operation, the circuit in Fig.5.3 can be modeled as shown in Fig.5.6. The conventional current mirrors (no FVF) have been replaced by ideal current-controlled current sources. The Flipped Voltage Follower (FVF) (M3a,b) was modeled with a voltage controlled current source, while device M1a,b and M2a,b as an ideal voltage buffer. The control voltage is equal to the voltage applied between terminals V1 and V2.

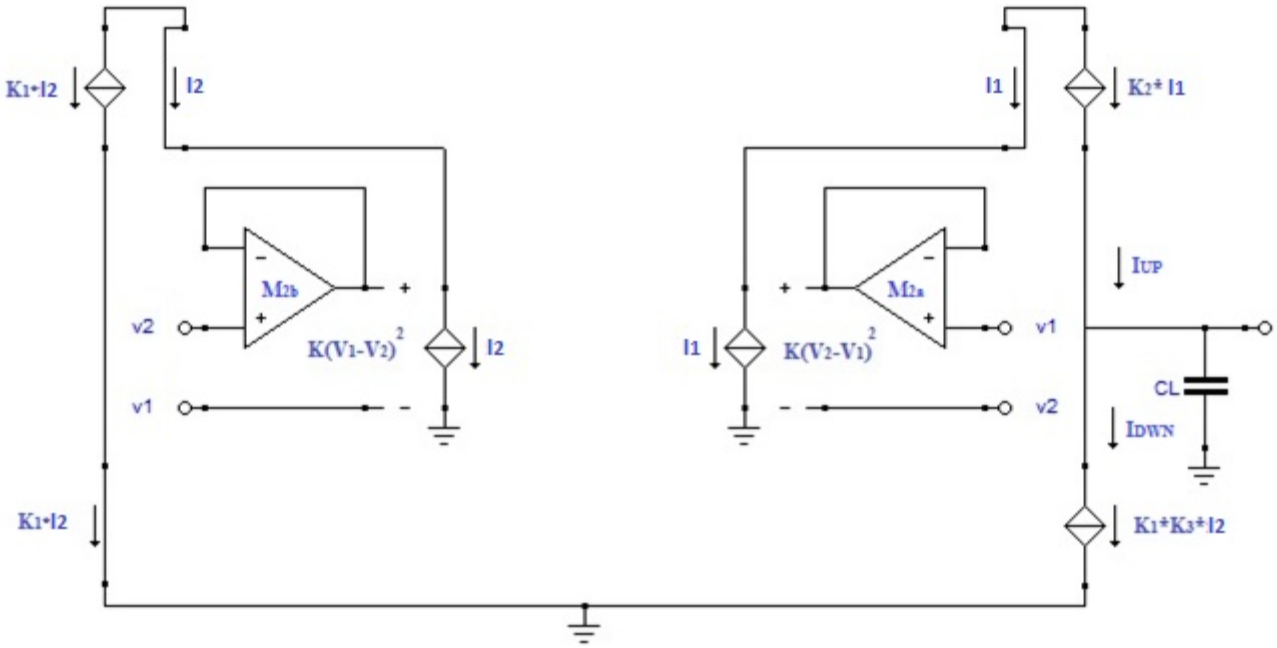


Fig.5. 6: Circuit equivalent to a large signal of the one shown in Fig.5.3

By applying a differential mode signal between input terminals V1 and V2, of the type:

$$V_1 = \frac{V_{id}}{2} \quad (5.6)$$

$$V_2 = -\frac{V_{id}}{2} \quad (5.7)$$

the differential mode signal results to be:

$$V_1 - V_2 = V_{id} \quad (5.8)$$

In Fig.5.7 the currents I1 and I2 are shown as a function of the differential mode signal. In Fig.5.8 the trend of the load current (I_L) is shown. The trend of the curve can be seen as the sum of two

regions: a linear one for $|V_{id}|<V_{GS}-V_T$ where the contributions of I_1 and I_2 are present; the second region, for $|V_{id}| >V_{GS}-V_T$, where only a current contribution (I_1 or I_2) is present, shows a quadratic behavior.

At this point two cases can be distinguished:

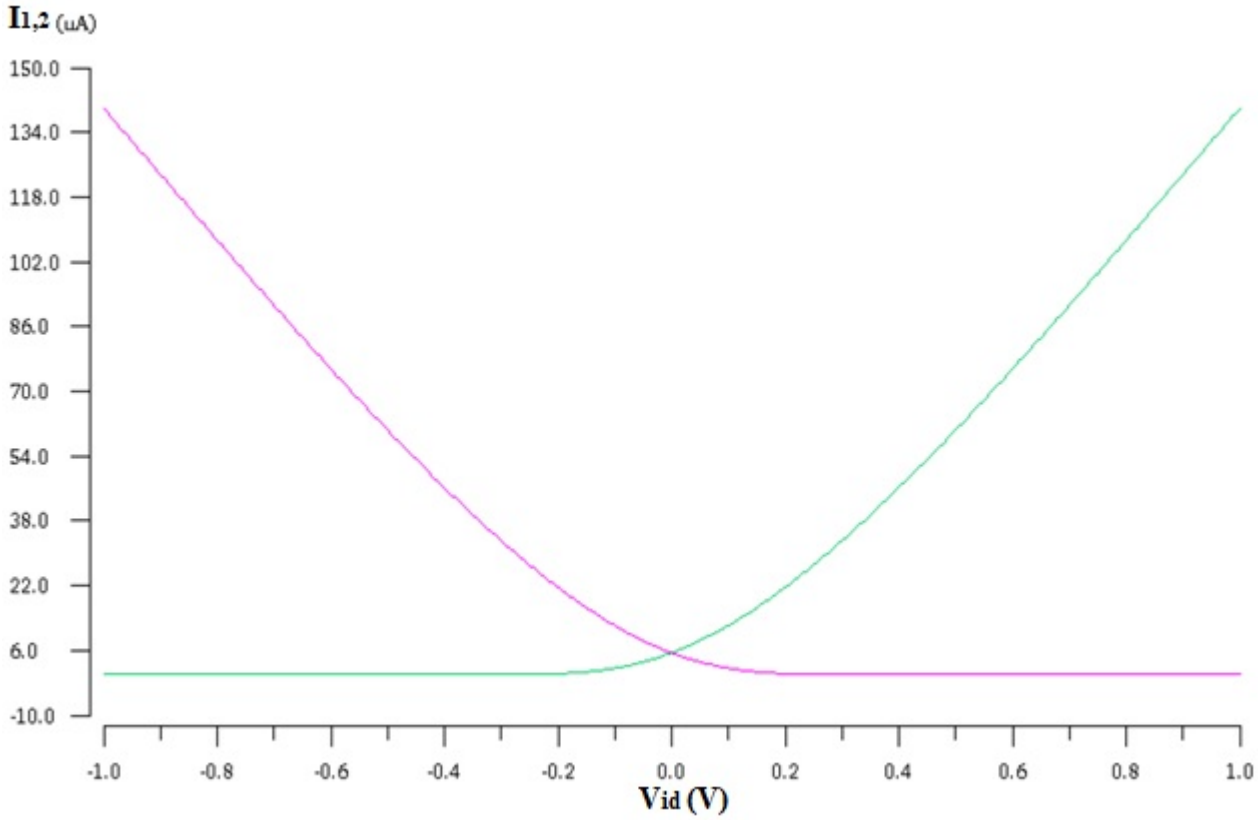


Fig.5. 7: Currents (I_1,I_2) depending on the signal Vid

Case 1: $|V_{id}| < V_{GS} - V_T$

In this case, both currents I_1 and I_2 are present. The respective equations are given by:

$$I_1 = I_{UP} = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2 \quad (5.9)$$

$$I_2 = I_{DWN} = K(V_{GS} - V_{id} - V_T)^2 = K(V_{OVQ} - V_{id})^2 \quad (5.10)$$

Writing the Kirchhoff equation for the equilibrium of currents at the output node, you get:

$$I_L = I_{UP} - I_{DWN} = K(V_{GS} + V_{id} - V_T)^2 - K(V_{GS} - V_{id} - V_T)^2 =$$

$$= 4K(V_{GS} - V_T)V_{id} = 4K(V_{OVQ})V_{id} \quad (5.11)$$

The equation (5.11) shows that the output current trend in the considered case is linear.

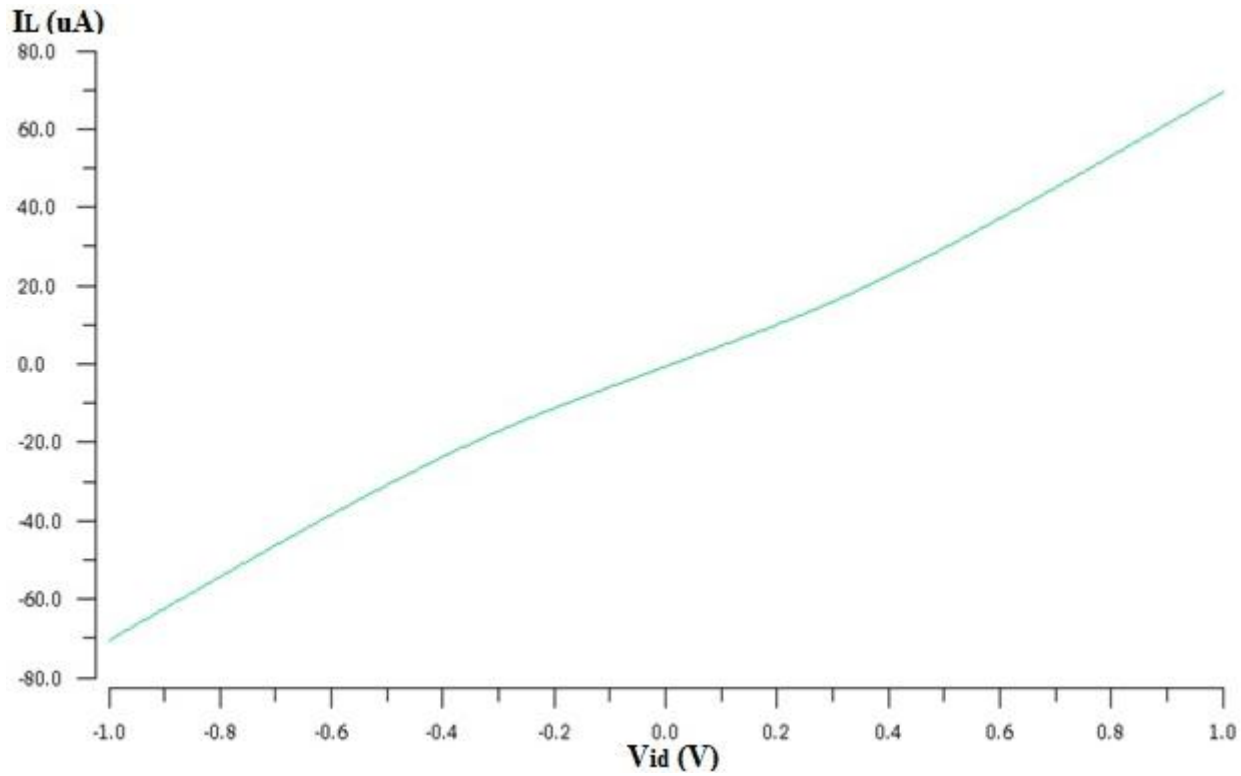


Fig.5. 8: Currents (I_L) depending on the signal Vid

Case 2: $|V_{id}| > V_{GS} - V_T$

In case 2, only one current (I_1 or I_2) should be considered as a branch is cut off. The related equations are:

$$I_{UP} = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2 \quad (5.12)$$

$$I_{DWN} = 0 \quad (5.13)$$

Writing again the Kirchhoff equation for the equilibrium of currents at the output node, now I get:

$$I_L = I_{UP} - I_{DWN} = I_{UP} = K(V_{OVQ} + V_{id})^2 \quad (5.14)$$

Equation (5.14) shows that the output current has a quadratic behavior. The equations (5.11) and (5.14) are valid for all topologies described in chapter 2.

5.3 Simplified model and equation for non linear trend I-V

In order to estimate the settling time of the OTA in Fig.5.3, the latter was closed in buffer configuration. The terminal indicated by V_1 was connected to the output terminal while a voltage step was applied to terminal V_2. Fig.5.9 shows the simplified scheme of the circuit in Fig.5.3 closed in a buffer configuration.

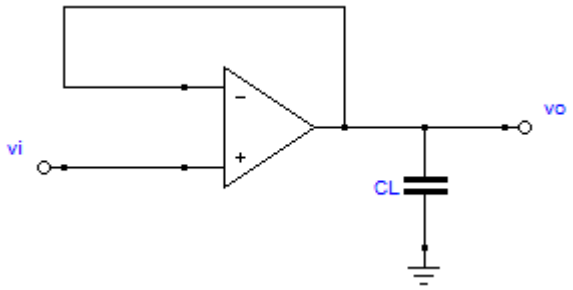


Fig.5. 9: Simplified model of the circuit of Fig.5.3 with buffered OTA

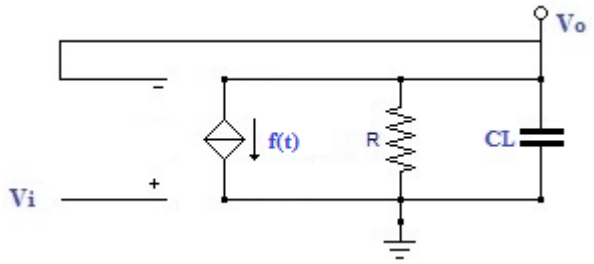


Fig.5. 10: Model of the circuit in Fig.5.3 in a buffer configuration

The hypothesis is made that a large step input is applied, and the capacitor is charged so that the V_{id} signal is greater than the overdrive voltage (V_{ov}).
Under the hypotheses made, I am in the condition described by case 2, in which $V_{id} > V_{GS} - V_T$. In this case let's assume that f(t) (see, the current model in Fig.5.10), is equal to equation (5.12):

$$\mathbf{f(t) = I_1 = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2} \quad (5.12)$$

So I can write:

$$f(t) = k(V_{OVQ} + V_{id})^2 \quad (5.15)$$

As the OTA is closed in buffer configuration, the differential input signal can be written as:

$$V_{id}(t) = V_i(t) - V_o(t) \quad (5.16)$$

Considering the circuit in Fig.5.10, I can write the Kirchhoff equation for the equilibrium of currents at the output node, so that:

$$f(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad (5.17)$$

From expressions derived in Appendix C, the following nonlinear differential equation is obtained:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{1}{C}(2kV_i + 2kV_{OVQ} - \frac{1}{R})V_o + \frac{k}{C}(V_{OVQ} + V_i)^2 \quad (5.18)$$

Equation (5.18) can be related to a known equation named "Riccati equation".
In case 1/R is negligible, Eq. (5.18) can be written as:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2(V_i + V_{OVQ})V_o + \frac{k}{C}(V_i + V_{OVQ})^2 \quad (5.19)$$

If I put the term:

$$(V_i + V_{OVQ}) = f(t), \quad (5.20)$$

I can rewrite:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad (5.21)$$

From expressions derived in Appendix C, I prove that:

$$f(t) = (V_i + V_{OVQ}) = costant\ , \quad (5.22)$$

is a solution of equation (5.19). Considering Eqs. (5.20), (5.18) I can write it in the more compact form:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2\alpha f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad (5.23)$$

Integration is possible if its particular integral y(x) = y_1(x) is known. In this case with appropriate changes of the variable, it can be brought back to a Bernoulli equation which in turn becomes a linear equation. With appropriate math steps reported in the Appendix C, I get a solution of the type:

$$y = y_1 - \frac{e^{-\int(A-2y_1B)dx}}{\int B\cdot e^{-\int(A-2y_1B)dx}\cdot dx + k} \quad (5.24)$$

where y_1 is:

$$y_1 = \overline{V_0} = \beta f(t) \quad (5.25)$$

and represents a particular solution of Riccati' equation, β is calculated in Appendix C.

Solving the integrals that appear in equation (5.24), I can write the general solution of Riccati' equation as:

$$V(t) = \overline{V_0} - \frac{1}{[-\frac{B}{T} + Qe^{Tt}]} \quad (5.26)$$

The integration constant is given by:

$$Q = \frac{1}{y_1 - y_0} + \frac{B}{T} \quad (5.27)$$

Expressions of terms B, T, Q are reported in the Appendix C.

5.4 Differential equation solution for I-V linear trend

When the load capacitance (C_L) is discharged, V_{id} tends to decrease, reaching the condition described by case 1 ($|V_{id}| < V_{GS} - V_T$). For convenience, equations in paragraph 5.2 regarding the case study 1, where the current dependence on the differential voltage is linear, are reported below:

Case 1: $|V_{id}| < V_{GS} - V_T$

$$I_1 = I_{UP} = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2 \quad (5.9)$$

$$I_2 = I_{DWN} = K(V_{GS} - V_{id} - V_T)^2 = K(V_{OVQ} - V_{id})^2 \quad (5.10)$$

$$I_L = I_{UP} - I_{DWN} = 4K(V_{OVQ})V_{id} \quad (5.11)$$

Considering "Case 1" ($|V_{id}| < V_{GS} - V_T$), a current is obtained as the difference of two current inputs generated by the two branches in Fig.5.6.

$$f(t) = I_1 - I_2 = 4K(V_{OVQ})V_{id} \quad (5.12)$$

Taking into account Fig.5.9 and Fig.5.10, I can write the input differential signal as:

$$V_{id}(t) = V_i(t) - V_o(t) \quad (5.16)$$

By writing the Kirchhoff equation for currents at the output node of the circuit depicted in Fig.5.10, I get:

$$f(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad (5.28)$$

which is a first-order differential equation:

$$\frac{dV_o}{dt} + A(t)V_o = B(t) \quad (5.29)$$

The equation (5.29) is a non homogeneous linear equation that shows a known solution. The general solution is:

$$V_o = \frac{\int e^{\int A(t)dt} B(t)dt}{e^{\int A(t)dt}} \quad (5.30)$$

from the accounts carried out in the Appendix C, Eq. (5.30) can be written as:

$$V_o = \frac{\int e^{\int A(t)dt} B(t)dt}{e^{\int A(t)dt}} = \frac{\frac{B}{A}e^{A\cdot t} + c}{e^{A\cdot t}} = \frac{B}{A} + c \cdot e^{-A\cdot t} \quad (5.31)$$

where,

$$A(t) = \left(\frac{4KV_{OVQ}}{C} + \frac{1}{CR}\right) \quad (5.32)$$

$$B(t) = \frac{4K(V_{OVQ})V_i}{C} \quad (5.33)$$

I can rewrite Eq. (5.31) as:

$$V_o(t) = \frac{V_i}{1 + \frac{1}{4KRV_{OVQ}}} + ce^{-A\cdot t} = \rho V_i + ce^{-A\cdot t} \quad (5.34)$$

where the integration constant can be calculated by imposing the initial condition:

$$V_o(0) = V_i - V_{ovq} \quad (5.35)$$

$$c = V_i(1 - \rho) - V_{ovq} < 0 \quad (5.36)$$

5.5 Calculation of the proposed model's settling time

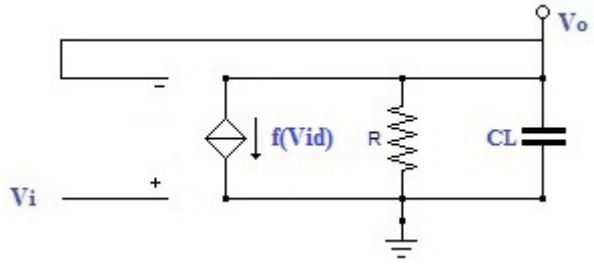


Fig.5. 11: Model proposed

The circuit shown in Fig.5.11 shows the model proposed for studying the behavior of class AB "OTA" in a buffer configuration under suitable hypotheses. Resistance R represents the equivalent that is seen at the output of the circuit of Fig.5.3 while the capacitance CL is equivalent to that used in the circuit of Fig.5.3. The function f(V_{id}), describes the behavior of a voltage-controlled current source that follows the laws given by the equations (5.37). The model of Fig.5.11 is valid under the hypothesis that the circuit in Fig.5.3 shows a single pole or dominant pole transfer function. Indeed, the circuit shows a second pole that is introduced by the current mirror, so that the hypothesis I'm doing is to have a structure with a wide phase margin (≥70°).

Obviously the currents of the real circuit and those of the model must be described by the same set of equations.

$$f(v_{id}) = \begin{cases} 4kV_{ovq}V_{id} & |V_{id}| < V_{ovq} \\ sgn(V_{id})k(V_{ovq} + V_{id})^2 & |V_{id}| > V_{ovq} \end{cases} \quad (5.37)$$

Since the circuit of Fig.5.11 is in a buffer configuration, the relation between input and output can be expressed as:

$$V_{id} = V_i - \beta V_o \quad (5.38)$$

with β=1. The initial condition is:

$$V_o = A_{VF}V_i \quad (5.39)$$

where A_{VF} is the closed loop gain, that can be expressed as:

$$A_{VF} = \frac{A_V}{1+\beta A_V} \quad (5.40)$$

where A_V is the open loop gain and is given by:

$$A_V = G(V_{id} = 0)R \quad (5.41)$$

where G is the transconductance:

$$G(V_{id} = 0) = 4kV_{ovq}N_{cm} \quad (5.42)$$

where Ncm is current mirror gain factor. R, is given by:

$$R = \frac{R_o}{N_{cm}} \quad (5.43)$$

If assume that N_{cm}=1, the regime output voltage is:

$$4kV_{ovq}(V_i - V_o) = \frac{V_o}{R} \quad (5.44)$$

$$V_o = \frac{4kRV_{ovq}}{1+4kRV_{ovq}}V_i \qquad (V_o = V_i \quad \text{for } R \to \infty) \quad (5.45)$$

To test the performance of the model, I consider an input step, defined as:

$$V_i(0^-) = V_1 \quad (5.46)$$

$$V_i(0^+) = V_2 = V_1 + \Delta \qquad \Delta > V_{ovq} \quad (5.47)$$

$$V_{id}(0^+) = V_2 - \frac{4kRV_{ovq}}{1+4kRV_{ovq}} V_1 > V_{ovq} \qquad (V_1 < 0) \tag{5.48}$$

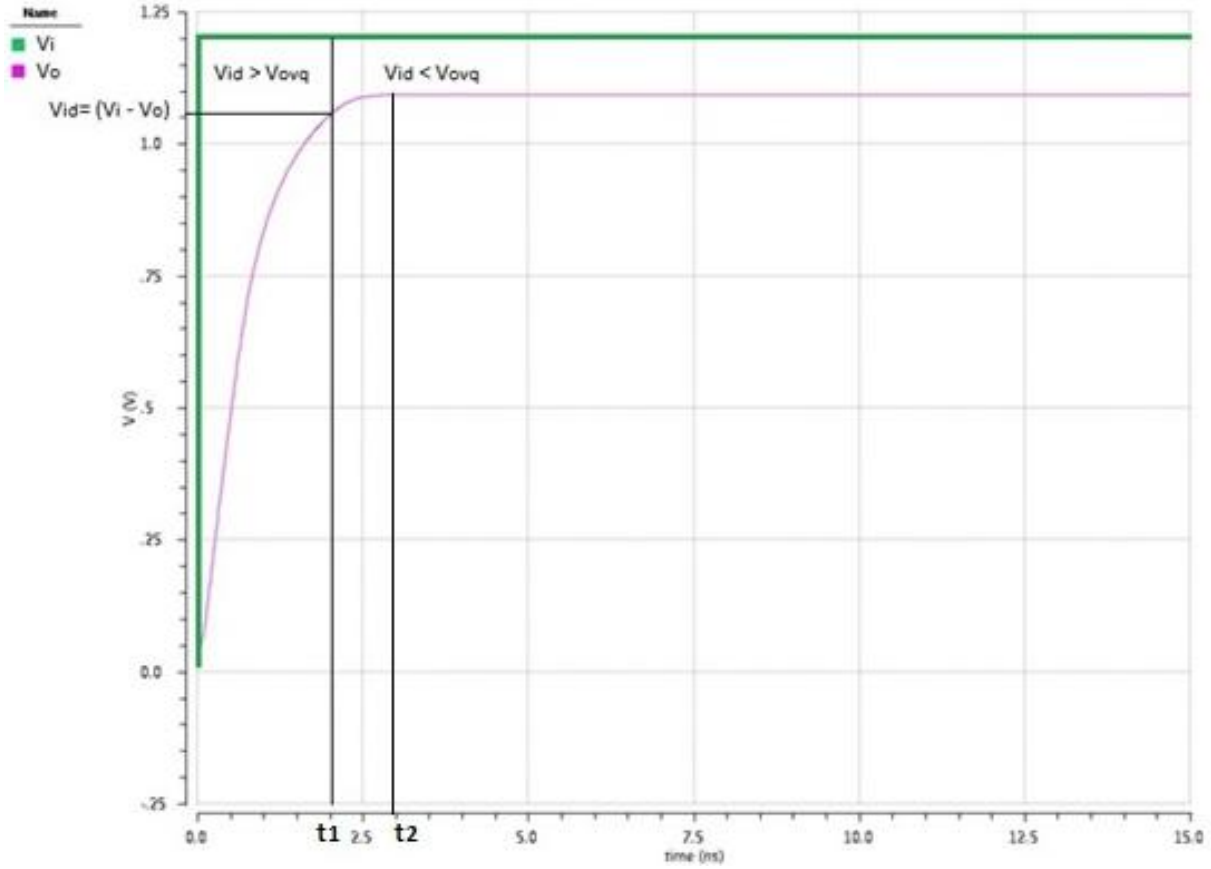


Fig.5. 12: Input voltage step response

The settling time, due to step response, can be written as the sum of two contributions, given by:

$t_{set}=t_1+t_2$ (5.49)

Time t_1 is due to the case where the current flowing in the load (I_L) is nonlinear (case 2) while t_2 is due to the case where the current I_L has a linear trend (case 1).

5.5.1 Time calculation t_1

To calculate the time t_1 I have to consider the case in which | Vid |> Vov where only one of the currents generated by the differential input transconductor, of the circuit of Fig.5.3, is mirrored to the output. The current generator f(V_{id}) will provide a current that follows a quadratic law according to what is written in the second of equations (5.37).

By highlighting the relation between input voltage and output voltage, I have

$V_{id} = V_i - V_0$ (5.50)

taking into account the differential input voltage value (Vid) that makes me pass from nonlinear to linear behavior, I can write

$V_{id} = V_{GS} - V_T = V_i - V_0 = V_{ov}$ (5.51)

by expressing the output voltage Vo as a function of V_{ov} and indicating with t_1, the time instant in which the output voltage reaches the final value, I have:

$V_0(t_1) = V_i - V_{ov}$ (5.52)

For convenience, some equations obtained for the calculation of the integral of the Riccati's equation and reported in Appendix C, are shown below. The particular integral of Riccati's equation is given by:

$$y_1 = \overline{V_0} = \beta f(t) \quad (5.25)$$

The general solution of Riccati's equation is:

$$V(t) = \overline{V_0} - \frac{1}{[-\frac{B}{T}+Qe^{Tt}]} \quad (5.26)$$

The integration constant is given by:

$$Q = \frac{1}{y_1 - y_0} + \frac{B}{T} \quad (5.27)$$

By imposing the condition that allows to get t_1:

$$V_0(t1) = V_i - V_{ov} = \overline{V_0} - \frac{1}{[-\frac{B}{T}+(\frac{1}{\overline{V_0}-y_0}+\frac{B}{T})e^{Tt}]} \quad (5.53)$$

with some analytical passages, reported in Appendix C, I get:

$$t_1 = \frac{1}{T}\ln\left(\frac{\frac{B}{T}-\frac{1}{(V_i-V_{ov}-\overline{V_0})}}{\frac{1}{\overline{V_0}-y_0}+\frac{B}{T}}\right) \quad (5.54)$$

5.5.2 Time calculation t_2

To calculate the time t_2 I have to consider the case in which | Vid |< Vov where both the currents generated by the differential input transconductor, for the circuit in Fig.5.3, are mirrored to the output. The current generator f(V_{id}) will provide a current that follows a linear law according to what is written in the first of equations (5.37).

In section 5.6, the general solution of the differential equation in the linear zone was found, reported below for convenience:

$$V_o(t=0) = \frac{V_2}{1+\frac{1}{4KRV_{OVQ}}} + ce^{-A\cdot t} = \rho V_2 + ce^{-A\cdot t} \quad (5.34)$$

where "c" is the integration constant and is given by:

$$c = V_2(1-\rho) - V_{ovq} < 0 \quad (5.36)$$

The settling time with an error ε is given by:

$$V_o = \rho V_2 - \rho(V_2 - V_1)\varepsilon \quad (5.55)$$

imposing such a condition I get:

$$\rho V_2 - \rho(V_2 - V_1)\varepsilon = \rho V_2 + ce^{-At_2} = \rho V_2 - |c|e^{-At_2} \quad (5.56)$$

with some analytical passages, reported in appendix, I obtain:

$$t_2 = \frac{1}{A} ln \frac{|c|}{\varepsilon\rho(V_2 - V_1)} \quad (5.57)$$

5.6 Model validation

In the design and prototyping of an integrated electronic circuit, four steps can be identified:

1. design,
2. manufacture,
3. packaging,
4. test.

The most important aspect of this section is that of design, that can be divided into three phases: ideation and modeling, optimization, validation.

Idea and modeling consists of transforming an idea into a model that manages to enclose in itself the function that the system will have to carry out. Specifically, the proposed model will implement the function defined by the equations (5.11 and 5.14) in order to get a behavior similar to that of a class AB OTA described by the same set of equations.

Modeling plays a crucial role in design and must be rigorous, as general as possible, and easy to understand. There are several ways to describe a model, among which can be cited: the Hardware Description Language (HDL), the flow charts, the schematic, and the geometric layout at the physical level of the circuit. The model in question has been implemented in CAD (Virtuoso CADENCE) as shown in the Fig5.13, for the Peluso topology in the single ended version.

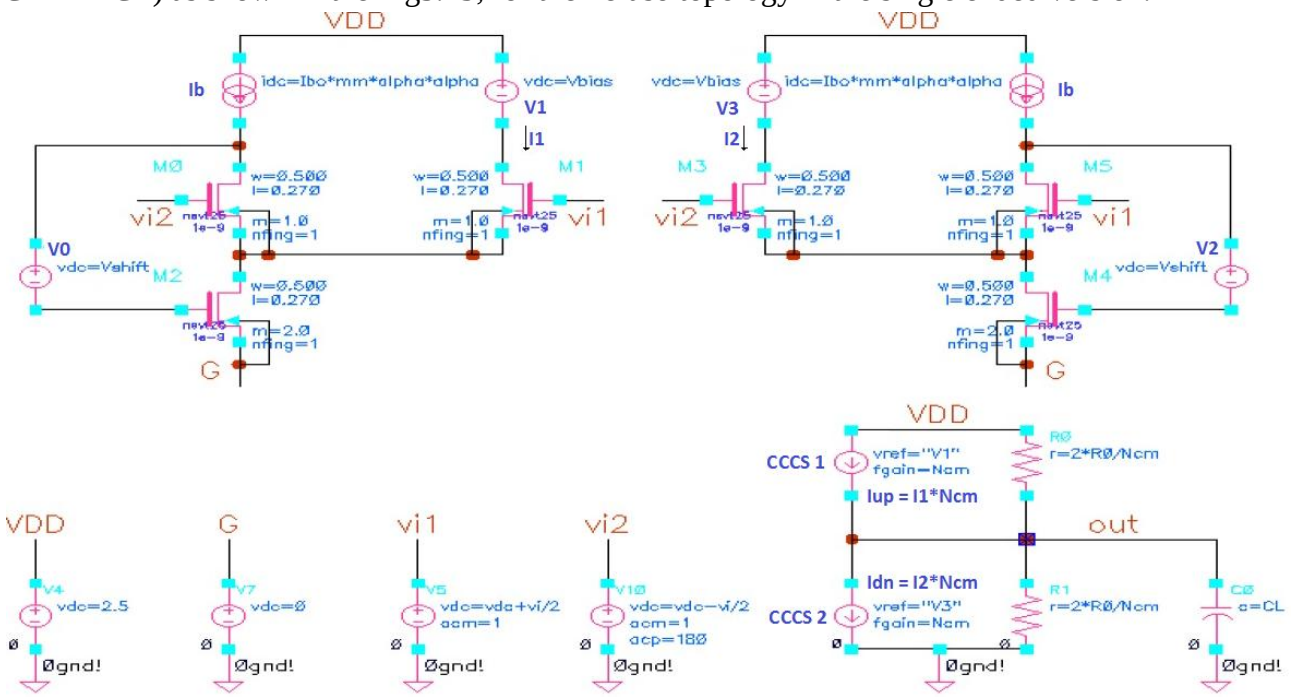


Fig.5. 13: Circuital implementation of the class AB OTA original model

Since the equations (5.14) used to describe the current behavior of the OTA in question follow a quadratic law, the choice of devices to be used fell on those who followed as much as possible a quadratic law to describe their behavior.

Then, to implement the circuital model, the I/O devices, of the technology with 40 nm production process provided by STMicroelectronics, are used. I/O devices have a channel length of 270 nm and have a more quadratic characteristic (Id-Vgs) than devices with a channel length of 40 nm.

The behavior of the circuit shown in the Fig.5.13 is described by the equation set (5.11 and 5.14) carried out in section 5.2. In section 5.3, by making the appropriate assumptions, an equivalent

model of that circuit implemented in CAD was proposed. The equivalent model is shown in Fig.5.11, and its behavior is described by the solution of two differential equations, one is linear of the first order, and the other is nonlinear and is named Riccati's equation. The combination of the solutions of the two differential equations allows to describe the behavior of the circuit according to some parameters. The analytic solution, due to the combination of the solutions of the two differential equations was subsequently simulated in Matlab environment, using the same parameter values used to perform simulations in CADENCE.
Optimization aims to maximize some figures of merit (FOMs) of the system in order to improve its performance. The features that need to be taken into account by optimization can be related to system performance, occupied area, power dissipation, testability, fault tolerance.
The validation step finally allows to verify the consistency of the models used during design as well as the properties of the original model. It consists in obtaining sufficient certainty that the circuit will operate correctly, regardless of any manufacturing faults.
Validation is carried out by simulation and verification in both Matlab environment and Virtuoso CADENCE environment.
The variables used to describe the circuital model are four: current mirror gain (Ncm), output resistance (R), transconductance (K), and overdrive voltage (Vov). The simulations were carried out by varying one parameter at a time by adopting appropriate arrangements, described below, to prevent the circuit being unbiased. The variables used for validation are summarized in Table 5.1.

Table 5.1

Model variables

alpha	mm	Ncm	Ro
used to vary the MOS overdrive voltage (Vov)	used to vary the multiplicity of MOS	used to vary the gain of the current mirrors	used to vary the output resistance

Ro represents the output resistance ($r_{on}||r_{op}$) divided by alpha factor that, as the default condition, is set equal to 1.

$$R_o = \left(\frac{r_{on}||r_{op}}{alpha}\right) = \left(\frac{R}{alpha}\right) \quad (5.58)$$

dividing *R* for the alpha parameter, when varies *Vov* acting on alpha the gain *Av* remains constant for a range of values (1÷3.5).

$$r = 2 * \frac{R_o}{Ncm} \quad (5.59)$$

where *r* represents the resistors depicted in Fig.5.13 and *Ncm* is the gain of the current mirrors does not affect the gain voltage (Av).
The MOS conductance parameter (K) depends on the parameters manufacturing technology and geometric dimensions:

$$K = mm\left(\frac{1}{2}\mu_{n,p}C_{ox}\frac{W}{L}\right) \qquad \left[\frac{A}{V^2}\right] \quad (5.60)$$

where:
- μ is the carriers mobility
- C_{ox} is the oxide capacitance
- W is the gate width
- L is the gate length

- mm is the multiplicity of MOS and is used in design tools.

As it can be seen, the parameter "*K*" is proportional to the transistor area and since *Vth* varies slightly with *W*, it is preferred to act by varying *mm*. To keep the bias point unaltered, the multiplicity of all the devices present in the circuit of Fig.5.13 needs to be varied appropriately, including current mirrors as shown in Table 5.2.

To vary *Vov*, I acts on current generators (IB) while maintain constant "*W*" and "*mm*" parameters.

Table 5.2				
Dependence of design variables from model variables				
IB	**Multiplicity $M_{0,1,3,5}$**	**Multiplicity $M_{2,4}$**	**$r_{0,1}$**	**$CCCS_{1,2}$**
IB0**mm**(*alpha*)^2	*mm*	2**mm*	2*R_0/*Ncm*	$I_{1,2}$**Ncm*

To vary *Vov* (and so *alpha* parameter) affects linearity, gain, and bias point. Linearity involves a maximum limit (alpha = 3.5). The gain depends little (in linear zone) on the bias point choices. Table 5.2 shows the dependence of design variables on those used for modeling. The current generator IB depends on the multiplicity of transistors (*mm*) and *alpha* parameter. By increasing the multiplicity of transistors, it is also necessary to increase the bias current to keep the bias point unchanged. The output resistors ($r_{0,1}$) of the circuit shown in Fig.5.13 simulates the output resistances of the MOS transistors that would be in a real circuit. R_0 and R_1 in the model of Fig.5.13 are taken equal. Their value is inversely proportional to the alpha value so as to contain the variations that would be on the voltage gain as shown in Table 5.5, where the voltage gain as function of *R* and R_0 is reported. The output resistors ($r_{0,1}$) are also inversely proportional to the current mirrors gain to maintain constant the gain voltage. The current-controlled current-source ($CCCS_{1,2}$) in the circuit of Fig.5.13 model the behavior of the current mirrors. They read the $I_{1,2}$ currents and output them multiplied by an *Ncm* factor. Tables 5.3 and 5.4 summarize the default condition of my circuital model. Before validation, I performed simulation of the circuital model with "Virtuoso CADENCE" tool to estimate the settling time, leaving all parameters set to their default values. Once the settling time was estimated, I proceeded with estimation of the transconductance parameter (*K*) used in the mathematical equations found in the previous paragraphs.

Table 5.3											
Bias of the circuit of Fig.5.13											
$M_{0,1,3,5}$						**$M_{2,4}$**					
W [µm]	**L [µm]**	**m**	**V_{GS} [V]**	**V_{DS} [V]**	**V_{th} [V]**	**W [µm]**	**L [µm]**	**m**	**V_{GS} [V]**	**V_{DS} [V]**	**V_{th} [V]**
0.5	0.27	1	0.55	0.7	0.45	0.5	0.27	2	0.55	0.7	0.45

Table 5.4						
Default condition						
VDD [V]	**IB [µA]**	**R [MΩ]**	**alpha**	**mm**	**Ncm**	**R0 [MΩ]**
2.5	5.4	1	1	1	1	1

Table 5.5		
Voltage gain variation in function of α, R, R0 parameters		
α	**Av(R)**	**Av(R0)**
0.5	89.45	178.9
1	210.3	210.3
1.5	324.3	206.2
2	419.4	209.7
2.5	493.4	197.36
3	544.3	181.43
3.5	561	160.28

K can be estimated from the I_D-V_{GS} curve of the MOS, or from the I-V_{id} curve of the OTA. To estimate the *K* value,I exported the "CSV" files of the feature $I_{1,2}$-V_{id} and the one of Id-VGS for the single MOS. Subsequently, I imported the "CSV" files in Matlab environment and I estimated the value of "*K*" by fitting the curves imported from "CADENCE".

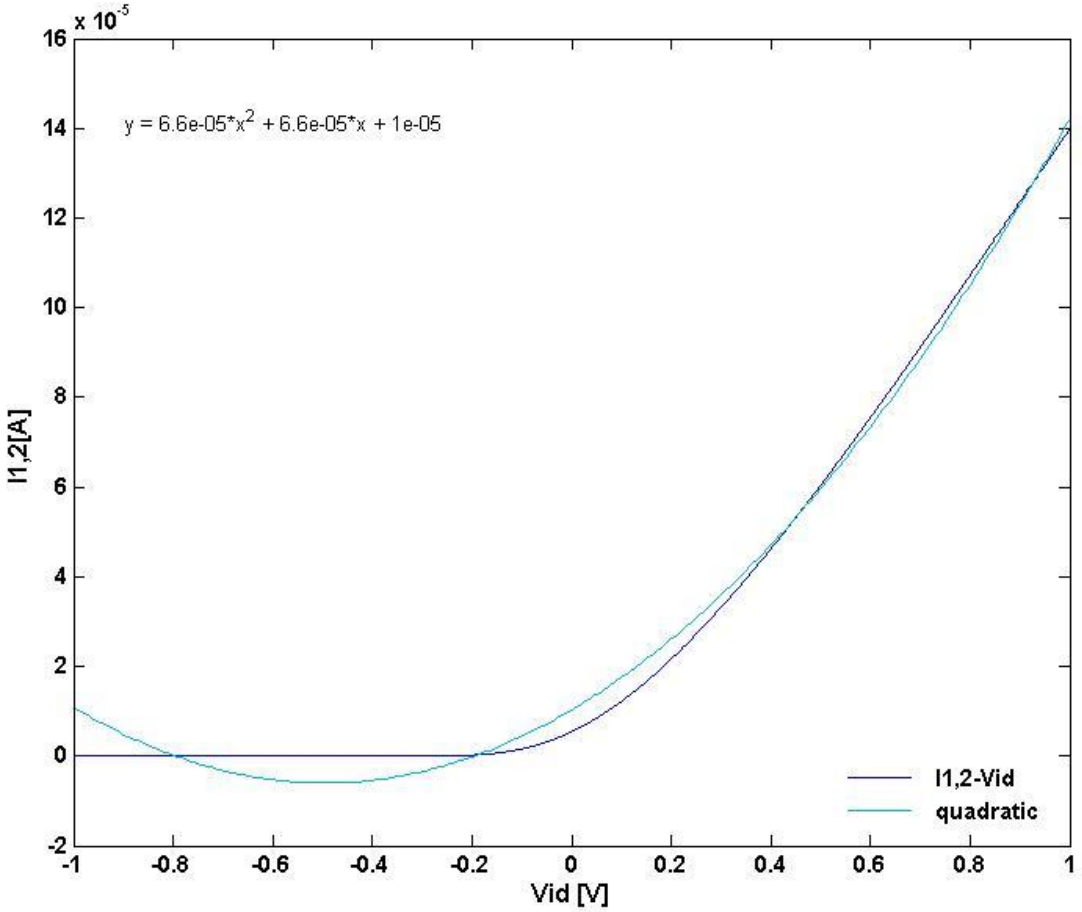


Fig.5. 14: Fitting of the curve from which it was estimated "*Kota2*"

In Fig.5.14, the current-voltage ($I_{1,2}$-V_{id}) characteristic of the circuit of Fig.5.13 is shown in blue, and the fitting curve is shown in cyan. The value of *K* was estimated by comparing the general equation of a parabola with that of the drain-current of a MOS in saturation.

$$\begin{cases} I_{1,2} = aV_x^2 + bV_x + c \\ I_{1,2} = K(V_{ov} + V_{id})^2 = KV_{id}^2 + 2KV_{ov}V_{id} + KV_{ov}^2 \end{cases} \quad (5.61)$$

where a, b, c are:

$$\begin{cases} a = K \\ b = 2KV_{ov} \\ c = KV_{ov}^2 \end{cases} \quad (5.62)$$

Also shown in Fig.5.14 is the parabola equation used to calculate one of the values of *K* used to estimate the settling time for the proposed model.

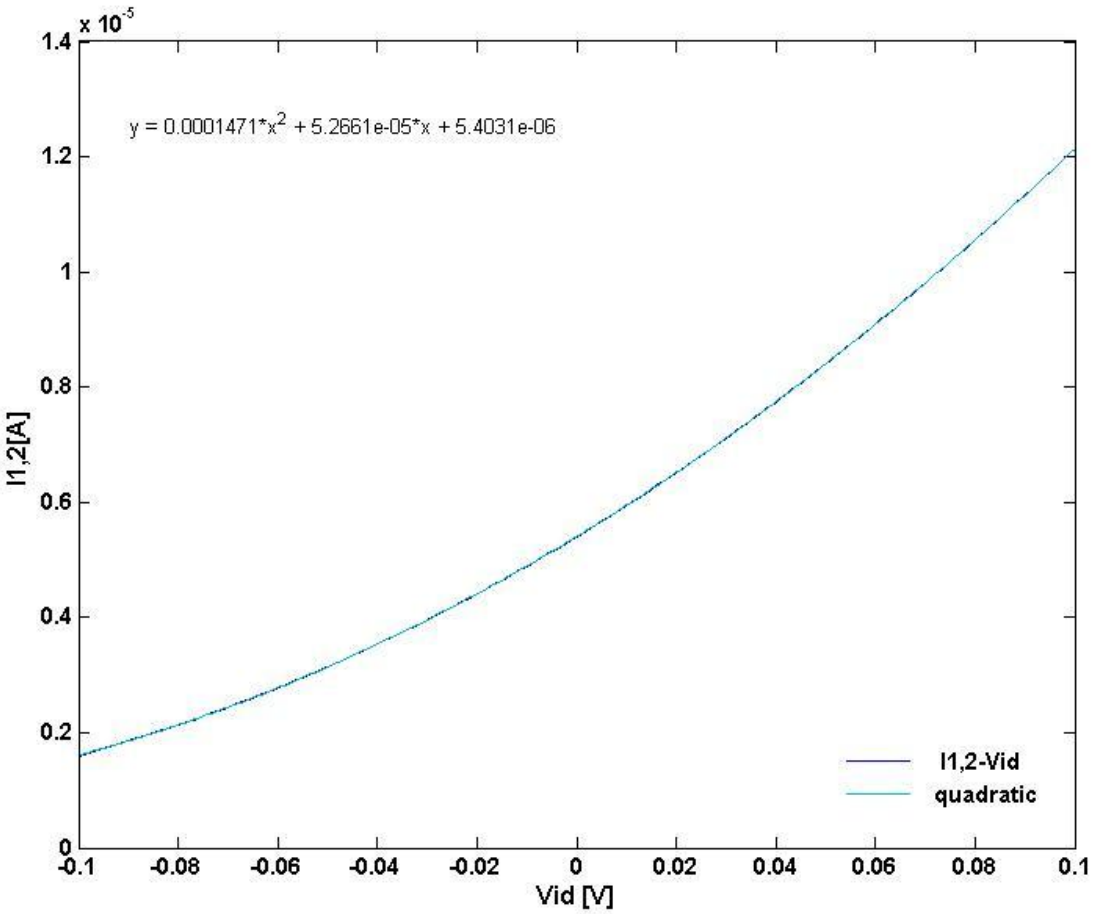


Fig.5. 15: Fitting of the curve from which it was estimated "*Kota1*"

Fig.5.15 shows that, by narrowing the fitting range, the result obtained for the estimate of "*K*" is very good.

Table 5.6

K-Vth value estimate by "OTA" fitting

VGS [V]	Vtho1 [V]	Vtho2 [V]	Vov1 [V]	Vov2 [V]	Kota1 $[A/V^2]$	Kota2 $[A/V^2]$
0.55	0.37101	0.0518	0.17899	0.49819	1.471e-4	6.6239e-5

Table 5.7 shows the values of *K*, Vov and Vth extracted from the equation of the fitting for a VGS value equal to that used in the CADENCE simulation.

Table 5.7				
Settling time for different value of K-Vth				
K[A/V^2] Vth[V]	**T1 [ns]**	**T2 [ns]**	**Tsetm [ns]**	**Tsetcad [ns]**
Kota1= 1.471e-4 **Vtho1=0**.37101	7.2137	57.452	64.665	12.8+52.2=65.08
Kota2= 6.6239e-5 **Vtho2=** 0.0518	0	51.958	51.958	12.8+52.2=65.08

In Table 5.7, T1 and T2 represent the settling time for the part of curve described by the solution of the Riccati equation and for the part of curve described by the solution of the first order differential equation, respectively. Tsetm is the settling time provided by the mathematical model implemented in matlab while Tsetcad is the settling time provided by the simulation in virtuoso CADENCE environment.

The *K* estimation was also made taking into account the I_d-V_{GS} characteristic of a single MOS. Fitting of I_d-V_{GS} curve was performed on three different curve portions as shown in Fig.5.16, 5.17, 5.18. Three values of *K* and V_{th} were obtained from the three fittings using the V_{GS} value used in circuit simulations in "Virtuoso CADENCE" environment, as shown in Table5.8.

Table 5.8									
K-Vth value estimate by "MOS" fitting									
VGS [V]	**Vth1 [V]**	**Vth2 [V]**	**Vth3 [V]**	**Vov1 [V]**	**Vov2 [V]**	**Vov3 [V]**	**K1 [A/V^2]**	**K2 [A/V^2]**	**K3 [A/V^2]**
0.55	0.22944	0.1905	0.18	0.3205	0.3595	0.37	1.1844e-4	1.4111e-4	1.4856e-4

For the three values of *K*-Vth, their respective settling times were estimated and compared to those obtained from simulations in "Virtuoso CADENCE" environment, as shown in Table 5.9.

Table 5.9				
Settling time for different value of K-Vth				
K[A/V^2] Vth[V]	**T1 [ns]**	**T2 [ns]**	**Tset [ns]**	**Tset(CADENCE) [ns]**
K1 =1.1844e-4 Vth1 =0.22944	1.43	43.77	45.21	12.8+52.2=65.08
K2 =1.4111 e-4 Vth2 =0.1905	0.515	33.37	33.89	12.8+52.2=65.08
K3 =1.4856 e-4 Vth3 =0.18	0.34599	30.94	31.29	12.8+52.2=65.08

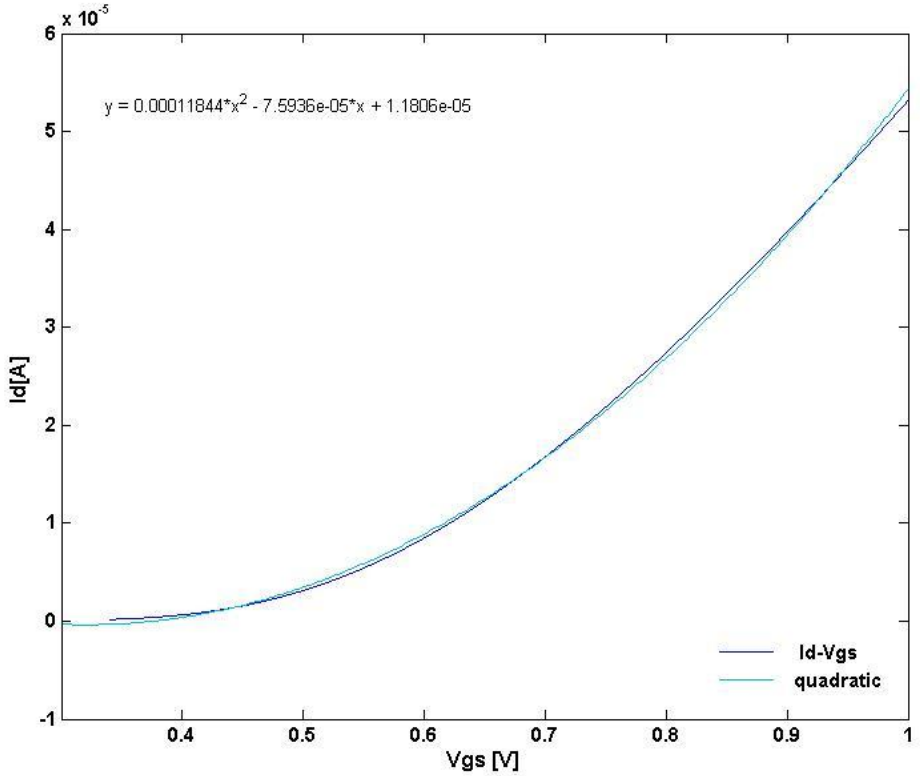


Fig.5. 16: Fitting for K_1 estimate

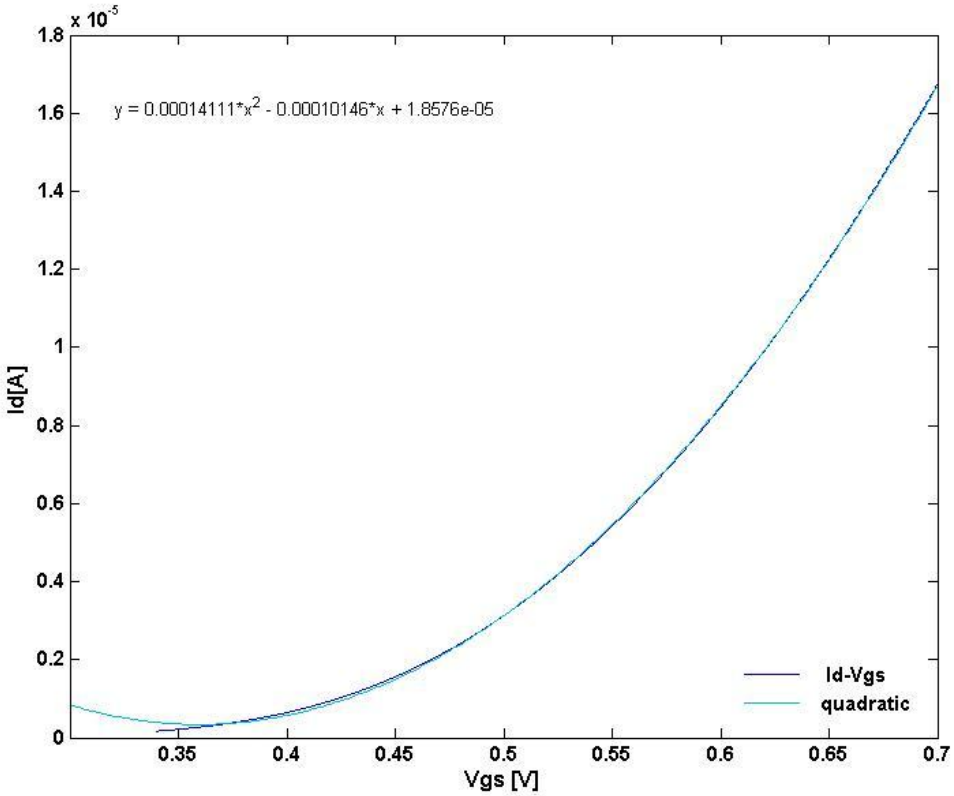


Fig.5. 17: Fitting for K_2 estimate

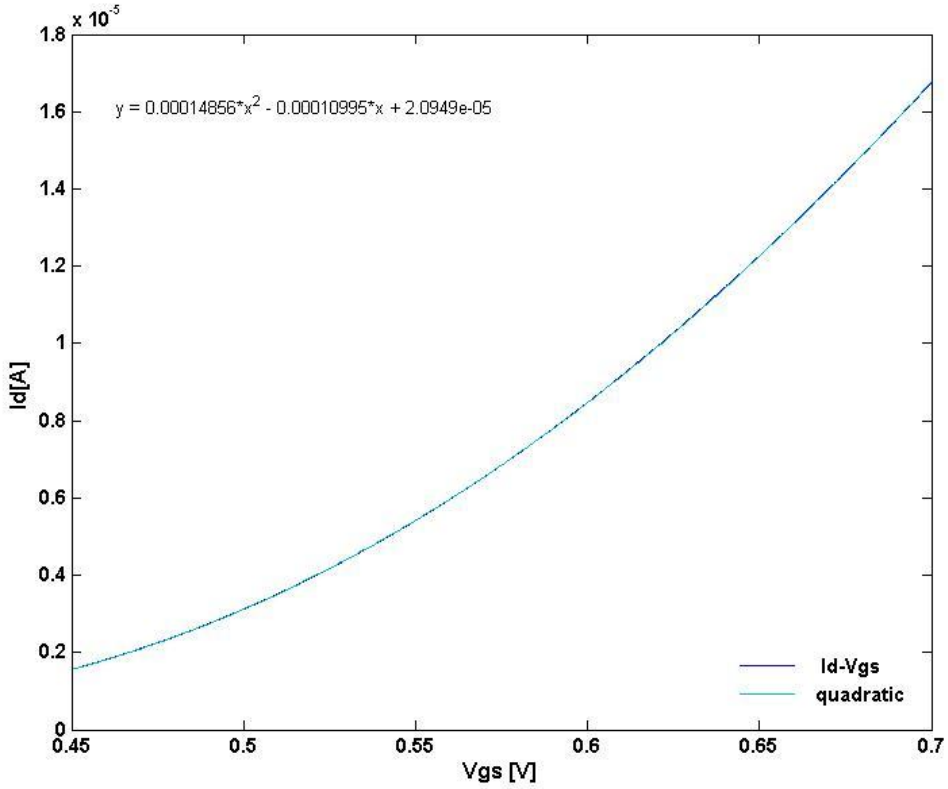


Fig.5. 18: Fitting for K_3 estimate

From the comparison of the results shown in Table 5.7 and Table 5.9, it is noted that the Kota1 is what makes it possible to obtain a settling time very similar to that obtained by the circuit simulation in the "virtuous CADENCE" environment.

The model was validated by performing a set of simulations in the Matlab environment as well as in the "Virtuoso CADENCE" environment by varying the parameters "*K*", Vov (*alpha*) ", *Ncm*, *mm*, one at a time as shown in Table 5.10.

Table 5.10

Validation Table

Kota1=1.471 e-4 $[A/V^2]$
Vtho1=0.37101 **[V]**

Avo [dB]	GBW [MHz]	nn	Ncm	α	mm	R0 [MΩ]	T1 [ns]	T2 [ns]	Tset Mat [ns]	Tset Cad [ns]	Ener Mat [pJ]	Ener Cad [pJ]	VGS [mV]	Vth [mV]
46.45	33.47	1	1	1	1	1	7.21	57.45	64.66	65.08	5,57	5,67	549.8	449.5
46.69	51.61	1	1	1.5	1	1	2.46	40.86	43.33	43.04	6,9	7,475	642.1	448.3
46.43	66.74	1	1	2	1	1	0.507	32.01	32.52	33.2	8,4	9,625	734.1	447.1
45.9	78.5	1	1	2.5	1	1	0	26.01	26.01	28.01	9,95	12,25	830	446
45.17	86.62	1	1	3	1	1	0	21.68	21.68	24.99	11,52	15,42	931	444.8
44.09	89.22	1	1	3.5	1	1	0	18.58	18.58	23.5	13,12	19,25	1030	443.6
6.45	29.4	1	1	1	1	0.01	4.43	29.15	33.58	33.12	24,25	8,275	549.8	449.5
26.45	33.43	1	1	1	1	0.1	6.77	52.87	59.65	59.9	8,625	6,1	549.8	449.5
40.43	33.47	1	1	1	1	0.5	7.16	56.9	64.06	64.4	5,925	5,725	549.8	449.5
46.45	50.2	1	1.5	1	1	1	7.2	38.3	45.5	43.3	4,9	4,35	549.8	449.5
46.45	66.94	1	2	1	1	1	7.19	28.72	35.92	32.4	4,7	3,675	549.8	449.5
46.45	66.94	1	2.5	1	1	1	7.19	22.98	30.17	25.7	4,7	3,275	549.8	449.5
46.45	100.4	1	3	1	1	1	7.18	19.15	26.33	21.4	4,8	3	549.8	449.5
46.45	117.1	1	3.5	1	1	1	7.17	16.41	23.59	18.3	4,95	2,8	549.8	449.5
52.47	66.94	1	1	1	2	1	3.6	28.72	32.33	32.5	4,7	5,625	549.8	449.5
55.99	100.4	1	1	1	3	1	2.4	19.15	21.55	21.59	4,4	5,6	549.8	449.5
58.49	133.8	1	1	1	4	1	1.8	14.36	16.16	16.07	4,275	5,55	549.8	449.5
60.43	167.3	1	1	1	5	1	1.44	11.49	12.93	12.89	4,175	5,575	549.8	449.5

Ibo= 5.4 **[µA]**
Vdd= 2.5 **[V]**
α=alpha

Table 5.10 shows that in the default case the estimated settling time in Matlab differs from the estimated "Virtuoso CADENCE" of 0.645%.

Fig.5.19 shows the input step and the output response of circuit represented in Fig.5.13. Fig.5.20 and Fig.5.21 represents the qualitative trends of the Riccati equation solution and linear differential equation solution.

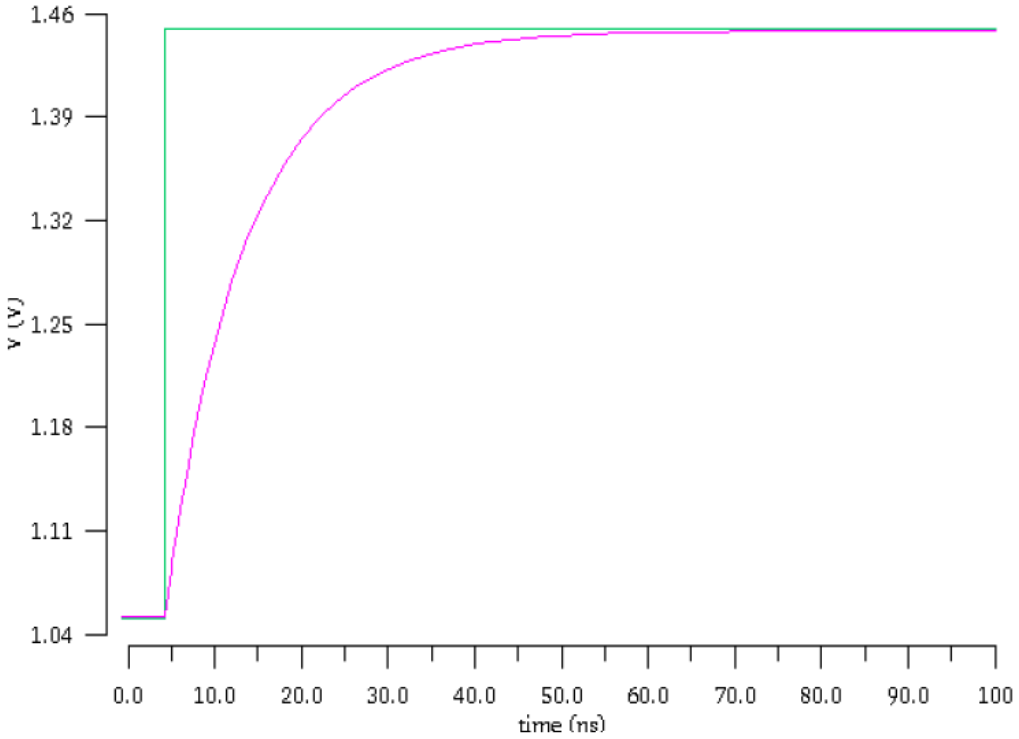


Fig.5. 19: Input step (green) and step response (magenta)

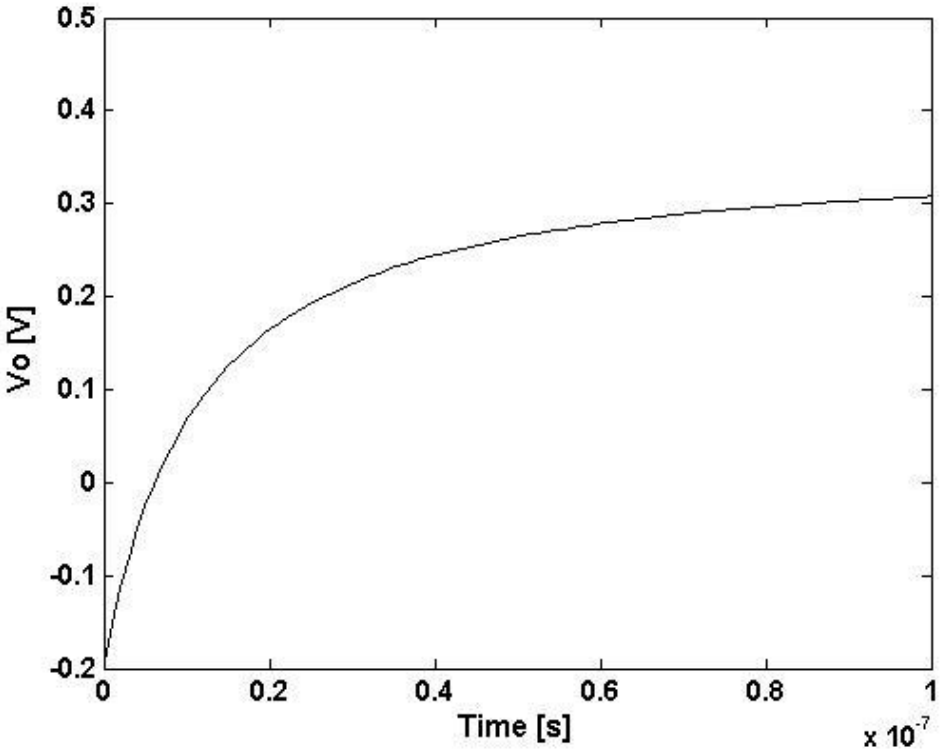


Fig.5. 20: Qualitative time trend of Riccati equation solution

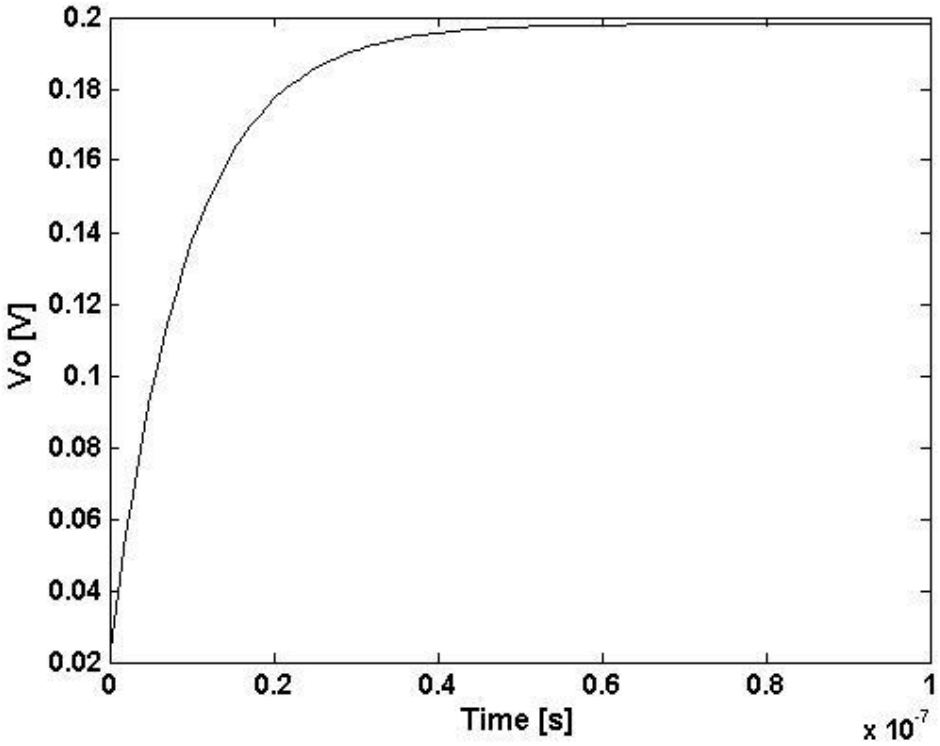


Fig.5. 21: Qualitative time trend of linear differential equation solution

5. 7 Settling time curves in function of *k* and Vov parameters

In this paragraph, graphical results are reported on the trend of the settling time as function of pairs of parameters. Since the resistance R_0 is fixed by the technology and the gain voltage value is determined by the desired static error, I decided to keep them constant and to vary in a case *K* and Vov and in the other *K* and *Ncm*.

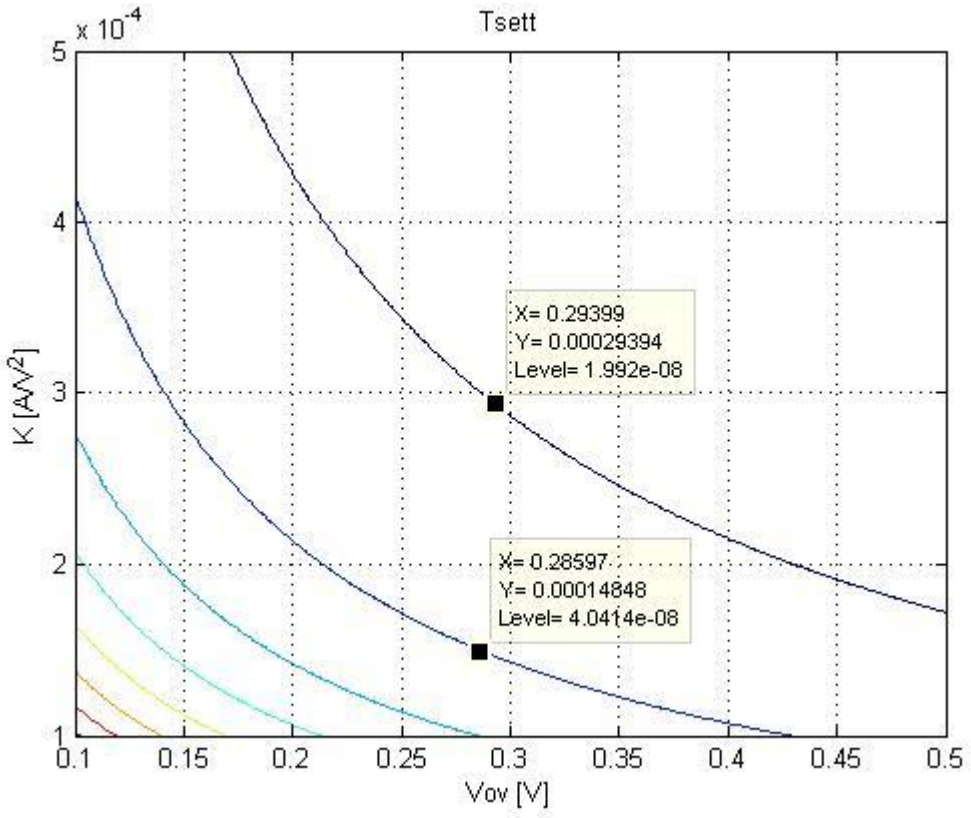


Fig.5. 22: Settling time level curves as function of parameters K and Vov

Fig.5.22 shows level curves that represent settling time in function of *K* and Vov parameters. For increasing values of *K* and Vov, the curves move to the right and upward at lower settling time values. Given a certain specification on settling-time, I can set one of the two parameters and see the other one as to be chosen. Fig5.23 shows the same results on a three-dimensional scale. Fig.5.24 shows the same results with a three-dimensional graph, in this case, it is immediately noted that the values at higher altitude (increasing settling time) are found for low K and Vov values. Fig.5.25 and Fig.5.26 describe the settling time level curves in case of K and Ncm variation. As can be seen the settling time decreases for *K* and *Ncm* increasing value. Also in these cases the curves move to the right and upward at lower settling time values. Fig.5.27 shows the same results with a three-dimensional graph.

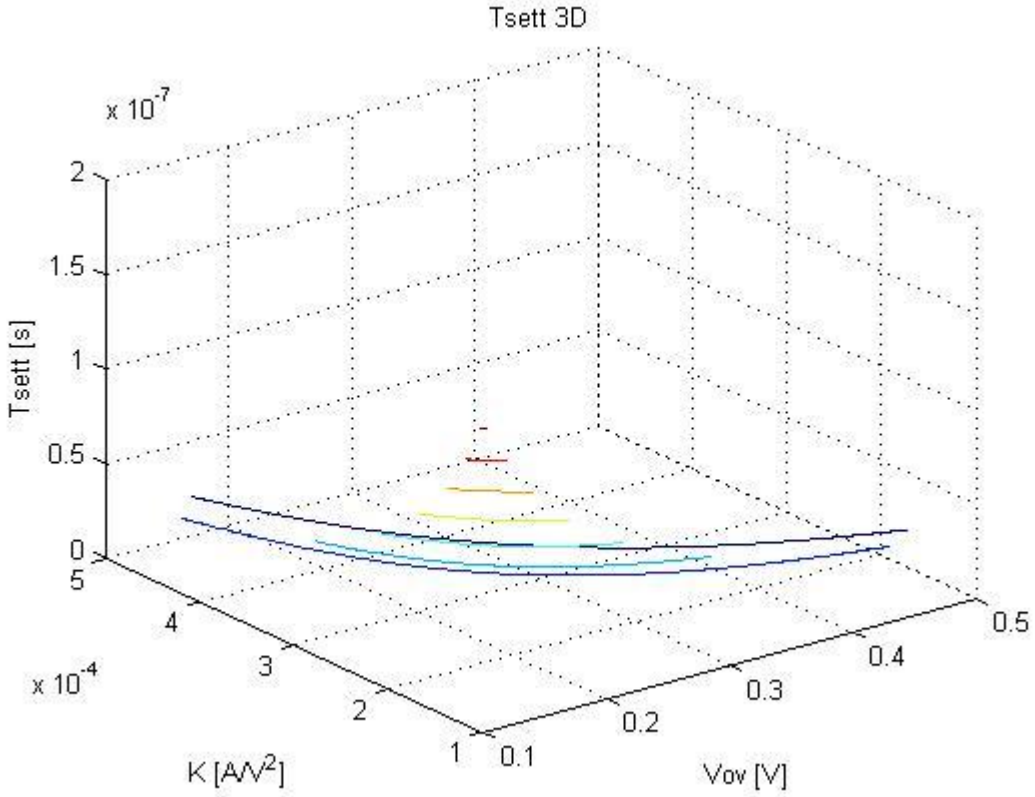


Fig.5. 23: Three-dimensional settling time level curves as function of parameters *K* and Vov

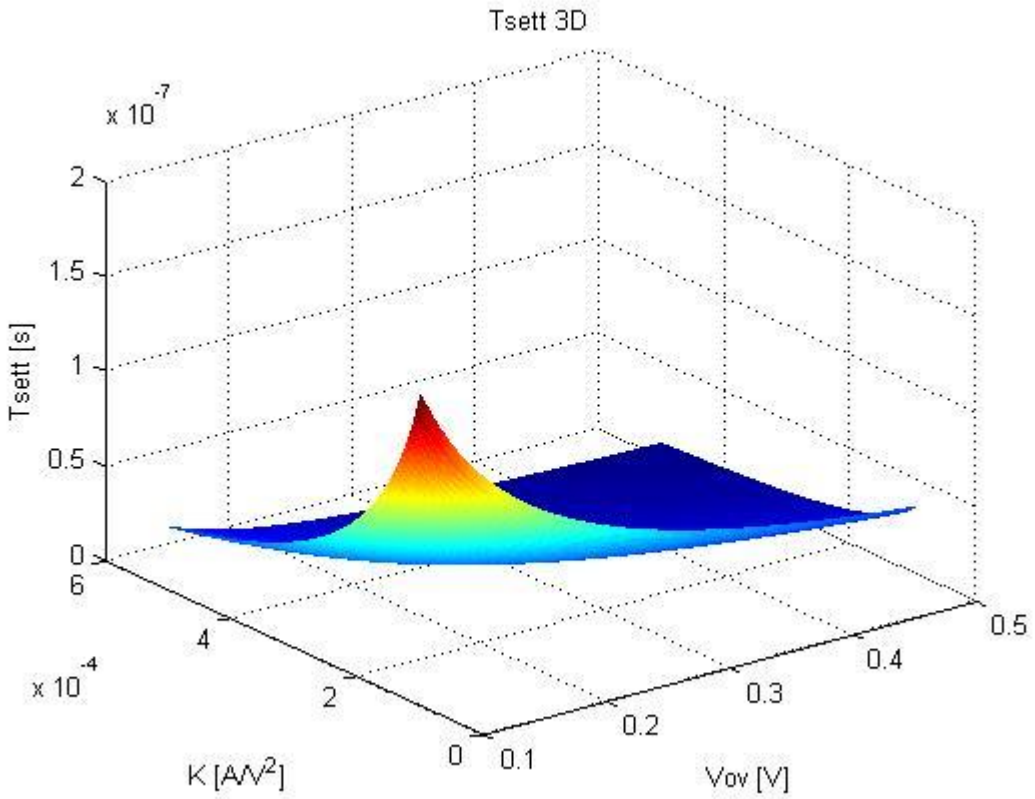


Fig.5. 24: Three-dimensional settling time graph as function of parameters *K* and Vov

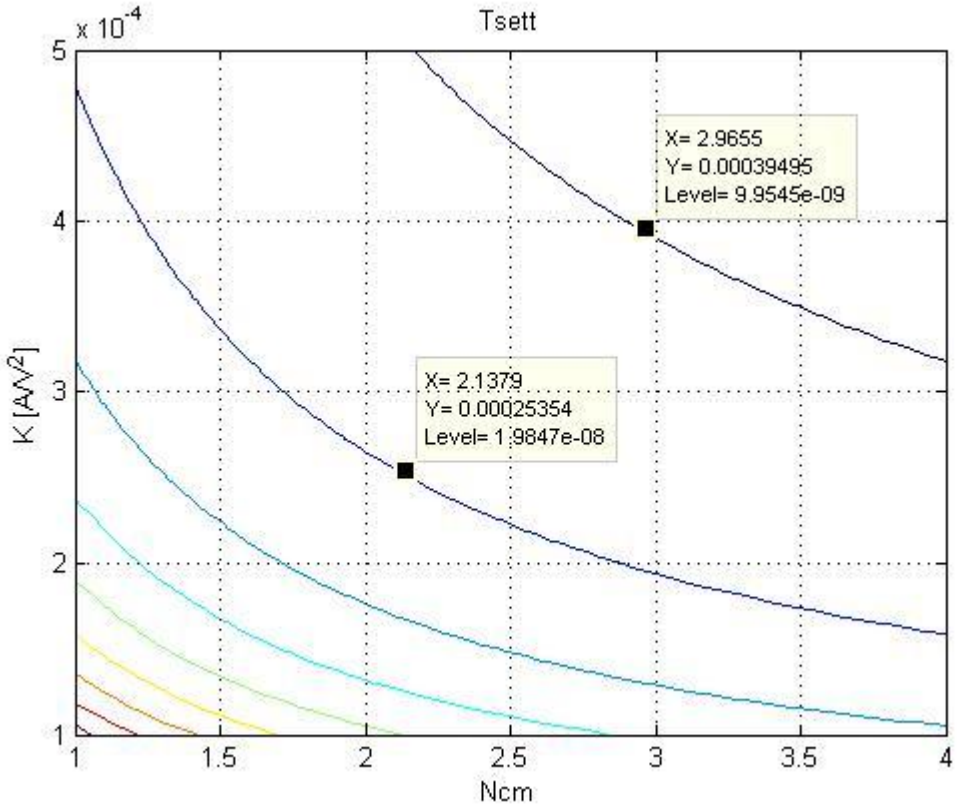


Fig.5. 25: Settling time level curves as function of parameters *K* and *Ncm*

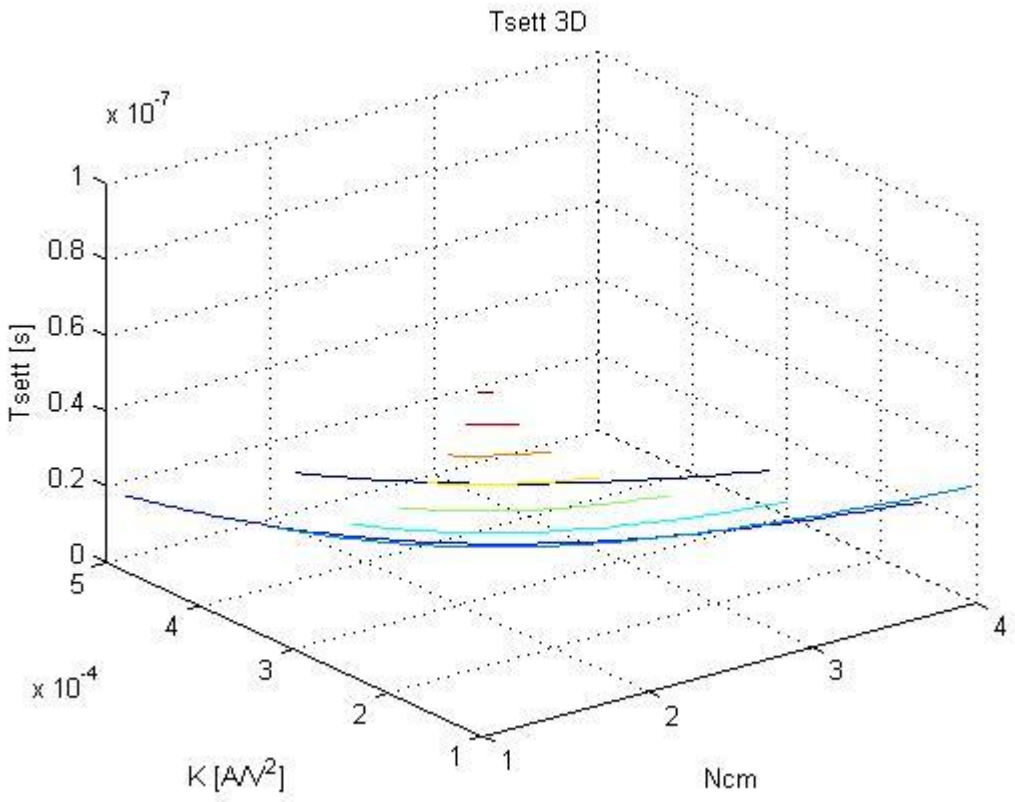


Fig.5. 26: Three-dimensional settling time level curves as function of parameters *K* and *Ncm*

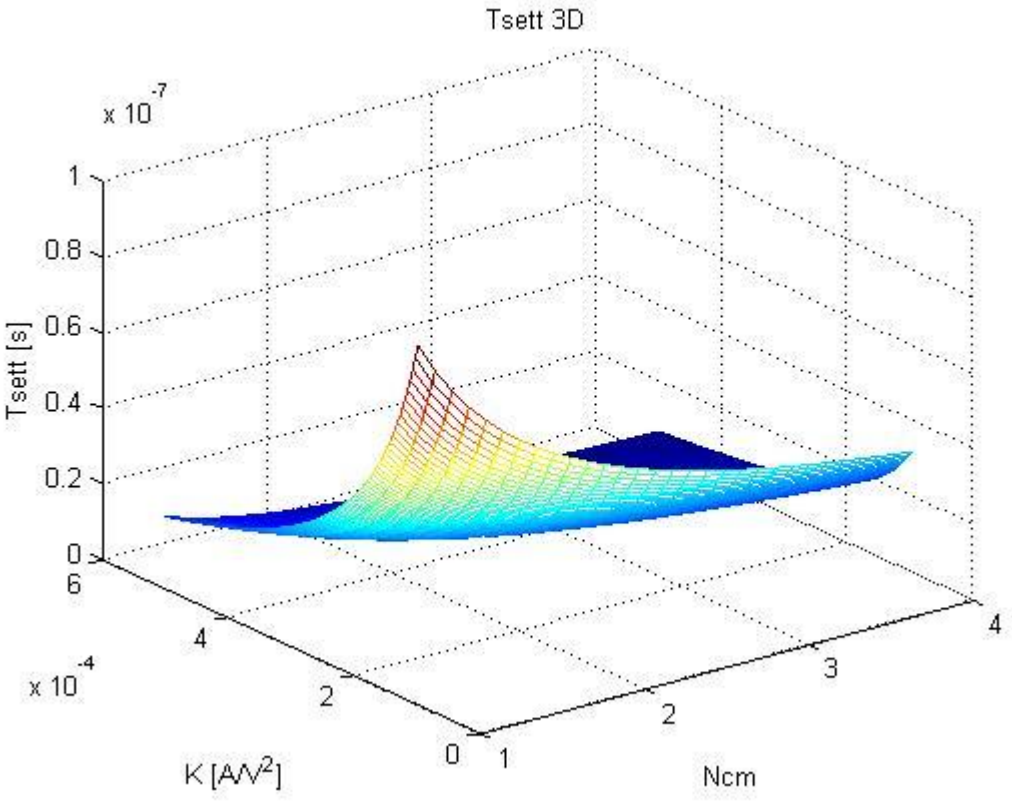


Fig.5. 27: Three-dimensional settling time graph as function of parameters *K* and *Ncm*

5.8 Energy dissipated during step response

Since the ultimate goal is to find the sizing that provides minimum consumption for a given settling time, it is also necessary to express the consumption according to the design parameters. To estimate consumption, consider the energy dissipated during step response

The energy dissipated during step response can be calculated as the difference between the energy supplied by the supply voltage and the energy stored by the capacitor.

$$E_{diss} = E_{alim} - E_{cond} \quad (5.63)$$

$$E_{cond} = \frac{1}{2} C_L (A_{VF} V_2)^2 - \frac{1}{2} C_L (A_{VF} V_1)^2 = \frac{1}{2} C_L A_{VF}^2 (V_2^2 - V_1^2) \quad (5.64)$$

$$E_{alim} = V_{DD} \int_0^{T_1} I_{TOT} dt + V_{DD} \int_0^{T_2} I_{TOT} dt \quad (5.65)$$

where, in general:

$$I_{TOT} = h_1 I_1 + h_2 I_2 + h_3 \quad (5.66)$$

The coefficients "$h_{1,2,3}$" take into account how the circuit is made (current mirrors, number of branches, bias current, etc.), so that they vary in general by, changing topology. For the circuit in Fig.5.3, and in the case of ascending step (so during t_1 I have only "I_1" and not "I_2"), I can write:

$$h_1 = 1 + N_{cm} \quad (5.67)$$

where, in simulation, *Ncm* represents the current mirror gain.

$$h_2 = 1 \quad (5.68)$$

$$h_3 = I_0 = 2I_b + \frac{V_{dd}}{4R} \quad (5.69)$$

where, I_0, in simulation, represents the static current.

$I_1 = K(V_{ovq} + V_{id})^2 \qquad V_{id} > -V_{ovq}$ (5.70)

$I_2 = K(V_{ovq} + V_{id})^2 \qquad V_{id} < V_{ovq}$ (5.71)

$V_{id} = V_{in} - V_o$, for t>0

in case of a positive step (V_2>V_1), I have

$E_{alim} = V_{DD} I_0 (T_1 + T_2) + V_{DD} \int_0^{T_1} h_1 I_1 dt + V_{DD} \int_0^{T_2} h_1 I_1 dt + V_{DD} \int_0^{T_2} h_2 I_2 dt$ (5.72)

$$\int_0^T I_1\, dt = K \int_0^T \left(V_{ovq} + V_2 - V_o\right)^2 dt = K \int_0^T (\Psi - V_o)^2 dt =$$

$$= \Psi^2 T - 2K\Psi \int_0^T V_o dt + K \int_0^T V_0^2\, dt \quad (5.73)$$

$$\int_0^T I_2\, dt = K \int_0^T \left(V_{ovq} - V_2 + V_o\right)^2 dt = K \int_0^T (V_o - \mathrm{V_o^*})^2 dt =$$

$$= K \int_0^T V_o^2\, dt - 2K\mathrm{V_o^*} \int_0^T V_o\, dt + KV_o^{*2} T \quad (5.74)$$

$J_{A1} = \int_0^T V_{oNL}\, dt$ (5.75)

$J_{A2} = \int_0^T V_{oNL}^2\, dt$ (5.76)

$J_{B1} = \int_0^T V_{oL}\, dt$ (5.77)

$J_{B2} = \int_0^T V_{oNL}^2\, dt$ (5.78)

where :

$V_{oNL} = \bar{V}_o \frac{\delta}{\delta c_1 e^{t/t_{NL}} - 1}$ (5.79)

and

$V_{oL} = A_{VF} V_2 - (A_{VF} V_2 - \mathrm{V_o^*})\mathrm{e}^{-\mathrm{t}/\tau}$ (5.80)

Alternatively, it is necessary to calculate it directly:

$J_1 = \int_0^T (\Psi - V_{oNL})^2\, dt = \int_0^T V_A^2\, dt$ (5.81)

$J_2 = \int_0^T (\Psi - V_{oL})^2\, dt = \int_0^T V_B^2\, dt$ (5.82)

$J_3 = \int_0^T (V_{oL} - \mathrm{V_o^*})^2\, dt = \int_0^T V_C^2\, dt$ (5.83)

$V_A = \Psi - \bar{V}_o + \frac{\delta}{\delta c_1 e^{t/t_{NL}} - 1} = (1-\gamma)\Psi + \frac{\delta}{\delta c_1 e^{t/\tau_{NL}} - 1}$ (5.84)

$V_B = (\Psi - A_{VF} V_2) + (A_{VF} V_2 - \mathrm{V_o^*})\mathrm{e}^{-\mathrm{t}/\tau}$ (5.85)

$V_C = (A_{VF} V_2 - \mathrm{V_o^*}) - (A_{VF} V_2 - \mathrm{V_o^*})\mathrm{e}^{-\mathrm{t}/\tau}$ (5.86)

is derived, (see Appendix C)

$f_a = \left(a + \frac{b}{ce^{dx} - 1}\right)^2$ (5.87)

$\int_0^x f_a dx = \frac{b^2/d}{1 - ce^{(dx)}} + (a-b)^2 x + \frac{b^2/d}{c-1} - \frac{b}{d}(2a-b)\ln(c-1) + \frac{b}{d}(2a-b)\ln(ce^{dx} - 1)$ (5.88)

$f_b = (a + ce^{-gx})^2$ (5.89)

$\int_0^x f_b dx = \frac{1}{2g}[c^2(1 - e^{2gx}) + 4ac(1 - e^{-gx}) + 2a^2 gx]$ (5.90)

$f_c = (a - ce^{-gx})^2$ (5.91)

$\int_0^x f_c dx = \frac{1}{2g}[c^2(1 - e^{2gx}) - 4ac(1 - e^{-gx}) + 2a^2 gx]$ (5.92)

replacing I get

$E_{alim} = V_{DD} h_1 K J_1(T_1) + V_{DD} h_1 K J_2(T_2) + V_{DD} h_2 K J_3(T_2) + V_{DD} I_o (T_1 + T_2)$ (5.93)

for the calculation of J_1:

$a = (1-\gamma)\Psi$ (5.94)

$b = \delta$ (5.95)

$c = \delta c_1$ (5.96)

$d = \frac{1}{\tau_{NL}}$ (5.97)

for J_2 calculation:

$a = \Psi - A_{VF} V_2$ (5.98)

$c = A_{VF} V_2 - V_o^*$ (5.99)

$g = \frac{1}{\tau}$ (5.100)

for J_3 calculation, I have $a = A_{VF} V_2 - V_o^* = c$.

In the case that $V_{id}(0) < V_{ovq}$ I have $T_1=0$, $J_1=0$, and for J_2 and J_3, I have:

$c = A_{VF} V_2 - V_0(0) = A_{VF}(V_2 - V_1)$ (5.101)

For what concerns small signal parameters, I have:

$A_V = 4KN_{cm} V_{ov} R = 4KV_{ov} R_0$ (5.102)

$R = \frac{R_0}{N_{cm}}$ (5.103)

$G_m = 4KV_{ov} N_{cm}$ (5.104)

$\omega_{3dB} = \frac{4KV_{ov} N_{cm}}{C_L} = \frac{G_m}{C_L}$ (5.105)

$I_Q = mKV_{ov}^2 = \frac{mA_V}{4R_0}$ (5.106)

where *m*, depends of the architecture.

5. 9 Energy curves as a function of *k* and Vov parameters

Similary to what has been done for settling-time estimation in function of pairs of parameters can be done in the case of energy. Fig.5.28 shows that the energy increases for *K* and Vov increasing values.

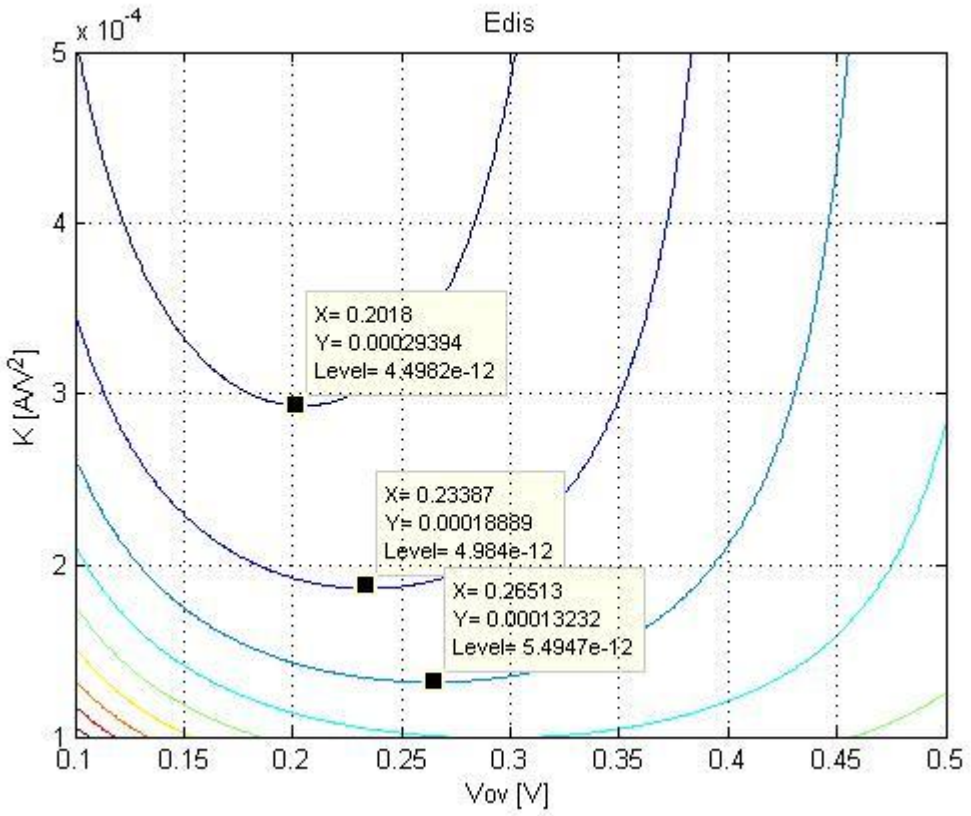


Fig.5. 28: Energy level curves as function of parameters *K* and Vov

Fig.5.29 shows the same results in a three dimensional graph where the highest curves represent higher values of dissipated energy. Fig.5.30 shows the same results with a three-dimensional graph. Fig.5.31 combines the results of Fig.5.22 and Fig.5.28, and so, given a certain settling time specification, I can choose *K* and Vov values in such a way to minimize power consumption.

Fig.5.32 represents the level curves in function of *K* and *Ncm* parameters. Fig.5.33 and Fig.5.34 represents the same results in a three-dimensional graph. Fig.5.35 combines the results of Fig.5.25 and Fig.5.32 and in this case I can choose *K* and *Ncm* values that minimize power consumption for a given settling time.

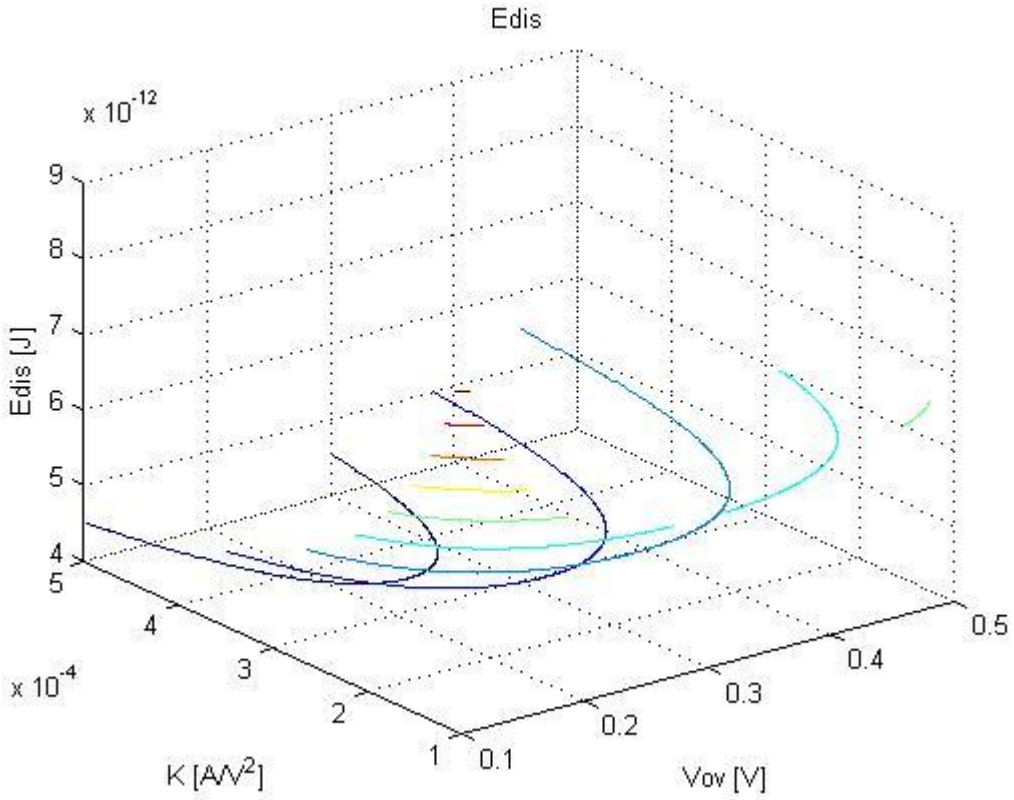


Fig.5. 29: Three-dimensional energy level curves as function of parameters *K* and Vov

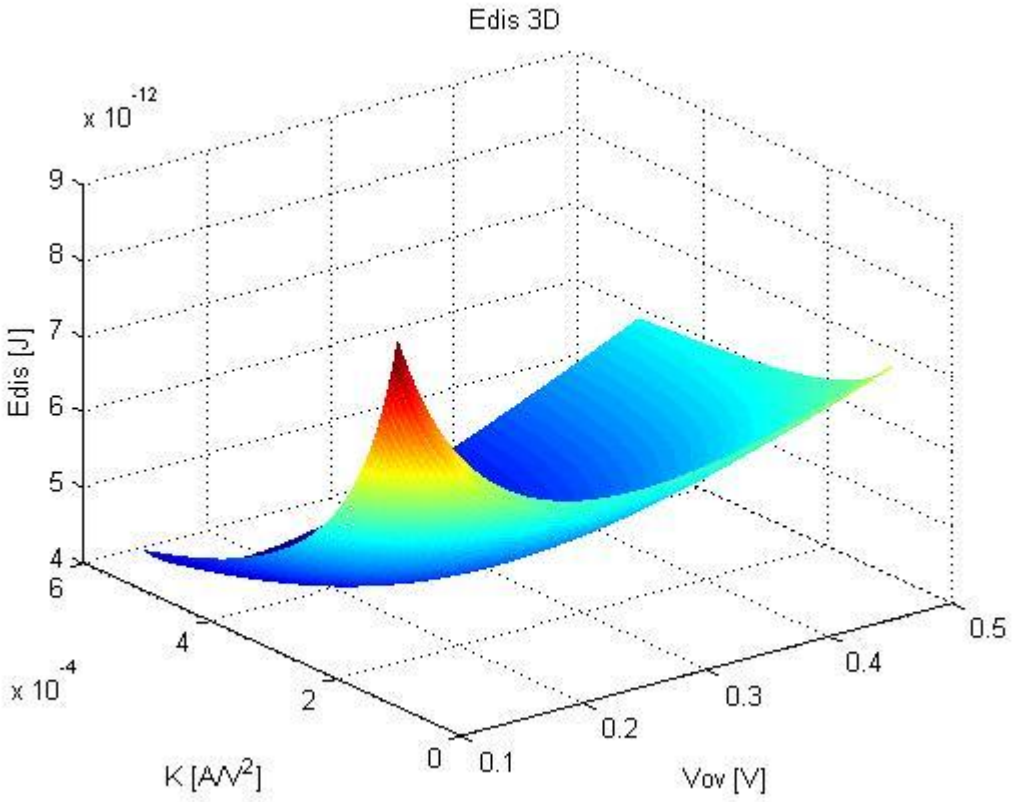


Fig.5. 30: Three-dimensional energy graph as function of parameters *K* and Vov

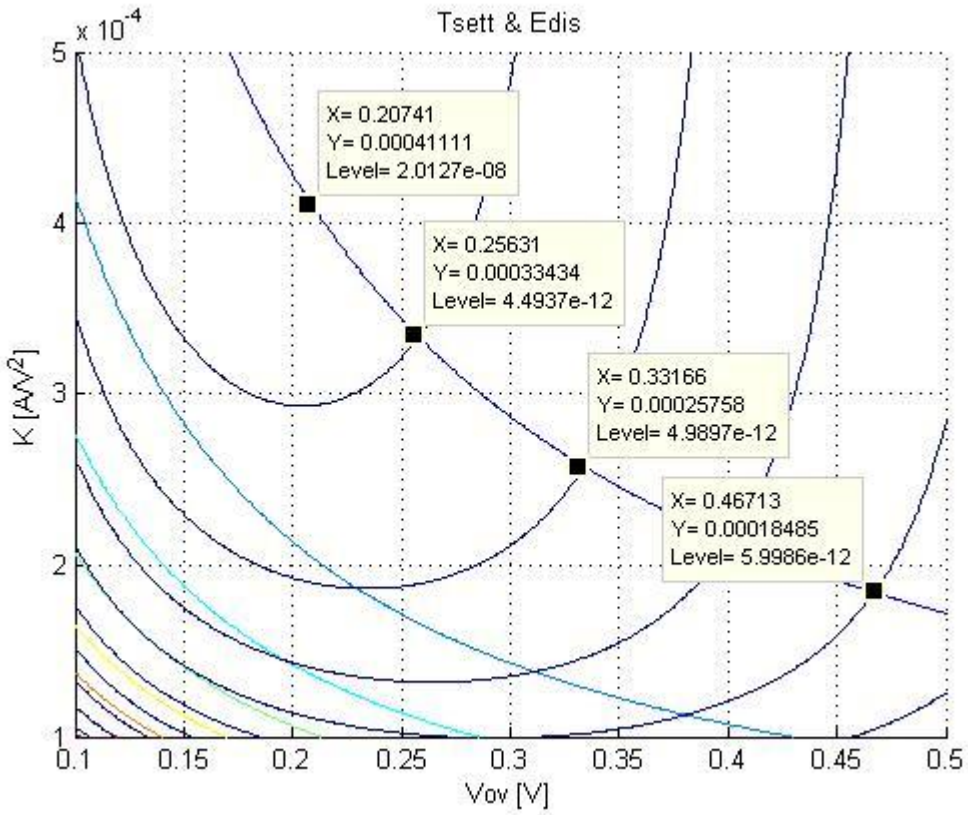


Fig.5. 31: Settling time level curves and energy level curves as function of parameters K and Vov

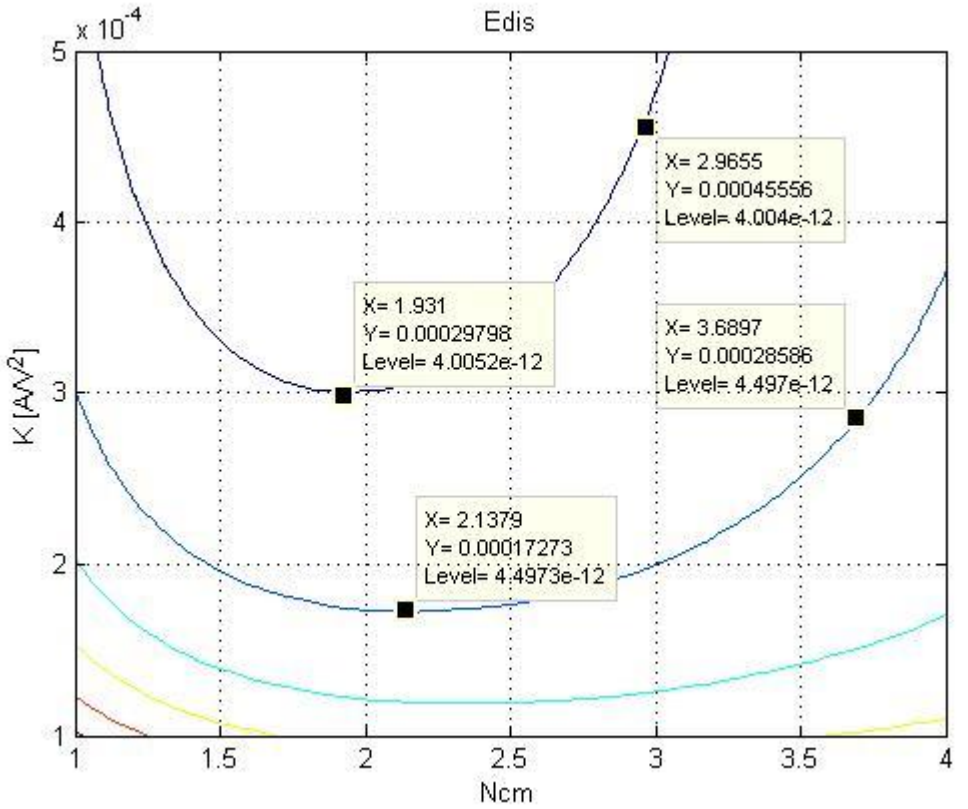


Fig.5. 32: Energy level curves as function of parameters *K* and *Ncm*

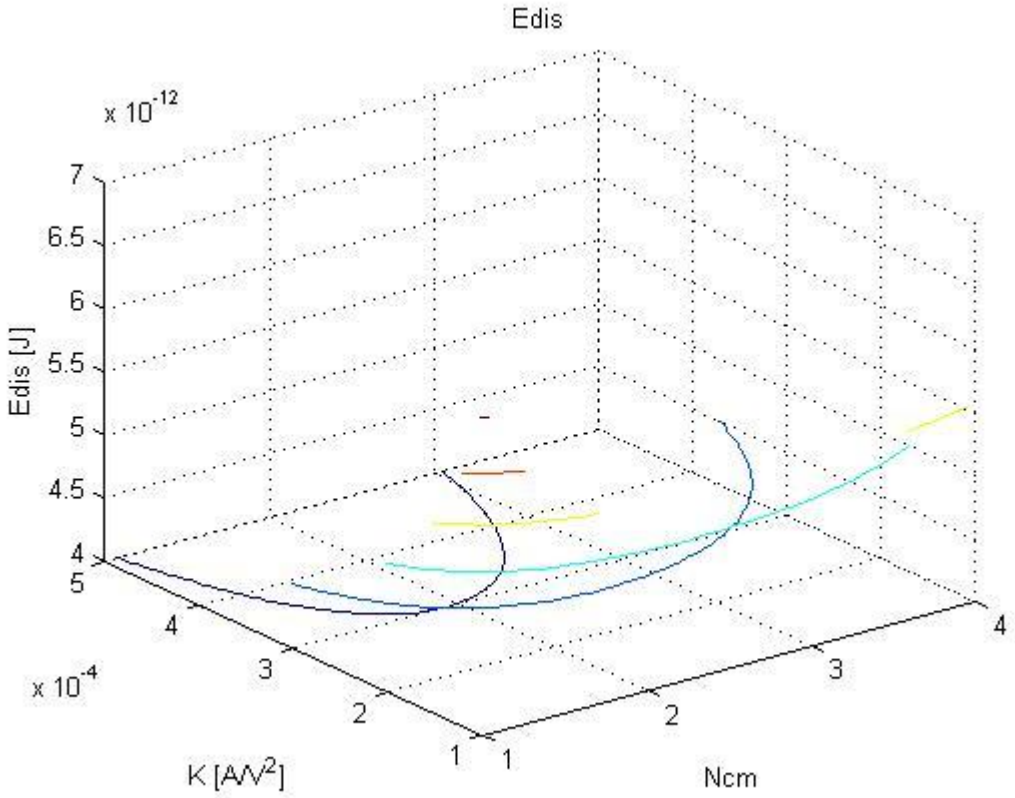


Fig.5. 33: Three-dimensional energy level curves as function of parameters *K* and *Ncm*

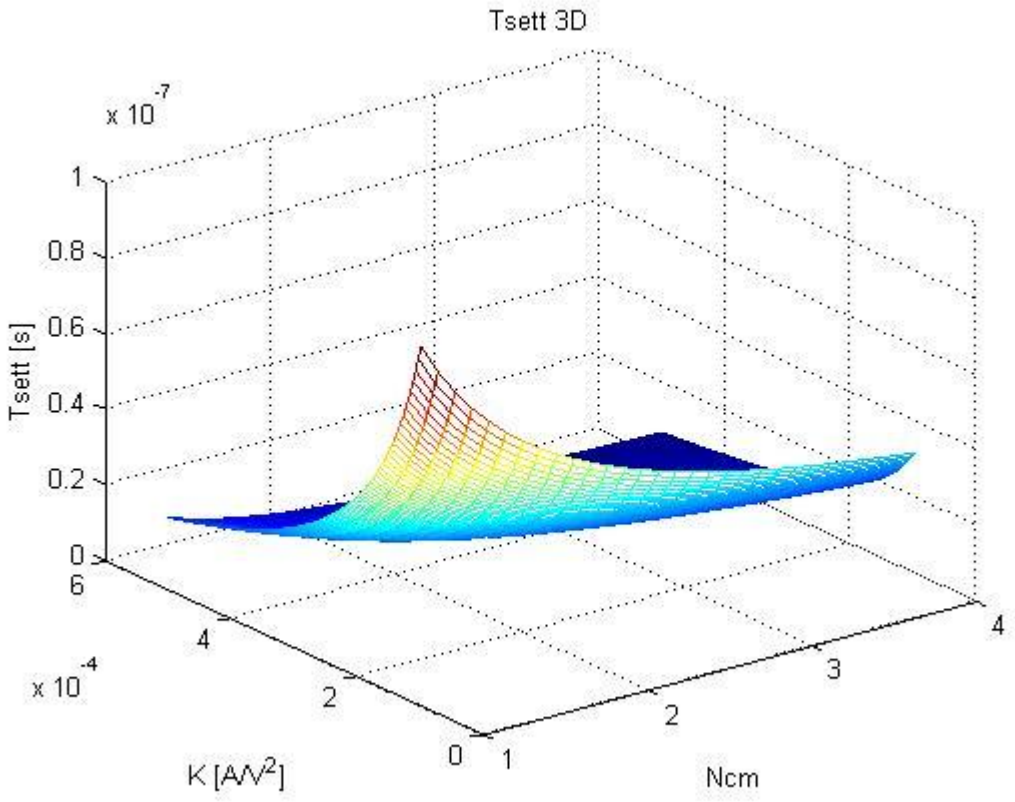


Fig.5. 34: Three-dimensional energy graph as function of parameters *K* and *Ncm*

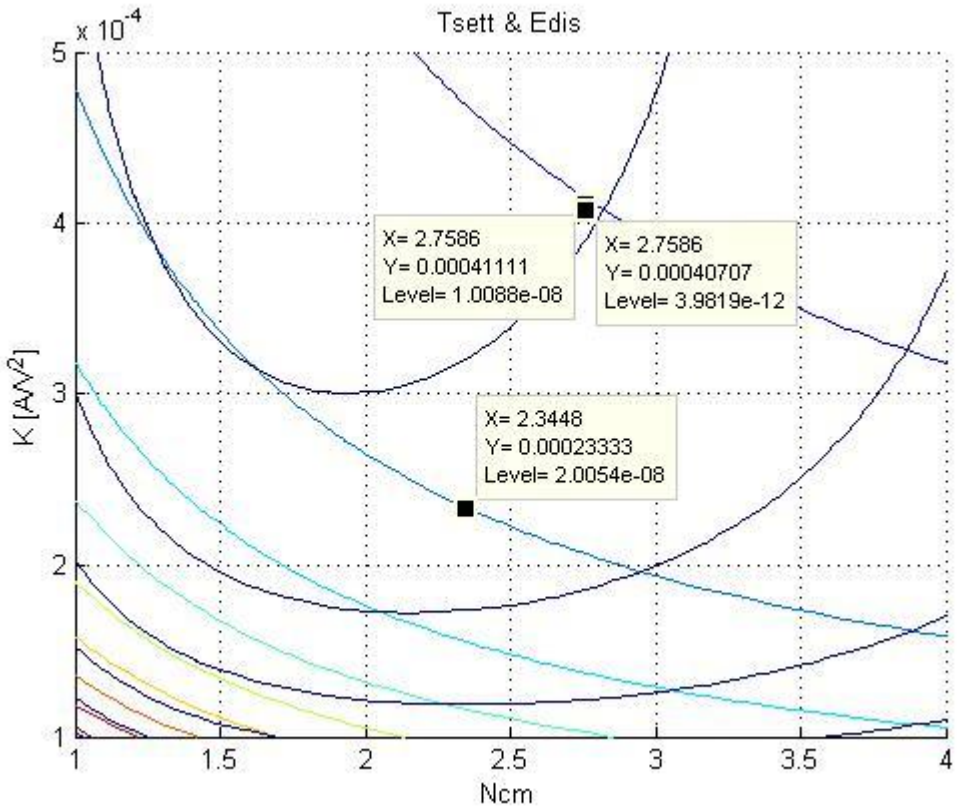


Fig.5. 35: Settling time level curves and energy level curves as function of parameters *K* and *Ncm*

Conclusions

During the Ph.D. I have addressed the issue of reducing consumption in the field of microelectronic design. I tried to make my contribution in this direction by addressing the OTA study in class AB. Such devices show the advantage of having little consumption in quiescent conditions and are not limited in terms of the current they can deliver to the load. As their field of use in electronic devices is wide, I have decided to narrow the scope of action by thinking of them for applications such as sample and hold amplifiers, A/D converters, and in general for devices where fast settling is required. Since such applications require devices that work in a completely different way, I have concentrated mainly on the study of fully differential topologies. However, the study of single-ended topologies has not been neglected since the latter, in general, can be transformed in a fully differential structure. Fully differential amplifiers in order to function properly require a CMFB that generally has an impact on energy consumption, so it must be carefully chosen.

For topologies covered in Chapter 3 I chose a CMFB that does not require additional power consumption since it can be integrated into the branches of the original structure and contains only devices operating in triode region.

This type of CMFB has been integrated into Peluso's topology as the first choice emerging from the state of the art (Chapter 2), making it preferable to other topologies considered for consumption, differential mode gain, bandwidth, and ability to deliver large current to the load. The only problem of Peluso's topology is the high common mode gain and consequently the low value of CMRR. In order to improve the CMRR of the structure and thus to make it the most powerful of the state of the art, I have proposed, in Chapter 3, new techniques. Such techniques have proved to be effective in improving the CMRR of the structure while leaving unaltered the other OTA performances, and have introduced small additional consumption. Specifically, two open loop techniques and one closed loop were proposed. All the three techniques turned out to be less robust under corner process variations, and I proposed a methodology that can be applied post-process to bring back performance to the nominal case. The topologies with performance improvement were then tested as Sample and Hold Amplifiers (SHA), generally achieving good performance.

Then I tested Peluso's topology for supply voltages below the 1 Volt, pushing it to 0.4V. The results obtained are promising because the topology continues to have good performance, and only maintains the same problem in terms of high common mode gain as shown at a 1.2 Volt supply voltage.

In Chapter 4 I proposed two topologies for voltages below 1 volt. In the first one I went down to 0.8V power supply and I used the body terminal of some devices to apply the control signal of an auto-referenced CMFB. The proposed method was shown to be valid by significantly improving the CMRR of the structure and also proved to be robust under corner process variations.

In the second one I went down to 0.6V supply voltage and went to consider the problems related to the input dynamics of a single ended output amplifier used in non-inverting configuration. Again starting from the Peluso topology, I proposed a circuit solution to improve the input dynamics of the amplifier. In order to implement the idea I proposed a FVF with MOS in triode added with respect to the classic configuration, the so-called 3 levels FVF (FVF3). The proposed technique was effective.

Along with the aim of reducing consumption, I passed to the Ramirez-Angulo topology, which in the original version provides an auxiliary block for generating the input common mode that in fact introduces additional consumption. In order to try to improve it from the point of view of consumption, I proposed a modification of the original structure by incorporating the block for generating the input common mode into the OTA structure. Again in this case, in order to make changes to the original structure, I used FVF at 3 levels.

In the last paragraph of chapter 4, always starting from Peluso topology, I showed how it is possible to derive a folded topology that has comparable performance with the state of the art.

From the studies carried out during the first year of PhD I noticed that in technical literature the information on how to design a class AB amplifier with the input differential transconductor that operate in class AB, was poor and fragmentary. From this ascertainment the idea came of trying to propose a model capable of responding to this need. In tackling new issues, generally, the most obvious thing is to start from simple case studies, and to complicate them later. That's exactly what I did.

The proposed model does not want to be a general, but it is a solution useful for all those topologies where the behavior of the differential input transconductor can be described with the same set of equations used to describe the proposed model.

In the last chapter, I proposed a model that allows me to link the settlig time to some project parameters such as: transconductance of the OTA/MOS, overdrive voltages (Vov), output resistance (R0) and gain of the current mirrors (Ncm).

In line with what I wrote earlier, I started the work from a simplified circuit model where the output is of a single ended type and that is based on the Peluso topology. In the simpler circuit model, the differential input transconductor is realized with FVFD exactly as in the original Peluso structure. The currents generated by the input differential transconductor are mirrored to the load by ideal current-controlled current sources. MOS output resistors have been modeled with ideal resistors, and the load capacitance has been left unchanged with respect to the original topology. The availability of such a circuit model requires to introduce simplifying hypotheses. In the simplified circuit model I neglect the poles that would be introduced by the real current mirrors so in fact i'm making the assumption of being single pole or limit in the case of dominant pole.

At analytical level, the equations describing the behavior of the input differential transistor currents were derived according to the parameters K and Vov. From the simplified circuit model and from the knowledge of the set of equations describing the current behavior of the OTA, I could add another level of abstraction to the circuit model. The circuit model I focused on in order to derive equations describing the behavior of the entire OTA has become a single time-constant (RC) parallel circuit with a current generator that models the current behavior of the input differential transconductor.

The equations found to describe the current behavior of the input differential transductor are of a quadratic type: therefore, the I/O devices provided by STMicroelectronics with 40nm production process have been chosen to validate the mathematical model. In order to find a way to estimate the parameter K that appears in the mathematical equations of the input differential transconductor, different approaches, described in chapter 4, were tried and to validate the model. Of the various ways I tried I chose one according to the criteria described in chapter 4 and I validated the model.

Future developments:

From a topological point of view, hybrid topologies with improved performance compared to individual starting structures could be derived from the topologies of Castello, Baswa, Ramirez-Angulo and Peluso .
From a theoretical point of view, a degree of complication can be added to the proposed model. In the simplified circuit model, real current mirrors can be added, which means that at least one second pole must be taken into account. By making the assumption that the mirrors introduce only one more pole, analytic equations become more complicate. Instead of managing a single Riccati differential equation, one needs to solve a system of differential equations of Riccati.

Papers list

Research efforts have resulted in 3 papers:

F. Centurelli, P. Monsurrò, G. Parisi, P. Tommasino, A. Trifiletti
'A Topology of Fully-Differential Class-AB Symmetrical OTA with improved CMRR'
IEEE Transactions on Circuits and Systems Part II: Express Briefs.

F. Centurelli, P. Monsurrò, G. Parisi, P. Tommasino, A. Trifiletti
'Fully differential class-AB OTA with improved CMRR'
Journal of Circuits Systems and Computers, vol. 26, n. 11, Nov. 2017, paper 1750169.

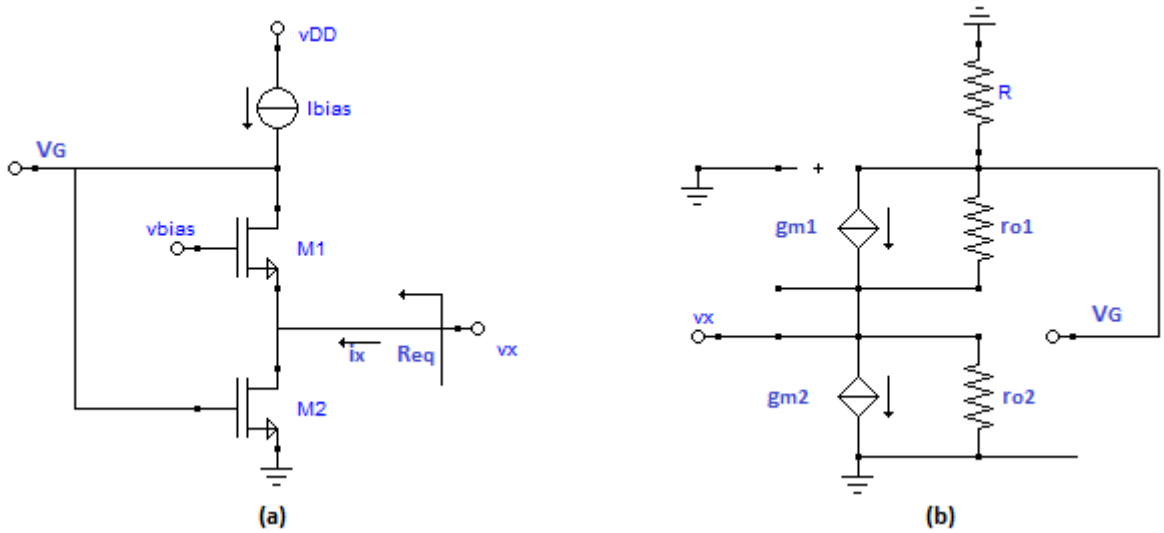
F. Centurelli, P. Monsurrò, G. Parisi, P. Tommasino, A. Trifiletti
'A fully-differential class-AB OTA with CMRR improved by local feedback'
ECCTD 17: 23rd European Conference on Circuit Theory and Design, Catania (Italy), 4 – 6 September 2017.

Appendix A

This appendix contains the accounts carried out to determine the results obtained in Chapter 2.

A.1 FVF small signal analysis

Here is the analysis of the Flipped Voltage Follower (FVF)



$$\begin{cases} i_x - g_{m1}v_x + \frac{V_G - v_x}{r_{o1}} = g_{m2}V_G + \frac{v_x}{r_{o2}} \\ \frac{V_G}{R} - g_{m1}v_x + \frac{V_G - v_x}{r_{o1}} = 0 \end{cases}$$

$$V_G(R + r_{o1}) = v_x(1 + g_{m1}r_{o1})R$$

$$\frac{i_x}{v_x}(R + r_{o1}) = (1 + g_{m1}r_{o1})(1 + g_{m2}R) + \frac{R + r_{o1}}{r_{o2}}$$

$$\frac{i_x}{v_x} = \frac{1}{R_{eq}} = \frac{(1+g_{m1}r_{o1})(1+g_{m2}R)}{(R+r_{o1})} + \frac{R+r_{o1}}{(R+r_{o1})r_{o2}} = \frac{(1+g_{m1}r_{o1})(1+g_{m2}R)}{(R+r_{o1})} + \frac{1}{r_{o2}}$$

$$\frac{i_x}{v_x} = \frac{1}{R_{eq}} = \frac{(1+g_{m1}r_{o1})(1+g_{m2}R)}{(R+r_{o1})} + \frac{1}{r_{o2}} \cong g_{m1}g_{m2}(r_{o1}//R)$$

$$R_{eq} = \frac{r_{o2}(R+r_{o1})}{r_{o1}+R+r_{o2}(1+g_{m1}r_{o1})(1+g_{m2}R)} = \frac{r_{o2}(R+r_{o1})}{D}$$

$$D = r_{o1} + R + r_{o2}(1 + g_{m1}r_{o1})(1 + g_{m2}R)$$

$$V_G(R + r_{o1}) = R(1 + g_{m1}r_{o1})R_{eq}i_x$$

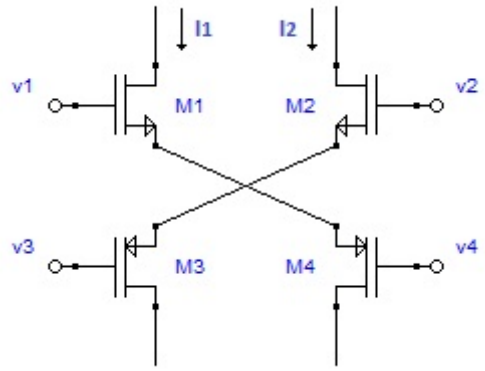
$$V_G = \frac{R(1+g_{m1}r_{o1})R_{eq}i_x}{(R+r_{o1})} = \frac{R(1+g_{m1}r_{o1})i_x}{(R+r_{o1})}\frac{r_{o2}(R+r_{o1})}{D} = \frac{R(1+g_{m1}r_{o1})r_{o2}i_x}{D}$$

$$r_{o2} = D\frac{R_{eq}}{(R+r_{o1})}$$

Replace r_{o2} in the V_G equation:

$$V_G = i_x\frac{r_{o2}(1+g_{m1}r_{o1})R}{D} = i_x D\frac{R_{eq}}{(R+r_{o1})}\frac{(1+g_{m1}r_{o1})R}{D} = i_x\frac{R_{eq}(1+g_{m1}r_{o1})R}{(R+r_{o1})}$$

A.2 Analysis of the class AB input stage based on the cross pair



$v_1 = v_{bn} + v_{id}/2$
$v_2 = v_{bn} - v_{id}/2$
$v_3 = v_{bp} + v_{id}/2$
$v_4 = v_{bp} - v_{id}/2$
Bias point
$k_n(v_{bn} - v_s - v_{Tn})^2 = k_p(v_s - v_{bp} - |v_{Tp}|)^2$
$\sqrt{k_n}(v_{bn} - v_s - v_{Tn}) = \sqrt{k_p}(v_s - v_{bp} - |v_{Tp}|)$
$v_s = \frac{\sqrt{k_n}(v_{bn} - v_{Tn}) + \sqrt{k_p}(v_{bp} + |v_{Tp}|)}{\sqrt{k_n} + \sqrt{k_p}} = v_{so}$
$I_{dc} = k_n(v_{bn} - v_s - v_{Tn})^2 = k_n(v_{bn} - \frac{\sqrt{k_n}(v_{bn} - v_{Tn}) + \sqrt{k_p}(v_{bp} + |v_{Tp}|)}{\sqrt{k_n} + \sqrt{k_p}} - v_{Tn})^2$
$I_{dc} = k_n(\frac{v_{bn}(\sqrt{k_n} + \sqrt{k_p}) - (\sqrt{k_n}(v_{bn} - v_{Tn}) + \sqrt{k_p}(v_{bp} + |v_{Tp}|)) - v_{Tn}(\sqrt{k_n} + \sqrt{k_p})}{(\sqrt{k_n} + \sqrt{k_p})})^2$
$I_{dc} = \left(\frac{\sqrt{k_n}}{\sqrt{k_n} + \sqrt{k_p}}\right)^2 (v_{bn}(\sqrt{k_n} + \sqrt{k_p}) - \sqrt{k_n}(v_{bn} - v_{Tn}) - \sqrt{k_p}(v_{bp} + |v_{Tp}|) - v_{Tn}(\sqrt{k_n} +$
kp))2
$I_{dc} = \left(\frac{\sqrt{k_n}}{\sqrt{k_n} + \sqrt{k_p}}\right)^2 (\sqrt{k_p}v_{bn} - \sqrt{k_p}(v_{bp} + |v_{Tp}|) - v_{Tn}\sqrt{k_p})^2$
$I_{dc} = \left(\frac{\sqrt{k_n}\sqrt{k_p}}{\sqrt{k_n} + \sqrt{k_p}}\right)^2 (v_{bn} - v_{bp} - |v_{Tp}| - v_{Tn})^2$
$\Delta = v_{bn} - v_{bp}$
$\theta = v_{Tn} + |v_{Tp}|$
$I_{dc} = k_n(v_{bn} - v_s - v_{Tn})^2 = \left(\frac{\sqrt{k_n}\sqrt{k_p}}{\sqrt{k_n} + \sqrt{k_p}}\right)^2 (v_{bn} - v_{bp} - |v_{Tp}| - v_{Tn})^2$
$I_{dc} = k_{eff}(\Delta - \theta)$

$k_{eff} = \left(\frac{\sqrt{k_n}\sqrt{k_p}}{\sqrt{k_n}+\sqrt{k_p}}\right)^2$

Signal:

$I_{1n} = k_n(v_1 - v_{s1} - v_{Tn})^2$

$I_{1p} = k_p(v_{s1} - v_4 - |v_{Tp}|)^2$

$I_{2n} = k_n(v_2 - v_{s2} - v_{Tn})^2$

$I_{2p} = k_p(v_{s2} - v_3 - |v_{Tp}|)^2$

$I_{1n} = I_{2n}$

$I_{1p} = I_{2p}$

$v_{s1,2} = v_{so} \pm \frac{\sqrt{k_n}-\sqrt{k_p}}{\sqrt{k_n}+\sqrt{k_p}}\frac{v_{id}}{2}$, until all the MOS devices are in saturation region

$v_{GS2} = v_{bn} - \frac{v_{id}}{2} - v_{s2} = v_{Tn}$

$v_{GS2} = v_{bn} - \frac{v_{id}}{2} - v_{s2} = v_{Tn}$

$v_{id} = 2(v_{bn} - v_{Tn} - v_{s2})$

$v_{id}{}^{(n)} = \frac{\sqrt{k_n}+\sqrt{k_p}}{\sqrt{k_p}}(v_{bn} - v_{Tn} - v_{so}) = \Delta - \theta$

$v_{SG2} = v_{s2} - v_{bp} - \frac{v_{id}}{2} = |v_{Tp}|$

$v_{id}{}^{(p)} = \frac{\sqrt{k_n}+\sqrt{k_p}}{\sqrt{k_n}}(v_{so} - v_{bp} - |v_{Tp}|) = \Delta - \theta$

For |vid|< Δ-θ :

$v_{bn} - v_{bp} + v_{id} = v_{Tn} + \sqrt{\frac{I_1}{k_n}} + |v_{Tp}| + \sqrt{\frac{I_1}{k_p}}$

$\sqrt{I_1}\left(\sqrt{\frac{1}{k_n}} + \sqrt{\frac{1}{k_p}}\right) = \Delta - \theta + v_{id}$

$I_{1,2} = k_{eff}(\Delta - \theta \pm v_{id})^2$

$I_1 - I_2 = k_{eff}4(\Delta - \theta)v_{id}$

Per |vid|> Δ-θ :

$I_1 = 0$ o $I_2 = 0$

Saturation limits:

$v_{Dn1} - v_{s1} = v_{bn} + \frac{v_{id}}{2} - v_{s1} - v_{Tn} \rightarrow \frac{v_{id}}{2} = v_{Dn1} - v_{bn} + v_{Tn}$

$v_{s1} - v_{Dp} = v_{s1} - v_{bp} + \frac{v_{id}}{2} - |v_{Tp}| \rightarrow \frac{v_{id}}{2} = v_{bp} - v_{Dp} + |v_{Tp}|$

Common mode input:

$v_{s1} = v_{so} + \frac{\sqrt{k_n}v_1+\sqrt{k_p}v_2}{\sqrt{k_n}+\sqrt{k_p}}$

$v_{s2} = v_{so} + \frac{\sqrt{k_n}v_2+\sqrt{k_p}v_1}{\sqrt{k_n}+\sqrt{k_p}}$

$v_1 = v_2 = v_{ic}$ $v_{s1} = v_{s2} = v_{so} + v_{ic}$

Differential mode input

$v_1 = -v_2 = \frac{v_{id}}{2}$

$I_1 = k_n(v_{bn} + v_1 - v_{s1} - v_{Tn})^2$

Per $v_{bn} + v_1 - v_{s1} - v_{Tn} > 0 \rightarrow v_1 - v_2 > -(\Delta - \theta)$

$I_2 = k_n(v_{bn} + v_2 - v_{s2} - v_{Tn})^2$

For $v_{bn} + v_2 - v_{s2} - v_{Tn} > 0 \rightarrow v_1 - v_2 < (\Delta - \theta)$

$|v_1 - v_2| < (\Delta - \theta)$

$I_{od} = I_1 - I_2 = 4k_{eff}(\Delta - \theta)v_{id}$

$I_{oc} = \frac{I_1 + I_2}{2} = k_{eff}[(\Delta - \theta)^2 + {v_{id}}^2]$

$v_1 - v_2 > -(\Delta - \theta)$

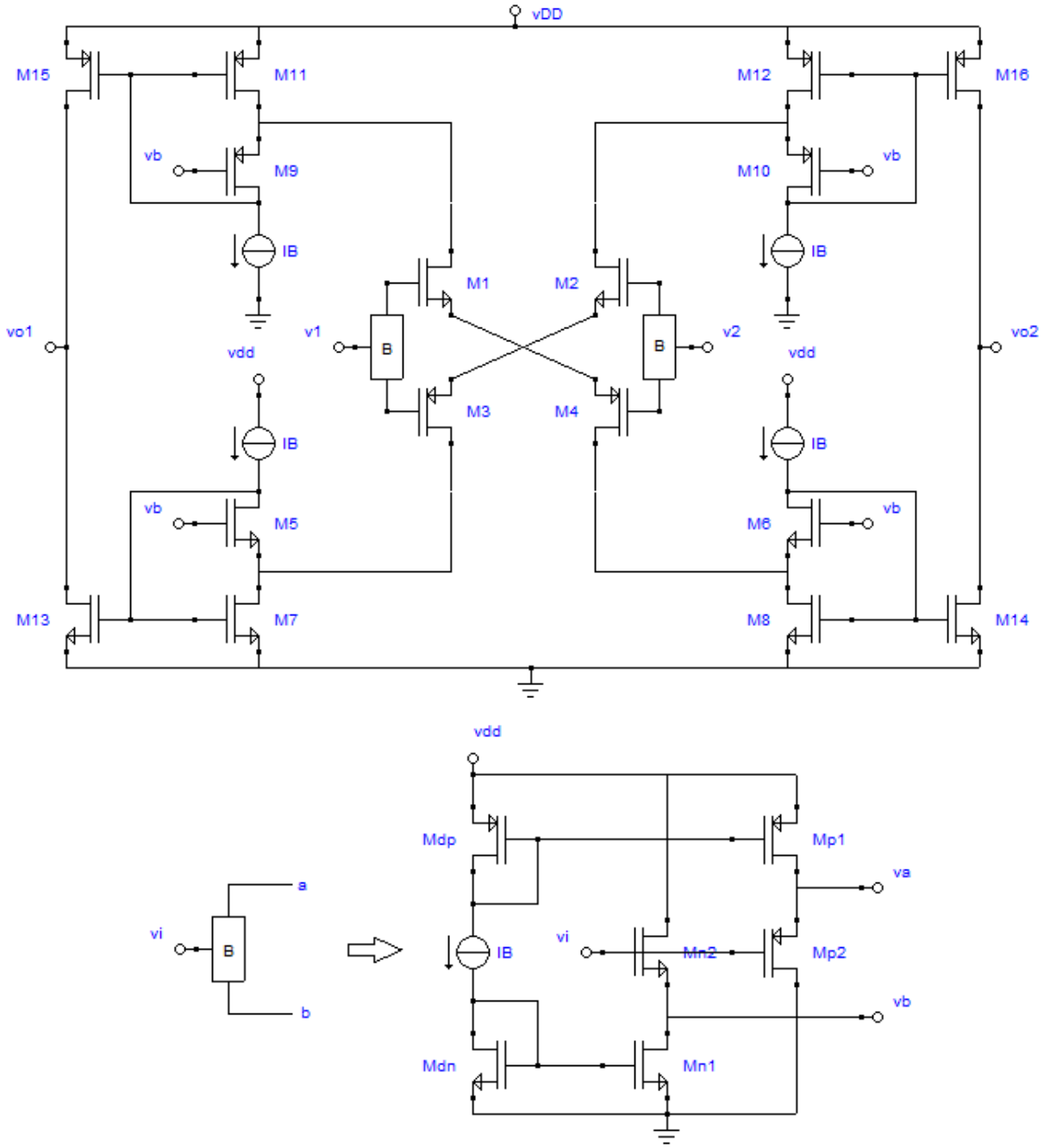
$I_2 = 0$

$I_1 = k_n(v_{bn} + v_1 - v_{s1} - v_{Tn})^2 = k_{eff}(\Delta - \theta + v_{id})^2$

$I_{od} = I_1$

$I_{oc} = \frac{I_1}{2}$

A.3 Cross-coupled class AB input stage (Castello 85)



Bias point

$I_1 = I_2 = I_3 = I_4 = I_x$, fixed by level shifter

$I_5 = I_6 = I_9 = I_{10} = I_B$

$I_{11} = I_{12} = I_7 = I_8 = I_B + I_x$

$I_{13} = I_{14} = I_{15} = I_{16} = k(I_B + I_x)$

$I_{QTOT} = [4I_B + I_x + k(I_B + I_x)]2 + I_{cmfb} + I_{ref\ buf})$

$I_{QOUT} = k(I_B + I_x)$

In detail:

$DP \qquad I_{Tail} = 2I_x$

$OUT \qquad I_{out} = 2k(I_B + I_x)$

$BUF \qquad I_{BUF} = \beta I_B \qquad \beta = 2$

$AUX \qquad I_{aux} = \alpha I_B \qquad \alpha = 2 \qquad Buf\ In \qquad I_{BI} = 4I_B$

$CMFB \qquad I_{cmfb} = \gamma I_{Tail}$

$F_c = \frac{k(I_B+I_x)}{4I_B+I_x+k(I_B+I_x)+\gamma I_B} = \frac{2k}{5+2k+\gamma} \qquad (I_x = I_B)$

Large signal

$I_2 = 0 \qquad I_1 = I_{1max}$

$I_{LOADmax} = kI_{1max}$

$I_{1max} = k_{eff}(v_{idmax} + \Delta - \theta)^2$

$k_{eff} = \left(\frac{\sqrt{k_n}\sqrt{k_p}}{\sqrt{k_n}+\sqrt{k_p}}\right)^2$

$\Delta = v_{bn} - v_{bp}$

$\theta = v_{Tn} + |v_{Tp}|$

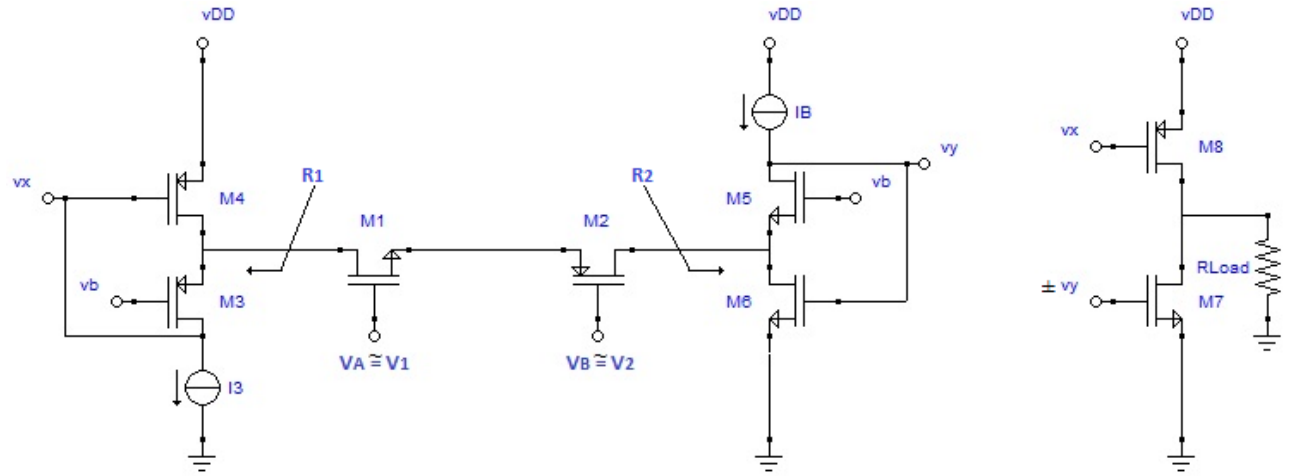
$I_x = k_{eff}(\Delta - \theta)^2$

$\Delta - \theta = \sqrt{\frac{I_x}{k_{eff}}}$

For $v_{dcin} = V_{DD}/2$, $v_{ic} = 0$, $v_{idmax} = V_{DD} - \frac{\Delta}{2}$

$F_{SR} = \frac{k_{eff}\left(V_{DD}-\frac{\Delta}{2}+\sqrt{\frac{I_x}{k_{eff}}}\right)^2}{4I_B} = \frac{k_{eff}\left(V_{DD}+\frac{\Delta}{2}-\theta\right)^2}{4I_B}$

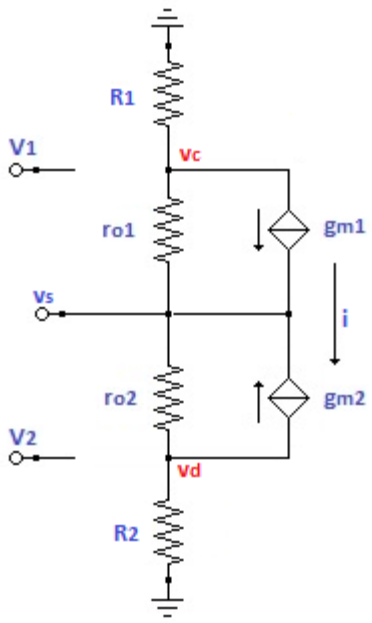
Small signal analysis



$v_x = f(v_c)$

$v_y = f(v_d)$

$$\begin{cases} v_c = -R_1 i \\ v_d = R_2 i \\ i = g_{m1}(v_1 - v_s) + \frac{v_c - v_s}{r_{o1}} \\ i = \frac{v_s - v_d}{r_{o2}} - g_{m2}(v_2 - v_s) \end{cases}$$



$$\begin{cases} v_c\left(\frac{1}{r_{o1}} + \frac{1}{R_1}\right) = -g_{m1}v_1 + v_s\left(g_{m1} + \frac{1}{r_{o1}}\right) \\ v_d\left(\frac{1}{r_{o2}} + \frac{1}{R_2}\right) = -g_{m2}v_2 + v_s\left(g_{m2} + \frac{1}{r_{o2}}\right) \\ g_{m1}v_1 + g_{m2}v_2 - v_s\left(g_{m1} + g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right) + \frac{v_c}{r_{o1}} + \frac{v_d}{r_{o2}} = 0 \end{cases}$$

$$\frac{g_{m1}}{R_1}\left(\frac{1}{r_{o2}} + \frac{1}{R_2}\right)v_1 + \frac{g_{m2}}{R_2}\left(\frac{1}{r_{o1}} + \frac{1}{R_1}\right)v_2 =$$

$$= v_s\left[\frac{1}{R_1}\left(g_{m1} + \frac{1}{r_{o1}}\right)\left(\frac{1}{r_{o2}} + \frac{1}{R_2}\right) + \left(g_{m2} + \frac{1}{r_{o2}}\right)\left(\frac{1}{r_{o1}} + \frac{1}{R_1}\right)\frac{1}{R_2}\right]$$

$$v_1(r_{o2} + R_2)g_{m1}r_{o1} + v_2(r_{o1} + R_1)g_{m2}r_{o2} = v_s[(1 + g_{m1}r_{o1})(r_{o2} + R_2) + (1 + g_{m2}r_{o2})(r_{o1} + R1]$$

$$v_c = \frac{R_1}{D}[g_{m1}r_{o1}(1 + g_{m2}r_{o2})v_1 - g_{m2}r_{o2}(1 + g_{m1}r_{o1})v_2$$

$$D = (1 + g_{m1}r_{o1})(r_{o2} + R_2) + (1 + g_{m2}r_{o2})(r_{o1} + R_1)$$

$$\eta = g_{m1}r_{o1}(1 + g_{m2}r_{o2})v_1 - g_{m2}r_{o2}(1 + g_{m1}r_{o1})v_2$$

$$v_c = -\frac{R_1}{D}\eta$$

$$v_d = -\frac{R_2}{D}\eta$$

$$i = \frac{\eta}{D}$$

$$R_1 = \frac{r_{o4}(r_{o3} + R)}{\delta_1}$$

$$R_2 = \frac{r_{o6}(r_{o5} + R)}{\delta_2}$$

$$\delta_1 = (r_{o3} + R) + r_{o4}(1 + g_{m3}r_{o3})(1 + g_{m4}R)$$

$$\delta_2 = (r_{o5} + R) + r_{o6}(1 + g_{m5}r_{o5})(1 + g_{m6}R)$$
$$v_x = -i\frac{(1+g_{m3}r_{o3})r_{o4}R}{\delta_1}$$
$$v_x = i\frac{(1+g_{m5}r_{o5})r_{o6}R}{\delta_2}$$

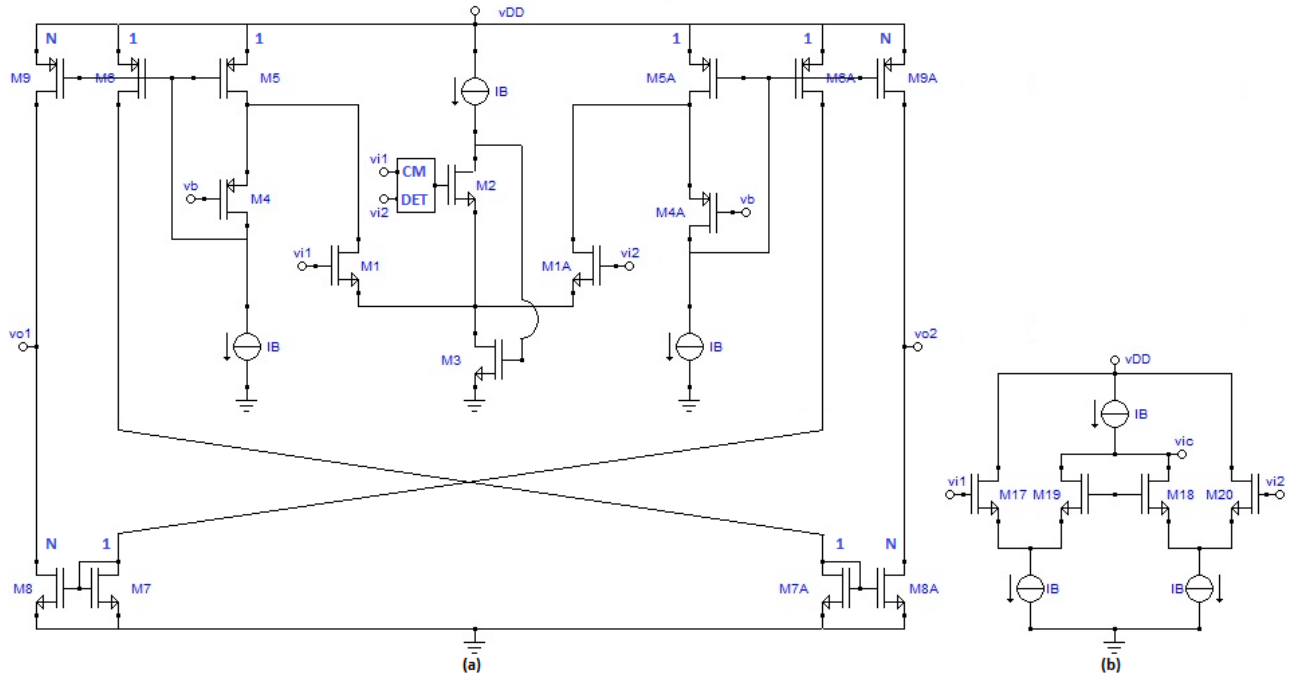
Differential Mode

$$v_1 = -v_2 = \frac{v_{id}}{2}$$
$$v_o = R_{Load}\left(g_{m8}v_x - g_{m7}v_y\right) = +R_{Load}G_D\frac{v_{id}}{2}$$
$$G_D = g_{m7}\frac{(1+g_{m5}r_{o5})r_{o6}R}{\delta_2} + g_{m8}\frac{(1+g_{m3}r_{o3})r_{o4}R}{\delta_1}\frac{\eta}{D}\frac{2}{v_{id}}$$
$$D = \frac{D_A}{\delta_1\delta_2}$$
$$D_A = (1 + g_{m1}r_{o1})[r_{o2}\delta_2 + r_{o6}(r_{o5} + R)] + (1 + g_{m2}r_{o2})[r_{o1}\delta_1 + r_{o4}(r_{o3} + R)] =$$
$$D_A = (1 + g_{m1}r_{o1})[(r_{o5} + R)(r_{o2} + r_{o6}) + r_{o6}(1 + g_{m5}r_{o5})(1 + g_{m6}R)] + (1 + g_{m2}r_{o2})[(r_{o3} +$$
Rro1+ro4+ro4(1+gm3ro3)(1+gm4R)
$$\eta_D = (g_{m1}r_{o1} + g_{m2}r_{o2} + 2g_{m1}r_{o1}g_{m2}r_{o2})\frac{v_{id}}{2} = \lambda\frac{v_{id}}{2}$$
$$G_D = \frac{\lambda}{D_A}\delta_1\delta_2\frac{N_D}{\delta_1\delta_2} = \frac{\lambda N_D}{D_A}$$
$$N_D = g_{m7}r_{o6}(1 + g_{m5}r_{o5})\delta_1 R + g_{m8}r_{o4}(1 + g_{m3}r_{o3})\delta_2 R$$

Common Mode

$$v_1 = v_2 = v_{ic}$$
$$v_o = -R_{Load}\left(g_{m8}v_x + g_{m7}v_y\right) = R_{Load}G_c v_{ic}$$
$$G_c = [g_{m8}\frac{(1+g_{m3}r_{o3})r_{o4}R}{\delta_1} - g_{m7}\frac{(1+g_{m5}r_{o5})r_{o6}R}{\delta_2}]\frac{\lambda\delta_1\delta_2}{D_A}\frac{1}{v_{ic}}$$
$$\eta = \eta_c = (g_{m1}r_{o1} - g_{m2}r_{o2})v_{ic} = \mu v_{ic}$$
$$G_c = \frac{\mu}{D_A}N_c$$
$$N_c = g_{m8}r_{o4}(1 + g_{m3}r_{o3})\delta_2 R - g_{m7}r_{o6}(1 + g_{m5}r_{o5})\delta_1 R$$
$$CMRR = \frac{G_D}{2G_c} = \frac{1}{2}\frac{\lambda N_D}{\mu N_c} = \frac{N_D}{N_c}CMRR_i$$
$$\lambda \cong 2g_{m1}r_{o1}g_{m2}r_{o2}$$
$$\mu = g_{m1}r_{o1} - g_{m2}r_{o2}$$
$$CMRR_i = \frac{\lambda}{\mu} \cong \frac{g_{m1}r_{o1}g_{m2}r_{o2}}{g_{m1}r_{o1} - g_{m2}r_{o2}} = \frac{1}{\frac{1}{g_{m2}r_{o2}} - \frac{1}{g_{m1}r_{o1}}}$$
$$N_D = g_{m3}r_{o3}g_{m5}r_{o5}r_{o4}r_{o6}R(g_{m8}g_{m6}) + (g_{m7}g_{m4})$$
$$N_c = g_{m3}r_{o3}g_{m5}r_{o5}r_{o4}r_{o6}R(g_{m8}g_{m6}) - (g_{m7}g_{m4})$$
$$CMRR \cong \frac{(g_{m8}g_{m6}) + (g_{m7}g_{m4})}{(g_{m8}g_{m6}) - (g_{m7}g_{m4})}\frac{1}{\frac{1}{g_{m2}r_{o2}} - \frac{1}{g_{m1}r_{o1}}}$$

A.4 Class AB input stage based on FVF (Ramirez-Angulo)



Bias point

$I_1 = I_2 = I_3$

$I_4 = 3I_1$

then $I_4 = 3I_B$

$I_{TAIL} = 2I_B$

$I_5 = I_6 = I_7 = I_8 = I_B$

$I_{11} = I_{12} = kI_B$

$I_{13} = I_{14} = I_{15} = I_{16} = k(I_B + I_x)$

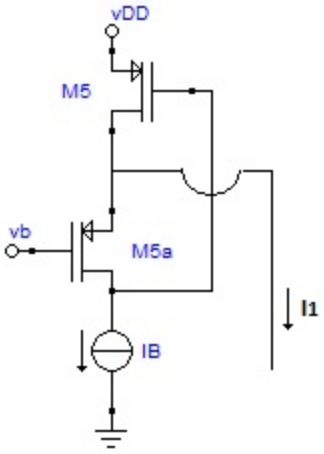
$I_{QTOT} = [(5 + 2k)I_B] + I_{cmfb} + I_{CM})$

$I_{QOUT} = 2kI_B$

using FVF Current Mirror

$I_{QTOT} = [(9 + 4k)I_B] + I_{cmfb} + I_{CM})$

$I_{QOUT} = 4kI_B$



In detail:

$DP \quad I_{Tail} = 2I_B$

$OUT \quad I_{out} = 2kI_{Tail} \quad (kI_{Tail})$

$BUF \quad I_{BUF} = \beta I_{Tail} \quad \beta = 3$

$AUX \quad I_{aux} = \alpha I_{Tail} \quad \alpha = \frac{1}{2} + \xi \quad I_{CM} = \xi I_{Tail}$

$CMFB \quad I_{cmfb} = \gamma I_{Tail}$

$F_c = \frac{4k}{4k+9+2\gamma+2\xi}$

Large signal

$I_2 = 0$

$I_1 = I_{1max}$

$I_{Load\,max} = kI_{1max}$

$I_{1max} = k_1(V_{GS1max} - V_T)^2$

$V_{G1} = V_{DCin} + V_{ic} + \frac{v_{id}}{2}$

$V_S = V_{DCin} + V_{ic} - V_{GS3}$

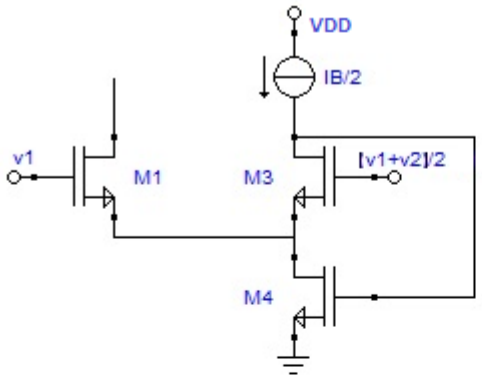
$V_{GS3} = V_T + \sqrt{\frac{I_B}{k_3}}$

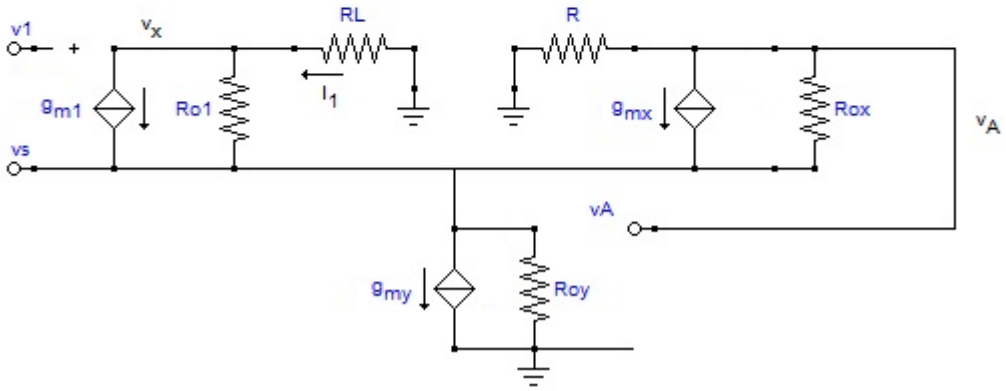
$I_{1max} = k_1(\frac{v_{id}}{2} + \sqrt{\frac{I_B}{k_3}})^2$

for example: $V_{DCin} = V_{DD}/2$, $V_{ic} = 0$, $v_{idmax} = V_{DD}$

$F_{SR} = \frac{k_1(\frac{v_{DD}}{2} + \sqrt{\frac{I_B}{k_3}})^2 - I_B}{4I_B}$

Small signal analysis





$$g_{mx} = \frac{g_{m3}}{2}$$
$$g_{my} = \frac{g_{m4}}{2}$$
$$r_{ox} = 2r_{o3}$$
$$r_{oy} = r_{o4}$$

$$\begin{cases} i_1 = g_{m1}(v_1 - v_s) + \frac{v_x - v_s}{r_{o1}} \\ v_x = -i_1 R_L \\ i_1 + g_{mx}(v_{ic} - v_s) + \frac{v_A - v_s}{r_{ox}} = g_{my} v_A + \frac{v_s}{r_{oy}} \\ g_{mx}(v_{ic} - v_s) + \frac{v_A - v_s}{r_{ox}} + \frac{v_A}{R} = 0 \end{cases}$$

$$\begin{cases} v_A\left(\frac{1}{r_{ox}} + \frac{1}{R}\right) = v_s\left(g_{mx} + \frac{1}{r_{ox}}\right) - g_{mx} v_{ic} \\ -v_x\left(\frac{1}{R_L} + \frac{1}{r_{o1}}\right) = g_{m1} v_1 - v_s\left(g_{m1} + \frac{1}{r_{o1}}\right) \\ i_1 = -\frac{v_x}{R_L} \\ g_{m1} v_1 + \frac{v_x}{r_{o1}} + g_{mx} v_{ic} - v_A\left(g_{my} - \frac{1}{r_{ox}}\right) - v_s\left(g_{m1} + \frac{1}{r_{o1}} + g_{mx} + \frac{1}{r_{ox}} + \frac{1}{r_{oy}}\right) = 0 \end{cases}$$

$$v_s = \frac{v_1 \frac{g_{m1}}{R_L}\left(\frac{1}{r_{ox}} + \frac{1}{R}\right) + v_{ic} g_{mx}\left(g_{m1} + \frac{1}{R}\right)\left(\frac{1}{r_{o1}} + \frac{1}{R_L}\right)}{\Delta}$$

$$\Delta = g_{m1} g_{mx}\left(\frac{1}{r_{o1}} + \frac{1}{R_L}\right) + g_{m1}\left(\frac{2}{r_{ox} R_L} + \frac{1}{r_{o1} r_{ox}} + \frac{1}{R_L R}\right) +$$
$$+ \frac{g_{mx}}{R}\left(\frac{1}{r_{o1}} + \frac{1}{R_L}\right) + \frac{1}{r_{o1} R_L}\left(\frac{1}{r_{ox}} + \frac{1}{R}\right) + \frac{1}{r_{ox} R}\left(\frac{1}{r_{o1}} + \frac{1}{R_L}\right) +$$
$$+ \frac{1}{r_{oy}}\left(\frac{1}{r_{o1} R} + \frac{1}{r_{o1} r_{ox}} + \frac{1}{R R_L} + \frac{1}{R_L r_{ox}}\right)$$

$$v_x = \frac{g_{m1}v_1 - \left(g_{m1}+\frac{1}{r_{o1}}\right)v_s}{\left(\frac{1}{r_{o1}}+\frac{1}{R_L}\right)} =$$

$$= \frac{v_1 g_{m1} X - v_{ic} g_{mx}\left(g_{m1}+\frac{1}{r_{o1}}\right)\left(g_{m1}+\frac{1}{R}\right)\left(\frac{1}{r_{o1}}+\frac{1}{R_L}\right)}{\left(\frac{1}{r_{o1}}+\frac{1}{R_L}\right)\Delta} =$$

$$X = \Delta - \left(g_{m1}+\frac{1}{r_{o1}}\right)\left(\frac{1}{r_{ox}}+\frac{1}{R}\right)\frac{1}{R_L} =$$

$$= g_{m1}g_{mx}\left(\frac{1}{r_{o1}}+\frac{1}{R_L}\right) + \frac{g_{m1}}{r_{ox}}\left(\frac{1}{R_L}+\frac{1}{r_{o1}}\right) + \frac{g_{mx}}{R}\left(\frac{1}{r_{o1}}+\frac{1}{R_L}\right) +$$

$$+ \frac{1}{r_{ox}R}\left(\frac{1}{r_{o1}}+\frac{1}{R_L}\right) + \frac{1}{r_{oy}}\left[\frac{1}{r_{o1}}\left(\frac{1}{R}+\frac{1}{r_{ox}}\right) + \frac{1}{R_L}\left(\frac{1}{R}+\frac{1}{r_{ox}}\right)\right]$$

$$v_x = \frac{v_1 g_{m1}\left[\left(g_{m1}+\frac{1}{R}\right)\left(g_{mx}+\frac{1}{r_{ox}}\right)+\frac{1}{r_{oy}}\left(\frac{1}{R}+\frac{1}{r_{ox}}\right)\right] - v_{ic}g_{mx}\left(g_{m1}+\frac{1}{r_{o1}}\right)\left(g_{m1}+\frac{1}{R}\right)}{\Delta} =$$

$$\cong \frac{v_1 g_{m1}^2 g_{mx} - v_{ic} g_{m1}^2 g_{mx}}{\Delta}$$

If $v_1=v_{ic}$

$$v_x = v_{ic}\frac{A}{\Delta}$$

$$A = g_{m1}\left(g_{m1}+\frac{1}{R}\right)\left(g_{mx}+\frac{1}{r_{ox}}\right) + \frac{g_{m1}}{r_{oy}}\left(\frac{1}{R}+\frac{1}{r_{ox}}\right) - g_{mx}\left(g_{m1}+\frac{1}{r_{o1}}\right)\left(g_{m1}+\frac{1}{R}\right) =$$

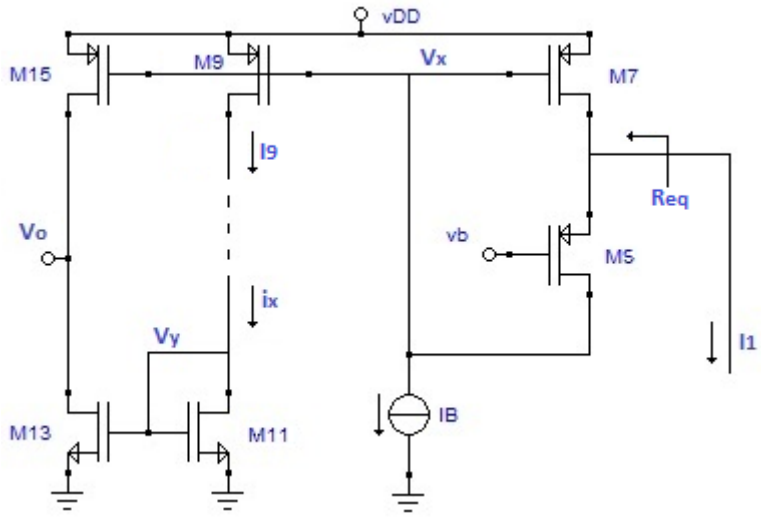
$$= \frac{g_{m1}}{r_{oy}}\left(\frac{1}{R}+\frac{1}{r_{ox}}\right) + \left(g_{m1}+\frac{1}{R}\right)\left[g_{m1}g_{mx} + \frac{g_{m1}}{r_{ox}} - g_{m1}g_{mx} - \frac{g_{mx}}{r_{o1}}\right] =$$

$$= \frac{g_{m1}}{r_{oy}}\left(\frac{1}{R}+\frac{1}{r_{ox}}\right) + \left(g_{m1}+\frac{1}{R}\right)\left[\frac{g_{m1}}{r_{ox}} - \frac{g_{mx}}{r_{o1}}\right]$$

if $v_1=-v_2=v_{id}/2$, $v_{ic}=0$, si ha che $v_s=0$

$i_1=g_{m1}v_{id}/2$ e $v_x=-g_{m1}R_Lv_{id}/2$

Small signal analysis



$$-\frac{v_o}{R_{Load}} = g_{m15}v_x + g_{m13}v_y$$

$$v_y = \frac{i_x}{g_{m11}}$$

$$i_x = \begin{cases} -i_9 & differential\ mode \\ i_9 & common\ mode \end{cases}$$

$$g_{m15} = kg_{m9}$$

$$g_{m13} = kg_{m11}$$

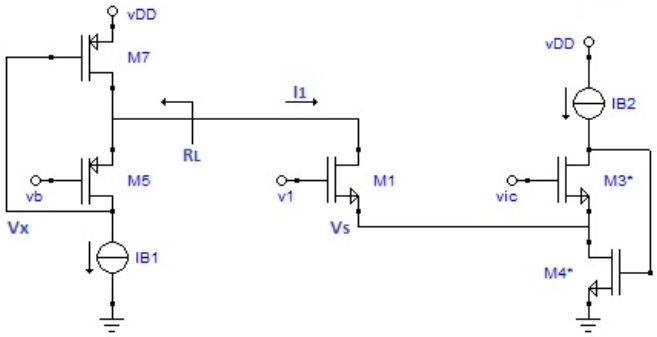
$g_{m9} = g_{m7}$
$i_9 = -g_{m9}v_x$
$g_{m13}v_y = \pm k g_{m11}\frac{1}{g_{m11}}g_{m9}v_x = \pm k g_{m9}v_x = g_{m15}v_x$
$v_x = -i_1\frac{r_{o7}(1+g_{m5}r_{o5})R}{D_p}$
$D_p = (r_{o5}+R)+(1+g_{m5}r_{o5})(1+g_{m7}R)r_{o7}$

Differential Mode

$v_1 = -v_2 = \frac{v_{id}}{2}$
$i_1 = g_{m1}\frac{v_{id}}{2}$
$v_5 = 0$
$v_o = g_{m1}\frac{r_{o7}(1+g_{m5}r_{o5})R}{D_p}R_{Load}2g_{m15}\frac{v_{id}}{2}$

Common Mode

$v_1 = v_2 = v_{ic}$
$i_1 = G_c v_{ic}$
$v_o = R_{Load}(g_{m15} - \frac{g_{m13}}{g_{m11}}g_{m9})\frac{r_{o7}(1+g_{m5}r_{o5})R}{D_p}G_c v_{ic}$
If $g_{m13} = k g_{m11}$; $g_{m15} = k g_{m9}$; $g_{m7} = g_{m9}$, si ha che $v_o = 0$
$CMRR = \frac{\frac{g_{m1}}{2}(g_{m15}+\frac{g_{m13}}{g_{m11}}g_{m9})}{G_c(g_{m15}-\frac{g_{m13}}{g_{m11}}g_{m9})}$



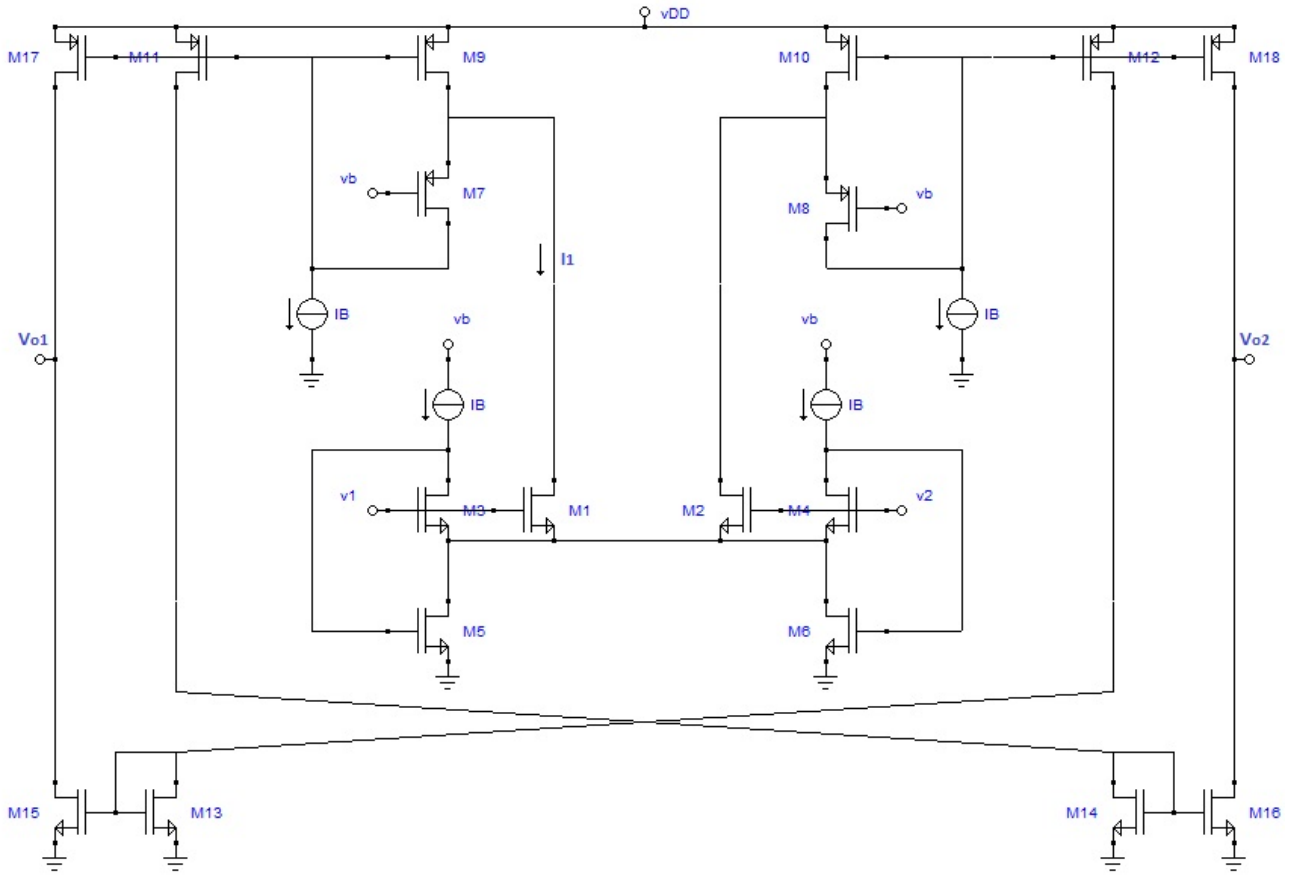
Note: M3* and M4* are half transistor
$i_1 = \frac{\alpha}{D}$
$D = \frac{Q}{Dp}$
$\alpha = g_{m1}r_{o1}(r_{o3}+R)v_1 + (1+g_{m4}R)r_{o4}\eta$
$\eta = g_{m1}r_{o1}(1+g_{m3}r_{o3})v_1 - g_{m3}r_{o3}(1+g_{m1}r_{o1})v_{ic}$
then $\alpha = \lambda v_{ic}$
$\lambda = g_{m1}r_{o1}(r_{o3}+R) + (g_{m1}r_{o1} - g_{m3}r_{o3})r_{o4}(1+g_{m4}R)$
$Q = \Delta Dp r_{o1} + \Delta r_{o7}(r_{o5}+R) + Dp r_{o4}(1+g_{m1}r_{o1})(r_{o3}+R)$
$\Delta = (r_{o3}+R) + (1+g_{m3}r_{o3})(1+g_{m4}R)r_{o4}$
$i_1 = \frac{Dp}{Q}\lambda v_{ic}$
$G_c = \frac{Dp}{Q}\lambda$

$$CMRR = \frac{(g_{m15}+\frac{g_{m13}}{g_{m11}}g_{m9})}{(g_{m15}-\frac{g_{m13}}{g_{m11}}g_{m9})}\frac{g_{m1}Q}{2Dp\lambda}$$

$$CMRR_i = \frac{g_{m1}Q}{2Dp\lambda} = \frac{\Delta}{2(r_{o3}+R)} \cong \frac{1}{2}g_{m4}r_{o4}g_{m3}(r_{o3}//R)$$

with gm_3 e gm_4 that in reality are $gm_3/2$ e $gm_4/2$ and r_{o3} e r_{o4} that in reality are $2r_{o3}$ e $2r_{o4}$.

A.5 Class AB input stage based on adaptive biasing WTA (Baswa 06)



Bias point

$I_1 = I_2 = I_3 = I_4 = I_B$
$I_5 = I_6 = 2I_B$
$I_7 = I_8 = I_B$
$I_9 = I_{10} = I_{11} = I_{12} = 2I_B$
$I_{13} = I_{14} = 2I_B$
$I_{15} = I_{16} = I_{17} = I_{18} = k2I_B$
$I_{QTOT} = 2(5 + 2k)I_B + I_{cmfb}$
$I_{QTOT} = 2(3 + 2k)I_B,\ with\ current\ mirror$
$I_{QTOT} = 2kI_B, simple$
$I_{QOUT} = 4kI_B$

In detail:

$DP \quad I_{Tail} = 2I_B$
$BUF \quad I_{BUF} = \beta I_{Tail} \quad \beta = 3$
$OUT \quad I_{out} = 2kI_{Tail}$

$AUX \quad I_{aux} = \alpha I_{Tail} \quad \alpha = 1$

$CMFB \quad I_{cmfb} = \gamma I_{Tail}$

$F_c = \frac{2k}{5+2k+\gamma}$

Large signal

$I_2 = I_B$

$I_1 = I_{1max}$

$I_{Load\,max} = k(I_{1max} - I_B)$

$I_{1max} = k_1(V_{GS1max} - V_T)^2$

$V_{G1} = V_{DCin} + V_{ic} + \frac{v_{id}}{2}$

$V_{S1} = V_{DCin} + V_{ic} - \frac{v_{id}}{2} - V_{GS3}$

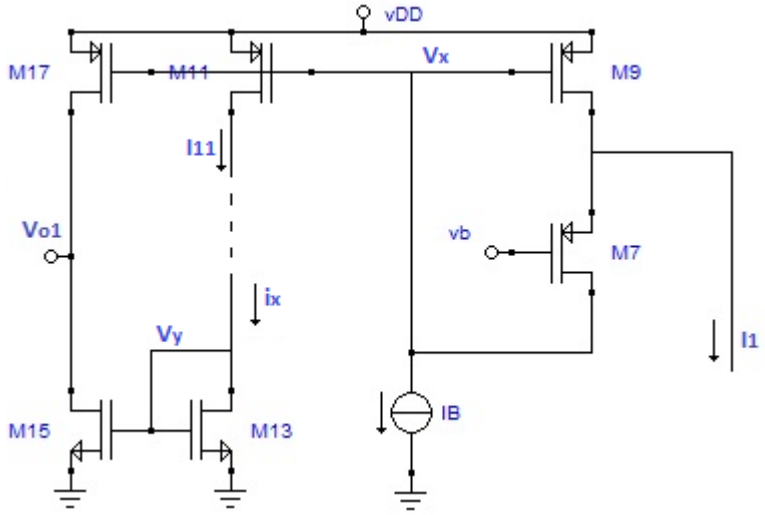
$V_{GS3} = V_T + \sqrt{\frac{I_B}{k_3}}$

$I_{1max} = k_1(v_{id} + \sqrt{\frac{I_B}{k_3}})^2$

For example: $V_{DCin} = V_{DD}/2$, $V_{ic} = 0$, $v_{idmax} = V_{DD}$

$F_{SR} = \frac{k_1(v_{DD}+\sqrt{\frac{I_B}{k_3}})^2 - I_B}{4I_B}$

Small signal analysis



$-\frac{v_o}{R_{Load}} = g_{m17}v_x + g_{m15}v_y$

$v_y = \frac{i_x}{g_{m13}}$

$i_x = \begin{cases} -i_{11} & differential\ mode \\ i_{11} & common\ mod \end{cases}$

$i_{11} = -g_{m11}v_x$

$v_x = -i_1 \frac{r_{o9}(1+g_{m7}r_{o7})R}{D_p}$

$D_p = (r_{o7} + R) + (1 + g_{m7}r_{o7})(1 + g_{m9}R)r_{o9}$

Differential Mode

$v_1 = -v_2 = \frac{v_{id}}{2}$

$i_1 = g_{m1}\frac{v_{id}}{2}$

$v_9 = 0$

$v_o = R_{Load}\frac{r_{o9}(1+g_{m7}r_{o7})R}{D_p} g_{m1}(g_{m17} + \frac{g_{m15}}{g_{m13}} g_{m11})\frac{v_{id}}{2}$

Se $g_{m17} = kg_{m9}$; $g_{m11} = g_{m9}$; $g_{m15} = kg_{m13}$, si ha:

$v_o = R_{Load}\frac{r_{o9}(1+g_{m7}r_{o7})R}{D_p} kg_{m1}g_{m9}v_{id}$

Common Mode

$v_1 = v_2 = v_{ic}$

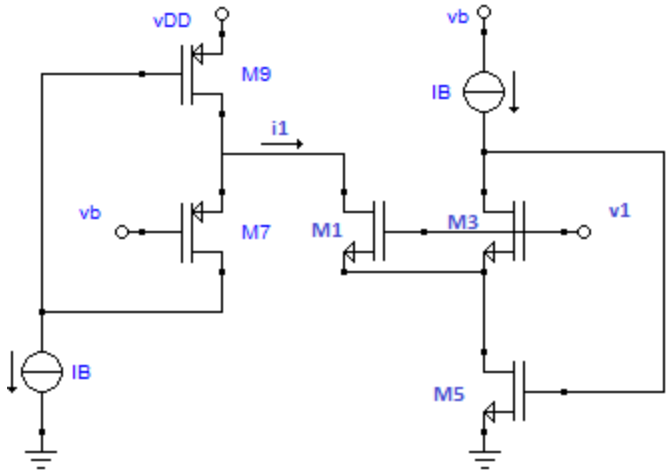
$i_1 = G_c v_{ic}$

$v_o = R_{Load}\frac{r_{o9}(1+g_{m7}r_{o7})R}{D_p} g_{m1}(g_{m17} - \frac{g_{m15}}{g_{m13}} g_{m11})v_{ic}$

Se $g_{m17} = kg_{m9}$; $g_{m11} = g_{m9}$; $g_{m15} = kg_{m13}$, si ha, $v_o = 0$

$CMRR = \frac{g_{m17}+\frac{g_{m15}}{g_{m13}}g_{m11}}{g_{m17}-\frac{g_{m15}}{g_{m13}}g_{m11}} CMRR_i$

$CMRR_i = \frac{g_{m1}}{2G_c}$



$i_1 = \frac{\alpha}{D}$

$D = \frac{Q}{D_p}$

$\alpha = g_{m1}r_{o1}(r_{o3} + R)v_1 + (1 + g_{m5}R)r_{o5}\eta = \mu v_1$

$\eta = (g_{m1}r_{o1} - g_{m3}r_{o3})v_1$

$\mu = g_{m1}r_{o1}(r_{o3} + R) + (g_{m1}r_{o1} - g_{m3}r_{o3})(1 + g_{m5}R)r_{o5}$

$Q = \Delta D_p r_{o1} + \Delta r_{o9}(r_{o7} + R) + D_p r_{05}(1 + g_{m1}r_{o1})(r_{o3} + R)$

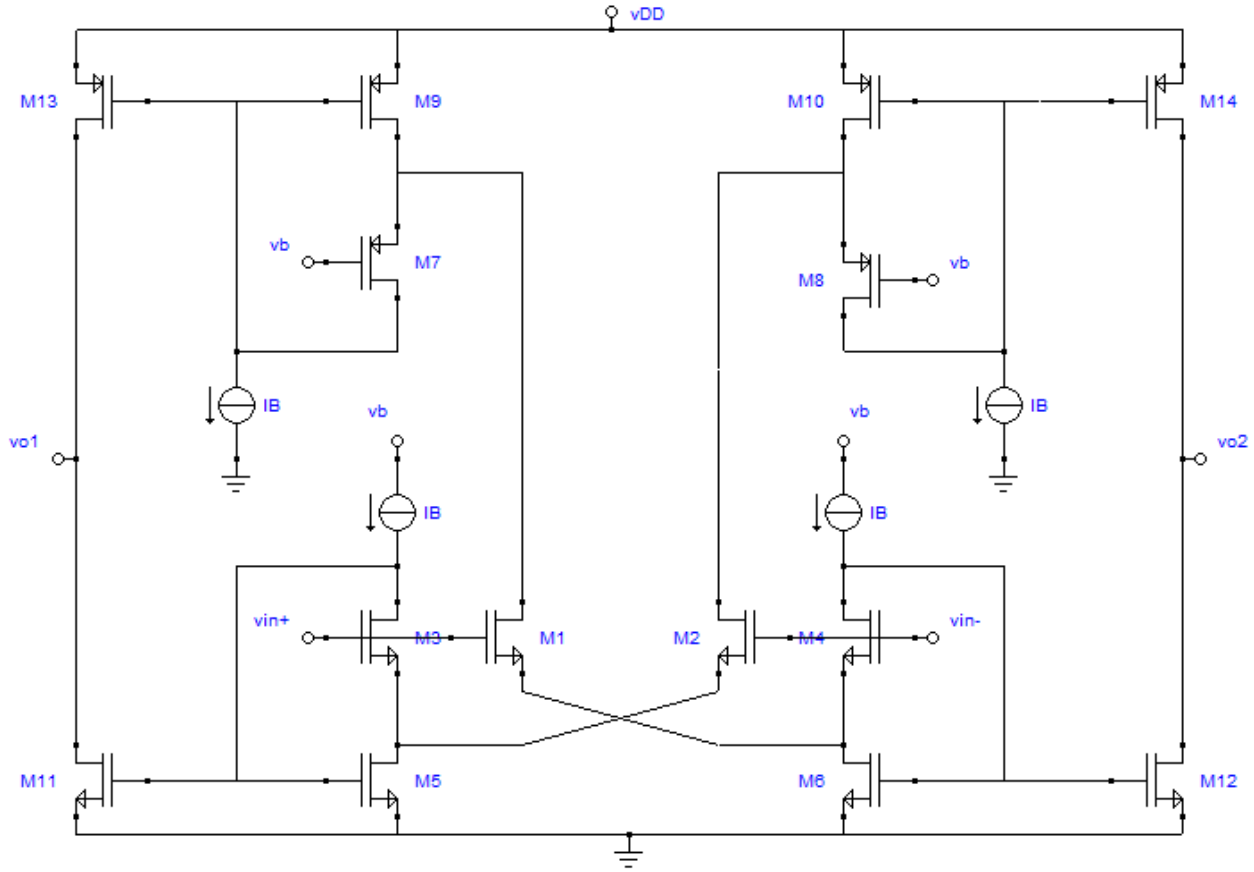
$\Delta = (r_{o3} + R) + (1 + g_{m3}r_{o3})(1 + g_{m5}R)r_{o5}$

$i_1 = \frac{D_p}{Q}\mu v_{ic}$

$G_c = \frac{D_p}{Q}\mu$

$CMRR_i = \frac{g_{m1}Q}{2D_p\mu} \cong \frac{\Delta}{2(r_{o3}+R)} + \frac{r_{o5}(1+g_{m1}r_{o1})}{2r_{o1}} \cong \frac{g_{m3}r_{o3}g_{m5}r_{o5}R}{2(r_{o3}+R)}$

A.6 Class AB input stage based on Peluso topology with Vs=-Vi (Peluso 97)



Bias point

$I_3 = I_B$
$I_1 = I_B$
$I_5 = 2I_B$
$I_7 = I_B$
$I_9 = 2I_B$
$I_{11} = I_{13} = 2kI_B$
$I_{QTOT} = 2(3 + 2k)I_B + I_{cmfb}$
$I_{QOUT} = 4kI_B$

In detail:

DP $I_{Tail} = 2I_B$
OUT $I_{out} = 2kI_{Tail}$
BUF $I_{BUF} = \beta I_{Tail}$ $\beta = 1$
AUX $I_{aux} = \alpha I_{Tail}$ $\alpha = 1$ (or α=0 if recycled IB)
$CMFB$ $I_{cmfb} = \gamma I_{Tail}$

$$F_c = \frac{2k}{2k+3+\gamma}$$

Large signal

$I_2 = 0$

$I_1 = I_{1max}$

$I_{Load\,max} = k(I_{1max})$

$I_{1max} = k_1(V_{GS1max} - V_T)^2$

$V_{G1} = V_{DCin} + V_{ic} + \frac{v_{id}}{2}$

$V_{S1} = V_{DCin} + V_{ic} - \frac{v_{id}}{2} - V_{GSQ}$

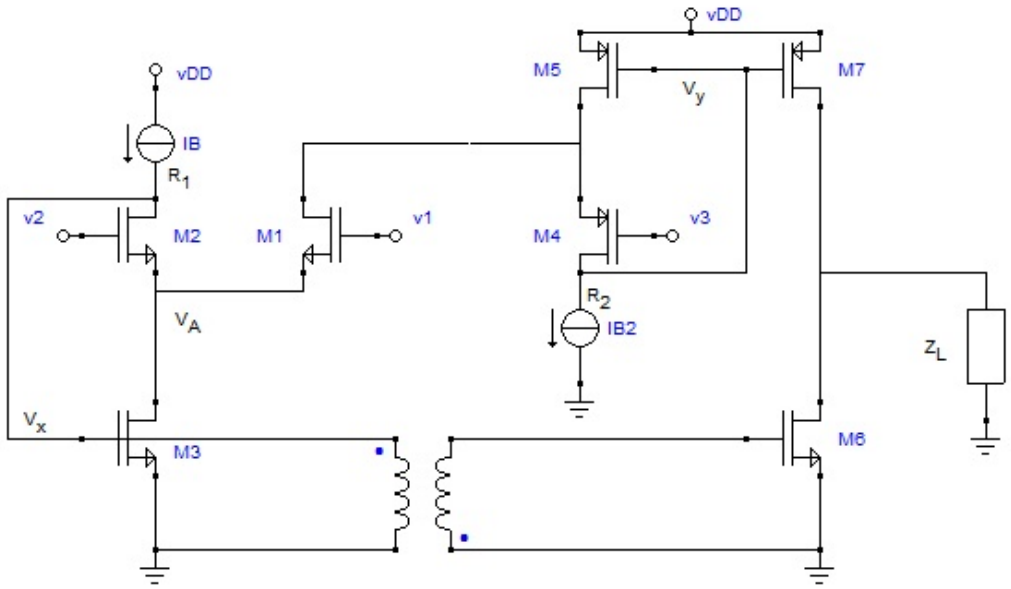
$V_{GSQ} = V_T + \sqrt{\frac{I_B}{k_3}}$

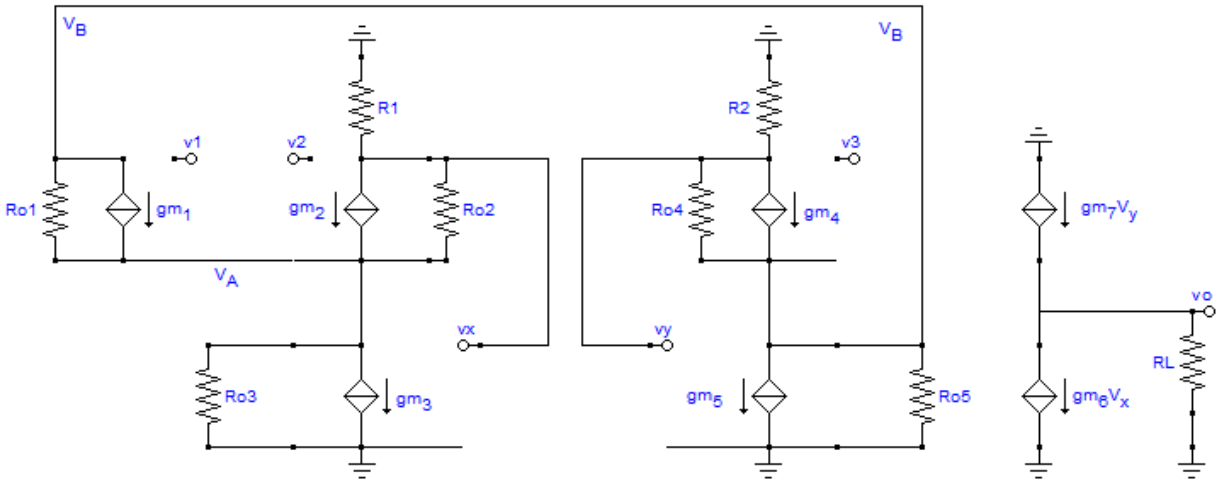
$I_{1max} = k_1(v_{id} + \sqrt{\frac{I_B}{k_3}})^2$

For example: $V_{DCin} = V_{DD}/2$, $V_{ic} = 0$, $v_{idmax} = V_{DD}$

$F_{SR} = \frac{k_1(v_{DD}+\sqrt{\frac{I_B}{k_3}})^2}{4I_B}$

Small signal analysis simplified (ro=0) differential mode





$$\begin{cases} g_{m1}(v_1 - v_A) + g_{m2}(v_2 - v_A) = g_{m3}v_x \\ g_{m2}(v_2 - v_A) + \frac{v_x}{R_1} = 0 \\ g_{m4}(v_3 - v_B) + \frac{v_y}{R_2} = 0 \\ g_{m4}(v_3 - v_B) = g_{m1}(v_1 - v_A) + g_{m5}v_y \\ g_{m6}v_x - g_{m7}v_y - \frac{v_o}{R_L} = 0 \end{cases}$$

$$g_{m2}v_A = g_{m2}v_2 + \frac{v_x}{R_1}$$

$$g_{m4}v_B = g_{m3}v_3 + \frac{v_y}{R_2}$$

$$g_{m1}v_1 + g_{m2}v_2 - (g_{m1} + g_{m2})\frac{g_{m2}v_2 + \frac{v_x}{R_1}}{g_{m2}} = g_{m3}v_x$$

$$g_{m4}v_3 - g_{m3}v_3 - \frac{v_y}{R_2} = g_{m1}v_1 + g_{m5}v_y - g_{m1}\frac{g_{m2}v_2 + \frac{v_x}{R_1}}{g_{m2}}$$

$$\frac{v_x}{R_1} = -g_{m2}(v_2 - v_A)$$

$$\frac{v_y}{R_2} = -g_{m4}(v_3 - v_B)$$

$$g_{m1}(v_1 - v_A) = v_x\left(g_{m3} + \frac{1}{R_1}\right) = -v_y\left(\frac{1}{R_2} + g_{m5}\right)$$

$$g_{m1}(v_1 - v_A) + g_{m2}(v_2 - v_A) = -g_{m3}g_{m2}R_1(v_2 - v_A)$$

$$g_{m1}v_1 + g_{m2}(1 + g_{m3}R_1)v_2 = v_A(g_{m1} + g_{m2} + g_{m2}g_{m3}R_1)$$

$$v_A = \frac{g_{m1}v_1 + g_{m2}(1+g_{m3}R_1)v_2}{(g_{m1}+g_{m2}+g_{m3}R_1)}$$

$$v_x = -g_{m2}R_1\left[v_2 - \frac{g_{m1}v_1 + g_{m2}(1+g_{m3}R_1)v_2}{g_{m1}+g_{m2}(1+g_{m3}R_1)}\right] =$$

$$= g_{m2}R_1\frac{g_{m1}(v_1 - v_2)}{g_{m1}+g_{m2}(1+g_{m3}R_1)}$$

$$v_y = -\frac{1+g_{m3}R_1}{R_1}\frac{R_2}{1+g_{m5}R_2}v_x = -\frac{1+g_{m3}R_1}{1+g_{m5}R_2}\frac{g_{m1}g_{m2}R_2(v_1 - v_2)}{g_{m1}+g_{m2}(1+g_{m2}R_1)}$$

$$v_o = -R_{LOAD}(g_{m7}v_y - g_{m6}v_x) =$$

$$= +R_{LOAD}\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}(1+g_{m2}R_1)}(v_1 - v_2)[g_{m6}R_1 + g_{m7}R_2\frac{1+g_{m3}R_1}{1+g_{m5}R_2}]$$

for the common mode, $v_1=v_2=v_{ic}$ e $v_o=-R_{LOAD}(gm_6v_x+gm_7v_y)$; neglecting r_o, $v_x=v_y=0$

Small signal analysis (v_3=0)

$$\begin{cases} g_{m1}(v_1 - v_A) + \frac{v_B - v_A}{r_{o1}} g_{m2}(v_2 - v_A) + \frac{v_x - v_A}{r_{o2}} = \frac{v_A}{r_{o3}} + g_{m3} v_x \\ \frac{v_x}{R_1} + \frac{v_x - v_A}{r_{o2}} + g_{m2}(v_2 - v_A) = 0 \\ \frac{v_y}{R_2} + \frac{v_y - v_B}{r_{o4}} - g_{m4} v_B += 0 \\ \frac{v_y - v_B}{r_{o4}} - g_{m4} v_B = g_{m5} v_y + \frac{v_B}{r_{o5}} + g_{m1}(v_1 - v_A) + \frac{v_B - v_A}{r_{o1}} \end{cases}$$

$$v_x \left(g_{m3} + \frac{1}{R_1}\right) + \frac{v_A}{r_{o3}} = -v_y \left(g_{m5} + \frac{1}{R_2}\right) - \frac{v_B}{r_{o5}}$$

$$\begin{cases} \alpha v_1 + \beta v_2 + \gamma v_x + \delta v_y = 0 \\ \varepsilon v_1 + \zeta v_2 + \eta v_x + \theta v_y = 0 \end{cases}$$

$$\alpha = g_{m1}\left(g_{m2} + \frac{1}{r_{o2}}\right)\left(g_{m4} + \frac{1}{r_{o4}}\right)$$

$$\beta = -g_{m2}\left(g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o3}}\right)\left(g_{m4} + \frac{1}{r_{o4}}\right)$$

$$\gamma = -\left(g_{m4} + \frac{1}{r_{o4}}\right)\left[\left(g_{m1} + \frac{1}{r_{o1}}\right)\left(\frac{1}{r_{o2}} + \frac{1}{R_1}\right) + \left(g_{m3} + \frac{1}{R_1}\right)\left(g_{m2} + \frac{1}{r_{o2}}\right) + \frac{1}{r_{o3}}\left(\frac{1}{r_{o2}} + \frac{1}{R_1}\right)\right]$$

$$\delta = \frac{1}{r_{o1}}\left(\frac{1}{r_{o4}} + \frac{1}{R_2}\right)\left(g_{m2} + \frac{1}{r_{o2}}\right)$$

$$\varepsilon = g_{m1}\left(g_{m2} + \frac{1}{r_{o2}}\right)\left(g_{m4} + \frac{1}{r_{o4}}\right)$$

$$\zeta = g_{m2}\left(g_{m1} + \frac{1}{r_{o1}}\right)\left(g_{m4} + \frac{1}{r_{o4}}\right)$$

$$\eta = -\left(g_{m1} + \frac{1}{r_{o1}}\right)\left(g_{m4} + \frac{1}{r_{o4}}\right)\left(\frac{1}{r_{o2}} + \frac{1}{R_1}\right)$$

$$\theta = \left(g_{m2} + \frac{1}{r_{o2}}\right)\left[\left(g_{m4} + \frac{1}{r_{o4}}\right)\left(g_{m5} + \frac{1}{R_2}\right) + \left(\frac{1}{r_{o1}} + \frac{1}{r_{o5}}\right)\left(\frac{1}{r_{o4}} + \frac{1}{R_2}\right)\right]$$

$$v_x = \frac{(\varepsilon\delta - \theta\alpha)v_1 + (\zeta\delta - \theta\beta)v_2}{\theta\gamma - \eta\delta}$$

$$v_y = \frac{(\alpha\eta - \gamma\varepsilon)v_1 + (\beta\eta - \gamma\zeta)v_2}{\theta\gamma - \eta\delta}$$

Differential Mode

$$v_1 = -v_2 = \frac{v_{id}}{2}$$

$$v_o = -R_{LOAD}\left(g_{m7} v_y - g_{m6} v_x\right)$$

$$v_o = -R_{LOAD}\frac{\Gamma}{\Delta}$$

$$\Delta = \theta\gamma - \eta\delta$$

$$\Gamma = \frac{v_{id}}{2}\left[g_{m7}(\alpha\eta - \gamma\varepsilon - \beta\eta + \gamma\zeta) - g_{m6}(\varepsilon\delta - \theta\alpha - \zeta\delta + \theta\beta)\right]$$

Common Mode

$$v_1 = v_2 = v_{ic}$$

$$v_o = -R_{LOAD}\left(g_{m6} v_x + g_{m7} v_y\right)$$

$$v_o = -R_{LOAD}\frac{\Sigma}{\Delta}$$

$$\Sigma = v_{ic}\left[g_{m6}(\varepsilon\delta - \theta\alpha + \zeta\delta - \theta\beta) + g_{m7}(\alpha\eta - \gamma\varepsilon + \beta\eta - \gamma\zeta)\right]$$

$$CMRR = \frac{\Sigma}{2\Gamma}$$

$$\Gamma = (\alpha - \beta)(g_{m6}\theta + g_{m7}\eta) + (\zeta - \varepsilon)(g_{m6}\delta + g_{m7}\gamma)$$

$$\Sigma = -(\alpha + \beta)(g_{m6}\theta - g_{m7}\eta) + (\zeta + \varepsilon)(g_{m6}\delta - g_{m7}\gamma)$$

$$\alpha-\beta=\left(g_{m4}+\frac{1}{r_{o4}}\right)\left(2g_{m1}g_{m2}+\frac{g_{m1}}{r_{o2}}+\frac{g_{m2}}{r_{o1}}+\frac{g_{m2}}{r_{o3}}\right)$$
$$\zeta-\varepsilon=\left(g_{m4}+\frac{1}{r_{o4}}\right)\left(2g_{m1}g_{m2}+\frac{g_{m1}}{r_{o2}}+\frac{g_{m2}}{r_{o1}}\right)$$
$$\alpha+\beta=\left(g_{m4}+\frac{1}{r_{o4}}\right)\left(\frac{g_{m1}}{r_{o2}}-\frac{g_{m2}}{r_{o1}}-\frac{g_{m2}}{r_{o3}}\right)$$
$$\zeta+\varepsilon=\left(g_{m4}+\frac{1}{r_{o4}}\right)\left(\frac{g_{m1}}{r_{o2}}-\frac{g_{m2}}{r_{o1}}\right)$$

placing

$g_{m1}=g_{m2}=g_{mn}$
$g_{m3}=2g_{mn}$
$g_{m4}=g_{mp}$
$g_{m5}=2g_{mp}$
$g_{m6}=kg_{mn}$
$g_{m7}=kg_{mp}$
$r_{o1}=r_{o2}=r_{on}$
$r_{o3}=r_{on}/2$
$r_{o5}=r_{op}/2$

I vave:

$$\Gamma=[\mathrm{A}(\alpha-\beta)+B(\zeta-\varepsilon)]\mathrm{k}$$
$$\Sigma=[-\mathrm{C}(\alpha+\beta)+D(\zeta+\varepsilon)]\mathrm{k}$$
$$\mathrm{A}=g_{mn}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(g_{mp}+\frac{1}{r_{op}}\right)\left(2g_{mp}+\frac{1}{R_2}\right)+$$
$$+g_{mn}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(\frac{1}{R_2}+\frac{1}{r_{op}}\right)\left(\frac{1}{r_{o1}}+\frac{2}{r_{op}}\right)-$$
$$-g_{mp}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(g_{mp}+\frac{1}{r_{op}}\right)\left(\frac{1}{R_1}+\frac{1}{r_{on}}\right)=$$
$$=\left(g_{mn}+\frac{1}{r_{on}}\right)\left(g_{mp}+\frac{1}{r_{op}}\right)\left[g_{mn}\left(2g_{mp}+\frac{1}{R_2}\right)-g_{mp}\left(\frac{1}{R_1}+\frac{1}{r_{on}}\right)\right]+$$
$$+g_{mn}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(\frac{1}{R_2}+\frac{1}{r_{op}}\right)\left(\frac{1}{r_{o1}}+\frac{2}{r_{op}}\right)\cong 2g_{mn}^2g_{mp}^2$$
$$B=g_{mn}\frac{1}{r_{on}}\left(\frac{1}{R_2}+\frac{1}{r_{op}}\right)\left(g_{mn}+\frac{1}{r_{on}}\right)-g_{mp}\left(g_{mp}+\frac{1}{r_{op}}\right)\left(g_{mn}+\frac{3}{r_{on}}\right)\left(\frac{1}{R_1}+\frac{1}{r_{on}}\right)-$$
$$-g_{mp}\left(g_{mp}+\frac{1}{r_{op}}\right)\left(g_{mn}+\frac{1}{r_{on}}\right)\left(2g_{mn}+\frac{1}{R_1}\right)\cong 2g_{mn}^2g_{mp}^2$$
$$\Gamma\cong \mathrm{k}2g_{mn}^2g_{mp}^2(\alpha-\beta-\varepsilon+\zeta)=2\mathrm{k}g_{mn}^3g_{mp}^3\frac{2}{r_{on}}$$
$$\mathrm{C}=g_{mn}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(g_{mp}+\frac{1}{r_{op}}\right)\left(2g_{mp}+\frac{1}{R_2}\right)+$$
$$+g_{mn}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(\frac{1}{r_{on}}+\frac{2}{r_{op}}\right)\left(\frac{1}{R_2}+\frac{1}{r_{op}}\right)+$$
$$+g_{mp}\left(g_{mn}+\frac{1}{r_{on}}\right)\left(g_{mp}+\frac{1}{r_{op}}\right)\left(\frac{1}{R_1}+\frac{1}{r_{on}}\right)=$$
$$=\left(g_{mn}+\frac{1}{r_{on}}\right)\left[\left(g_{mp}+\frac{1}{r_{op}}\right)\left(2g_{mn}g_{mp}+\frac{g_{mn}}{R_2}+\frac{g_{mp}}{R_1}+\frac{g_{mp}}{r_{on}}\right)+\right.$$
$$\left.+g_{mn}\left(\frac{1}{R_2}+\frac{1}{r_{op}}\right)\left(\frac{1}{r_{on}}+\frac{2}{r_{op}}\right)\right]\cong 2g_{mn}^2g_{mp}^2$$
$$D=g_{mn}\frac{1}{r_{on}}\left(\frac{1}{R_2}+\frac{1}{r_{op}}\right)\left(g_{mn}+\frac{1}{r_{on}}\right)+g_{mp}\left(g_{mp}+\frac{1}{r_{op}}\right)\frac{2}{r_{on}}\left(\frac{1}{R_1}+\frac{1}{r_{on}}\right)+$$

$$+g_{mp}\left(g_{mp}+\frac{1}{r_{op}}\right)\left(g_{mn}+\frac{1}{r_{on}}\right)\left(\frac{1}{R_1}+\frac{1}{r_{on}}\right)+$$

$$+g_{mp}\left(g_{mp}+\frac{1}{r_{op}}\right)\left(g_{mn}+\frac{1}{r_{on}}\right)\left(2g_{mn}+\frac{1}{R_1}\right)\cong 2g_{mn}^2 g_{mp}^2$$

$$\Sigma = 2\mathrm{k}g_{mn}^2 g_{mp}^2(-\alpha-\beta+\zeta+\varepsilon) = 2\mathrm{k}g_{mn}^3 g_{mp}^3\frac{2}{r_{on}}$$

$$\mathrm{i}_1 = \frac{\alpha}{\mathrm{D}}$$

$$\alpha = g_{m1}r_{o1}(r_{o2}+R)v_1 + (1+g_{m3}R)r_{o3}\eta$$

$$\eta = g_{m1}r_{o1}(1+g_{m2}r_{o2})v_1 - g_{m2}r_{o2}(1+g_{m1}r_{o1})v_2$$

$$\alpha = Av_1 + Bv_2$$

$$A = g_{m1}r_{o1}[r_{o2}+R+r_{o3}(1+g_{m2}r_{o2})(1+g_{m3}R)] = g_{m1}r_{o1}\Delta$$

$$B = -g_{m2}r_{o2}(1+g_{m1}r_{o1})(1+g_{m3}R)r_{o3}$$

$$R_L = \frac{r_{o5}(1+g_{m4}r_{o4})R}{\Delta_p}$$

$$\Delta_p = (r_{o4}+R)+(1+g_{m4}r_{o4})(1+g_{m5}R)r_{o5}$$

$$\Delta = (r_{o2}+R)+(1+g_{m2}r_{o2})(1+g_{m3}R)r_{o3}$$

$$\mathrm{D} = \Delta\left(r_{o1}+\frac{r_{o5}(r_{o4}+R)}{\Delta_p}+(1+g_{m1}r_{o1})(r_{o2}+R)r_{o3}\right) = \frac{Q}{\Delta_p}$$

$$Q = \Delta\Delta_p r_{o1} + \Delta r_{o5}(r_{o4}+R) + \Delta_p r_{o3}(1+g_{m1}r_{o1})(r_{o2}+R)$$

$$v_y = -\mathrm{i}_1\frac{r_{o5}(1+g_{m4}r_{o4})R}{\Delta_p} = -\frac{\alpha}{\mathrm{Q}}r_{o5}(1+g_{m4}r_{o4})R = -\frac{\mathrm{R}}{\mathrm{Q}}\zeta$$

$$v_x = -\frac{\mathrm{R}}{\mathrm{D}}\beta = -\mathrm{R}\frac{\delta}{\mathrm{Q}}$$

$$\delta = \left[\Delta_p r_{o1} + r_{o5}(r_{o4}+R)\right]g_{m2}r_{o2}v_2 - \Delta_p r_{o3}\eta$$

$$\delta = \mathrm{C}v_1 + Dv_2$$

$$\mathrm{C} = -g_{m1}r_{o1}(1+g_{m2}r_{o2})r_{o3}\Delta_p$$

$$\mathrm{D} = g_{m2}r_{o2}[\Delta_p r_{o1} + r_{o3}\Delta_p(1+g_{m1}r_{o1}) + (r_{o4}+R)r_{o5}]$$

for the common mode, I have:

$$v_o = -R_{LOAD}\left(g_{m7}v_y - g_{m6}v_x\right)$$

as it would be

$$v_o = -R_{LOAD}\left(g_{m7}v_y + g_{m6}v_x^{'}\right)$$

with, $v_x^{'} = -\frac{\mathrm{R}}{\mathrm{Q}}(\mathrm{C}-\mathrm{D})\frac{v_{id}}{2} = -v_x$

$$v_{od} = -R_{LOAD}\frac{\mathrm{R}}{\mathrm{Q}}(g_{m6}\delta - g_{m7}\zeta) = -R_{LOAD}\frac{\mathrm{R}}{\mathrm{Q}}\Delta_{\mathrm{d}}\frac{v_{id}}{2}$$

$$\Delta_{\mathrm{d}} = g_{m6}C - g_{m6}D - g_{m7}r_{o5}(1+g_{m4}r_{o4})A + g_{m7}r_{o5}(1+g_{m4}r_{o4})B \cong$$

$$\cong -[g_{m1}r_{o1}(1+g_{m2}r_{o2}) + g_{m2}r_{o2}(1+g_{m1}r_{o1})]r_{o3}[g_{m6}\Delta_p + g_{m7}r_{o5}(1+g_{m4}r_{o4})(1+g_{m3}R)$$

for the common mode, I have:

$$v_o = -R_{LOAD}\left(g_{m6}v_x + g_{m7}v_y\right) = R_{LOAD}\frac{\mathrm{R}}{\mathrm{Q}}(g_{m6}\delta + g_{m7}\zeta) = R_{LOAD}\frac{\mathrm{R}}{\mathrm{Q}}\Delta_{\mathrm{c}}\mathrm{v_{ic}}$$

$$\Delta_{\mathrm{c}} = g_{m6}C + g_{m7}D + g_{m7}r_{o5}(1+g_{m4}r_{o4})A + g_{m7}r_{o5}(1+g_{m4}r_{o4})B =$$

$$= g_{m6}g_{m2}r_{o2}\left[\Delta_p r_{o1} + r_{o5}(r_{o4}+R)\right] + g_{m7}g_{m1}r_{o1}(r_{o2}+R) *$$

$$* r_{o5}(1+g_{m4}r_{o4}) + (g_{m1}r_{o1} - g_{m2}r_{o2})r_{o3}\{r_{o5}(1+g_{m4}r_{o4}) *$$

$$* [g_{m7}(1+g_{m3}R) - g_{m6}(1+g_{m5}R)] - g_{m6}(r_{o4}+R)\} \cong$$

$$\cong g_{m6}g_{m2}r_{o2}\Delta_p r_{o1}$$

$$CMRR = \frac{1}{2}\xi_n \left(1 + \frac{g_{mn}}{g_{mp}}\right)$$

con $\xi_n = g_{mn} r_{on}$

Appendix B

B.1 Evaluation of the performance limit through analysis in the symbolic domain with Sapwin 4

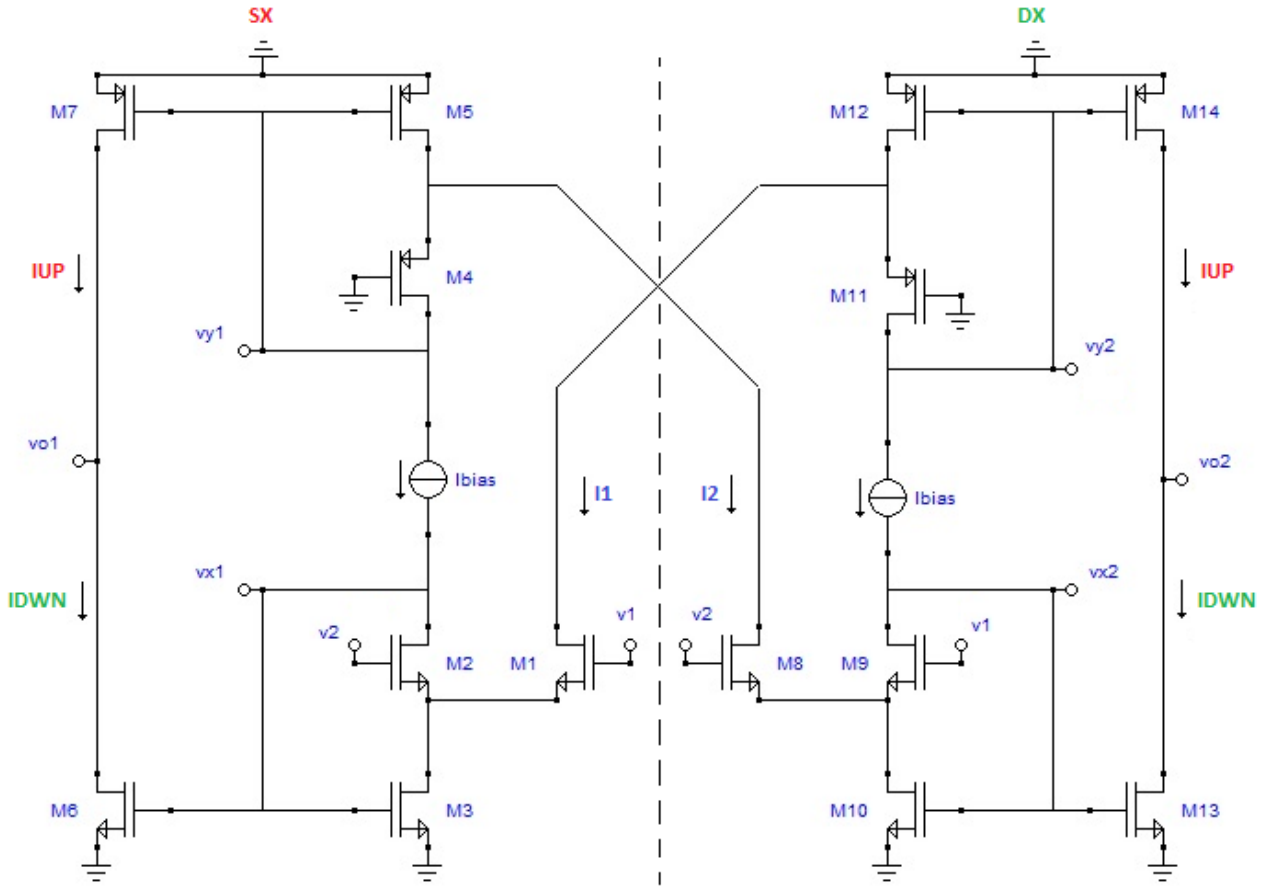


Fig.B. 1: Fully differential class AB OTA

$$\begin{cases} I_{DWN} \propto gm_6 * v_{x1,2} \\ I_{UP} \propto gm_7 * v_{y1,2} \end{cases} \quad \text{(B.1)}$$

$$V_{icm} = \frac{V_1+V_2}{2} \quad \text{(B.2)}$$

B.1.2 Transfer function Vy/Vicm

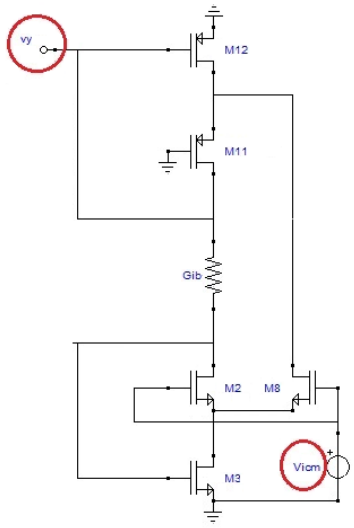


Fig.B. 2: circuit to calculate transfer function Vy/Vicm

Vy/Vicm=

[-gm8Gd3Gd2Gd11-gm8gm3Gd2Gd11+gm3gm2Gd8Gd11-gm8gm11Gd3Gd2-
gm8gm3gm11Gd2+gm3gm2gm11Gd8+Gib(-gm2Gd3Gd11-gm8Gd3Gd11+gm8Gd2Gd12-
gm2Gd3Gd12-gm2Gd8Gd12-gm2Gd8Gd3-gm2gm11Gd3-gm8gm11Gd3)]

(Gd3Gd2Gd12Gd11+Gd8Gd2Gd12Gd11+GibGd2Gd12Gd11+gm3Gd2Gd12Gd11+
gm8Gd2Gd12Gd11+GibGd3Gd12Gd11+GibGd8Gd12Gd11+gm2GibGd12Gd11+gm8Gib
Gd12Gd11+gm3gm2Gd12Gd11+Gd8Gd3Gd2Gd11+GibGd3Gd2Gd11+gm12Gd3Gd2Gd11+
gm12Gd8Gd2Gd11+gm3Gd8Gd2Gd11+gm12GibGd2Gd11+gm3GibGd2Gd11+gm3gm12Gd2Gd1
1+gm8gm12Gd2Gd11+GibGd8Gd3Gd11+gm12GibGd3Gd11+gm12GibGd8Gd11+gm3GibGd8Gd
11+gm3gm2Gd8Gd11+gm2gm12GibGd11+gm8gm12GibGd11+gm3gm2GibGd11
+gm8gm3GibGd11+gm3gm2gm12Gd11+GibGd3Gd2Gd12+GibGd8Gd2Gd12+gm3GibGd2Gd12
+gm8GibGd2Gd12+gm3gm2GibGd12+GibGd8Gd3Gd2+gm11GibGd3Gd2+gm12gm11Gd3Gd2+
gm12GibGd8Gd2+gm3GibGd8Gd2+gm12gm11Gd8Gd2+gm12gm11GibGd2+gm3gm11GibGd2+
gm3gm12gm11Gd2+gm8gm12gm11Gd2+gm12gm11GibGd3+gm12gm11GibGd8+gm3gm11Gib
Gd8+gm2gm12GibGd8+gm3gm2GibGd8+gm2gm12gm11Gib+gm8gm12gm11
Gib+gm3gm2gm11Gib+gm8gm3gm11Gib+gm3gm2gm12gm11)

B.1.3 Transfer function Vx/Vicm

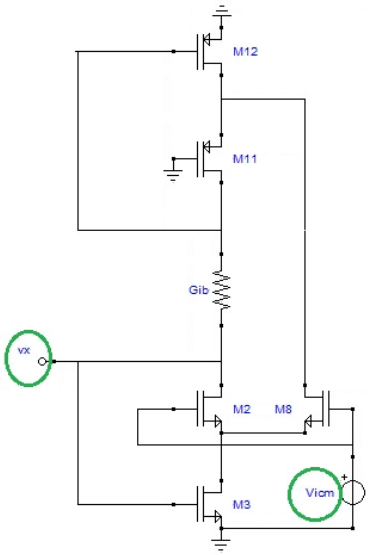


Fig.B. 3: circuit to calculate transfer function Vx/Vicm

Vx/Vicm=

(gm8Gd2Gd12Gd11-gm2Gd3Gd12Gd11-gm2Gd8Gd12Gd11+gm8gm12Gd2Gd11-
gm2Gd8Gd3Gd11- gm2gm12Gd3Gd11-gm2gm12Gd8Gd11+gm8gm12gm11Gd2-gm2 gm12 gm11
Gd3-gm2gm12gm11Gd8+Gib(-gm2Gd3Gd11-gm8Gd3Gd11+gm8Gd2Gd12-gm2Gd3Gd12-
gm2Gd8Gd12-gm2Gd8Gd3-gm2gm11Gd3-gm8gm11Gd3)

(Gd3Gd2Gd12Gd11+Gd8Gd2Gd12Gd11+GibGd2Gd12Gd11+gm3Gd2Gd12Gd11+
gm8Gd2Gd12Gd11+GibGd3Gd12Gd11+GibGd8Gd12Gd11+gm2GibGd12Gd11+gm8Gib
Gd12Gd11+gm3gm2Gd12Gd11+Gd8Gd3Gd2Gd11+GibGd3Gd2Gd11+gm12Gd3Gd2Gd11+
gm12Gd8Gd2Gd11+gm3Gd8Gd2Gd11+gm12GibGd2Gd11+gm3GibGd2Gd11+gm3gm12Gd2Gd1
1+gm8gm12Gd2Gd11+GibGd8Gd3Gd11+gm12GibGd3Gd11+gm12GibGd8Gd11+gm3GibGd8Gd
11+gm3gm2Gd8Gd11+gm2gm12GibGd11+gm8gm12GibGd11+gm3gm2GibGd11
+gm8gm3GibGd11+gm3gm2gm12Gd11+GibGd3Gd2Gd12+GibGd8Gd2Gd12+gm3GibGd2Gd12
+gm8GibGd2Gd12+gm3gm2GibGd12+GibGd8Gd3Gd2+gm11GibGd3Gd2+gm12gm11Gd3Gd2+
gm12GibGd8Gd2+gm3GibGd8Gd2+gm12gm11Gd8Gd2+gm12gm11GibGd2+gm3gm11GibGd2+
gm3gm12gm11Gd2+gm8gm12gm11Gd2+gm12gm11GibGd3+gm12gm11GibGd8+gm3gm11Gib
Gd8+gm2gm12GibGd8+gm3gm2GibGd8+gm2gm12gm11Gib+gm8gm12gm11
Gib+gm3gm2gm11Gib+gm8gm3gm11Gib+gm3gm2gm12gm11)

B.1.4 Comparison of transfer functions V_X/Vicm vs. V_Y/Vicm:

By comparing the obtained transfer functions (Vx/Vicm and Vy/Vicm), note that the denominators are identical while the numerators have a common part and one that differs. This difference between the Vx/Vicm and Vy/Vicm numerators causes the difference between the I_{UP} and I_{DWN} currents flowing in M7 and M6 of the circuit shown in Fig.B.1, which originates from a common output mode signal.

B.2 Peluso topology counts with triode CMFB

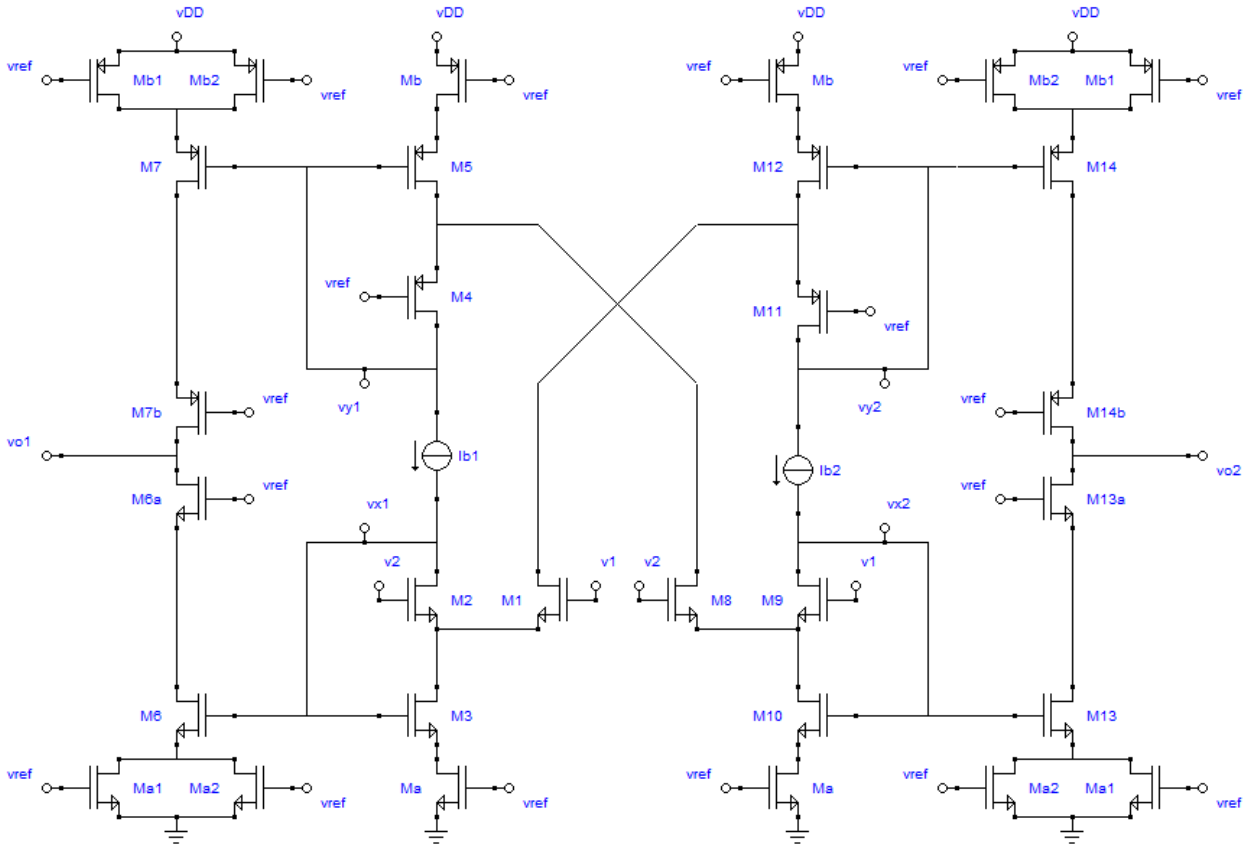


Fig.B. 4: Topology by Peluso with triode CMFB

For calculating the Vo1 / Vicm transfer function, the overall function can be broken in two parts.

$$AV_{CM} = \frac{V_{o1}}{V_{icm}} = \frac{I_L}{V_{icm}}\frac{V_{y1}}{I_L}\frac{V_{o1}}{V_{y1}} + \frac{V_{x1}}{V_{icm}}\frac{V_{o1}}{V_{x1}} \quad (B.3)$$

$$F_{UP} = F_1 = \frac{I_L}{V_{icm}}\frac{V_{y1}}{I_L}\frac{V_{o1}}{V_{y1}} = A \cdot B \cdot C \quad (B.4)$$

$$F_{DWN} = F_2 = \frac{V_{x1}}{V_{icm}}\frac{V_{o1}}{V_{x1}} = D \cdot E \quad (B.5)$$

The F_{UP} function is intrinsically linked to the I_{UP} current while the F_{DWN} function is linked to the I_{DWN} current. In turn, F_{UP} and F_{DWN} functions have been decomposed into the product of multiple functions in order to make the calculations simpler. To calculate these functions, from time to time, a part of the circuit of Fig.B.4 was taken into account in which elements were introduced that take account of any load effects.

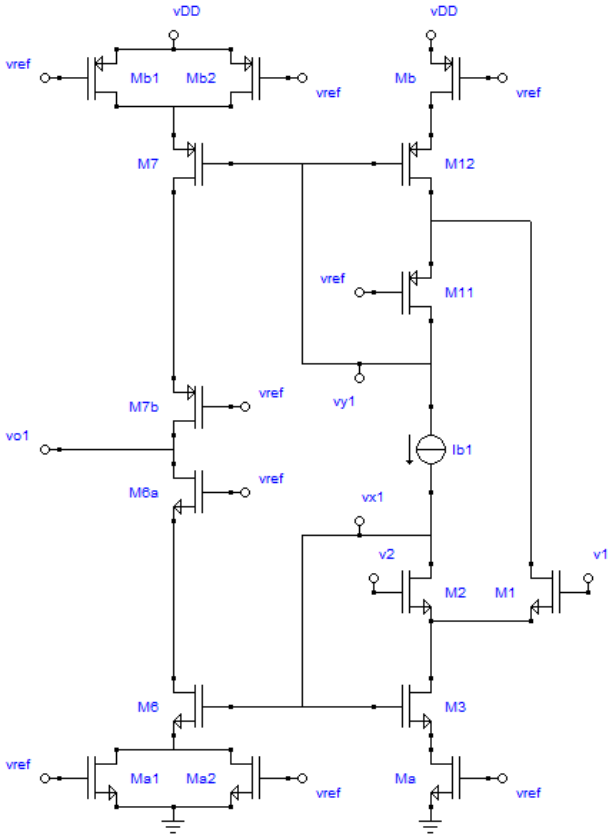


Fig.B. 5: half circuit for calculating the functions needed to determine AVCM

To calculate the transfer functions A, B, D, the circuit of Fig.B.6(c) was taken into account, in which the term GL which represents the load effects due to the circuit of Fig.B.6(b).

$$AV_{CM} = \frac{V_{o1}}{V_{icm}} = \frac{I_L}{V_{icm}} \frac{V_{y1}}{I_L} \frac{V_{o1}}{V_{y1}} + \frac{V_{x1}}{V_{icm}} \frac{V_{o1}}{V_{x1}} \quad (B.3)$$

Gib conductance, instead, replaces the independent current generator and is sized to provide the bias current (I_{bias}) required to operate the structure. For the calculation of the functions C and E, reference will be made to the circuit of Fig.B.7(b) and (c).

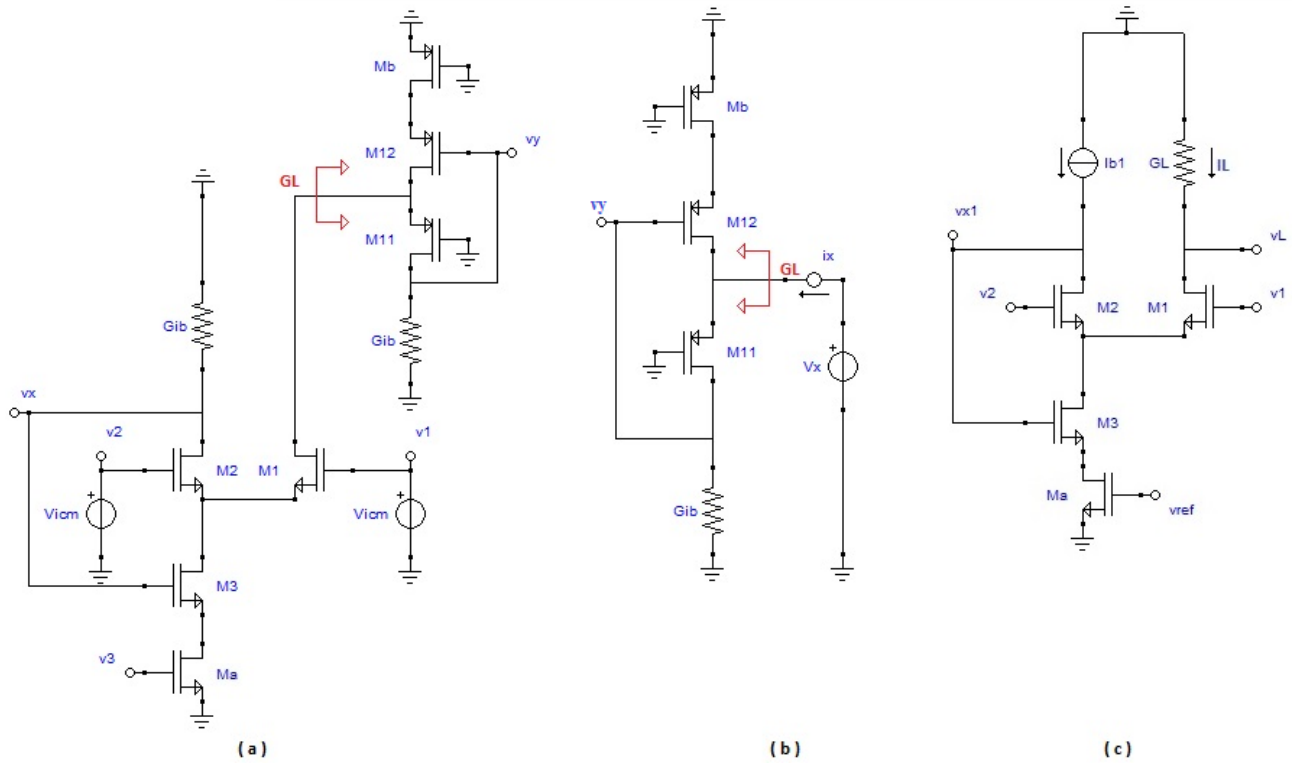


Fig.B. 6: equivalent circuits for partial function calculation

From the circuits shows in Fig.B.6, I define:

$$A = \frac{I_L}{V_{icm}} \quad (B.6)$$

$$B = \frac{V_{y1}}{I_L} \quad (B.7)$$

$$D = \frac{V_{x1}}{V_{icm}} \quad (B.8)$$

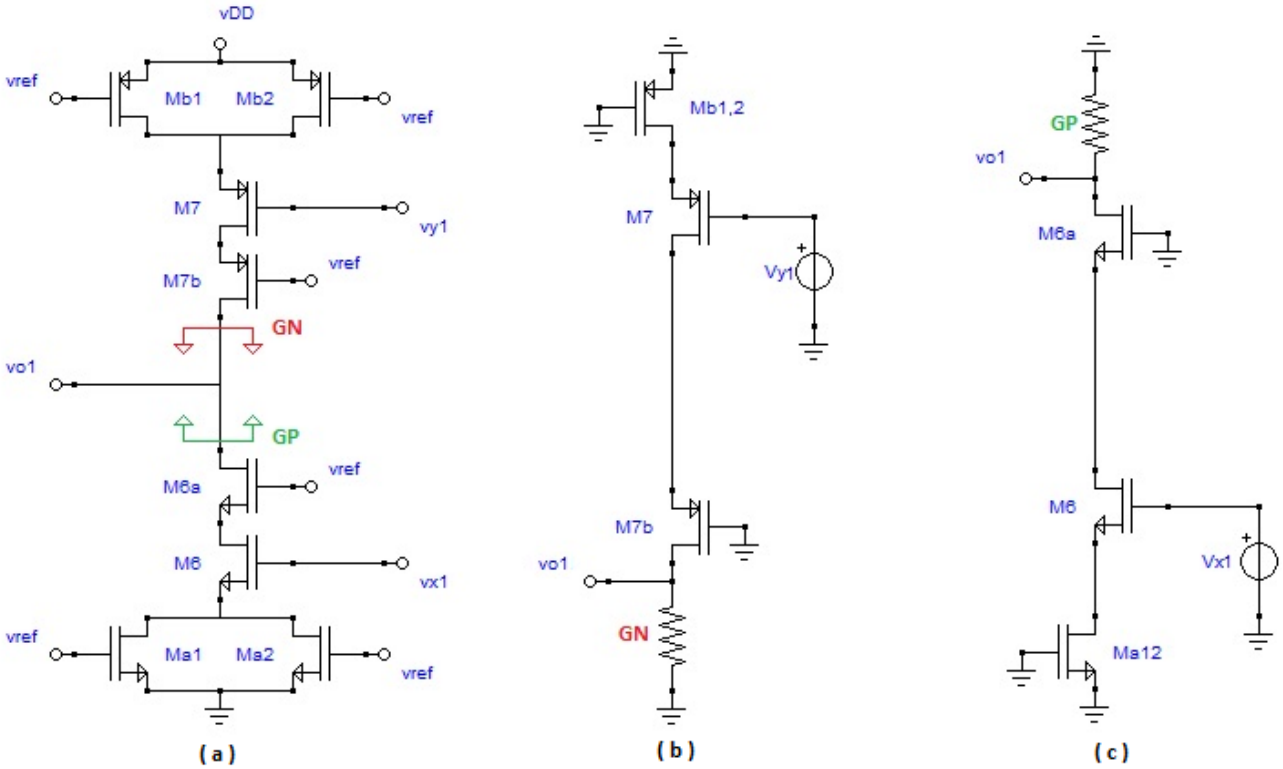


Fig.B. 7: equivalent circuits for partial function calculation

From the circuits shows in Fig.B.7, I define:

$$C = \frac{V_{o1}}{V_{y1}} \quad \text{(B.9)}$$

$$E = \frac{V_{o1}}{V_{x1}} \quad \text{(B.10)}$$

$$V_{o1} = V_{icm}(F_{UP} + F_{DWN}) \quad \text{(B.11)}$$

The difference between the two F_{UP} and F_{DWN} functions causes an output common mode signal not negligible.

B.3 Analysis of the partial transfer functions defined above

In this section, accounts will be performed to determine the transfer functions defined above, A, B, C, D, E, and summarized below.

$$A = \frac{I_L}{V_{icm}} = \frac{V_{oL}G_L}{V_{icm}} \quad \text{(B.6)}$$

$$B = \frac{V_{y1}}{I_L} \quad \text{(B.7)}$$

$$C = \frac{V_{o1}}{V_{y1}} \quad \text{(B.9)}$$

$$D = \frac{V_{x1}}{V_{icm}} \quad \text{(B.8)}$$

$$E = \frac{V_{o1}}{V_{x1}} \quad \text{(B.10)}$$

To perform the accounts, the effect overlay principle will be applied by enabling a source at a time. The sources in question are V_1 and V_2. In the first instance, the GL term is determined to determine the V_{oL}/V_1 and V_{oL}/V_2 transfer functions. From these functions I can then determine the IL/V_1 and IL/V_2 functions.

B.3.1 Conductance (GL) analysis

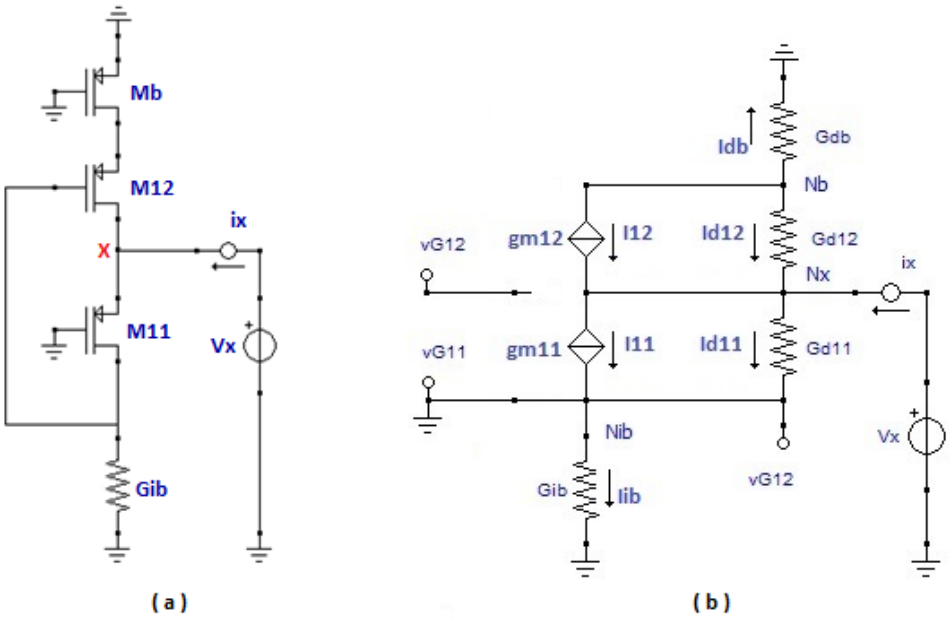


Fig.B. 8: (a) circuit to determine GL; (b) Equivalent Circuit

For the calculation of GL, reference is made to the circuit of Fig.B.8(a) in which, as input to node X, an independent voltage supply Vx was placed. To determine GL we have to derive the ix current, since:

$$G_L = \frac{i_x}{V_x} \tag{B.12}$$

To do this, use the equivalent circuit shown in Fig.B.8(b). In this circuit are indicated the terms Nib, Nx and Nb, the nodes to which the first law of Kirchhoff KCL (Kirchhoff Current Law) will be applied.

As mentioned earlier, proceed with writing the equilibrium equation of currents at the Nib node:

$$I_{11} + I_{d11} = I_{ib} \tag{B.13}$$

$$(V_{S11} - V_{G11})gm_{11} + (V_{S11} - V_{G12})G_{d11} = V_{G12}G_{ib} \tag{B.14}$$

$$V_{S11} = V_x \tag{B.15}$$

$$V_{G11} = 0 \tag{B.16}$$

$$V_x gm_{11} + V_x G_{d11} - V_{G12}G_{d11} = V_{G12}G_{ib} \tag{B.17}$$

By highlighting the terms in V_x and V_{G12}, I get:

$$V_x(G_{d11} + gm_{11}) = V_{G12}(G_{ib} + G_{d11}) \tag{B.18}$$

$$V_{G12} = V_x \frac{(G_{d11}+gm_{11})}{(G_{ib}+G_{d11})} \tag{B.19}$$

To ease the notation, the following form is adopted:

$$V_{G12} = V_x \frac{N_{00}}{D_{00}} \tag{B.20}$$

$$N_{00} = (G_{d11} + gm_{11}) \tag{B.21}$$

$$D_{00} = (G_{ib} + G_{d11}) \tag{B.22}$$

Node Nx:

$$I_{12} + I_{d12} + I_x = I_{11} + I_{d11} \tag{B.23}$$

From the circuit of Fig.B.8(b), I can write:

$$-I_{db} = I_{12} + I_{d12} \quad (B.24)$$

$$I_{ib} = I_{11} + I_{d11} \quad (B.25)$$

replacing (B.24) and (B.25) in (B.23), I get:

$$-I_{db} + I_x = I_{ib} \quad (B.26)$$

$$I_x = I_{ib} + I_{db} \quad (B.27)$$

$$I_x = V_{G12}G_{ib} + V_{S12}G_{db} \quad (B.28)$$

I write KCL at Nb node:

$$I_{12} + I_{d12} + I_{db} = 0 \quad (B.29)$$

$$-(V_{G12} - V_{S12})gm_{12} + (V_{S12} - V_x)G_{d12} + V_{S12}G_{db} = 0 \quad (B.30)$$

$$-V_{G12}gm_{12} + V_{S12}G_{d12} + V_{S12}G_{db} + V_{S12}gm_{12} - V_xG_{d12} = 0 \quad (B.31)$$

$$-V_{G12}gm_{12} + V_{S12}(G_{d12} + G_{db} + gm_{12}) - V_xG_{d12} = 0 \quad (B.32)$$

$$V_{S12}(G_{d12} + G_{db} + gm_{12}) = V_xG_{d12} + V_{G12}gm_{12} \quad (B.33)$$

$$V_{S12} = V_x\frac{G_{d12}}{(G_{d12}+G_{db}+gm_{12})} + V_{G12}\frac{gm_{12}}{(G_{d12}+G_{db}+gm_{12})} \quad (B.34)$$

$$V_{S12} = V_x\frac{G_{d12}}{D_{01}} + V_{G12}\frac{gm_{12}}{D_{01}} \quad (B.35)$$

$$D_{01} = (G_{d12} + G_{db} + gm_{12}) \quad (B.36)$$

Replacing (B.20) in (B.35):

$$V_{G12} = V_x\frac{N_{00}}{D_{00}} \quad (B.20)$$

$$V_{S12} = V_x\frac{G_{d12}}{D_{01}} + V_{G12}\frac{gm_{12}}{D_{01}} \quad (B.34)$$

$$V_{S12} = V_x\frac{G_{d12}}{D_{01}} + V_x\frac{N_{00}}{D_{00}}\frac{gm_{12}}{D_{01}} \quad (B.37)$$

$$N_{00} = (G_{d11} + gm_{11}) \quad (B.21)$$

$$D_{00} = (G_{ib} + G_{d11}) \quad (B.22)$$

$$D_{01} = (G_{d12} + G_{db} + gm_{12}) \quad (B.36)$$

$$V_{S12} = V_x[\frac{G_{d12}D_{00}}{D_{01}D_{00}} + \frac{N_{00}}{D_{00}}\frac{gm_{12}}{D_{01}}] \quad (B.38)$$

From equation (B.28) at Nx Node:

$$I_x = V_{G12}G_{ib} + V_{S12}G_{db} \quad (B.28)$$

Replacing V_{G12} (B.20) and V_{S12} (B.38)

$$I_x = V_x\frac{N_{00}}{D_{00}}G_{ib} + V_x[\frac{G_{d12}D_{00}}{D_{01}D_{00}} + \frac{N_{00}}{D_{00}}\frac{gm_{12}}{D_{01}}]G_{db} \quad (B.39)$$

$$I_x = V_x[\frac{N_{00}D_{01}G_{ib}}{D_{00}D_{01}} + \frac{D_{00}G_{d12}G_{db}}{D_{00}D_{01}} + \frac{N_{00}gm_{12}G_{db}}{D_{00}D_{01}}] \quad (B.40)$$

$$\frac{I_x}{V_x} = [\frac{N_{00}D_{01}G_{ib}}{D_{00}D_{01}} + \frac{D_{00}G_{d12}G_{db}}{D_{00}D_{01}} + \frac{N_{00}gm_{12}G_{db}}{D_{00}D_{01}}] \quad (B.41)$$

$$\frac{I_x}{V_x} = [\frac{N_{T1}}{D_T} + \frac{N_{T2}}{D_T} + \frac{N_{T3}}{D_T}] \quad (B.42)$$

$$N_{T1} = N_{00}D_{01}G_{ib} \quad (B.43)$$

$$N_{T2} = D_{00}G_{d12}G_{db} \quad (B.44)$$

$$N_{T3} = N_{00}gm_{12}G_{db} \quad (B.45)$$

$$D_T = D_{00}D_{01} \quad (B.46)$$

$$N_{00} = (G_{d11} + gm_{11}) \quad (B.21)$$

$$D_{00} = (G_{ib} + G_{d11}) \quad (B.22)$$

$$D_{01} = (G_{d12} + G_{db} + gm_{12}) \quad (B.36)$$

$$N_{T1} = N_{00}D_{01}G_{ib} = (G_{d11} + gm_{11})(G_{d12} + G_{db} + gm_{12})G_{ib} =$$

$$= G_{ib}G_{d11}(G_{d12} + G_{db} + gm_{12}) + G_{ib}gm_{11}(G_{d12} + G_{db} + gm_{12}) \quad \text{(B.47)}$$

$$N_{T2} = D_{00}G_{d12}G_{db} = G_{d12}G_{db}(G_{ib} + G_{d11}) \quad \text{(B.48)}$$

$$N_{T3} = N_{00}gm_{12}G_{db} = gm_{12}G_{db}(G_{d11} + gm_{11}) \quad \text{(B.49)}$$

$$D_T = D_{00}D_{01} = (G_{ib} + G_{d11})(G_{d12} + G_{db} + gm_{12}) =$$
$$= G_{ib}(G_{d12} + G_{db} + gm_{12}) + G_{d11}(G_{d12} + G_{db} + gm_{12}) \quad \text{(B.50)}$$

$$\frac{I_x}{V_x} = [\frac{N_{T1}+N_{T2}+N_{T3}}{D_T}] \quad \text{(B.51)}$$

$$N_T = N_{T1} + N_{T2} + N_{T3} =$$
$$= G_{ib}G_{d11}(G_{d12} + G_{db} + gm_{12}) + +G_{ib}gm_{11}(G_{d12} + G_{db} + gm_{12}) +$$
$$+G_{d12}G_{db}(G_{ib} + G_{d11}) + gm_{12}G_{db}(G_{d11} + gm_{11}) \quad \text{(B.52)}$$

$$D_T = G_{ib}(G_{d12} + G_{db} + gm_{12}) + G_{d11}(G_{d12} + G_{db} + gm_{12}) \quad \text{(B.53)}$$

B.3.2 Vo/V1 analysis

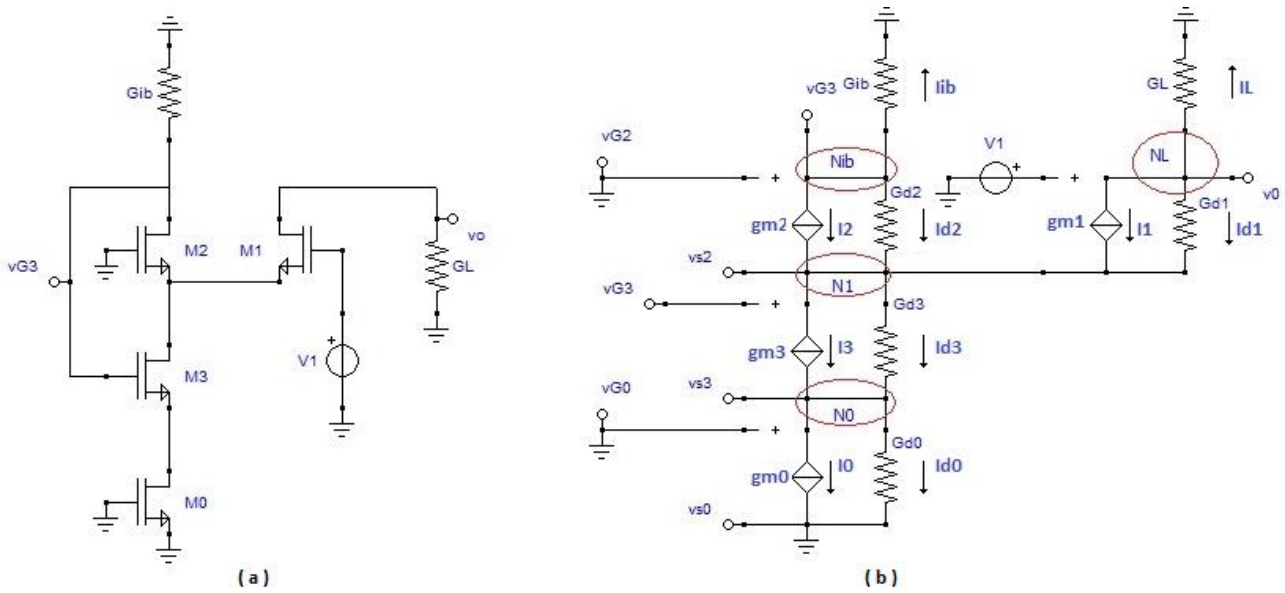


Fig.B. 9: (a) circuit for the calculation of Vo / V1; (b) equivalent circuit

I apply KCL to the node N0 of the circuit depicted in Fig.B.9:

$V_{G0} = V_{S0} = 0$ (B.54)

$I_0 = 0$ (B.55)

$$I_3 + I_{d3} = I_{d0} \quad \text{(B.56)}$$

$$(V_{S2} - V_{S3})G_{d3} + (V_{G3} - V_{S3})gm_3 = V_{S3}G_{d0} \quad \text{(B.57)}$$

$$V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 = V_{S3}G_{d0} \quad \text{(B.58)}$$

$$V_{S2}G_{d3} + V_{G3}gm_3 = V_{S3}(G_{d0} + G_{d3} + gm_3) \quad \text{(B.59)}$$

$$V_{S3} = \frac{V_{S2}G_{d3} + V_{G3}gm_3}{(G_{d0} + G_{d3} + gm_3)} \quad \text{(B.60)}$$

$$V_{S3} = \frac{V_{S2}G_{d3} + V_{G3}gm_3}{D_0} \quad \text{(B.61)}$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad \text{(B.62)}$$

I apply KCL to the node N1:

$$I_{d2} + I_2 + I_{d1} + I_1 = I_3 + I_{d3} \quad \text{(B.63)}$$

$$I_{d2} + I_2 = -I_{ib} \quad \text{(B.64)}$$

$$I_{d1} + I_1 = -I_L \quad \text{(B.65)}$$

Replacing (B.64) and (B.65) in (B.63):

$$-(I_{ib} + I_L) = I_3 + I_{d3} \quad \text{(B.66)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = (V_{G3} - V_{S3})gm_3 + (V_{S2} - V_{S3})G_{d3} \quad \text{(B.67)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 \quad \text{(B.68)}$$

$$-V_{G3}(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad \text{(B.69)}$$

I apply KCL to the node NL:

$$I_1 + I_{d1} + I_L = 0 \quad \text{(B.70)}$$

$$(V_0 - V_{S2})G_{d1} + (V_1 - V_{S2})gm_1 + V_0G_L = 0 \quad \text{(B.71)}$$

$$V_0G_{d1} - V_{S2}G_{d1} + V_1gm_1 - V_{S2}gm_1 + V_0G_L = 0 \quad \text{(B.72)}$$

$$V_0(G_{d1} + G_L) + V_1gm_1 = V_{S2}(G_{d1} + gm_1) \quad \text{(B.73)}$$

$$V_{S2} = V_0 \frac{(G_{d1}+G_L)}{(G_{d1}+gm_1)} + V_1 \frac{gm_1}{(G_{d1}+gm_1)} = V_0 \frac{N_1}{D_1} + V_1 \frac{N_2}{D_1} \quad (B.74)$$

$$D_1 = (G_{d1} + gm_1) \quad (B.75)$$

$$N_1 = (G_{d1} + G_L) \quad (B.76)$$

$$N_2 = gm_1 \quad (B.77)$$

I apply KCL to the node Nib:

$$I_2 + I_{d2} + I_{ib} = 0 \quad (B.78)$$

$$(V_{G3} - V_{S2})G_{d2} - V_{S2}gm_2 + V_{G3}G_{ib} = 0 \quad (B.79)$$

$$V_{G3}G_{d2} - V_{S2}G_{d2} - V_{S2}gm_2 - V_{S2}gm_1 + V_{G3}G_{ib} = 0 \quad (B.80)$$

$$V_{G3}(G_{d2} + G_{ib}) = V_{S2}(G_{d2} + gm_2) \quad (B.81)$$

$$V_{G3} = V_{S2} \frac{(G_{d2}+gm_2)}{(G_{d2}+G_{ib})} = V_{S2} \frac{N_3}{D_3} \quad (B.82)$$

$$D_3 = (G_{d2} + G_{ib}) \quad (B.83)$$

$$N_3 = (G_{d2} + gm_2) \quad (B.84)$$

I take equation (B.69), obtained at node N1:

$$-V_{G3}(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad (B.69)$$

replacing (B.82), (B.74), (B.62) in (B.69)

$$V_{G3} = V_{S2} \frac{(G_{d2}+gm_2)}{(G_{d2}+G_{ib})} = V_{S2} \frac{N_3}{D_3} \quad (B.82)$$

$$V_{S2} = V_0 \frac{(G_{d1}+G_L)}{(G_{d1}+gm_1)} + V_1 \frac{gm_1}{(G_{d1}+gm_1)} = V_0 \frac{N_1}{D_1} + V_1 \frac{N_2}{D_1} \quad (B.74)$$

$$V_{S3} = \frac{V_{S2}G_{d3}+V_{G3}gm_3}{D_0} \quad (B.61)$$

By replacing, equation (B.69) becomes:

$$-V_{S2} \frac{N_3}{D_3}(G_{ib} + gm_3) - V_0G_L = \left(V_0 \frac{N_1}{D_1} + V_1 \frac{N_2}{D_1}\right) G_{d3} - \left(\frac{V_{S2}G_{d3}+V_{G3}gm_3}{D_0}\right)(G_{d3} + gm_3) \quad (B.85)$$

$$-V_{S2} \frac{N_3}{D_3}(G_{ib} + gm_3) - V_0G_L = V_0 \frac{N_1}{D_1}G_{d3} + V_1 \frac{N_2}{D_1}G_{d3} - V_{S2}\left(\frac{G_{d3}+\frac{N_3}{D_3}gm_3}{D_0}\right)(G_{d3} + gm_3) \quad (B.86)$$

$$V_{S2}\left[\left(\frac{G_{d3}+\frac{N_3}{D_3}gm_3}{D_0}\right)(G_{d3} + gm_3) - \frac{N_3}{D_3}(G_{ib} + gm_3)\right] = \quad V_0\left(G_L + \frac{N_1}{D_1}G_{d3}\right) + V_1 \frac{N_2}{D_1}G_{d3} \quad (B.87)$$

replacing (B.74) in (B.87), I have:

$$\left(V_0 \frac{N_1}{D_1} + V_1 \frac{N_2}{D_1}\right)\left[\left(\frac{G_{d3}+\frac{N_3}{D_3}gm_3}{D_0}\right)(G_{d3} + gm_3) - \frac{N_3}{D_3}(G_{ib} + gm_3)\right] =$$

$$= V_0\left(G_L + \frac{N_1}{D_1}G_{d3}\right) + V_1 \frac{N_2}{D_1}G_{d3} \quad (B.88)$$

The equation from this moment will be fragmented to make calculations easier:

$$A \cdot B = C \quad (B.89)$$

where,

$$A = \left(V_0 \frac{N_1}{D_1} + V_1 \frac{N_2}{D_1}\right) \quad (B.90)$$

$$B = \left[\left(\frac{G_{d3}+\frac{N_3}{D_3}gm_3}{D_0}\right)(G_{d3} + gm_3) - \frac{N_3}{D_3}(G_{ib} + gm_3)\right] \quad (B.91)$$

$$C = V_0\left(G_L + \frac{N_1}{D_1}G_{d3}\right) + V_1 \frac{N_2}{D_1}G_{d3} \quad (B.92)$$

$$B = \left[\left(\frac{G_{d3}+\frac{N_3}{D_3}gm_3}{D_0}\right)(G_{d3} + gm_3) - \frac{N_3}{D_3}(G_{ib} + gm_3)\right] =$$

$$= \left[\frac{G_{d3}}{D_0}(G_{d3}+gm_3)+\left(\frac{N_3 gm_3}{D_3 D_0}\right)(G_{d3}+gm_3)-\frac{N_3}{D_3}G_{ib}-\frac{N_3}{D_3}gm_3\right] =$$

$$= \left[\frac{G_{d3}D_3}{D_0 D_3}(G_{d3}+gm_3)+\left(\frac{N_3 gm_3}{D_3 D_0}\right)(G_{d3}+gm_3)-\frac{N_3 D_0}{D_0 D_3}G_{ib}-\frac{N_3 D_0}{D_0 D_3}gm_3\right] =$$

$$= \left[\frac{G_{d3}D_3(G_{d3}+gm_3)+N_3 gm_3(G_{d3}+gm_3)-N_3 D_0 G_{ib}-N_3 D_0 gm_3}{D_0 D_3}\right] = \left[\frac{B'}{D_0 D_3}\right] \quad \text{(B.93)}$$

$$B' = G_{d3}D_3(G_{d3}+gm_3)+N_3 gm_3(G_{d3}+gm_3)-N_3 D_0 G_{ib}-N_3 D_0 gm_3 \quad \text{(B.94)}$$

$$B' = G_{d3}D_3(G_{d3}+gm_3)+N_3 gm_3(G_{d3}+gm_3)-N_3 D_0 G_{ib}-N_3 D_0 gm_3 \quad \text{(B.94)}$$

where D_0, D_3 e N_3, are:

$$D_0 = (gm_3+G_{d3}+G_{d0}) \quad \text{(B.62)}$$

$$D_3 = (G_{ib}+G_{d2}) \quad \text{(B.83)}$$

$$N_3 = (G_{d2}+gm_2) \quad \text{(B.84)}$$

$$B' = G_{d3}(G_{ib}+G_{d2})(G_{d3}+gm_3)+gm_3(G_{d2}+gm_2)(G_{d3}+gm_3)+$$
$$-(G_{d2}+gm_2)(gm_3+G_{d3}+G_{d0})G_{ib}-(G_{d2}+gm_2)(gm_3+G_{d3}+G_{d0})gm_3 = \quad \text{(B.95)}$$

$$= G_{d3}(G_{ib}G_{d3}+G_{ib}gm_3+G_{d2}G_{d3}+G_{d2}gm_3)+gm_3(G_{d2}G_{d3}+G_{d2}gm_3+gm_2G_{d3}+gm_2gm_3)$$
$$-G_{ib}(G_{d2}gm_3+G_{d2}G_{d3}+G_{d2}G_{d0}+gm_2gm_3+gm_2G_{d3}+gm_2G_{d0})+$$
$$-gm_3(G_{d2}gm_3+G_{d2}G_{d3}+G_{d2}G_{d0}+gm_2gm_3+gm_2G_{d3}+gm_2G_{d0}) = \quad \text{(B.96)}$$

$$= G_{ib}G_{d3}^2+G_{ib}gm_3G_{d3}+G_{d3}^2G_{d2}+G_{d2}gm_3G_{d3}+G_{d2}G_{d3}gm_3+G_{d2}gm_3^2+gm_3gm_2G_{d3}+$$
$$gm_2gm_3^2+$$
$$-G_{ib}G_{d2}gm_3-G_{ib}G_{d2}G_{d3}-G_{ib}G_{d2}G_{d0}-G_{ib}gm_2gm_3-G_{ib}gm_2G_{d3}-G_{ib}gm_2G_{d0}+$$
$$-G_{d2}gm_3^2-G_{d2}G_{d3}gm_3-gm_3G_{d2}G_{d0}-gm_2gm_3^2-gm_3gm_2G_{d3}-gm_3gm_2G_{d0} \quad \text{(B.97)}$$

simplifying I get:

$$B' = G_{ib}G_{d3}^2+G_{ib}gm_3G_{d3}+G_{d3}^2G_{d2}+G_{d2}gm_3G_{d3}+$$
$$-G_{ib}G_{d2}gm_3-G_{ib}G_{d2}G_{d3}-G_{ib}G_{d2}G_{d0}-G_{ib}gm_2gm_3-G_{ib}gm_2G_{d3}-G_{ib}gm_2G_{d0}+$$
$$-gm_3G_{d2}G_{d0}-gm_3gm_2G_{d0} \quad \text{(B.98)}$$

As regards the product of terms A and B, I can write:

$$A\cdot B = A\cdot\frac{B'}{D_0 D_3} \quad \text{(B.99)}$$

$$A\cdot B = \left(V_0\frac{N_1}{D_1}+V_1\frac{N_2}{D_1}\right)\cdot\frac{B'}{D_0 D_3} = V_0\frac{N_1 B'}{D_1 D_0 D_3}+V_1\frac{N_2 B'}{D_1 D_0 D_3} \quad \text{(B.100)}$$

As regards the product of term C, I can write:

$$C = V_0\left(G_L+\frac{N_1}{D_1}G_{d3}\right)+V_1\frac{N_2}{D_1}G_{d3} = V_0\left(\frac{G_L D_1+N_1 G_{d3}}{D_1}\right)+V_1\frac{N_2 G_{d3}}{D_1} \quad \text{(B.101)}$$

$$A\cdot B = C \quad \text{(B.89)}$$

$$V_0\frac{N_1 B'}{D_1 D_0 D_3}+V_1\frac{N_2 B'}{D_1 D_0 D_3} = V_0\left(\frac{G_L D_1+N_1 G_{d3}}{D_1}\right)+V_1\frac{N_2 G_{d3}}{D_1} \quad \text{(B.102)}$$

reworking and simplifying the common terms right and left, the equation can be rewritten as:

$$V_0 N_1 B'+V_1 N_2 B' = V_0 D_0 D_3(G_L D_1+N_1 G_{d3})+V_1 D_0 D_3 N_2 G_{d3} \quad \text{(B.103)}$$

$$V_0[N_1 B'-D_0 D_3(G_L D_1+N_1 G_{d3})] = V_1[D_0 D_3 N_2 G_{d3}-N_2 B'] \quad \text{(B.104)}$$

$$\frac{V_0}{V_1} = \frac{D_0 D_3 N_2 G_{d3}-N_2 B'}{N_1 B'-D_0 D_3(G_L D_1+N_1 G_{d3})} = \frac{N_T}{D_T} \quad \text{(B.105)}$$

calculations for the numerator N_T and for the denominator D_T, will be performed separately. First, however, I recall the expressions of terms D_0, D_1, D_3, N_1, N_2:

$$D_0 = (gm_3+G_{d3}+G_{d0}) \quad \text{(B.62)}$$

$$D_1 = (gm_1+G_{d1}) \quad \text{(B.75)}$$

$$D_3 = (G_{ib}+G_{d2}) \quad \text{(B.83)}$$

$$N_1 = (G_L+G_{d1}) \quad \text{(B.76)}$$

$$N_2 = gm_1 \quad \text{(B.77)}$$

$$D_0 \cdot D_3 = (gm_3 + G_{d3} + G_{d0})(G_{ib} + G_{d2}) =$$
$$= (gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.106)}$$

$$D_0D_3N_2G_{d3} = D_0D_3gm_1G_{d3} =$$
$$= (gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})gm_1G_{d3} = \quad \text{(B.107)}$$
$$= gm_1(gm_3G_{ib}G_{d3} + gm_3G_{d2}G_{d3} + G_{d3}G_{ib}G_{d3} + G_{d3}G_{d2}G_{d3} + G_{d0}G_{ib}G_{d3} + G_{d0}G_{d2}G_{d3})$$

$$-N_2B' = -gm_1B' = \quad \text{(B.108)}$$

$$-gm_1B' = -gm_1(G_{ib}G_{d3}^2 + G_{ib}gm_3G_{d3} + G_{d3}^2G_{d2} + G_{d2}gm_3G_{d3} +$$
$$-G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} - G_{ib}gm_2G_{d0} +$$
$$-gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0})$$

by putting together the members of the numerator, I get:

$$N_T = D_0D_3N_2G_{d3} - N_2B' =$$
$$= gm_1\left(gm_3G_{ib}G_{d3} + gm_3G_{d2}G_{d3} + G_{ib}G_{d3}^2 + G_{d3}^2G_{d2} + G_{d0}G_{ib}G_{d3} + G_{d0}G_{d2}G_{d3}\right) +$$
$$gm_1(-G_{ib}G_{d3}^2 - gm_3G_{ib}G_{d3} - G_{d3}^2G_{d2} - gm_3G_{d2}G_{d3} +$$
$$+G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} + G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} +$$
$$+gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0}) \quad \text{(B.109)}$$

Simplifying, I get:

$$N_T = gm_1(G_{d0}G_{ib}G_{d3} + G_{d0}G_{d2}G_{d3} + G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} +$$
$$+G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} + gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0}) \quad \text{(B.110)}$$

calculate the individual denominator members :

$$D_T = N_1B' - D_0D_3(G_LD_1 + N_1G_{d3}) =$$
$$= (G_L + G_{d1})B' - D_0D_3[G_LD_1 + (G_L + G_{d1})G_{d3}] =$$
$$= G_LB' + G_{d1}B' - G_L(D_0D_3D_1) - G_L(D_0D_3G_{d3}) - G_{d1}(D_0D_3G_{d3}) =$$
$$= G_L[B' - (D_0D_3D_1) - (D_0D_3G_{d3})] + G_{d1}[B' - (D_0D_3G_{d3})] \quad \text{(B.111)}$$

$$-(D_0D_3D_1) = -D_0D_3(gm_1 + G_{d1}) = -D_0D_3gm_1 - D_0D_3G_{d1} =$$
$$= -gm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$$
$$-G_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.112)}$$

$$-(D_0D_3G_{d3}) =$$
$$= -G_{d3}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.113)}$$

$$D_T = G_L[B' - (D_0D_3D_1) - (D_0D_3G_{d3})] + G_{d1}[B' - (D_0D_3G_{d3})] \quad \text{(B.114)}$$

$$D_T = G_L[X] + G_{d1}[Y] \quad \text{(B.115)}$$

$$X = B' - (D_0D_3D_1) - (D_0D_3G_{d3}) \quad \text{(B.116)}$$

$$Y = B' - (D_0D_3G_{d3}) \quad \text{(B.117)}$$

$$X = B' - (D_0D_3D_1) - (D_0D_3G_{d3}) \quad \text{(B.116)}$$

$$B' = G_{ib}G_{d3}^2 + G_{ib}gm_3G_{d3} + G_{d3}^2G_{d2} + G_{d2}gm_3G_{d3} +$$
$$-G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} - G_{ib}gm_2G_{d0} +$$
$$-gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0} \quad \text{(B.98)}$$

$$-(D_0D_3D_1) = -gm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$$
$$-G_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.112)}$$

$$-(D_0D_3G_{d3}) = -G_{d3}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.113)}$$

by making the appropriate simplifications, from (B.116), I get:

$$X = -G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} - G_{ib}gm_2G_{d0} +$$
$$-gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0} +$$

$$-gm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$$
$$-G_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$$
$$-G_{d3}(G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.118)}$$

$$Y = B' - (D_0D_3G_{d3}) \quad \text{(B.119)}$$

$$B' = G_{ib}G_{d3}^2 + G_{ib}gm_3G_{d3} + G_{d3}^2G_{d2} + G_{d2}gm_3G_{d3} +$$
$$-G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} - G_{ib}gm_2G_{d0} +$$
$$-gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0} \quad \text{(B.98)}$$

$$-(D_0D_3G_{d3}) = -G_{d3}(gm_3G_{ib} + gm_3G_{d2} + \quad G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.113)}$$

by making the appropriate simplifications, from (B.117), I get:

$$Y = B' - (D_0D_3G_{d3}) \quad \text{(B.117)}$$

$$Y = -G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} - G_{ib}gm_2G_{d0} +$$
$$-gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0} +$$
$$-G_{d3}(G_{d0}G_{ib} + G_{d0}G_{d2}) \quad \text{(B.120)}$$

$$D_T = G_L[X] + G_{d1}[Y] \quad \text{(B.121)}$$

$$G_L[X] = G_L[-G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} - G_{ib}gm_2G_{d0}$$
$$-gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0} +$$
$$-gm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$$
$$-G_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$$
$$-G_{d3}(G_{d0}G_{ib} + G_{d0}G_{d2}] \quad \text{(B.122)}$$

$$G_{d1}[Y] = G_{d1}[-G_{ib}G_{d2}gm_3 - G_{ib}G_{d2}G_{d3} - G_{ib}G_{d2}G_{d0} - G_{ib}gm_2gm_3 - G_{ib}gm_2G_{d3} -$$
$$G_{ib}gm_2G_{d0} - gm_3G_{d2}G_{d0} - gm_3gm_2G_{d0} - G_{d3}(G_{d0}G_{ib} + G_{d0}G_{d2})] \quad \text{(B.123)}$$

D_T can be write as:

$$D_T = -G_L[G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} + G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} +$$
$$+gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0} +$$
$$+gm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$$
$$+G_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$$
$$+G_{d3}(G_{d0}G_{ib} + G_{d0}G_{d2}] +$$
$$+G_{d1}[G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} + G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} +$$
$$+gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0} +$$
$$+G_{d3}(G_{d0}G_{ib} + G_{d0}G_{d2})] \quad \text{(B.124)}$$

in conclusion, the Vo/V1 transfer function can be written:

$$\frac{V_0}{V_1} = \frac{N_T}{D_T} = \quad \text{(B.125)}$$
$$= -gm_1(G_{d0}G_{ib}G_{d3} + G_{d0}G_{d2}G_{d3} + G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} +$$
$$+G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} + gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0})$$

$$G_L[G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} + G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} +$$
$$+gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0} + gm_1gm_3G_{ib} + gm_1gm_3G_{d2} + gm_1G_{d3}G_{ib} + gm_1G_{d3}G_{d2} +$$
$$+gm_1G_{d0}G_{ib} + gm_1G_{d0}G_{d2} + G_{d1}gm_3G_{ib} + gm_3G_{d2}G_{d1} + G_{d3}G_{ib}G_{d1} + G_{d3}G_{d2}G_{d1} +$$
$$+G_{d0}G_{ib}G_{d1} + G_{d0}G_{d2}G_{d1} + G_{d3}G_{d0}G_{ib} + G_{d0}G_{d2}G_{d3}] +$$
$$+G_{d1}[G_{ib}G_{d2}gm_3 + G_{ib}G_{d2}G_{d3} + G_{ib}G_{d2}G_{d0} + G_{ib}gm_2gm_3 + G_{ib}gm_2G_{d3} + G_{ib}gm_2G_{d0} +$$
$$+gm_3G_{d2}G_{d0} + gm_3gm_2G_{d0} + G_{d3}G_{d0}G_{ib} + G_{d0}G_{d2}G_{d3}]$$

B.3.3 Vo/V_2 analysis

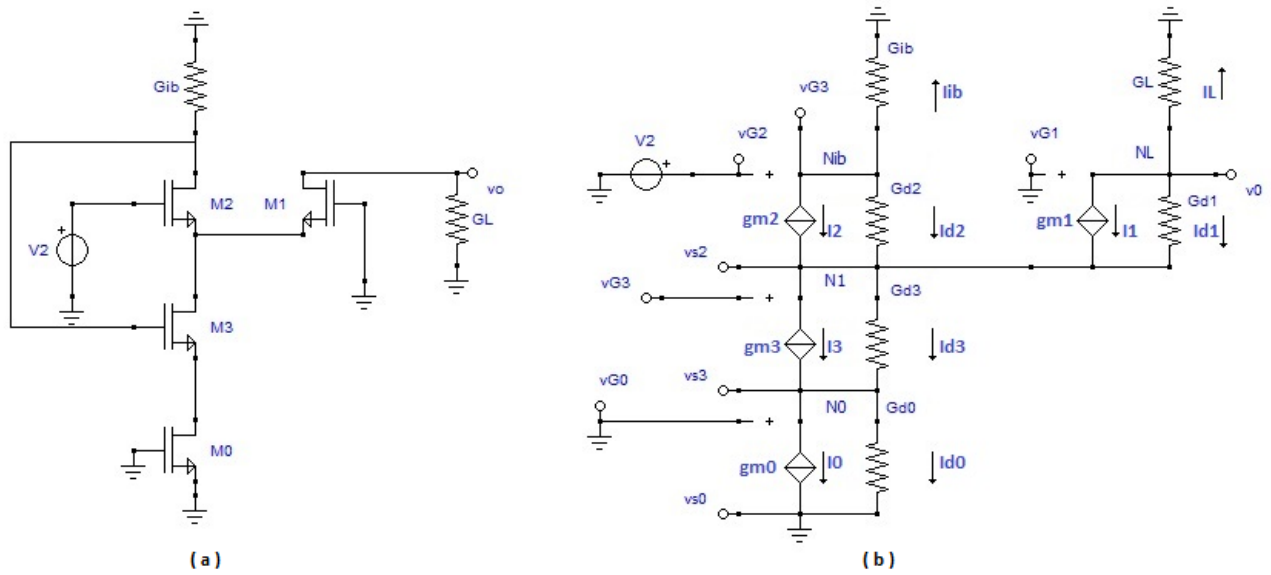


Fig.B. 10: (a) circuit for the calculation of Vo/V2; (b) equivalent circuit

For the calculation of all the following transfer functions, the same procedure used to calculate the first transfer function was followed, so I omit the comments.

I apply KCL to the node N0 of the circuit depicted in Fig.B.10:

$V_{G0} = V_{S0} = 0$ (B.126)

$I_0 = 0$ (B.127)

$I_3 + I_{d3} = I_{d0}$ (B.128)

$(V_{S2} - V_{S3})G_{d3} + (V_{G3} - V_{S3})gm_3 = V_{S3}G_{d0}$ (B.129)

$V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 = V_{S3}G_{d0}$ (B.130)

$V_{S2}G_{d3} + V_{G3}gm_3 = V_{S3}(G_{d0} + G_{d3} + gm_3)$ (B.131)

$V_{S3} = \frac{V_{S2}G_{d3} + V_{G3}gm_3}{(G_{d0} + G_{d3} + gm_3)}$ (B.132)

$V_{S3} = \frac{V_{S2}G_{d3} + V_{G3}gm_3}{D_0}$ (B.133)

$D_0 = (G_{d0} + G_{d3} + gm_3)$ (B.134)

I apply KCL to the node N1:

$I_{d2} + I_2 + I_{d1} + I_1 = I_3 + I_{d3}$ (B.135)

$I_{d2} + I_2 = -I_{ib}$ (B.136)

$I_{d1} + I_1 = -I_L$ (B.137)

$-(I_{ib} + I_L) = I_3 + I_{d3}$ (B.138)

$-(V_{G3}G_{ib} + V_0G_L) = (V_{G3} - V_{S3})gm_3 + (V_{S2} - V_{S3})G_{d3}$ (B.139)

$-(V_{G3}G_{ib} + V_0G_L) = V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3$ (B.140)

$-V_{G3}(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3)$ (B.141)

I apply KCL to the node NL:

$I_1 + I_{d1} + I_L = 0$ (B.142)

$(V_0 - V_{S2})G_{d1} + (-V_{S2})gm_1 + V_0G_L = 0$ (B.143)

$V_0G_{d1} - V_{S2}G_{d1} - V_{S2}gm_1 + V_0G_L = 0$ (B.144)

$V_0(G_{d1} + G_L) = V_{S2}(G_{d1} + gm_1)$ (B.145)

$$V_{S2} = V_0 \frac{(G_{d1}+G_L)}{(G_{d1}+gm_1)} = V_0 \frac{N_1}{D_1} \quad \text{(B.146)}$$

$$D_1 = (G_{d1} + gm_1) \quad \text{(B.147)}$$

$$N_1 = (G_{d1} + G_L) \quad \text{(B.148)}$$

I apply KCL to the node Nib:

$$I_2 + I_{d2} + I_{ib} = 0 \quad \text{(B.149)}$$

$$(V_{G3} - V_{S2})G_{d2} + (V_2 - V_{S2})gm_2 + V_{G3}G_{ib} = 0 \quad \text{(B.150)}$$

$$V_{G3}G_{d2} - V_{S2}G_{d2} + V_2gm_2 - V_{S2}gm_2 + V_{G3}G_{ib} = 0 \quad \text{(B.151)}$$

$$V_{G3}(G_{d2} + G_{ib}) = V_{S2}(G_{d2} + gm_2) - V_2gm_2 \quad \text{(B.152)}$$

$$V_{G3} = V_{S2} \frac{(G_{d2}+gm_2)}{(G_{d2}+G_{ib})} - V_2 \frac{gm_2}{(G_{d2}+G_{ib})} = V_{S2} \frac{N_3}{D_3} - V_2 \frac{N_4}{D_3} \quad \text{(B.153)}$$

$$V_{G3} = V_0 \frac{N_1}{D_1}\frac{N_3}{D_3} - V_2 \frac{N_4}{D_3} \quad \text{(B.154)}$$

$$D_3 = (G_{d2} + G_{ib}) \quad \text{(B.155)}$$

$$N_3 = (G_{d2} + gm_2) \quad \text{(B.156)}$$

$$N_4 = gm_2 \quad \text{(B.157)}$$

I consider (B.133):

$$V_{S3} = \frac{V_{S2}G_{d3}+V_{G3}gm_3}{D_0} \quad \text{(B.133)}$$

$$V_{S3} = \frac{V_0\frac{N_1}{D_1}G_{d3}+V_0\frac{N_1N_3}{D_1D_3}gm_3-\frac{N_4}{D_3}gm_3}{D_0} \quad \text{(B.158)}$$

$$V_{S3} = \frac{V_0\frac{N_1D_3}{D_1D_3}G_{d3}+V_0\frac{N_1N_3}{D_1D_3}gm_3-V_2\frac{N_4D_1}{D_3D_1}gm_3}{D_0} \quad \text{(B.159)}$$

$$V_{S3} = \frac{V_0N_1D_3G_{d3}+V_0N_1N_3gm_3-V_2N_4D_1gm_3}{D_0D_1D_3} \quad \text{(B.160)}$$

$$V_{S3} = \frac{V_0(N_1D_3G_{d3}+N_1N_3gm_3)-V_2N_4D_1gm_3}{D_0D_1D_3} \quad \text{(B.161)}$$

I consider (B.141):

$$-V_{G3}(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad \text{(B.141)}$$

$$V_{G3} = V_0 \frac{N_1}{D_1}\frac{N_3}{D_3} - V_2 \frac{N_4D_1}{D_1D_3} \quad \text{(B.152)}$$

$$V_{S2} = V_0 \frac{N_1}{D_1} \quad \text{(B.146)}$$

$$V_{S3} = \frac{V_0(N_1D_3G_{d3}+N_1N_3gm_3)-V_2N_4D_1gm_3}{D_0D_1D_3} \quad \text{(B.156)}$$

$$-\left(V_0 \frac{N_1}{D_1}\frac{N_3}{D_3} - V_2 \frac{N_4D_1}{D_1D_3}\right)(G_{ib} + gm_3) - V_0G_L \quad =$$

$$= V_0 \frac{N_1}{D_1}G_{d3} - \frac{V_0(N_1D_3G_{d3}+N_1N_3gm_3)-V_2N_4D_1gm_3}{D_0D_1D_3}(G_{d3} + gm_3) \quad \text{(B.162)}$$

$$\frac{-V_0[N_1N_3(G_{ib}+gm_3)+G_LD_1D_3]+V_2N_4D_1(G_{ib}+gm_3)}{D_1D_3} =$$

$$= V_0 \frac{N_1D_0D_3G_{d3}}{D_0D_1D_3} - \frac{V_0(N_1D_3G_{d3}+N_1N_3gm_3)(G_{d3}+gm_3)-V_2N_4D_1gm_3(G_{d3}+gm_3)}{D_0D_1D_3} \quad \text{(B.163)}$$

$$-V_0D_0[N_1N_3(G_{ib} + gm_3) + G_LD_1D_3] + V_2N_4D_0D_1(G_{ib} + gm_3) =$$

$$= V_0N_1D_0D_3G_{d3} - V_0(N_1D_3G_{d3} + N_1N_3gm_3)(G_{d3} + gm_3) - V_2N_4D_1gm_3(G_{d3} + gm_3)] \quad \text{(B.164)}$$

By highlighting the terms in V_0 and V_2, I get:

$$V_0[-D_0N_1N_3(G_{ib} + gm_3) - G_LD_0D_1D_3 - N_1D_0D_3G_{d3} + (N_1D_3G_{d3} + N_1N_3gm_3)(G_{d3} + gm_3)] =$$

$$= V_2[N_4D_1gm_3(G_{d3} + gm_3) - N_4D_0D_1(G_{ib} + gm_3)] \quad \text{(B.165)}$$

The transfer function becomes:

$$\frac{V_0}{V_2}=\frac{N_T}{D_T}=$$

$$=\frac{[N_4D_1gm_3(G_{d3}+gm_3)-N_4D_0D_1(G_{ib}+gm_3)]}{[-D_0N_1N_3(G_{ib}+gm_3)-G_LD_0D_1D_3-N_1D_0D_3G_{d3}+(N_1D_3G_{d3}+N_1N_3gm_3)(G_{d3}+gm_3)]} \quad \text{(B.166)}$$

Calculation of the numerator (NT), of the function found:

$$N_4=gm_2 \quad \text{(B.157)}$$

$$D_0=(gm_3+G_{d3}+G_{d0}) \quad \text{(B.134)}$$

$$D_1=(gm_1+G_{d1}) \quad \text{(B.147)}$$

$$N_T=[N_4D_1gm_3(G_{d3}+gm_3)-N_4D_0D_1(G_{ib}+gm_3)]=N_{T1}+N_{T2} \quad \text{(B.167)}$$

$$N_{T1}=N_4D_1gm_3(G_{d3}+gm_3)=$$

$$=N_4(gm_1+G_{d1})gm_3(G_{d3}+gm_3)=$$

$$=gm_2gm_3(gm_1+G_{d1})(G_{d3}+gm_3)=$$

$$=gm_2gm_3(gm_1G_{d3}+gm_1gm_3+G_{d1}G_{d3}+G_{d1}gm_3)= \quad \text{(B.168)}$$

$$N_{T2}=-N_4D_0D_1(G_{ib}+gm_3)=-gm_2(gm_3+G_{d3}+G_{d0})(gm_1+G_{d1})(G_{ib}+gm_3)=$$

$$=-gm_2(gm_3+G_{d3}+G_{d0})(gm_1G_{ib}+gm_1gm_3+G_{d1}G_{ib}+G_{d1}gm_3)=$$

$$=-gm_2gm_3\ \ (gm_1G_{ib}+gm_1gm_3+G_{d1}G_{ib}+G_{d1}gm_3)+$$

$$-gm_2G_{d3}(gm_1G_{ib}+gm_1gm_3+G_{d1}G_{ib}+G_{d1}gm_3)+$$

$$-gm_2G_{d0}(gm_1G_{ib}+gm_1gm_3+G_{d1}G_{ib}+G_{d1}gm_3) \quad \text{(B.169)}$$

$$N_T=N_{T1}+N_{T2}=-gm_2gm_3\ \ (gm_1G_{ib}+G_{d1}G_{ib})+$$

$$-gm_2G_{d3}(gm_1G_{ib}+G_{d1}G_{ib})+$$

$$-gm_2G_{d0}(gm_1G_{ib}+gm_1gm_3+G_{d1}G_{ib}+G_{d1}gm_3) \quad \text{(B.170)}$$

D_T calculation:

$$=\frac{[N_4D_1gm_3(G_{d3}+gm_3)-N_4D_0D_1(G_{ib}+gm_3)]}{[-D_0N_1N_3(G_{ib}+gm_3)-G_LD_0D_1D_3-N_1D_0D_3G_{d3}+(N_1D_3G_{d3}+N_1N_3gm_3)(G_{d3}+gm_3)]} \quad \text{(B.166)}$$

$$D_T=-D_0N_1N_3(G_{ib}+gm_3)-G_LD_1D_0D_3-N_1D_0D_3G_{d3}+(N_1D_3G_{d3}+N_1N_3gm_3)(G_{d3}+gm_3)$$

where,

$$D_0=(gm_3+G_{d3}+G_{d0}) \quad \text{(B.134)}$$

$$D_1=(gm_1+G_{d1}) \quad \text{(B.147)}$$

$$D_3=(G_{ib}+G_{d2}) \quad \text{(B.155)}$$

$$N_1=(G_L+G_{d1}) \quad \text{(B.148)}$$

$$N_3=(G_{d2}+gm_2) \quad \text{(B.156)}$$

$$D_0D_3=(gm_3+G_{d3}+G_{d0})(G_{ib}+G_{d2})=$$

$$=(gm_3G_{ib}+gm_3G_{d2}+G_{d3}G_{ib}+G_{d3}G_{d2}+G_{d0}G_{ib}+G_{d0}G_{d2}) \quad \text{(B.171)}$$

$$N_1N_3=(G_L+G_{d1})(G_{d2}+gm_2)=$$

$$=(G_LG_{d2}+G_Lgm_2+G_{d1}G_{d2}+G_{d1}gm_2) \quad \text{(B.172)}$$

$$N_1D_3=(G_L+G_{d1})(G_{ib}+G_{d2})=$$

$$=(G_LG_{ib}+G_LG_{d2}+G_{d1}G_{ib}+G_{d1}G_{d2}) \quad \text{(B.173)}$$

$$D_0(G_{ib}+gm_3)=(gm_3+G_{d3}+G_{d0})(G_{ib}+gm_3)=$$

$$(gm_3G_{ib}+gm_3^2+G_{d3}G_{ib}+G_{d3}gm_3+G_{d0}G_{ib}+G_{d0}gm_3) \quad \text{(B.174)}$$

$$D_T=-D_0(G_{ib}+gm_3)N_1N_3-G_LD_1D_0D_3-N_1D_0D_3G_{d3}+$$

$$+(N_1D_3G_{d3}^2+N_1D_3G_{d3}gm_3+N_1N_3gm_3G_{d3}+N_1N_3gm_3^2) \quad \text{(B.175)}$$

$$D_T=A+B+C+D+E+F+G \quad \text{(B.176)}$$

$$A=-D_0(G_{ib}+gm_3)N_1N_3=-(gm_3G_{ib}+gm_3^2+G_{d3}G_{ib}+G_{d3}gm_3+G_{d0}G_{ib}+G_{d0}gm_3)N_1N_3$$

$$=-(gm_3G_{ib}+gm_3^2+G_{d3}G_{ib}+G_{d3}gm_3+G_{d0}G_{ib}+G_{d0}gm_3)N_1N_3=$$

$= -(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3)(G_LG_{d2} + G_Lgm_2 + G_{d1}G_{d2} + G_{d1}gm_2) =$

$= -G_LG_{d2}(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_Lgm_2(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_{d1}G_{d2}(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_{d1}gm_2(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3)$ (B.177)

$B = -G_LD_1D_0D_3 =$

$=-(G_Lgm_1 + G_LG_{d1})(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) =$

$= -G_Lgm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$
$-G_LG_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$ (B.178)

$C = -N_1D_0D_3G_{d3} = -G_{d3}(G_L + G_{d1})D_0D_3 =$

$= -(G_{d3}G_L + G_{d3}G_{d1})(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) =$

$-G_{d3}G_L(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$
$-G_{d3}G_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$ (B.179)

$D = N_1D_3G_{d3}^2 = G_{d3}^2(G_LG_{ib} + G_LG_{d2} + G_{d1}G_{ib} + G_{d1}G_{d2})$ (B.180)

$E = N_1D_3G_{d3}gm_3 = G_{d3}gm_3(G_LG_{ib} + G_LG_{d2} + G_{d1}G_{ib} + G_{d1}G_{d2})$ (B.181)

$F = N_1N_3gm_3G_{d3} = G_{d3}gm_3(G_LG_{d2} + G_Lgm_2 + G_{d1}G_{d2} + G_{d1}gm_2)$ (B.182)

$G = N_1N_3gm_3^2 = gm_3^2(G_LG_{d2} + G_Lgm_2 + G_{d1}G_{d2} + G_{d1}gm_2)$ (B.183)

simplifying some terms:

$A = -G_LG_{d2}(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_Lgm_2(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_{d1}G_{d2}(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_{d1}gm_2(gm_3G_{ib} + gm_3^2 + G_{d3}G_{ib} + G_{d3}gm_3 + G_{d0}G_{ib} + G_{d0}gm_3)$ (B.184)

$B = -G_Lgm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$
$-G_LG_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$ (B.185)

$C = -G_{d3}G_L(gm_3G_{ib} + gm_3G_{d2} + \quad G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$
$-G_{d3}G_{d1}(gm_3G_{ib} + gm_3G_{d2} + \quad G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$ (B.186)

$D = N_1D_3G_{d3}^2 = G_{d3}^2(G_LG_{ib} + G_LG_{d2} + G_{d1}G_{ib} + G_{d1}G_{d2})$ (B.187)

$E = N_1D_3G_{d3}gm_3 = G_{d3}gm_3(G_LG_{ib} + G_LG_{d2} + G_{d1}G_{ib} + G_{d1}G_{d2})$ (B.188)

$F = N_1N_3gm_3G_{d3} = G_{d3}gm_3(G_LG_{d2} + G_Lgm_2 + G_{d1}G_{d2} + G_{d1}gm_2)$ (B.189)

$G = N_1N_3gm_3^2 = gm_3^2(G_LG_{d2} + G_Lgm_2 + G_{d1}G_{d2} + G_{d1}gm_2)$ (B.190)

The terms D, E, F, G simplify completely:

$A = -G_LG_{d2}(gm_3G_{ib} + G_{d3}G_{ib} + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_Lgm_2(gm_3G_{ib} + G_{d3}G_{ib} + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_{d1}G_{d2}(gm_3G_{ib} + G_{d3}G_{ib} + G_{d0}G_{ib} + G_{d0}gm_3) +$
$-G_{d1}gm_2(gm_3G_{ib} + G_{d3}G_{ib} + G_{d0}G_{ib} + G_{d0}gm_3)$ (B.191)

$B = -G_Lgm_1(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2}) +$
$-G_LG_{d1}(gm_3G_{ib} + gm_3G_{d2} + G_{d3}G_{ib} + G_{d3}G_{d2} + G_{d0}G_{ib} + G_{d0}G_{d2})$ (B.192)

$C = -G_{d3}G_L(G_{d0}G_{ib} + G_{d0}G_{d2}) +$
$-G_{d3}G_{d1}(G_{d0}G_{ib} + G_{d0}G_{d2})$ (B.193)

B.3.4 V_{y1}/I_L analysis

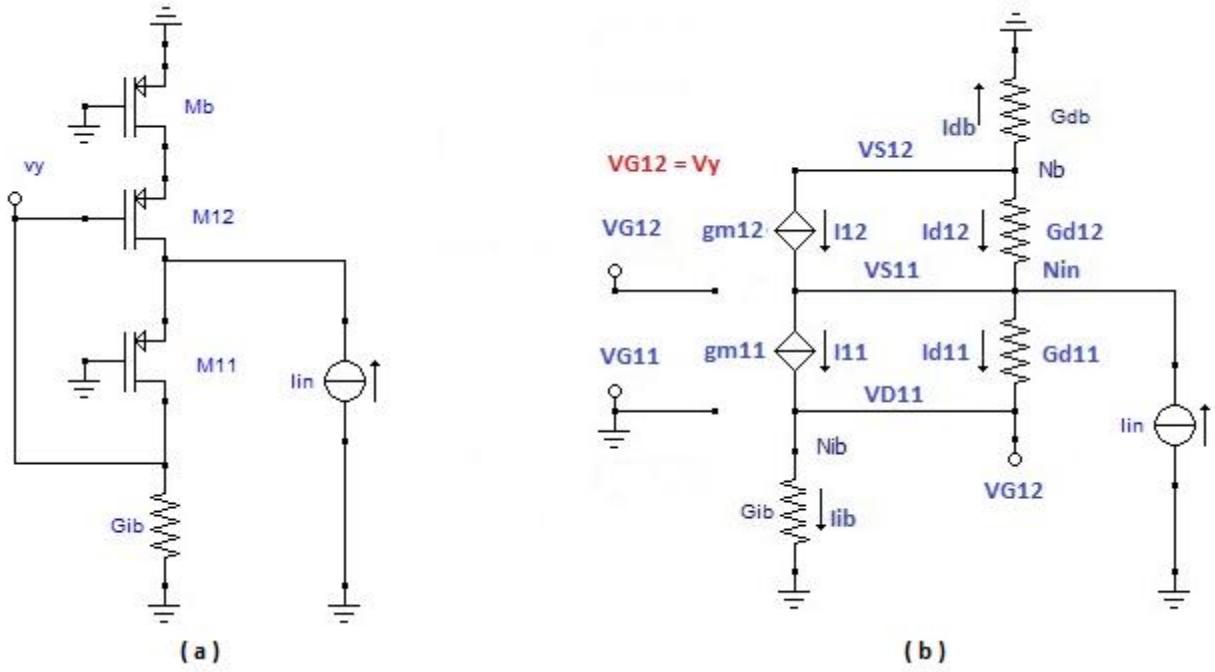


Fig.B. 11: (a) circuit for the calculation of Vy/Iin; (b) equivalent circuit

I apply KCL to the node Nib Depicted in Fig.B.11:

$$I_{11} + I_{d11} = I_{ib} \quad \text{(B.194)}$$

$$-(V_{G11} - V_{S11})gm_{11} + (V_{S11} - V_{G12})G_{d11} = V_{G12}G_{ib} \quad \text{(B.195)}$$

$$V_{G11} = 0 \quad \text{(B.196)}$$

$$V_{G12} = V_y \quad \text{(B.197)}$$

$$-V_{G11}gm_{11} + V_{S11}gm_{11} + V_{S11}G_{d11} - V_{G12}G_{d11} = V_{G12}G_{ib} \quad \text{(B.198)}$$

$$V_{S11}gm_{11} + V_{S11}G_{d11} - V_yG_{d11} = V_yG_{ib} \quad \text{(B.199)}$$

$$V_{S11}(gm_{11} + G_{d11}) = V_y(G_{ib} + G_{d11}) \quad \text{(B.200)}$$

$$V_{S11} = V_y\frac{(G_{ib}+G_{d11})}{(gm_{11}+G_{d11})} \quad \text{(B.201)}$$

$$V_{S11} = V_y\frac{N_{00}}{D_{00}} \quad \text{(B.202)}$$

$$N_{00} = (G_{ib} + G_{d11}) \quad \text{(B.203)}$$

$$D_{00} = (gm_{11} + G_{d11}) \quad \text{(B.204)}$$

I apply KCL to the node Nin:

$$I_{12} + I_{d12} + I_{in} = I_{11} + I_{d11} \quad \text{(B.205)}$$

$$I_{11} + I_{d11} = I_{ib} \quad \text{(B.206)}$$

$$I_{12} + I_{d12} + I_{in} = I_{ib} \quad \text{(B.207)}$$

$$-(V_{G12} - V_{S12})gm_{12} + (V_{S12} - V_{S11})G_{d12} + I_{in} = V_{G12}G_{ib} \quad \text{(B.208)}$$

$$V_{G12} = V_y \quad \text{(B.197)}$$

$$-V_ygm_{12} + V_{S12}gm_{12} + V_{S12}G_{d12} - V_{S11}G_{d12} + I_{in} = V_yG_{ib} \quad \text{(B.209)}$$

$$-V_y(G_{ib} + gm_{12}) + V_{S12}(gm_{12} + G_{d12}) - V_{S11}G_{d12} + I_{in} = 0 \quad \text{(B.210)}$$

$$V_y(G_{ib} + gm_{12}) - V_{S12}(gm_{12} + G_{d12}) + V_{S11}G_{d12} = I_{in} \quad \text{(B.211)}$$

I apply KCL to the node Nb:

$$I_{12} + I_{d12} + I_{db} = 0 \quad \text{(B.212)}$$
$$-(V_{G12} - V_{S12})gm_{12} + (V_{S12} - V_{S11})G_{d12} + V_{S12}G_{db} = 0 \quad \text{(B.213)}$$
$$-V_y gm_{12} + V_{S12}gm_{12} + V_{S12}G_{d12} - V_{S11}G_{d12} + V_{S12}G_{db} = 0 \quad \text{(B.214)}$$
$$V_{S12}gm_{12} + V_{S12}G_{d12} + V_{S12}G_{db} = V_y gm_{12} + V_{S11}G_{d12} \quad \text{(B.215)}$$
$$V_{S12}(gm_{12} + G_{d12} + G_{db}) = V_y gm_{12} + V_{S11}G_{d12} \quad \text{(B.216)}$$
$$V_{S12} = V_y \frac{gm_{12}}{(gm_{12}+G_{d12}+G_{db})} + V_{S11} \frac{G_{d12}}{(gm_{12}+G_{d12}+G_{db})} \quad \text{(B.217)}$$
$$V_{S12} = V_y \frac{gm_{12}}{D_{01}} + V_{S11} \frac{G_{d12}}{D_{01}} \quad \text{(B.218)}$$
$$D_{01} = (gm_{12} + G_{d12} + G_{db}) \quad \text{(B.219)}$$

Replacing (B.202) in (B.218):

$$V_{S11} = V_y \frac{N_{00}}{D_{00}} \quad \text{(B.202)}$$
$$N_{00} = (G_{ib} + G_{d11}) \quad \text{(B.203)}$$
$$D_{00} = (gm_{11} + G_{d11}) \quad \text{(B.204)}$$
$$D_{01} = (gm_{12} + G_{d12} + G_{db}) \quad \text{(B.219)}$$
$$V_{S12} = V_y \frac{gm_{12}}{D_{01}} + V_{S11} \frac{G_{d12}}{D_{01}} \quad \text{(B.218)}$$
$$V_{S12} = V_y \frac{gm_{12}}{D_{01}} + V_y \frac{N_{00}}{D_{00}} \frac{G_{d12}}{D_{01}} \quad \text{(B.220)}$$
$$V_{S12} = V_y \frac{D_{00}gm_{12}}{D_{00}D_{01}} + V_y \frac{N_{00}}{D_{00}} \frac{G_{d12}}{D_{01}} \quad \text{(B.221)}$$
$$V_{S12} = V_y \left[\frac{D_{00}gm_{12}+N_{00}G_{d12}}{D_{00}D_{01}}\right] \quad \text{(B.222)}$$

From the equation to the node Nin:

$$I_{in} = V_y(G_{ib} + gm_{12}) - V_{S12}(gm_{12} + G_{d12}) + V_{S11}G_{d12} \quad \text{(B.211)}$$

Replacing V_{S11} (B.202)) e V_{S12} (B.222):

$$I_{in} = V_y(G_{ib} + gm_{12}) - V_y \left[\frac{D_{00}gm_{12}+N_{00}G_{d12}}{D_{00}D_{01}}\right](gm_{12} + G_{d12}) + V_y \frac{N_{00}}{D_{00}} G_{d12} \quad \text{(B.223)}$$
$$I_{in} = V_y \frac{D_{00}D_{01}(G_{ib}+gm_{12})}{D_{00}D_{01}} - V_y \left[\frac{D_{00}gm_{12}+N_{00}G_{d12}}{D_{00}D_{01}}\right](gm_{12} + G_{d12}) + V_y \frac{D_{01}N_{00}}{D_{00}D_{01}} G_{d12} \quad \text{(B.224)}$$
$$I_{in}D_{00}D_{01} = V_y D_{00}D_{01}(G_{ib} + gm_{12}) - V_y(D_{00}gm_{12} + N_{00}G_{d12})(gm_{12} + G_{d12}) + V_y D_{01}N_{00}G_{d12} \quad \text{(B.225)}$$

$$I_{in}D_{00}D_{01} = V_y[D_{00}D_{01}(G_{ib} + gm_{12}) - (D_{00}gm_{12} + N_{00}G_{d12})(gm_{12} + G_{d12}) + D_{01}N_{00}G_{d12}] \quad \text{(B.226)}$$
$$\frac{V_y}{I_{in}} = \frac{D_{00}D_{01}}{[D_{00}D_{01}(G_{ib}+gm_{12})-(D_{00}gm_{12}+N_{00}G_{d12})(gm_{12}+G_{d12})+D_{01}N_{00}G_{d12}]} \quad \text{(B.227)}$$
$$\frac{V_y}{I_{in}} = \left[\frac{N_T}{D_T}\right] = \frac{N_T}{D_{T1}+D_{T2}+D_{T3}} \quad \text{(B.228)}$$
$$N_T = D_{00}D_{01} \quad \text{(B.229)}$$
$$D_{T1} = D_{00}D_{01}(G_{ib} + gm_{12}) \quad \text{(B.230)}$$
$$D_{T2} = -(D_{00}gm_{12} + N_{00}G_{d12})(gm_{12} + G_{d12}) \quad \text{(B.231)}$$
$$D_{T3} = D_{01}N_{00}G_{d12} \quad \text{(B.232)}$$
$$N_{00} = (G_{ib} + G_{d11}) \quad \text{(B.203)}$$
$$D_{00} = (gm_{11} + G_{d11}) \quad \text{(B.204)}$$
$$D_{01} = (gm_{12} + G_{d12} + G_{db}) \quad \text{(B.219)}$$

$$N_T = D_{00}D_{01} = (gm_{11} + G_{d11})(gm_{12} + G_{d12} + G_{db}) =$$
$$= gm_{11}(gm_{12} + G_{d12} + G_{db}) + G_{d11}(gm_{12} + G_{d12} + G_{db}) = \quad \text{(B.233)}$$
$$D_{T1} = D_{00}D_{01}(G_{ib} + gm_{12}) = (gm_{11} + G_{d11})(gm_{12} + G_{d12} + G_{db})(G_{ib} + gm_{12})$$
$$= (gm_{11} + G_{d11})(G_{ib} + gm_{12})(gm_{12} + G_{d12} + G_{db}) =$$
$$= (gm_{11}G_{ib} + gm_{11}gm_{12} + G_{d11}G_{ib} + G_{d11}gm_{12})(gm_{12} + G_{d12} + G_{db}) =$$
$$= gm_{12}(gm_{11}G_{ib} + gm_{11}gm_{12} + G_{d11}G_{ib} + G_{d11}gm_{12}) +$$
$$+G_{d12}(gm_{11}G_{ib} + gm_{11}gm_{12} + G_{d11}G_{ib} + G_{d11}gm_{12}) +$$
$$+G_{db}(gm_{11}G_{ib} + gm_{11}gm_{12} + G_{d11}G_{ib} + G_{d11}gm_{12}) \quad \text{(B.234)}$$
$$D_{T2} = -(D_{00}gm_{12} + N_{00}G_{d12})(gm_{12} + G_{d12}) =$$
$$= -\big((gm_{11} + G_{d11})gm_{12} + (G_{ib} + G_{d11})G_{d12}\big)(gm_{12} + G_{d12}) =$$
$$= -(gm_{11}gm_{12} + G_{d11}gm_{12} + G_{ib}G_{d12} + G_{d11}G_{d12})(gm_{12} + G_{d12}) =$$
$$= -gm_{12}(gm_{11}gm_{12} + G_{d11}gm_{12} + G_{ib}G_{d12} + G_{d11}G_{d12}) +$$
$$-G_{d12}(gm_{11}gm_{12} + G_{d11}gm_{12} + G_{ib}G_{d12} + G_{d11}G_{d12}) \quad \text{(B.235)}$$
$$D_{T3} = D_{01}N_{00}G_{d12} =$$
$$= (gm_{12} + G_{d12} + G_{db})(G_{ib} + G_{d11})G_{d12} =$$
$$= (gm_{12}G_{ib} + gm_{12}G_{d11})G_{d12} + (G_{d12}G_{ib} + G_{d12}G_{d11})G_{d12} + (G_{db}G_{ib} + G_{db}G_{d11})G_{d12} =$$
$$= G_{d12}(gm_{12}G_{ib} + gm_{12}G_{d11} + G_{d12}G_{ib} + G_{d12}G_{d11} + G_{db}G_{ib} + G_{db}G_{d11}) \quad \text{(B.236)}$$
$$D_T = gm_{12}(gm_{11}G_{ib} + G_{d11}G_{ib}) + G_{d12}(gm_{11}G_{ib} + G_{d11}G_{ib}) +$$
$$+G_{db}(gm_{11}G_{ib} + gm_{11}gm_{12} + G_{d11}G_{ib} + G_{d11}gm_{12}) + G_{d12}(G_{db}G_{ib} + G_{db}G_{d11}) \quad \text{(B.237)}$$
$$D_T = gm_{12}(gm_{11}G_{ib} + G_{d11}G_{ib}) + G_{d12}(gm_{11}G_{ib} + G_{d11}G_{ib}) +$$
$$+G_{db}(gm_{11}G_{ib} + gm_{11}gm_{12} + G_{d11}G_{ib} + G_{d11}gm_{12}) + G_{d12}(G_{db}G_{ib} + G_{db}G_{d11}) \quad \text{(B.238)}$$

B.3.5 Vo1/Vy1 analysis

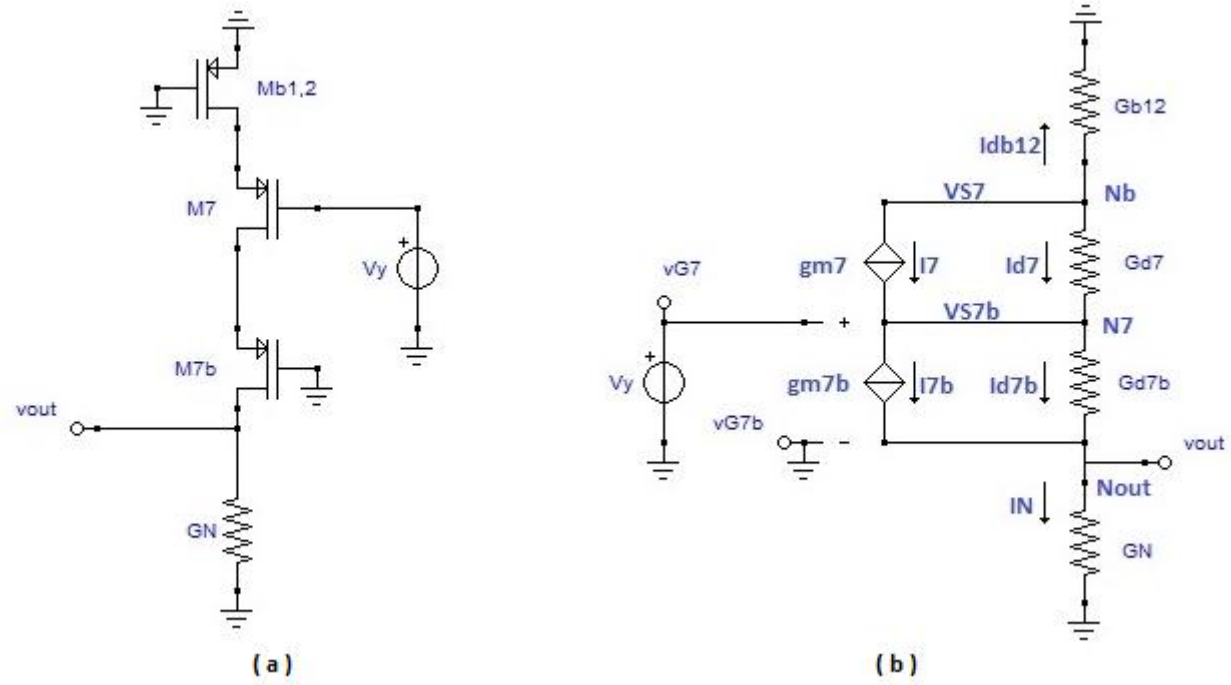


Fig.B. 12: (a) circuit for the calculation of Vout/Vy; (b) equivalent circuit

I apply KCL to the node Nout depicted in Fig.B.12:

$$I_{7b} + I_{d7b} = I_N \quad \text{(B.239)}$$

$$-(V_{G7b} - V_{S7b})gm_{7b} + (V_{S7b} - V_{out})G_{d7b} = V_{out}G_N \quad \text{(B.240)}$$

$$-V_{G7b}gm_{7b} + V_{S7b}gm_{7b} - V_{out}G_{d7b} + V_{S7b}G_{d7b} = V_{out}G_N \quad \text{(B.241)}$$

$$V_{G7b} = 0 \quad \text{(B.242)}$$

$$V_{S7b}gm_{7b} + V_{S7b}G_{d7b} = V_{out}G_N + V_{out}G_{d7b} \quad \text{(B.243)}$$

$$V_{S7b}(gm_{7b} + G_{d7b}) = V_{out}(G_N + G_{d7b}) \quad \text{(B.244)}$$

$$V_{S7b} = V_{out}\frac{(G_N + G_{d7b})}{(gm_{7b} + G_{d7b})} = V_{out}\frac{N_0}{D_0} \quad \text{(B.245)}$$

$$N_0 = (G_N + G_{d7b}) \quad \text{(B.246)}$$

$$D_0 = (gm_{7b} + G_{d7b}) \quad \text{(B.247)}$$

I apply KCL to the node N7:

$$I_7 + I_{d7} = I_{7b} + I_{d7b} \quad \text{(B.248)}$$

$$-(V_{G7} - V_{S7})gm_7 + (V_{S7} - V_{S7b})G_{d7} = -(V_{G7b} - V_{S7b})gm_{7b} + (V_{S7b} - V_{out})G_{d7b} \quad \text{(B.249)}$$

$$-V_{G7}gm_7 + V_{S7}gm_7 + V_{S7}G_{d7} - V_{S7b}G_{d7} =$$
$$= -V_{G7b}gm_{7b} + V_{S7b}gm_{7b} + V_{S7b}G_{d7b} - V_{out}G_{d7b} \quad \text{(B.2.50)}$$

$$V_{G7b} = 0;\ V_{G7} = V_y \quad \text{(B.251)}$$

$$-V_ygm_7 + V_{S7}gm_7 + V_{S7}G_{d7} - V_{S7b}G_{d7} = V_{S7b}gm_{7b} + V_{S7b}G_{d7b} - V_{out}G_{d7b} \quad \text{(B.252)}$$

$$V_{S7}(gm_7 + G_{d7}) = V_{S7b}(gm_{7b} + G_{d7b} + G_{d7}) + V_ygm_7 - V_{out}G_{d7b} \quad \text{(B.253)}$$

Replacing V_{S7b}:

$$V_{S7}(gm_7 + G_{d7}) = V_{S7b}(gm_{7b} + G_{d7b} + G_{d7}) + V_ygm_7 - V_{out}G_{d7b} \quad \text{(B.253)}$$

$$V_{S7b} = V_{out}\frac{N_0}{D_0} \quad \text{(B.245)}$$

$$V_{S7}(gm_7 + G_{d7}) = V_{out}\frac{N_0}{D_0}(gm_{7b} + G_{d7b} + G_{d7}) + V_ygm_7 - V_{out}G_{d7b} \quad \text{(B.254)}$$

$$V_{S7} = \frac{V_{out}[N_0(gm_{7b}+G_{d7b}+G_{d7})-G_{d7b}D_0]+V_yD_0gm_7}{D_0(gm_7+G_{d7})} \quad (B.255)$$

$$V_{S7} = V_{out}\frac{N_1}{D_1} + V_y\frac{N_2}{D_1} \quad (B.256)$$

$$N_1 = [N_0(gm_{7b} + G_{d7b} + G_{d7}) - G_{d7b}D_0] \quad (B.257)$$

$$N_2 = D_0gm_7 \quad (B.258)$$

$$D_1 = D_0(gm_7 + G_{d7}) \quad (B.259)$$

I apply KCL to the node Nb:

$$I_7 + I_{d7} + I_{db12} = 0 \quad (B.260)$$

$$-(V_{G7} - V_{S7})gm_7 + (V_{S7} - V_{S7b})G_{d7} + V_{S7}G_{db12} = 0 \quad (B.261)$$

$$-V_{G7}gm_7 + V_{S7}gm_7 + V_{S7}G_{d7} - V_{S7b}G_{d7} + V_{S7}G_{db12} = 0 \quad (B.262)$$

$$V_{G7} = V_y \quad (B.251)$$

$$-V_ygm_7 + V_{S7}gm_7 + V_{S7}G_{d7} - V_{S7b}G_{d7} + V_{S7}G_{db12} = 0 \quad (B.263)$$

$$-V_ygm_7 - V_{S7b}G_{d7} = -V_{S7}(G_{db12} + gm_7 + G_{d7}) \quad (B.264)$$

$$V_{S7} = V_y\frac{gm_7}{(G_{db12}+gm_7+G_{d7})} + V_{S7b}\frac{G_{d7}}{(G_{db12}+gm_7+G_{d7})} \quad (B.265)$$

$$V_{S7} = V_y\frac{gm_7}{D_2} + V_{S7b}\frac{G_{d7}}{D_2} \quad (B.266)$$

$$D_2 = (G_{db12} + gm_7 + G_{d7}) \quad (B.267)$$

summarizing some of the previous results, I have:

$$V_{S7b} = V_{out}\frac{(G_N+G_{d7b})}{(gm_{7b}+G_{d7b})} = V_{out}\frac{N_0}{D_0} \quad (B.245)$$

$$V_{S7} = V_y\frac{gm_7}{D_2} + V_{S7b}\frac{G_{d7}}{D_2} \quad (B.266)$$

$$V_{S7} = +V_y\frac{gm_7}{D_2} + V_{out}\frac{N_0}{D_0}\frac{G_{d7}}{D_2} \quad (B.268)$$

$$V_{S7} = \frac{V_{out}[N_0(gm_{7b}+G_{d7b}+G_{d7})-G_{d7b}D_0]+V_yD_0gm_7}{D_0(gm_7+G_{d7})} \quad (B.269)$$

$$V_{S7} = V_{out}\frac{N_1}{D_1} + V_y\frac{N_2}{D_1} \quad (B.256)$$

equalizing the (B.268) with (B.B.256), I get:

$$V_y\frac{gm_7}{D_2} + V_{out}\frac{N_0}{D_0}\frac{G_{d7}}{D_2} = V_{out}\frac{N_1}{D_1} + V_y\frac{N_2}{D_1} \quad (B.270)$$

$$V_y\frac{D_0D_1gm_7}{D_0D_2D_1} + V_{out}\frac{N_0D_1G_{d7}}{D_0D_2D_1} = V_{out}\frac{D_0D_2N_1}{D_0D_2D_1} + V_y\frac{D_0D_2N_2}{D_0D_2D_1} \quad (B.271)$$

$$+V_yD_0D_1gm_7 + V_{out}N_0D_1G_{d7} = V_{out}D_0D_2N_1 + V_yD_0D_2N_2 \quad (B.272)$$

$$V_{out}N_0D_1G_{d7} - V_{out}D_0D_2N_1 = V_yD_0D_2N_2 - V_yD_0D_1gm_7 \quad (B.273)$$

$$V_{out}(N_0D_1G_{d7} - D_0D_2N_1) = V_y(D_0D_2N_2 - D_0D_1gm_7) \quad (B.274)$$

$$V_{out}(N_0D_1G_{d7} - D_0D_2N_1) = V_y(D_0D_2N_2 - D_0D_1gm_7) \quad (B.275)$$

$$\frac{V_{out}}{V_y} = \frac{(D_0D_2N_2-D_0D_1gm_7)}{(N_0D_1G_{d7}-V_{out}D_0D_2N_1)} = \frac{N_T}{D_T} \quad (B.278)$$

$$N_1 = [N_0(gm_{7b} + G_{d7b} + G_{d7}) - G_{d7b}D_0] \quad (B.257)$$

$$N_2 = D_0gm_7 \quad (B.258)$$

$$D_1 = D_0(gm_7 + G_{d7}) \quad (B.259)$$

$$\frac{V_{out}}{V_y} = \frac{(D_0D_2N_2-D_0D_0(gm_7+G_{d7})gm_7)}{(N_0D_0(gm_7+G_{d7})G_{d7}-D_0D_2N_1)} = \frac{N_T}{D_T} \quad (B.279)$$

$$\frac{V_{out}}{V_y} = \frac{(D_2N_2-D_0(gm_7+G_{d7})gm_7)}{N_0(gm_7+G_{d7})G_{d7}-D_2N_1)} = \frac{N_T}{D_T} \quad (B.280)$$

$$D_2 = (G_{db12} + gm_7 + G_{d7}) \quad (B.267)$$

$$N_0 = (G_N + G_{d7b}) \quad \text{(B.245)}$$

$$D_0 = (gm_{7b} + G_{d7b}) \quad \text{(B.246)}$$

$$N_1 = [N_0(gm_{7b} + G_{d7b} + G_{d7}) - G_{d7b}D_0] =$$
$$= [(G_N + G_{d7b})(gm_{7b} + G_{d7b} + G_{d7}) - G_{d7b}(gm_{7b} + G_{d7b})] = \quad \text{(B.281)}$$
$$= [(G_N + G_{d7b})(gm_{7b} + G_{d7b}) + (G_N + G_{d7b})G_{d7} - G_{d7b}(gm_{7b} + G_{d7b})] =$$
$$= [G_N(gm_{7b} + G_{d7b}) + G_{d7b}(gm_{7b} + G_{d7b}) + (G_N + G_{d7b})G_{d7} - G_{d7b}(gm_{7b} + G_{d7b})]$$

$$N_1 = [G_N(gm_{7b} + G_{d7b}) + (G_N + G_{d7b})G_{d7}] \quad \text{(B.282)}$$

$$N_2 = D_0 gm_7 = (gm_{7b} + G_{d7b})gm_7 \quad \text{(B.283)}$$

$$D_1 = D_0(gm_7 + G_{d7}) = (gm_{7b} + G_{d7b})(gm_7 + G_{d7}) \quad \text{(B.284)}$$

$$D_2 = (G_{db12} + gm_7 + G_{d7}) \quad \text{(B.267)}$$

$$N_0 = (G_N + G_{d7b}) \quad \text{(B.245)}$$

$$D_0 = (gm_{7b} + G_{d7b}) \quad \text{(B.246)}$$

$$\frac{(D_2N_2 - D_0(gm_7 + G_{d7})gm_7)}{(N_0(gm_7 + G_{d7})G_{d7} - D_2N_1)} = \frac{N_T}{D_T} \quad \text{(B.280)}$$

$$N_T = (D_2N_2 - D_0(gm_7 + G_{d7})gm_7) = N_{T1} + N_{T2} \quad \text{(B.285)}$$

$$N_{T1} = D_2N_2 = (G_{db12} + gm_7 + G_{d7})(gm_{7b} + G_{d7b})gm_7 \quad \text{(B.286)}$$

$$N_{T2} = -D_0(gm_7 + G_{d7})gm_7 = -(gm_{7b} + G_{d7b})(gm_7 + G_{d7})gm_7 \quad \text{(B.287)}$$

$$N_T = (G_{da12}gm_7)(gm_{7b} + G_{d7b}) \quad \text{(B.288)}$$

$$D_T = (N_0(gm_7 + G_{d7})G_{d7} - D_2N_1) = D_{T1} + D_{T2} \quad \text{(B.289)}$$

$$D_{T1} = N_0(gm_7 + G_{d7})G_{d7} = (G_N + G_{d7b})(gm_7 + G_{d7})G_{d7} \quad \text{(B.290)}$$

$$D_{T2} = -(D_2N_1) =$$
$$= -(G_{db12} + gm_7 + G_{d7})[G_N(gm_{7b} + G_{d7b}) + (G_N + G_{d7b})G_{d7}] =$$
$$= -(G_{db12} + gm_7 + G_{d7})[G_N(gm_{7b} + G_{d7b})] +$$
$$-(G_{db12} + gm_7 + G_{d7})[(G_N + G_{d7b})G_{d7}] =$$
$$= -(G_{db12} + gm_7 + G_{d7})[G_N gm_{7b}] +$$
$$-(G_{db12} + gm_7 + G_{d7})[G_N G_{d7b}] +$$
$$-(gm_7 + G_{d7})[(G_N + G_{d7b})G_{d7}]$$
$$-(G_{db12})[(G_N + G_{d7b})G_{d7}] \quad \text{(B.291)}$$

$$D_T = D_{T2}$$

$$N_T = (G_{db12}gm_7)(gm_{7b} + G_{d7b}) \quad \text{(B.288)}$$

$$\frac{N_T}{D_T} = \frac{(G_{db12}gm_7)(gm_{7b} + G_{d7b})}{-(G_{db12} + gm_7 + G_{d7})G_N gm_{7b} - (G_{db12} + gm_7 + G_{d7})G_N G_{d7b} - (G_{db12})(G_N + G_{d7b})G_{d7}} \quad \text{(B.292)}$$

B.3.6 Vx/V1 analysis

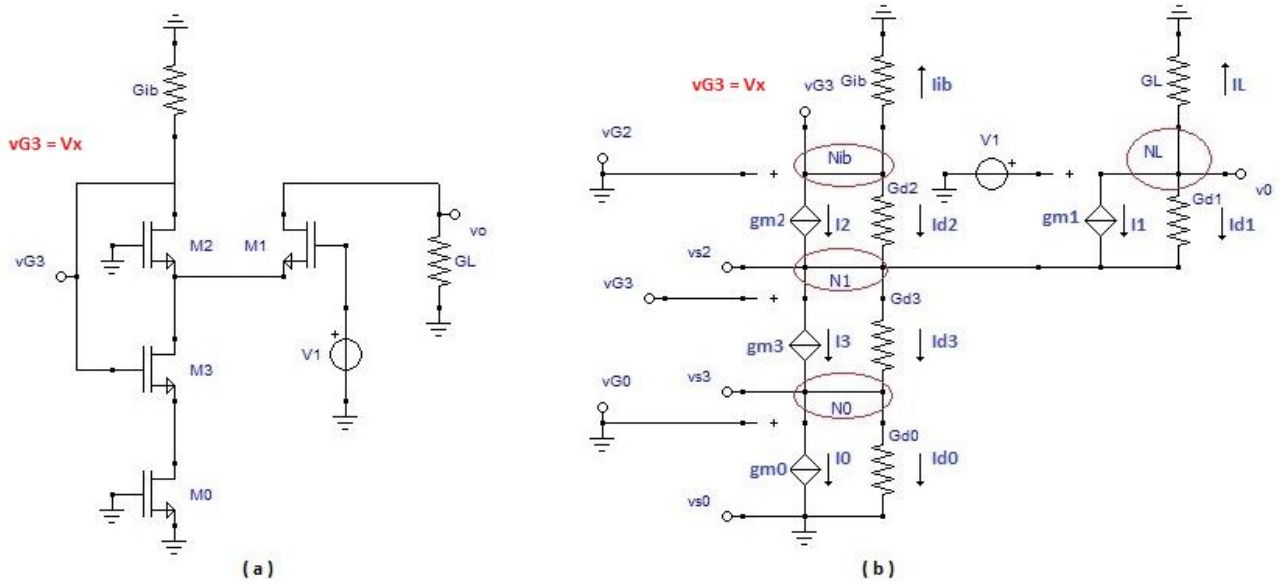


Fig.B. 13: (a) circuit for the calculation of Vx/V1; (b) equivalent circuit

I apply KCL to the node N0 depicted in Fig.B.13:

Being V_{G0} =V_{S0}=0, it follows that I0=0.

$$I_3 + I_{d3} = I_{d0} \quad \text{(B.293)}$$

$$(V_{S2} - V_{S3})G_{d3} + (V_{G3} - V_{S3})gm_3 = V_{S3}G_{d0} \quad \text{(B.294)}$$

$$V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 = V_{S3}G_{d0} \quad \text{(B.295)}$$

$$V_{S2}G_{d3} + V_{G3}gm_3 = V_{S3}(G_{d0} + G_{d3} + gm_3) \quad \text{(B.296)}$$

$$V_{S3} = \frac{V_{S2}G_{d3}+V_{G3}gm_3}{(G_{d0}+G_{d3}+gm_3)} \quad \text{(B.297)}$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad \text{(B.298)}$$

$$V_{S3} = \frac{V_{S2}G_{d3}+V_{G3}gm_3}{D_0} \quad \text{(B.299)}$$

I place:

$$V_{G3}=Vx \quad \text{(B.300)}$$

$$V_{S3} = \frac{V_{S2}G_{d3}+V_x gm_3}{D_0} \quad \text{(B.301)}$$

I apply KCL to the node N:

$$I_{d2} + I_2 + I_{d1} + I_1 = I_3 + I_{d3} \quad \text{(B.302)}$$

$$I_{d2} + I_2 = -I_{ib} \quad \text{(B.303)}$$

$$I_{d1} + I_1 = -I_L \quad \text{(B.304)}$$

$$-(I_{ib} + I_L) = I_3 + I_{d3} \quad \text{(B.305)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = (V_{G3} - V_{S3})gm_3 + (V_{S2} - V_{S3})G_{d3} \quad \text{(B.306)}$$

$$-V_{G3}G_{ib} - V_0G_L = V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 \quad \text{(B.307)}$$

$$V_{G3}=Vx \quad \text{(B.300)}$$

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad \text{(B.308)}$$

I apply KCL to the node NL:

$$I_1 + I_{d1} + I_L = 0 \quad \text{(B.309)}$$

$$(V_0 - V_{S2})G_{d1} + (V_1 - V_{S2})gm_1 + V_0G_L = 0 \quad \text{(B.310)}$$

$$V_0G_{d1} - V_{S2}G_{d1} + V_1gm_1 - V_{S2}gm_1 + V_0G_L = 0 \quad \text{(B.311)}$$

$$V_0(G_{d1} + G_L) + V_1 gm_1 = V_{S2}(G_{d1} + gm_1) \quad (B.312)$$

$$V_0(G_{d1} + G_L) = V_{S2}(G_{d1} + gm_1) - V_1 gm_1 \quad (B.313)$$

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} - V_1\frac{gm_1}{(G_{d1}+G_L)} \quad (B.314)$$

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} - V_1\frac{gm_1}{(G_{d1}+G_L)} = V_{S2}\frac{N_1}{D_1} - V_1\frac{N_2}{D_1} \quad (B.315)$$

$$N_1 = (G_{d1} + gm_1) \quad (B.316)$$

$$N_2 = gm_1 \quad (B.317)$$

$$D_1 = (G_{d1} + G_L) \quad (B.318)$$

I apply KCL to the node Nib:

$$I_2 + I_{d2} + I_{ib} = 0 \quad (B.319)$$

$$(V_{G3} - V_{S2})G_{d2} - V_{S2}gm_2 + V_{G3}G_{ib} = 0 \quad (B.320)$$

$$V_{G3}G_{d2} - V_{S2}G_{d2} - V_{S2}gm_2 - V_{S2}gm_1 + V_{G3}G_{ib} = 0 \quad (B.321)$$

$$V_{G3}(G_{d2} + G_{ib}) = V_{S2}(G_{d2} + gm_2) \quad (B.322)$$

I place:

V_{G3}=Vx (B.300)

$$V_{S2} = V_x\frac{(G_{d2}+G_{ib})}{(G_{d2}+gm_2)} = V_x\frac{N_3}{D_3} \quad (B.323)$$

$$N_3 = (G_{d2} + G_{ib}) \quad (B.324)$$

$$D_3 = (G_{d2} + gm_2) \quad (B.325)$$

1) I consider (B.308):

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad (B.308)$$

Replace $V_{S2,}$ V_0 e V_{S3}, but first summarize the results obtained previously:

Nib:

$$V_{S2} = V_x\frac{(G_{d2}+G_{ib})}{(G_{d2}+gm_2)} = V_x\frac{N_3}{D_3} \quad (B.323)$$

$$N_3 = (G_{d2} + G_{ib}) \quad (B.324)$$

$$D_3 = (G_{d2} + gm_2) \quad (B.325)$$

NL:

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} - V_1\frac{gm_1}{(G_{d1}+G_L)} = V_{S2}\frac{N_1}{D_1} - V_1\frac{N_2}{D_1} \quad (B.315)$$

$$N_1 = (G_{d1} + gm_1) \quad (B.316)$$

$$N_2 = gm_1 \quad (B.317)$$

$$D_1 = (G_{d1} + G_L) \quad (B.318)$$

N0:

$$V_{S3} = \frac{V_{S2}G_{d3}+V_x gm_3}{D_0} \quad (B.301)$$

$$V_{S3} = \frac{V_x\frac{N_3}{D_3}G_{d3}+V_x gm_3}{D_0} \quad (B.326)$$

$$V_{S3} = \frac{V_x(N_3G_{d3}+D_3gm_3)}{D_0D_3} \quad (B.327)$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad (B.298)$$

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad (B.308)$$

$$-V_x(G_{ib} + gm_3) - V_{S2}\frac{N_1}{D_1} - V_1\frac{N_2}{D_1}G_L = V_{S2}G_{d3} - \frac{V_x(N_3G_{d3}+D_3gm_3)}{D_0D_3}(G_{d3} + gm_3) \quad (B.328)$$

$$-V_x\frac{(G_{ib}+gm_3)D_1D_3}{D_1D_3} - V_x\frac{N_3}{D_3}\frac{N_1}{D_1} - V_1\frac{D_3N_2G_L}{D_1D_3} =$$

$$= \frac{V_x D_0 N_3 G_{d3}}{D_0 D_3} - \frac{V_x (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)}{D_0 D_3} \quad \text{(B.329)}$$

$$-V_x \frac{(G_{ib} + gm_3) D_1 D_3}{D_1 D_3} - V_x \frac{N_3}{D_3} \frac{N_1}{D_1} - \frac{V_x D_0 N_3 G_{d3}}{D_0 D_3} + \frac{V_x (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)}{D_0 D_3} =$$

$$= V_1 \frac{D_3 N_2 G_L}{D_1 D_3} \quad \text{(B.330)}$$

$$V_x \left[\frac{(N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)}{D_0 D_3} - \frac{(G_{ib} + gm_3) D_1 D_3}{D_1 D_3} - \frac{N_3}{D_3} \frac{N_1}{D_1} - \frac{D_0 N_3 G_{d3}}{D_0 D_3}\right] = V_1 \frac{D_3 N_2 G_L}{D_1 D_3} \quad \text{(B.331)}$$

$$V_x \left[\frac{(N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)}{D_0} - \frac{(G_{ib} + gm_3) D_1 D_3}{D_1} - \frac{N_3 N_1}{D_1} - \frac{D_0 N_3 G_{d3}}{D_0}\right] = V_1 \frac{D_3 N_2 G_L}{D_1} \quad \text{(B.332)}$$

$$V_x \left[\frac{D_1 (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)}{D_0 D_1} - \frac{(G_{ib} + gm_3) D_0 D_1 D_3}{D_0 D_1} - \frac{D_0 N_3 N_1}{D_0 D_1} - \frac{D_0 D_1 N_3 G_{d3}}{D_0 D_1}\right] =$$

$$= V_1 \frac{D_0 D_3 N_2 G_L}{D_0 D_1} \quad \text{(B.333)}$$

$$V_x [D_1 (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3) - (G_{ib} + gm_3) D_0 D_1 D_3 - D_0 N_3 N_1 - D_0 D_1 N_3 G_{d3}] =$$

$$= V_1 D_0 D_3 N_2 G_L \quad \text{(B.334)}$$

$$\frac{V_x}{V_1} =$$

$$= \frac{D_0 D_3 N_2 G_L}{[D_1 (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3) - (G_{ib} + gm_3) D_0 D_1 D_3 - D_0 N_3 N_1 - D_0 D_1 N_3 G_{d3}]} \quad \text{(B.335)}$$

$$\frac{V_x}{V_1} = \frac{N_T}{D_T} \quad \text{(B.336)}$$

$$N_1 = (G_{d1} + gm_1) \quad \text{(B.316)}$$

$$N_2 = gm_1 \quad \text{(B.317)}$$

$$N_3 = (G_{d2} + G_{ib}) \quad \text{(B.324)}$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad \text{(B.298)}$$

$$D_1 = (G_{d1} + G_L) \quad \text{(B.318)}$$

$$D_3 = (G_{d2} + gm_2) \quad \text{(B.325)}$$

$$N_T = D_0 D_3 N_2 G_L = gm_1 G_L (G_{d0} + G_{d3} + gm_3)(G_{d2} + gm_2) =$$

$$= gm_1 G_{d2} G_L (G_{d0} + G_{d3} + gm_3) + gm_1 gm_2 G_L (G_{d0} + G_{d3} + gm_3) \quad \text{(B.337)}$$

B.3..7 Vx/V_2 analysis

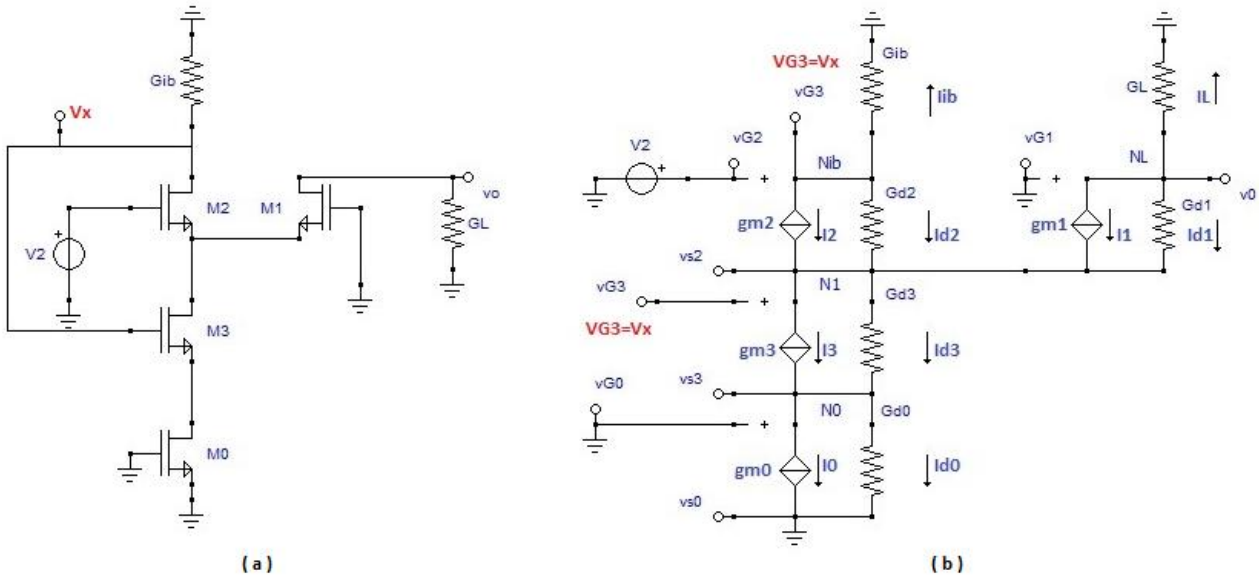


Fig.B. 14: (a) circuit for the calculation of Vx / V2; (b) equivalent circuit

I apply KCL to the node N0 depicted in Fig.B.14:

Being V_{G0} =V_{S0}=0, it follows that I0=0.

$$I_3 + I_{d3} = I_{d0} \quad \text{(B.338)}$$

$$(V_{S2} - V_{S3})G_{d3} + (V_{G3} - V_{S3})gm_3 = V_{S3}G_{d0} \quad \text{(B.339)}$$

$$V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 = V_{S3}G_{d0} \quad \text{(B.340)}$$

$$V_{S2}G_{d3} + V_{G3}gm_3 = V_{S3}(G_{d0} + G_{d3} + gm_3) \quad \text{(B.341)}$$

I place:

V_{G3}=Vx (B.342)

$$V_{S3} = \frac{V_{S2}G_{d3} + V_x gm_3}{(G_{d0} + G_{d3} + gm_3)} \quad \text{(B.343)}$$

$$V_{S3} = \frac{V_{S2}G_{d3} + V_x gm_3}{D_0} \quad \text{(B.344)}$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad \text{(B.345)}$$

I apply KCL to the node N:

$$I_{d2} + I_2 + I_{d1} + I_1 = I_3 + I_{d3} \quad \text{(B.346)}$$

$$I_{d2} + I_2 = -I_{ib} \quad \text{(B.347)}$$

$$I_{d1} + I_1 = -I_L \quad \text{(B.348)}$$

$$-(I_{ib} + I_L) = I_3 + I_{d3} \quad \text{(B.349)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = (V_{G3} - V_{S3})gm_3 + (V_{S2} - V_{S3})G_{d3} \quad \text{(B.350)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 \quad \text{(B.351)}$$

V_{G3}=Vx (B.342)

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad \text{(B.352)}$$

I apply KCL to the node NL:

$$I_1 + I_{d1} + I_L = 0 \quad \text{(B.353)}$$

$$(V_0 - V_{S2})G_{d1} + (V_1 - V_{S2})gm_1 + V_0G_L = 0 \quad \text{(B.354)}$$

$$V_0G_{d1} - V_{S2}G_{d1} + V_1gm_1 - V_{S2}gm_1 + V_0G_L = 0 \quad \text{(B.355)}$$

$$V_0(G_{d1} + G_L) + V_1gm_1 = V_{S2}(G_{d1} + gm_1) \quad \text{(B.356)}$$

$$V_0(G_{d1} + G_L) = V_{S2}(G_{d1} + gm_1) - V_1gm_1 \quad \text{(B.357)}$$

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} - V_1\frac{gm_1}{(G_{d1}+G_L)} \quad (B.358)$$

$$V_1 = 0 \quad (B.359)$$

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} = V_{S2}\frac{N_1}{D_1} \quad (B.360)$$

$$N_1 = (G_{d1} + gm_1) \quad (B.361)$$

$$D_1 = (G_{d1} + G_L) \quad (B.362)$$

I apply KCL to the node Nib:

$$I_2 + I_{d2} + I_{ib} = 0 \quad (B.363)$$

$$(V_{G3} - V_{S2})G_{d2} + (V_{G2} - V_{S2})gm_2 + V_{G3}G_{ib} = 0 \quad (B.364)$$

$$V_{G2} = V_2 \quad (B.365)$$

$$V_{G3}G_{d2} - V_{S2}G_{d2} + V_2gm_2 - V_{S2}gm_2 - V_{S2}gm_1 + V_{G3}G_{ib} = 0 \quad (B.366)$$

$$V_{G3}(G_{d2} + G_{ib}) + V_2gm_2 = V_{S2}(G_{d2} + gm_2) \quad (B.367)$$

V_{G3}=Vx (B.342)

$$V_{S2} = V_x\frac{(G_{d2}+G_{ib})}{(G_{d2}+gm_2)} + V_2\frac{gm_2}{(G_{d2}+gm_2)} = V_x\frac{N_3}{D_3} + V_2\frac{gm_2}{D_3} \quad (B.368)$$

$$N_3 = (G_{d2} + G_{ib}) \quad (B.369)$$

$$D_3 = (G_{d2} + gm_2) \quad (B.370)$$

I consider (B.352):

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad (B.352)$$

Replace $V_{S2,}$ V_0 e V_{S3}, but first summarize the results obtained previously:

Nib:

$$V_{S2} = V_x\frac{(G_{d2}+G_{ib})}{(G_{d2}+gm_2)} + V_2\frac{gm_2}{(G_{d2}+gm_2)} = V_x\frac{N_3}{D_3} + V_2\frac{gm_2}{D_3} \quad (B.368)$$

$$N_3 = (G_{d2} + G_{ib}) \quad (B.369)$$

$$D_3 = (G_{d2} + gm_2) \quad (B.370)$$

NL:

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} = V_{S2}\frac{N_1}{D_1} \quad (B.360)$$

$$N_1 = (G_{d1} + gm_1) \quad (B.361)$$

$$D_1 = (G_{d1} + G_L) \quad (B.362)$$

N0:

$$V_{S3} = \frac{V_{S2}G_{d3}+V_xgm_3}{D_0} \quad (B.344)$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad (B.345)$$

$$V_{S3} = \frac{V_x\frac{N_3G_{d3}}{D_3}+V_2\frac{gm_2G_{d3}}{D_3}+V_xgm_3}{D_0} \quad (B.371)$$

$$V_{S3} = \frac{V_x(N_3G_{d3}+D_3gm_3)+V_2gm_2G_{d3}}{D_0D_3} \quad (B.372)$$

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad (B.352)$$

$$-V_x(G_{ib} + gm_3) - V_{S2}\frac{N_1}{D_1}G_L = V_{S2}G_{d3} - \frac{V_x(N_3G_{d3}+D_3gm_3)+V_2gm_2G_{d3}}{D_0D_3}(G_{d3} + gm_3) \quad (B.373)$$

$$-V_x(G_{ib} + gm_3) - V_x\frac{N_3}{D_3}\frac{N_1}{D_1}G_L - V_2\frac{gm_2}{D_3}\frac{N_1}{D_1}G_L =$$

$$= V_x\frac{N_3}{D_3}G_{d3} + V_2\frac{gm_2}{D_3}G_{d3} - \frac{V_x(N_3G_{d3}+D_3gm_3)+V_2gm_2G_{d3}}{D_0D_3}(G_{d3} + gm_3) \quad (B.374)$$

$$-V_x\frac{D_3D_1(G_{ib}+gm_3)}{D_3D_1} - V_x\frac{N_3}{D_3}\frac{N_1}{D_1}G_L - V_2\frac{gm_2}{D_3}\frac{N_1}{D_1}G_L =$$

$$= V_x \frac{D_0 N_3 G_{d3}}{D_0 D_3} + V_2 \frac{D_0 gm_2 G_{d3}}{D_0 D_3} - \frac{V_x (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3) + V_2 gm_2 G_{d3}(G_{d3} + gm_3)}{D_0 D_3} \quad \text{(B.375)}$$

$$\frac{-V_x D_3 D_1 (G_{ib} + gm_3)}{D_1} + \frac{-V_x N_3 N_1 G_L}{D_1} + \frac{-V_2 gm_2 N_1 G_L}{D_1} =$$

$$= \frac{V_x D_0 N_3 G_{d3}}{D_0} + \frac{V_2 D_0 gm_2 G_{d3}}{D_0} + \frac{-V_x (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3) - V_2 gm_2 G_{d3}(G_{d3} + gm_3)}{D_0} \quad \text{(B.376)}$$

$$-V_x D_0 D_3 D_1 (G_{ib} + gm_3) - V_x D_0 N_3 N_1 G_L - V_2 D_0 gm_2 N_1 G_L =$$

$$= V_x D_0 D_1 N_3 G_{d3} + V_2 D_0 D_1 gm_2 G_{d3} - V_x D_1 (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3) - V_2 D_1 gm_2 G_{d3}(G_{d3} + gm_3) \quad \text{(B.377)}$$

$$-V_x [D_0 D_3 D_1 (G_{ib} + gm_3) - D_0 N_3 N_1 G_L - D_0 D_1 N_3 G_{d3} + D_1 (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)] =$$

$$= V_2 [D_0 D_1 gm_2 G_{d3} - D_1 gm_2 G_{d3}(G_{d3} + gm_3) + D_0 gm_2 N_1 G_L] \quad \text{(B.378)}$$

$$\frac{V_x}{V_2} = -\frac{[D_0 D_1 gm_2 G_{d3} - D_1 gm_2 G_{d3}(G_{d3} + gm_3) + D_0 N_1 gm_2 G_L]}{[D_0 D_3 D_1 (G_{ib} + gm_3) - D_0 N_3 N_1 G_L - D_0 D_1 N_3 G_{d3} + D_1 (N_3 G_{d3} + D_3 gm_3)(G_{d3} + gm_3)]} \quad \text{(B.379)}$$

$$\frac{V_x}{V_1} = \frac{N_T}{D_T} \quad \text{(B.380)}$$

$$N_1 = (G_{d1} + gm_1); \qquad N_2 = gm_1; \qquad N_3 = (G_{d2} + G_{ib})$$

$$D_0 = (G_{d0} + G_{d3} + gm_3); \quad D_1 = (G_{d1} + G_L); \quad D_3 = (G_{d2} + gm_2)$$

$$N_T = N_{T1} + N_{T2} + N_{T3} = [D_0 D_1 gm_2 G_{d3} - D_1 gm_2 G_{d3}(G_{d3} + gm_3) - D_0 N_1 gm_2 G_L] \quad \text{(B.381)}$$

$$N_{T1} = D_0 D_1 gm_2 G_{d3} = gm_2 G_{d3}(G_{d0} + G_{d3} + gm_3)(G_{d1} + G_L) \quad \text{(B.382)}$$

$$N_{T1} = D_0 D_1 gm_2 G_{d3} = gm_2 G_{d3} G_{d0}(G_{d1} + G_L) + gm_2 G_{d3}(G_{d3} + gm_3)(G_{d1} + G_L) \quad \text{(B.383)}$$

$$N_{T2} = -D_1 gm_2 G_{d3}(G_{d3} + gm_3) = -gm_2 G_{d3}(G_{d1} + G_L)(G_{d3} + gm_3) \quad \text{(B.384)}$$

$$N_{T3} = +D_0 N_1 gm_2 G_L = +gm_2 G_L (G_{d0} + G_{d3} + gm_3)(G_{d1} + gm_1) \quad \text{(B.385)}$$

$$N_{T1} = gm_2 G_{d3} G_{d0}(G_{d1} + G_L) \quad \text{(B.386)}$$

$$N_{T3} = +gm_2 G_L G_{d1}(G_{d0} + G_{d3} + gm_3) + gm_2 G_L gm_1 (G_{d0} + G_{d3} + gm_3) \quad \text{(B.387)}$$

$$N_{T1} + N_{T3} = gm_2 G_{d3} G_{d0}(G_{d1} + G_L) +$$

$$+gm_2 G_L G_{d1}(G_{d0} + G_{d3} + gm_3) + gm_2 G_L gm_1 (G_{d0} + G_{d3} + gm_3) \quad \text{(B.388)}$$

B.3.8 Vout/Vx analysis

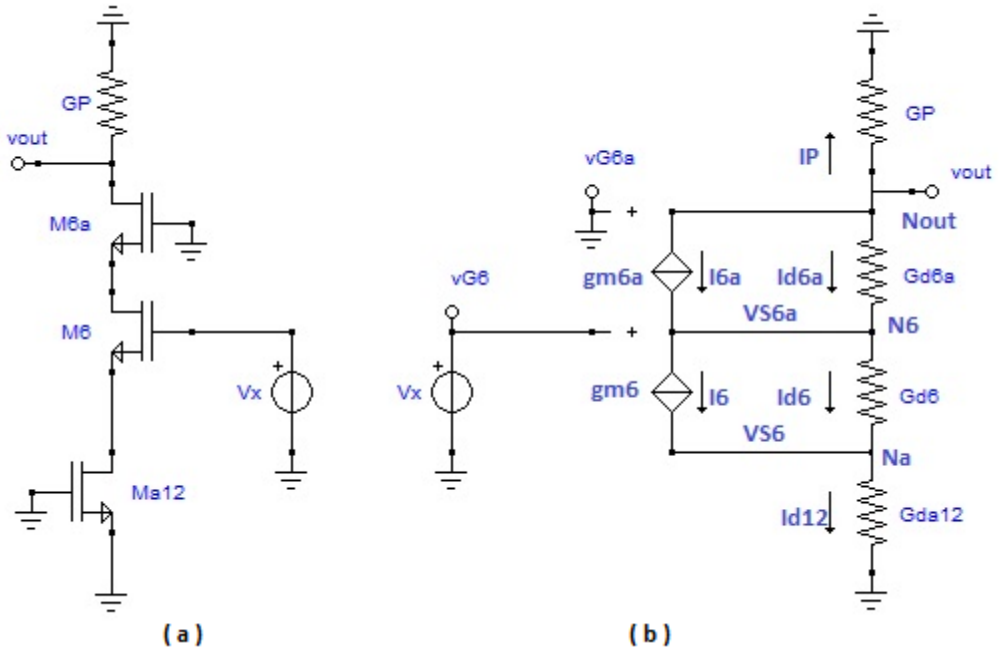


Fig.B. 15: (a) circuit for the calculation of Vout / Vx; (b) equivalent circuit

I apply KCL to the node Nout depicted in Fig.B.15:

$$I_{6a} + I_{d6a} = -I_P \quad \text{(B.389)}$$

$$(V_{G6a} - V_{S6a})gm_{6a} + (V_{out} - V_{S6a})G_{d6a} = -V_{out}G_P \quad \text{(B.390)}$$

$$V_{G6a}gm_{6a} - V_{S6a}gm_{6a} + V_{out}G_{d6a} - V_{S6a}G_{d6a} = -V_{out}G_P \quad \text{(B.391)}$$

$$V_{G6a}gm_{6a} - V_{S6a}gm_{6a} + V_{out}G_{d6a} - V_{S6a}G_{d6a} = -V_{out}G_P \quad \text{(B.392)}$$

$$V_{G6a} = 0 \quad \text{(B.393)}$$

$$-V_{S6a}(gm_{6a} + G_{d6a}) = -V_{out}(G_P + G_{d6a}) \quad \text{(B.394)}$$

$$V_{S6a} = V_{out}\frac{(G_P + G_{d6a})}{(gm_{6a} + G_{d6a})} = V_{out}\frac{N_0}{D_0} \quad \text{(B.395)}$$

$$N_0 = (G_P + G_{d6a}) \quad \text{(B.396)}$$

$$D_0 = (gm_{6a} + G_{d6a}) \quad \text{(B.397)}$$

I apply KCL to the node N6:

$$I_6 + I_{d6} = I_{6a} + I_{d6a} \quad \text{(B.398)}$$

$$(V_{G6} - V_{S6})gm_6 + (V_{S6a} - V_{S6})G_{d6} = (V_{G6a} - V_{S6a})gm_{6a} + (V_{out} - V_{S6a})G_{d6a} \quad \text{(B.399)}$$

$$V_{G6}gm_6 - V_{S6}gm_6 + V_{S6a}G_{d6} - V_{S6}G_{d6} = V_{G6a}gm_{6a} - V_{S6a}gm_{6a} + V_{out}G_{d6a} - V_{S6a}G_{d6a} \quad \text{(B.400)}$$

$$V_{G6a} = 0; \qquad V_{G6} = V_x \quad \text{(B.401)}$$

$$V_x gm_6 - V_{S6}gm_6 + V_{S6a}G_{d6} - V_{S6}G_{d6} = -V_{S6a}gm_{6a} + V_{out}G_{d6a} - V_{S6a}G_{d6a} \quad \text{(B.402)}$$

$$-V_{S6}(gm_6 + G_{d6}) = -V_{S6a}(gm_{6a} + V_{S6a}G_{d6a} + V_{S6a}G_{d6}) + V_{out}G_{d6a} - V_x gm_6 \quad \text{(B.403)}$$

$$V_{S6}(gm_6 + G_{d6}) = +V_{S6a}(gm_{6a} + G_{d6a} + G_{d6}) - V_{out}G_{d6a} + V_x gm_6 \quad \text{(B.404)}$$

$$V_{S6}(gm_6 + G_{d6}) = +V_{S6a}(gm_{6a} + G_{d6a} + G_{d6}) - V_{out}G_{d6a} + V_x gm_6 \quad \text{(B.405)}$$

$$V_{S6a} = +V_{out}\frac{N_0}{D_0} \quad \text{(B.406)}$$

$$V_{S6} = \frac{V_{out}[N_0(gm_{6a} + G_{d6a} + G_{d6}) - G_{d6a}D_0] + V_x D_0 gm_6}{D_0(gm_6 + G_{d6})} \quad \text{(B.407)}$$

$$V_{S6} = V_{out}\frac{N_1}{D_1} + V_x\frac{N_2}{D_1} \quad (B.408)$$

$$N_1 = [N_0(gm_{6a} + G_{d6a} + G_{d6}) - G_{d6a}D_0] \quad (B.409)$$

$$N_2 = D_0 gm_6 \quad (B.410)$$

$$D_1 = D_0(gm_6 + G_{d6}) \quad (B.411)$$

I apply KCL to the node Na:

$$I_6 + I_{d6} = I_{d12} \quad (B.412)$$

$$(V_{G6} - V_{S6})gm_6 + (V_{S6a} - V_{S6})G_{d6} = V_{S6}G_{da12} \quad (B.413)$$

$$V_{G6} = V_x \quad (B.401)$$

$$V_x gm_6 - V_{S6}gm_6 + V_{S6a}G_{d6} - V_{S6}G_{d6} = V_{S6}G_{da12} \quad (B.414)$$

$$V_x gm_6 + V_{S6a}G_{d6} = V_{S6}G_{da12} + V_{S6}gm_6 + V_{S6}G_{d6} \quad (B.415)$$

$$V_x gm_6 + V_{S6a}G_{d6} = V_{S6}(G_{da12} + gm_6 + G_{d6}) \quad (B.416)$$

$$V_{S6} = V_x\frac{gm_6}{(G_{da12}+gm_6+G_{d6})} + V_{S6a}\frac{G_{d6}}{(G_{da12}+gm_6+G_{d6})} \quad (B.417)$$

$$V_{S6} = V_x\frac{gm_6}{D_2} + V_{S6a}\frac{G_{d6}}{D_2} \quad (B.418)$$

$$D_2 = (G_{da12} + gm_6 + G_{d6}) \quad (B.419)$$

summarize the results obtained previously:

$$V_{S6a} = V_{out}\frac{(G_P+G_{d6a})}{(gm_{6a}+G_{d6a})} = V_{out}\frac{N_0}{D_0} \quad (B.395)$$

$$V_{S6} = V_x\frac{gm_6}{D_2} + V_{S6a}\frac{G_{d6}}{D_2} \quad (B.418)$$

$$V_{S6} = V_x\frac{gm_6}{D_2} + V_{out}\frac{N_0}{D_0}\frac{G_{d6}}{D_2} \quad (B.420)$$

$$V_{S6} = \frac{V_{out}[N_0(gm_{6a}+G_{d6a}+G_{d6})-G_{d6a}D_0]+V_x D_0 gm_6}{D_0(gm_6+G_{d6})} \quad (B.421)$$

$$V_{S6} = V_{out}\frac{N_1}{D_1} + V_x\frac{N_2}{D_1} \quad (B.408)$$

$$V_x\frac{gm_6}{D_2} + V_{out}\frac{N_0}{D_0}\frac{G_{d6}}{D_2} = V_{out}\frac{N_1}{D_1} + V_x\frac{N_2}{D_1} \quad (B.422)$$

$$V_x\frac{D_0D_1gm_6}{D_0D_2D_1} + V_{out}\frac{N_0D_1G_{d6}}{D_0D_2D_1} = V_{out}\frac{D_0D_2N_1}{D_0D_2D_1} + V_x\frac{D_0D_2N_2}{D_0D_2D_1} \quad (B.423)$$

$$V_x D_0D_1gm_6 + V_{out}N_0D_1G_{d6} = V_{out}D_0D_2N_1 + V_x D_0D_2N_2 \quad (B.424)$$

$$V_{out}(N_0D_1G_{d6} - D_0D_2N_1) = V_x(D_0D_2N_2 - D_0D_1gm_6) \quad (B.425)$$

$$\frac{V_{out}}{V_x} = \frac{(D_0D_2N_2-D_0D_1gm_6)}{(N_0D_1G_{d6}-V_{out}D_0D_2N_1)} \quad (B.426)$$

$$\frac{V_{out}}{V_x} = \frac{(D_0D_2N_2-D_0D_1gm_6)}{(N_0D_1G_{d6}-D_0D_2N_1)} = \frac{N_T}{D_T}$$

(B.427)(2.8.38)

$$D_1 = D_0(gm_6 + G_{d6})$$

I have:

$$\frac{V_{out}}{V_x} = \frac{(D_0D_2N_2-D_0D_0(gm_6+G_{d6})gm_6)}{(N_0D_0(gm_6+G_{d6})G_{d6}-D_0D_2N_1)} = \frac{N_T}{D_T} \quad (B.428)$$

$$\frac{V_{out}}{V_x} = \frac{(D_2N_2-D_0(gm_6+G_{d6})gm_6)}{N_0(gm_6+G_{d6})G_{d6}-D_2N_1)} = \frac{N_T}{D_T} \quad (B.429)$$

$$D_2 = (G_{da12} + gm_6 + G_{d6})$$

$$N_1 = [N_0(gm_{6a} + G_{d6a} + G_{d6}) - G_{d6a}D_0] =$$

$$= [(G_P + G_{d6a})(gm_{6a} + G_{d6a} + G_{d6}) - G_{d6a}(gm_{6a} + G_{d6a})] = \quad (B.430)$$

$$= [(G_P + G_{d6a})(gm_{6a} + G_{d6a}) + (G_P + G_{d6a})G_{d6} - G_{d6a}(gm_{6a} + G_{d6a})] =$$

$$= [G_P(gm_{6a} + G_{d6a}) + G_{d6a}(gm_{6a} + G_{d6a}) + (G_P + G_{d6a})G_{d6} - G_{d6a}(gm_{6a} + G_{d6a})] =$$

$$N_1 = [G_P(gm_{6a} + G_{d6a}) + (G_P + G_{d6a})G_{d6}] \quad \text{(B.431)}$$

$$N_2 = D_0 gm_6 = (gm_{6a} + G_{d6a})gm_6 \quad \text{(B.432)}$$

$$D_1 = D_0(gm_6 + G_{d6}) = (gm_{6a} + G_{d6a})(gm_6 + G_{d6})$$

$$D_2 = (G_{da12} + gm_6 + G_{d6})$$

$$N_0 = (G_P + G_{d6a})$$

$$D_0 = (gm_{6a} + G_{d6a})$$

$$\frac{(D_2N_2 - D_0(gm_6+G_{d6})gm_6)}{(N_0(gm_6+G_{d6})G_{d6} - D_2N_1)} = \frac{N_T}{D_T} \quad \text{(B.429)}$$

$$N_T = (D_2N_2 - D_0(gm_6 + G_{d6})gm_6) = N_{T1} + N_{T2} \quad \text{(B.433)}$$

$$N_{T1} = D_2N_2 = (G_{da12} + gm_6 + G_{d6})(gm_{6a} + G_{d6a})gm_6 \quad \text{(B.434)}$$

$$N_{T2} = -D_0(gm_6 + G_{d6})gm_6 = -(gm_{6a} + G_{d6a})(gm_6 + G_{d6})gm_6 \quad \text{(B.435)}$$

$$N_T = (G_{da12}gm_6)(gm_{6a} + G_{d6a}) \quad \text{(B.436)}$$

$$D_T = (N_0(gm_6 + G_{d6})G_{d6} + D_2N_1) = D_{T1} + D_{T2} \quad \text{(B.437)}$$

$$D_{T1} = N_0(gm_6 + G_{d6})G_{d6} = (G_P + G_{d6a})(gm_6 + G_{d6})G_{d6} \quad \text{(B.438)}$$

$$D_{T2} = -(D_2N_1) = \quad \text{(B.439)}$$

$$= -(G_{da12} + gm_6 + G_{d6})[G_P(gm_{6a} + G_{d6a}) + (G_P + G_{d6a})G_{d6}] =$$

$$= -(G_{da12} + gm_6 + G_{d6})[G_P(gm_{6a} + G_{d6a})] +$$

$$-(G_{da12} + gm_6 + G_{d6})[(G_P + G_{d6a})G_{d6}] =$$

$$= -(G_{da12} + gm_6 + G_{d6})[G_P gm_{6a}] +$$

$$-(G_{da12} + gm_6 + G_{d6})[G_P G_{d6a}] +$$

$$-(gm_6 + G_{d6})[(G_P + G_{d6a})G_{d6}]$$

$$-(G_{da12})[(G_P + G_{d6a})G_{d6}]$$

$$D_T = D_{T2}$$

$$N_T = (G_{da12}gm_6)(gm_{6a} + G_{d6a}) \quad \text{(B.436)}$$

$$\frac{N_T}{D_T} = \frac{(G_{da12}gm_6)(gm_{6a}+G_{d6a})}{-(G_{da12}+gm_6+G_{d6})G_P gm_{6a} - (G_{da12}+gm_6+G_{d6})G_P G_{d6a} - [(G_P+G_{d6a})G_{d6}G_{da12}]} \quad \text{(B.440)}$$

B.4 V3 signal

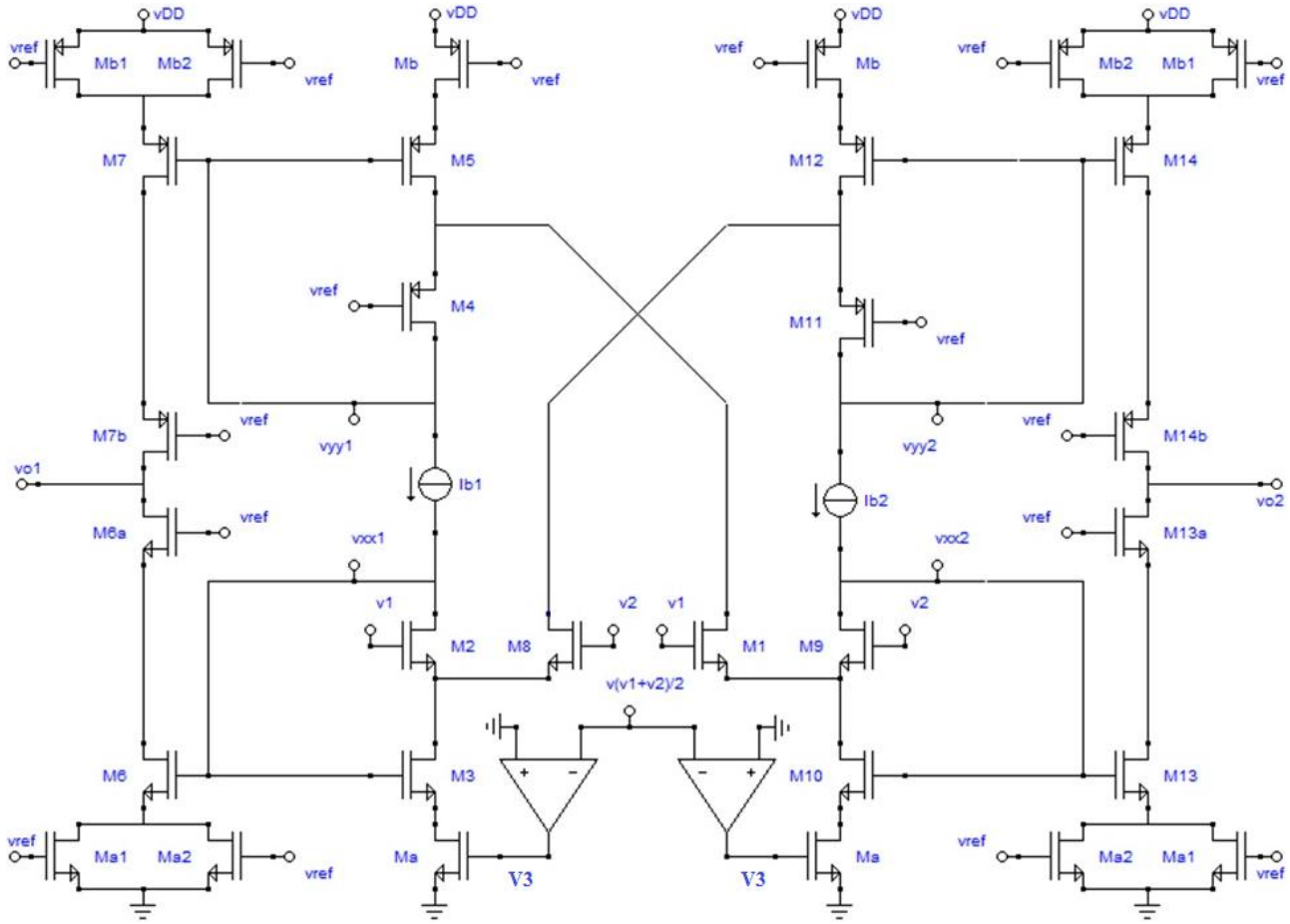


Fig.B. 16: AVcm correction from MOS in triode

The voltage signal to be applied on Ma gate transistors (indicated by V3) must be proportional to the input common mode signal (v_{icm}) that is applied to the terminals v1 and v2 of the OTA shown in Fig. B.16. In this way, in the presence of differential signal (V1 = -V2) on the gate of the MOS Ma, there will be no signal presence and therefore the differential mode gain will not be altered.

$$FDT_{V3} = \frac{V_{o1}}{V_3} = \frac{I_L}{V_3}\frac{V_{y1}}{I_L}\frac{V_{o1}}{V_{y1}} + \frac{V_{x1}}{V_3}\frac{V_{o1}}{V_{x1}} \quad \text{(B.441)}$$

$$F_{UP2} = \frac{I_L}{V_3}\frac{V_{y1}}{I_L}\frac{V_{o1}}{V_{y1}} = A^I \cdot B \cdot C \quad \text{(B.442)}$$

$$F_{DWN2} = \frac{V_{x1}}{V_3}\frac{V_{o1}}{V_{x1}} = D^I \cdot E \quad \text{(B.443)}$$

From the equations (B.441), (B.442), (B.443) it is noted that functions B, C, E are the same ones that were used in the calculation of the AVcm transfer function of the appendix B.3. For the FDT_{V3} study, the circuit of Fig.B.17 can be considered and the following paragraphs will calculate the A^I and D^I functions.

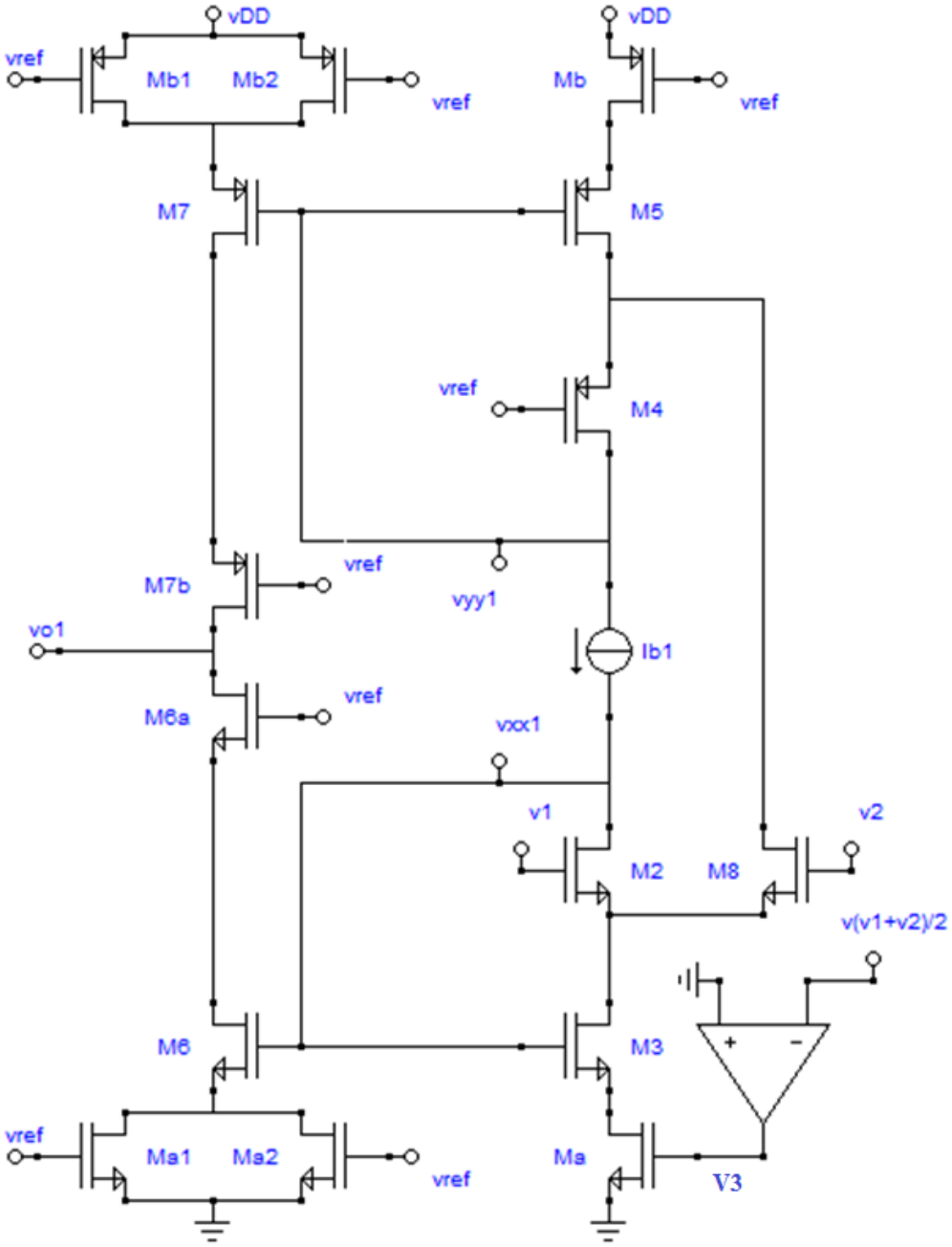


Fig.B. 17: half-circuit for the study of the Vo1/V3 transfer function

$$A^I = \frac{I_L}{V_3} = \frac{V_o G_L}{V_3} \quad \text{(B.444)}$$

$$D^I = \frac{V_{x1}}{V_3} \quad \text{(B.445)}$$

$$V_{o1} = V_3(F_{UP2} + F_{DWN2}) \quad \text{(B.446)}$$

B.4.1 Vo/V3 analysis

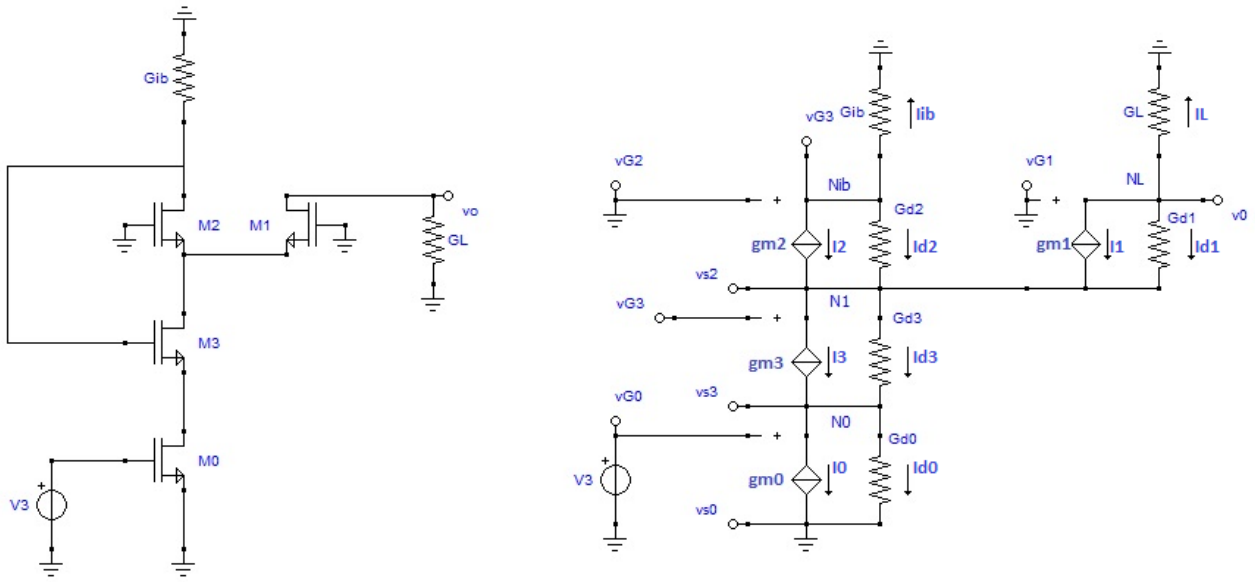


Fig.B. 18: (a) circuit to determine Vo/V3; (b) Equivalent Circuit

vo/v3=

=(- gm0 Gd3 Gd2 Gd1 - gm3 gm0 Gd2 Gd1 - gm0 Gib Gd3 Gd1 - gm3 gm0 Gib Gd1 - gm1 gm0 Gd3 Gd2 - gm3 gm1 gm0 Gd2 - gm1 gm0 Gib Gd3 - gm3 gm1 gm0 Gib)

+ (Gd3 Gd2 Gd1 Gd0 + Gib Gd2 Gd1 Gd0 + GL Gd2 Gd1 Gd0 + gm3 Gd2 Gd1 Gd0 + Gib Gd3 Gd1 Gd0 + GL Gib Gd1 Gd0 + gm2 Gib Gd1 Gd0 + gm3 gm2 Gd1 Gd0 + GL Gd3 Gd2 Gd0 + GL Gib Gd2 Gd0 + gm1 GL Gd2 Gd0 + gm3 GL Gd2 Gd0 + GL Gib Gd3 Gd0 + gm1 GL Gib Gd0 + gm2 GL Gib Gd0 + gm3 gm2 GL Gd0 + Gib Gd3 Gd2 Gd1 + GL Gd3 Gd2 Gd1 + gm3 Gib Gd2 Gd1 + gm3 GL Gd2 Gd1 + GL Gib Gd3 Gd1 + gm2 Gib Gd3 Gd1 + gm3 GL Gib Gd1 + gm3 gm2 Gib Gd1 + GL Gib Gd3 Gd2 + gm1 GL Gd3 Gd2 + gm3 GL Gib Gd2 + gm3 gm1 GL Gd2 + gm1 GL Gib Gd3 + gm2 GL Gib Gd3 + gm3 gm1 GL Gib + gm3 gm2 GL Gib) (B.447)

I apply KCL to the node N0

$V_{G0} = V_3$ (B.448)

I0=0 (B.449)

$I_3 + I_{d3} = I_0 + I_{d0}$ (B.450)

$(V_{S2} - V_{S3})G_{d3} + (V_{G3} - V_{S3})gm_3 = gm_0 V_3 + V_{S3} G_{d0}$ (B.451)

$V_{S2} G_{d3} - V_{S3} G_{d3} + V_{G3} gm_3 - V_{S3} gm_3 = gm_0 V_3 + V_{S3} G_{d0}$ (B.453)

$V_{S2} G_{d3} + V_{G3} gm_3 - gm_0 V_3 = V_{S3}(G_{d0} + G_{d3} + gm_3)$ (B.454)

$V_{S3} = \frac{V_{S2} G_{d3} + V_{G3} gm_3 - gm_0 V_3}{(G_{d0} + G_{d3} + gm_3)}$ (B.455)

$D_0 = (G_{d0} + G_{d3} + gm_3)$ (B.456)

$V_{S3} = \frac{V_{S2} G_{d3} + V_{G3} gm_3 - gm_0 V_3}{D_0}$ (B.457)

I apply KCL to the node N1

$I_{d2} + I_2 + I_{d1} + I_1 = I_3 + I_{d3}$ (B.458)

$I_{d2} + I_2 = -I_{ib}$ (B.459)

$I_{d1} + I_1 = -I_L$ (B.460)

$$-(I_{ib}+I_L)=I_3+I_{d3} \quad (B.461)$$
$$-(V_{G3}G_{ib}+V_0G_L)=(V_{G3}-V_{S3})gm_3+(V_{S2}-V_{S3})G_{d3} \quad (B.462)$$
$$-(V_{G3}G_{ib}+V_0G_L)=V_{S2}G_{d3}-V_{S3}G_{d3}+V_{G3}gm_3-V_{S3}gm_3 \quad (B.463)$$
$$-V_{G3}(G_{ib}+gm_3)-V_0G_L=V_{S2}G_{d3}-V_{S3}(G_{d3}+gm_3) \quad (B.464)$$

I apply KCL to the node NL

$$I_1+I_{d1}+I_L=0 \quad (B.465)$$
$$(V_0-V_{S2})G_{d1}+(-V_{S2})gm_1+V_0G_L=0 \quad (B.466)$$
$$V_0G_{d1}-V_{S2}G_{d1}-V_{S2}gm_1+V_0G_L=0 \quad (B.467)$$
$$V_0(G_{d1}+G_L)=V_{S2}(G_{d1}+gm_1) \quad (B.468)$$
$$V_{S2}=V_0\frac{(G_{d1}+G_L)}{(G_{d1}+gm_1)}=V_0\frac{N_1}{D_1} \quad (B.469)$$

-Nib

$$I_2+I_{d2}+I_{ib}=0 \quad (B.470)$$
$$(V_{G3}-V_{S2})G_{d2}-V_{S2}gm_2+V_{G3}G_{ib}=0 \quad (B.471)$$
$$V_{G3}G_{d2}-V_{S2}G_{d2}-V_{S2}gm_2+V_{G3}G_{ib}=0 \quad (B.472)$$
$$V_{G3}(G_{d2}+G_{ib})=V_{S2}(G_{d2}+gm_2) \quad (B.473)$$
$$V_{G3}=V_{S2}\frac{(G_{d2}+gm_2)}{(G_{d2}+G_{ib})}=V_{S2}\frac{N_3}{D_3} \quad (B.474)$$
$$V_{G3}=V_0\frac{N_1}{D_1}\frac{N_3}{D_3} \quad (B.475)$$

From N1:

$$-(I_{ib}+I_L)=I_3+I_{d3} \quad (B.476)$$
$$-V_{G3}(G_{ib}+gm_3)-V_0G_L=V_{S2}G_{d3}-V_{S3}(G_{d3}+gm_3) \quad (B.477)$$
$$V_{S2}=V_0\frac{(G_{d1}+G_L)}{(G_{d1}+gm_1)}=V_0\frac{N_1}{D_1} \quad (B.469)$$
$$V_{S3}=\frac{V_{S2}G_{d3}+V_{G3}gm_3-gm_0V_3}{D_0} \quad (B.478)$$
$$V_{G3}=V_0\frac{N_1}{D_1}\frac{N_3}{D_3} \quad (B.475)$$
$$-V_0\frac{N_1}{D_1}\frac{N_3}{D_3}(G_{ib}+gm_3)-V_0G_L=\quad V_0\frac{N_1}{D_1}G_{d3}-\frac{V_{S2}G_{d3}+V_{G3}gm_3-gm_0V_3}{D_0}(G_{d3}+gm_3) \quad (B.479)$$
$$-V_0\frac{N_1}{D_1}\frac{N_3}{D_3}(G_{ib}+gm_3)-V_0G_L=\quad V_0\frac{N_1}{D_1}G_{d3}-\frac{V_0\frac{N_1}{D_1}G_{d3}+V_0\frac{N_1}{D_1}\frac{N_3}{D_3}gm_3-gm_0V_3}{D_0}(G_{d3}+gm_3)$$
$$-V_0\frac{N_1}{D_1}\frac{N_3}{D_3}(G_{ib}+gm_3)-V_0G_L=$$
$$=V_0\frac{N_1}{D_1}G_{d3}-\frac{\left[V_0\left(\frac{N_1D_3}{D_1D_3}G_{d3}+\frac{N_1N_3}{D_1D_3}gm_3\right)-gm_0V_3\frac{D_1D_3}{D_1D_3}\right](G_{d3}+gm_3)}{D_0}$$
$$-V_0\frac{N_1N_3(G_{ib}+gm_3)-D_1D_3G_L}{D_1D_3}=$$
$$=V_0\frac{N_1}{D_1}G_{d3}-\frac{\left[V_0\left(\frac{N_1D_3G_{d3}+N_1N_3gm_3}{D_1D_3}\right)-\frac{gm_0V_3D_1D_3}{D_1D_3}\right](G_{d3}+gm_3)}{D_0}$$
$$-V_0\frac{N_1N_3(G_{ib}+gm_3)-D_1D_3G_L}{D_1D_3}=$$
$$=V_0\frac{D_0D_3N_1G_{d3}}{D_0D_1D_3}-\frac{[V_0(N_1D_3G_{d3}+N_1N_3gm_3)-gm_0V_3D_1D_3](G_{d3}+gm_3)}{D_0D_1D_3}$$
$$-V_0[D_0N_1N_3(G_{ib}+gm_3)-D_0D_1D_3G_L]=$$
$$=V_0D_0D_3N_1G_{d3}-[V_0(N_1D_3G_{d3}+N_1N_3gm_3)-gm_0V_3D_1D_3](G_{d3}+gm_3) \quad (B.480)$$
$$V_0[-D_0N_1N_3(G_{ib}+gm_3)+D_0D_1D_3G_L-D_0D_3N_1G_{d3}+(N_1D_3G_{d3}+N_1N_3gm_3)(G_{d3}+gm_3)]=$$

$= V_3[gm_0 D_1 D_3](G_{d3} + gm_3)$ (B.481)

$\frac{V_0}{V_3} =$

$= \frac{[gm_0 D_1 D_3](G_{d3}+gm_3)}{[-D_0 N_1 N_3(G_{ib}+gm_3)+D_0 D_1 D_3 G_L - D_0 D_3 N_1 G_{d3}+(N_1 D_3 G_{d3}+N_1 N_3 gm_3)(G_{d3}+gm_3)]}$ (B.482)

$\frac{V_0}{V_3} = \frac{N_T}{D_T}$ (B.483)

$N_T = gm_0 G_{d3} D_1 D_3 + gm_0 gm_3 D_1 D_3$ (B.484)

$D_1 = (gm_1 + G_{d1})$ (B.485)

$D_3 = (G_{ib} + G_{d2})$ (B.486)

$D_1 D_3 = (gm_1 + G_{d1})(G_{ib} + G_{d2}) = (gm_1 G_{ib} + gm_1 G_{d2} + G_{d1} G_{ib} + G_{d1} G_{d2})$ (B.487)

$N_T = gm_0 G_{d3} \ (gm_1 G_{ib} + gm_1 G_{d2} + G_{d1} G_{ib} + G_{d1} G_{d2})$

$+gm_0 gm_3 \ (gm_1 G_{ib} + gm_1 G_{d2} + G_{d1} G_{ib} + G_{d1} G_{d2})$ (B.488)

Vo/ V3=

(- gm0 Gd3 Gd2 Gd1 - gm3 gm0 Gd2 Gd1 - gm0 Gib Gd3 Gd1 - gm3 gm0 Gib Gd1 - gm1 gm0 Gd3 Gd2 - gm3 gm1 gm0 Gd2 - gm1 gm0 Gib Gd3 - gm3 gm1 gm0 Gib)

+ (Gd3 Gd2 Gd1 Gd0 + Gib Gd2 Gd1 Gd0 + GL Gd2 Gd1 Gd0 + gm3 Gd2 Gd1 Gd0 + Gib Gd3 Gd1 Gd0 + GL Gib Gd1 Gd0 + gm2 Gib Gd1 Gd0 + gm3 gm2 Gd1 Gd0 + GL Gd3 Gd2 Gd0 + GL Gib Gd2 Gd0 + gm1 GL Gd2 Gd0 + gm3 GL Gd2 Gd0 + GL Gib Gd3 Gd0 + gm1 GL Gib Gd0 + gm2 GL Gib Gd0 + gm3 gm2 GL Gd0 + Gib Gd3 Gd2 Gd1 + GL Gd3 Gd2 Gd1 + gm3 Gib Gd2 Gd1 + gm3 GL Gd2 Gd1 + GL Gib Gd3 Gd1 + gm2 Gib Gd3 Gd1 + gm3 GL Gib Gd1 + gm3 gm2 Gib Gd1 + GL Gib Gd3 Gd2 + gm1 GL Gd3 Gd2 + gm3 GL Gib Gd2 + gm3 gm1 GL Gd2 + gm1 GL Gib Gd3 + gm2 GL Gib Gd3 + gm3 gm1 GL Gib + gm3 gm2 GL Gib) (B.489)

B.4.2 Vx/V3 analysis

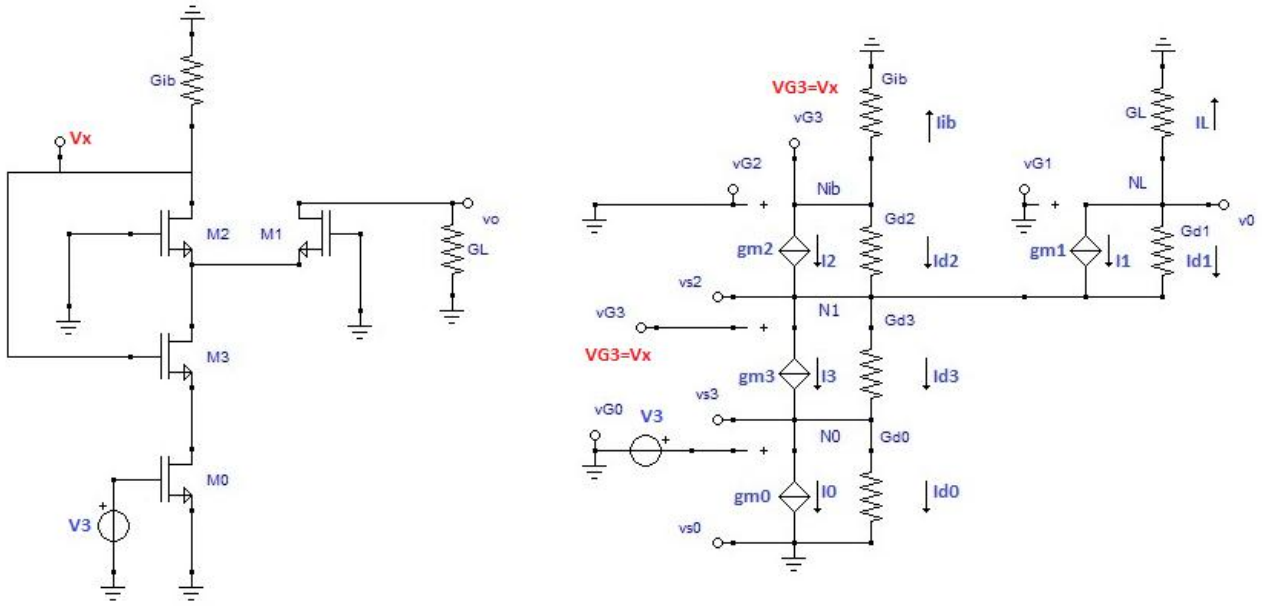


Fig.B. 19: (a) circuit to determine Vx/V3; (b) Equivalent Circuit

I apply KCL to the node N0

Being $V_{G0}=V_{S0}=0$, follows that the current is: I0=0.

$$I_3 + I_{d3} = I_0 + I_{d0} \quad \text{(B.490)}$$

$$(V_{S2} - V_{S3})G_{d3} + (V_{G3} - V_{S3})gm_3 = (V_{G0} - V_{S0})gm_0 + V_{S3}G_{d0} \quad \text{(B.491)}$$

$$V_{G0} = V_3 \quad \text{(B.492)}$$

$$V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 = V_3gm_0 + V_{S3}G_{d0} \quad \text{(B.493)}$$

$$V_{S2}G_{d3} + V_{G3}gm_3 - V_3gm_3 = V_{S3}(G_{d0} + G_{d3} + gm_3) \quad \text{(B.494)}$$

$$V_{S3} = \frac{V_{S2}G_{d3} + V_{G3}gm_3 - V_3gm_0}{(G_{d0} + G_{d3} + gm_3)} \quad \text{(B.495)}$$

$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad \text{(B.496)}$$

I place V_{G3}=Vx

$$V_{S3} = \frac{V_{S2}G_{d3} + V_xgm_3 - V_3gm_3}{D_0} \quad \text{(B.497)}$$

I apply KCL to the node N1

$$I_{d2} + I_2 + I_{d1} + I_1 = I_3 + I_{d3} \quad \text{(B.498)}$$

$$I_3 + I_{d3} = I_0 + I_{d0} = V_3gm_3 + V_{S3}G_{d0} \quad \text{(B.499)}$$

$$I_{d2} + I_2 = -I_{ib} \quad \text{(B.500)}$$

$$I_{d1} + I_1 = -I_L \quad \text{(B.501)}$$

$$-(I_{ib} + I_L) = I_3 + I_{d3} \quad \text{(B.502)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = V_3gm_0 + V_{S3}G_{d0} \quad \text{(B.503)}$$

$$-(V_xG_{ib} + V_0G_L) = V_3gm_0 + V_{S3}G_{d0} \quad \text{(B.504)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = (V_{G3} - V_{S3})gm_3 + (V_{S2} - V_{S3})G_{d3} \quad \text{(B.505)}$$

$$-(V_{G3}G_{ib} + V_0G_L) = V_{S2}G_{d3} - V_{S3}G_{d3} + V_{G3}gm_3 - V_{S3}gm_3 \quad \text{(B.506)}$$

V_{G3}=Vx

$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad \text{(B.508)}$$

I apply KCL to the node NL

$$I_1 + I_{d1} + I_L = 0 \quad \text{(B.509)}$$
$$(V_0 - V_{S2})G_{d1} + (V_1 - V_{S2})gm_1 + V_0G_L = 0 \quad \text{(B.510)}$$
$$V_0G_{d1} - V_{S2}G_{d1} + V_1gm_1 - V_{S2}gm_1 + V_0G_L = 0 \quad \text{(B.511)}$$
$$V_0(G_{d1} + G_L) + V_1gm_1 = V_{S2}(G_{d1} + gm_1) \quad \text{(B.512)}$$
$$V_0(G_{d1} + G_L) = V_{S2}(G_{d1} + gm_1) - V_1gm_1 \quad \text{(B.513)}$$
$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} - V_1\frac{gm_1}{(G_{d1}+G_L)} \quad \text{(B.514)}$$
$$V_1 = 0 \quad \text{(B.515)}$$
$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} = V_{S2}\frac{N_1}{D_1} \quad \text{(B.516)}$$
$$N_1 = (G_{d1} + gm_1) \quad \text{(B.517)}$$
$$D_1 = (G_{d1} + G_L) \quad \text{(B.518)}$$

I apply KCL to the node Nib

$$I_2 + I_{d2} + I_{ib} = 0 \quad \text{(B.519)}$$
$$(V_{G3} - V_{S2})G_{d2} + (V_{G2} - V_{S2})gm_2 + V_{G3}G_{ib} = 0 \quad \text{(B.520)}$$
$$V_{G2} = V_2 = 0 \quad \text{(B.521)}$$
$$V_{G3}G_{d2} - V_{S2}G_{d2} - V_{S2}gm_2 - V_{S2}gm_1 + V_{G3}G_{ib} = 0 \quad \text{(B.522)}$$
$$V_{G3}(G_{d2} + G_{ib}) = V_{S2}(G_{d2} + gm_2) \quad \text{(B.523)}$$

V_{G3}=Vx

$$V_{S2} = V_x\frac{(G_{d2}+G_{ib})}{(G_{d2}+gm_2)} = V_x\frac{N_3}{D_3} \quad \text{(B.524)}$$
$$N_3 = (G_{d2} + G_{ib}) \quad \text{(B.525)}$$
$$D_3 = (G_{d2} + gm_2) \quad \text{(B.526)}$$
$$-V_x(G_{ib} + gm_3) - V_0G_L = V_{S2}G_{d3} - V_{S3}(G_{d3} + gm_3) \quad \text{(B.527)}$$
$$-(V_xG_{ib} + V_0G_L) = V_3gm_0 + V_{S3}G_{d0} \quad \text{(B.528)}$$

Nib:

$$V_{S2} = V_x\frac{(G_{d2}+G_{ib})}{(G_{d2}+gm_2)} = V_x\frac{N_3}{D_3} \quad \text{(B.524)}$$
$$N_3 = (G_{d2} + G_{ib}) \quad \text{(B.525)}$$
$$D_3 = (G_{d2} + gm_2) \quad \text{(B.526)}$$

NL:

$$V_0 = V_{S2}\frac{(G_{d1}+gm_1)}{(G_{d1}+G_L)} = V_{S2}\frac{N_1}{D_1} = V_x\frac{N_3}{D_3}\frac{N_1}{D_1} \quad \text{(B.529)}$$
$$N_1 = (G_{d1} + gm_1) \quad \text{(B.517)}$$
$$D_0 = (G_{d0} + G_{d3} + gm_3) \quad \text{(B.496)}$$
$$D_1 = (G_{d1} + G_L) \quad \text{(B.518)}$$

N0:

$$V_{S3} = \frac{V_{S2}G_{d3}+V_xgm_3-V_3gm_0}{D_0} \quad \text{(B.497)}$$
$$V_{S3} = \frac{V_x\frac{N_3G_{d3}}{D_3}+V_xgm_3-V_3gm_0}{D_0} \quad \text{(B.530)}$$
$$V_{S3} = \frac{V_x(N_3G_{d3}+D_3gm_3)-V_3D_3gm_0}{D_0D_3} \quad \text{(B.531)}$$
$$-(V_xG_{ib} + V_0G_L) = V_3gm_0 + V_{S3}G_{d0} \quad \text{(B.532)}$$
$$-(V_xG_{ib} + V_x\frac{N_3}{D_3}\frac{N_1}{D_1}G_L) = V_3gm_0 + \frac{V_x(N_3G_{d3}+D_3gm_3)-V_3D_3gm_0}{D_0D_3}G_{d0} \quad \text{(B.533)}$$
$$-(\frac{V_xD_1D_3G_{ib}+V_xN_3N_1G_L}{D_1D_3}) = \frac{V_3D_0D_3gm_0+V_xG_{d0}(N_3G_{d3}+D_3gm_3)-V_3D_3gm_0G_{d0}}{D_0D_3} \quad \text{(B.534)}$$

$$\left(\frac{-V_x D_1 D_3 G_{ib} - V_x N_3 N_1 G_L}{D_1}\right) = \frac{V_3 D_0 D_3 gm_0 + V_x G_{d0}(N_3 G_{d3} + D_3 gm_3) - V_3 D_3 gm_0 G_{d0}}{D_0} \quad \text{(B.535)}$$

$$-V_x D_0 D_1 D_3 G_{ib} - V_x D_0 N_3 N_1 G_L =$$
$$= V_3 D_0 D_1 D_3 gm_0 + V_x D_1 G_{d0}(N_3 G_{d3} + D_3 gm_3) - V_3 D_1 D_3 gm_0 G_{d0} \quad \text{(B.536)}$$

$$-V_x D_0 D_1 D_3 G_{ib} - V_x D_0 N_3 N_1 G_L - V_x D_1 G_{d0}(N_3 G_{d3} + D_3 gm_3) =$$
$$= V_3 D_0 D_1 D_3 gm_0 - V_3 D_1 D_3 gm_0 G_{d0} \quad \text{(B.537)}$$

$$-V_x[D_0 D_1 D_3 G_{ib} - D_0 N_3 N_1 G_L - D_1 G_{d0}(N_3 G_{d3} + D_3 gm_3)] =$$
$$= V_3(D_0 D_1 D_3 gm_3 - D_1 D_3 gm_3 G_{d0}) \quad \text{(B.538)}$$

$$\frac{V_x}{V_3} = -\frac{(D_0 D_1 D_3 gm_0 - D_1 D_3 gm_0 G_{d0})}{[D_0 D_1 D_3 G_{ib} - D_0 N_3 N_1 G_L - D_1 G_{d0}(N_3 G_{d3} + D_3 gm_3)]} \quad \text{(B.539)}$$

$$\frac{V_x}{V_3} = \frac{N_T}{D_T} \quad \text{(B.540)}$$

$$N_1 = (G_{d1} + gm_1); \qquad N_2 = gm_1; \qquad N_3 = (G_{d2} + G_{ib}) \quad \text{(B.517)}$$

$$D_0 = (G_{d0} + G_{d3} + gm_3); \quad D_1 = (G_{d1} + G_L); \quad D_3 = (G_{d2} + gm_2) \quad \text{(B.518)}$$

$$N_T = N_{T1} + N_{T2} = (D_0 D_1 D_3 gm_0 - D_1 D_3 gm_0 G_{d0}) = \quad \text{(B.541)}$$

$$N_{T1} = D_0 D_1 D_3 gm_0 = gm_0(G_{d0} + G_{d3} + gm_3)(G_{d1} + G_L)(G_{d2} + gm_2) =$$
$$= gm_0 G_{d0} D_1 D_3 + gm_0(G_{d3} + gm_3)(G_{d1} + G_L)(G_{d2} + gm_2) = \quad \text{(B.542)}$$

$$N_{T2} = -D_1 D_3 gm_0 G_{d0} \quad \text{(B.543)}$$

$$N_T = gm_0(G_{d3} G_{d1} + G_{d3} G_L + gm_3 G_{d1} + gm_3 G_L)(G_{d2} + gm_2) = \quad \text{(B.544)}$$

$$N_T = G_{d2} gm_0(G_{d3} G_{d1} + G_{d3} G_L + gm_3 G_{d1} + gm_3 G_L) +$$
$$+ gm_2 gm_0(G_{d3} G_{d1} + G_{d3} G_L + gm_3 G_{d1} + gm_3 G_L) \quad \text{(B.544)}$$

Vx/V3=:

(- gm0 Gd3 Gd2 Gd1 - gm3 gm0 Gd2 Gd1 - gm2 gm0 Gd3 Gd1 - gm3 gm2 gm0 Gd1 - gm0 GL Gd3 Gd2 - gm3 gm0 GL Gd2 - gm2 gm0 GL Gd3 - gm3 gm2 gm0 GL)

+ (Gd3 Gd2 Gd1 Gd0 + Gib Gd2 Gd1 Gd0 + GL Gd2 Gd1 Gd0 + gm3 Gd2 Gd1 Gd0 + Gib Gd3 Gd1 Gd0 + GL Gib Gd1 Gd0 + gm2 Gib Gd1 Gd0 + gm3 gm2 Gd1 Gd0 + GL Gd3 Gd2 Gd0 + GL Gib Gd2 Gd0 + gm1 GL Gd2 Gd0 + gm3 GL Gd2 Gd0 + GL Gib Gd3 Gd0 + gm1 GL Gib Gd0 + gm2 GL Gib Gd0 + gm3 gm2 GL Gd0 + Gib Gd3 Gd2 Gd1 + GL Gd3 Gd2 Gd1 + gm3 Gib Gd2 Gd1 + gm3 GL Gd2 Gd1 + GL Gib Gd3 Gd1 + gm2 Gib Gd3 Gd1 + gm3 GL Gib Gd1 + gm3 gm2 Gib Gd1 + GL Gib Gd3 Gd2 + gm1 GL Gd3 Gd2 + gm3 GL Gib Gd2 + gm3 gm1 GL Gd2 + gm1 GL Gib Gd3 + gm2 GL Gib Gd3 + gm3 gm1 GL Gib + gm3 gm2 GL Gib)

B.4.3 Total transfer function considering the sources V1, V2, V3

Once I have calculated all the partial functions, I can proceed with the calculation of F_{UP}, F_{DWN}, F_{UP2} ed F_{DWN2}.

Summarizing, I have:

$$V_{icm} = \frac{V_1+V_2}{2} \quad (B.2)$$

$$\frac{V_{out}}{V_{icm}} = F_{UP} + F_{DWN} \quad (B.3)$$

$$\frac{V_{out}}{V_3} = F_{UP2} + F_{DWN2} \quad (B.441)$$

The overall transfer function will be due to the overlap of the effects due to the V_{icm} and V_3 sources:

$$F_{TOT} = \frac{V_{out}}{V_{icm}} + \frac{V_{out}}{V_3} = F_{UP} + F_{DWN} + F_{UP2} + F_{DWN2}$$

Applying instead of source V_3, a signal of the type:

V_3=-K*V_{icm},

it will be possible to reduce the effects of V_{icm}.

K is a attenuation factor and V_{icm} is the common mode source. The minus sign is to indicate that the signal will be in phase opposition to that applied to the terminals V_1 and V_2 of the circuit in Fig.B.4.

$$\frac{V_{out}}{V_3} = \frac{V_{out}}{-KV_{icm}} = \frac{1}{-K}\frac{V_{out}}{V_{icm}} = \frac{1}{-K}(F_{UP} + F_{DWN}) = F_{UP2} + F_{DWN2}$$

The value of K can be determined as follows:

$$K = -\frac{F_{UP}+F_{DWN}}{F_{UP2}+F_{DWN2}}$$

The K can be chosen in such a way that, for $V_{icm} \neq 0$, it must be $F_{TOT} = 0$:

$$F_{TOT} = \frac{V_{out}}{V_{icm}} + \frac{V_{out}}{V_3} = F_{UP} + F_{DWN} - KF_{UP} - KF_{DWN} = 0$$

A value of $(F_{UP}+F_{DWN})\neq 0$ will exist, at least in theoretical line, a K value which will allow me to tense the common mode gain of the entire circuit.

B.4.4 approximation of the functions previously calculated

The criteria used to approximate the partial functions previously calculated are:

- for MOS in saturation region:

$$(G_{dsx} + gm_x) \rightarrow gm_x$$

- for MOS in triode region:

$$(G_{dsx} + gm_x) \rightarrow G_{dsx}$$

B.4.5 Compact writing of the approximate functions F_{UP}, F_{DWN}, F_{UP2}, F_{DWN2}

The "a" pedicel in the functions indicates that these are approximate functions.

$F_{UPa}=$

$$\frac{G_{d0}\mathbf{G_L}[(gm_3gm_2G_{d1}-gm_3gm_1G_{d2})+G_{ib}(gm_2G_1-gm_1G_3-gm_1G_{d2})][G_{db}gm_{11}+gm_{12}gm_{11}](-gm_{7b}gm_7G_{db12})}{[G_{d0}G_L(gm_3gm_2)+(gm_1+gm_2)(G_{d0}G_LG_{ib}+G_LG_{ib}gm_3)][G_{ib}gm_{12}gm_{11}+G_{db}gm_{11}(G_{ib}+gm_{12})][G_{db12}(G_{d7b}G_{d7}+gm_{7b}G_N)+gm_{7b}(G_NG_{d7}+gm_7G_N)]}$$

$F_{DWNa}=$

$$\frac{G_L\,[G_{d0}(gm_1Gd_2-gm_2Gd_1-gm_2G_{d3})+gm_3(gm_1G_{d2}-gm_2G_{d1})](-gm_{6a}gm_6G_{da12})}{\{G_{d0}G_L[(gm_1G_{d2}+gm_3gm_{\,2}+gm_3G_{d2})+G_{ib}(gm_1+gm_2)]+G_LG_{ib}gm_3(gm_1+gm_2)\}(G_{da12}G_{d6a}G_{d6}+gm_{6a}G_PG_{da12})}$$

$$F_{UP2a}=\frac{V_{out}}{V_3}=\frac{NumC}{DenC}=\frac{I_L}{V_3}\frac{V_y}{I_L}\frac{V_{out}}{V_y}=$$

$$=\frac{V_3gm_0G_{ib}gm_1(G_{db}gm_{11}gm_{7b}gm_7G_{db12}+gm_{12}gm_{11}gm_{7b}gm_7G_{db12})}{(G_{d0}gm_2)(G_{ib}gm_{12}gm_{11}+G_{ib}G_{db}gm_{11}+G_{db}gm_{12}gm_{11})(G_{db12}G_{d7b}G_{\,d7}+gm_{7b}G_NG_{d7}+gm_{7b}G_NG_{db12}+gm_{7b}gm_7G_N)}$$

$$F_{DWN2a}=\frac{V_{out}}{V_3}=\frac{NumD}{DenD}=\frac{V_x}{V_3}\frac{V_{out}}{V_x}=$$

$$=\frac{Kgm_0(gm_3gm_2)(gm_{6a}gm_6G_{da12})}{[G_{d0}(gm_3gm_2)+G_{ib}G_{d0}(gm_1+gm_2)+G_{ib}(gm_3gm_1+gm_3gm_2)](G_{da12}G_{d6a}G_{d6}+gm_{6a}G_PG_{da12})}$$

The K that appears in the two functions can be used as a variable to correct the common mode signal.

$V_3=-k*V_{icm}$

If the source V_3 is set equal to the input common mode signal but out of phase by 180 ° and suitably attenuated, the output common mode signal can be corrected by leaving the output differential mode signal unaltered.

Appendix C
Proposed model

In this appendix there are the equations for Chapter 5 and where required are the mathematical passages that have allowed me to reach the end result.

C.1 Analytical equations

By applying a differential mode signal between input terminals V1 and V2 of the circuit represented in Fig.5.3, of the type:

$$V_1 = \frac{V_{id}}{2} \quad (C.1)$$

$$V_2 = -\frac{V_{id}}{2} \quad (C.2)$$

The differential mode signal result:

$$V_1 - V_2 = V_{id} \quad (C.3)$$

Case 1: $\mathbf{|V_{id}| < V_{GS} - V_T}$

In this case, both currents I_1 and I_2 are present. The respective equations are given by:

$$I_1 = I_{UP} = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2 \quad (C.4)$$

$$I_2 = I_{DWN} = K(V_{GS} - V_{id} - V_T)^2 = K(V_{OVQ} - V_{id})^2 \quad (C.5)$$

Writing the Kirchhoff equation for the equilibrium of currents at the output node, you get:

$$I_L = I_{UP} - I_{DWN} = K(V_{GS} + V_{id} - V_T)^2 - K(V_{GS} - V_{id} - V_T)^2 =$$
$$= K[(V_{GS} - V_T)^2 + {V_{id}}^2 + 2(V_{GS} - V_T)V_{id}] - K[(V_{GS} - V_T)^2 + {V_{id}}^2 - 2(V_{GS} - V_T)V_{id}] =$$
$$= K[2(V_{GS} - V_T)V_{id}] + K[2(V_{GS} - V_T)V_{id}] =$$
$$= 4K(V_{GS} - V_T)V_{id} = 4K(V_{OVQ})V_{id} \quad (C.6)$$

Case 2: $\mathbf{|V_{id}| > V_{GS} - V_T}$

In case 2 only one current (I_1 or I_2) should be considered as a branch is cut off. The respective equations are given by:

$$I_{UP} = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2 \quad (C.7)$$

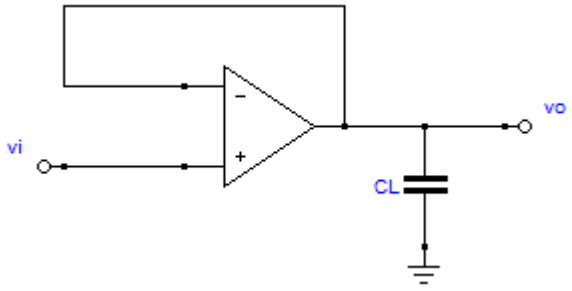
$$I_{DWN} = 0 \quad (C.8)$$

Writing the Kirchhoff equation for the equilibrium of currents at the output node, you get:

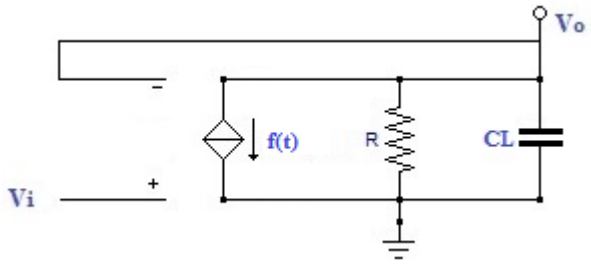
$$I_L = I_{UP} - I_{DWN} = I_{UP} = K(V_{OVQ} + V_{id})^2 \quad (C.9)$$

C.2 Simplified model and equation for non linear trend I-V

To estimate the settling time of the OTA of Fig.5.3, the latter was closed in buffer configuration. The terminals indicated by V_1 were connected to the output terminal while a voltage step was applied to terminal V_2.



Simplified model of the circuit of Fig.5.3 with buffered OTA



Model of the circuit in Fig.5.3

I consider case 2, in which $V_{id} > V_{GS} - V_T$. In this case assume that my f(t), shown in Fig.5.10, is equal to equation (C.7):

$$\mathbf{f(t) = I_1 = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2} \quad \text{(C.7)}$$

So I can write:

$$f(t) = k(V_{OVQ} + V_{id})^2 \quad \text{(C.10)}$$

Having closed the OTA as buffers the differential input signal can be written as:

$$V_{id}(t) = V_i(t) - V_o(t) \quad \text{(C.11)}$$

Considering the circuit in Fig.5.10, I can write the Kirchhoff equation for the equilibrium of currents at the output node, I get:

$$f(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad \text{(C.12)}$$

Developing the second member of (C.10), I get:

$$f(t) = kV_{OVQ}^2 + kV_{id}^2 + 2kV_{OVQ}V_{id} \quad \text{(C.13)}$$

Replace (C.11) ($V_{id} = V_i - V_o$) in (C.13), and I get:

$$f(t) = kV_{OVQ}^2 + k(V_i - V_o)^2 + 2kV_{OVQ}(V_i - V_o) \quad \text{(C.14)}$$

By developing terms in brackets, I get:

$$f(t) = kV_{OVQ}^2 + kV_i^2 + kV_o^2 - 2kV_iV_o + 2kV_{OVQ}V_i - 2kV_{OVQ}V_o \quad \text{(C.15)}$$

Highlighting some terms, I get:

$$f(t) = kV_o^2 - (2kV_i + 2kV_{OVQ})V_o + kV_{OVQ}^2 + kV_i^2 + 2kV_{OVQ}V_i \quad \text{(C.16)}$$

$$f(t) = kV_o^2 - (2kV_i + 2kV_{OVQ})V_o + k(V_{OVQ} + V_i)^2 \quad \text{(C.17)}$$

Going to replace C.17 in C.12, I get:

$$f(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad \text{(C.12)}$$

$$kV_o^2 - (2kV_i + 2kV_{OVQ})V_o + k(V_{OVQ} + V_i)^2 = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad \text{(C.18)}$$

Bringing all the terms to the left, C.18 becomes:

$$kV_o^2 - (2kV_i + 2kV_{OVQ})V_o - \frac{V_o}{R} - C\frac{dV_o}{dt} + k(V_{OVQ} + V_i)^2 = 0 \quad \text{(C.19)}$$

Common factor grouping, C.19 becomes:

$$kV_o^2 - (2kV_i + 2kV_{OVQ} - \frac{1}{R})V_o - C\frac{dV_o}{dt} + k(V_{OVQ} + V_i)^2 = 0 \quad \text{(C.20)}$$

By ordering the terms 4.20 can be rewritten as:

$$C\frac{dV_o}{dt} = kV_o^2 - (2kV_i + 2kV_{OVQ} - \frac{1}{R})V_o + k(V_{OVQ} + V_i)^2 \quad \text{(C.21)}$$

Dividing for C the first and second members, I get:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{1}{C}(2kV_i + 2kV_{OVQ} - \frac{1}{R})V_o + \frac{k}{C}(V_{OVQ} + V_i)^2 \quad \text{(C.22)}$$

Term 1/R negligible:

In case that R is much greater than 1, the C.22 can be written as:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2(V_i + V_{OVQ})V_o + \frac{k}{C}(V_i + V_{OVQ})^2 \quad \text{(C.23)}$$

If I put the term $(V_i + V_{OVQ}) = f(t)$, I can rewrite:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad \text{(C.24)}$$

If I put Vo = f (t), and I'm going to make the replacement in C.24, I get:

$$f'_{(t)} = \frac{k}{c}f_{(t)}^2 - \frac{k}{C}2f_{(t)}f_{(t)} + \frac{k}{C}f_{(t)}^2 \quad \text{(C.25)}$$

The terms for the second member are simplified, and I get:

$$f'_{(t)} = 0 \quad \text{(C.26)}$$

$$\frac{df_{(t)}}{dt} = \frac{d}{dt}(V_i + V_{OVQ}) = 0 \quad \text{(C.27)}$$

$$f(t) = (V_i + V_{OVQ}) = \text{costant} \quad \text{(C.28)}$$

The equation C.28 is a solution of equation C.23.

Term 1/R not negligible

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{1}{C}(2kV_i + 2kV_{OVQ} - \frac{1}{R})V_o + \frac{k}{C}(V_{OVQ} + V_i)^2 \quad \text{(C.22)}$$

If I put $(V_i + V_{OVQ}) = f(t)$ I can rewrite:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2f(t)V_o + \frac{1}{RC}V_o + \frac{k}{C}f_{(t)}^2 \quad \text{(C.29)}$$

C.3 Particolar solution of Riccati equation

As seen in the previous section if I ignore the term 1/R, and consider the input signal as constant then Vo=Vi = cost is a particular solution of equation C.23. Returning for convenience the equations considered in the previous section for R >> 1:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2(V_i + V_{OVQ})V_o + \frac{k}{C}(V_i + V_{OVQ})^2 \quad (C.23)$$

By putting the term $(V_i + V_{OVQ}) = f(t)$, the C.23 becomes:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad (C.24)$$

Equation C.24 admits as a solution Vo=f (t)=cost.

In the generic case where I do not neglect the term 1/R, I can write equation C.22 in a form similar to C.24.

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{1}{C}(2kV_i + 2kV_{OVQ} - \frac{1}{R})V_o + \frac{k}{C}(V_{OVQ} + V_i)^2 \quad (C.22)$$

If I put $(V_i + V_{OVQ}) = f(t)$ I can rewrite:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2f(t)V_o + \frac{1}{RC}V_o + \frac{k}{C}f_{(t)}^2 \quad (C.29)$$

The equation C.29 I can rewrite as:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2\alpha f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad (C.30)$$

By comparing C.29 with C.30 I can determine the parameter α

$$\frac{k}{c}V_o^2 - \frac{k}{C}2f(t)V_o + \frac{1}{RC}V_o + \frac{k}{C}f_{(t)}^2 = \frac{k}{c}V_o^2 - \frac{k}{C}2\alpha f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad (C.31)$$

By simplifying common terms, I get

$$-\frac{k}{C}2f(t) + \frac{1}{RC} = -\frac{k}{C}2\alpha f(t) \quad (C.32)$$

$$\frac{-2KRf(t)+1}{RC} = -\frac{k}{C}2\alpha f(t) \quad (C.33)$$

$$\frac{-2KRf(t)+1}{R} = -2k\alpha f(t) \quad (C.34)$$

$$\frac{2KRf(t)-1}{2kRf(t)} = \alpha \quad (C.35)$$

Equation C.35, can be rewritten as

$$\alpha = 1 - \frac{1}{2kRf(t)} \quad (C.36)$$

the equation C.30 admits type solution:

$$\overline{V_0} = \beta f(t) \quad (C.37)$$

With β and f(t) constants. Going to replace C.37 in C.30, I get:

$$0 = \frac{k}{c}(\beta f(t))^2 - \frac{k}{C}2\alpha f(t)\beta f + \frac{k}{C}f_{(t)}^2 \quad (C.38)$$

$$0 = \beta^2 f^2 - 2\alpha\beta f^2 + f^2 \quad (C.39)$$

Simplifying, I get:

$$0 = \beta^2 - 2\alpha\beta + 1 \quad (C.40)$$

The C.40 is a second-degree equation in the unknown β, which admits two solutions:

$$\beta_{1,2} = \alpha \pm \sqrt{\alpha^2 - 1} \quad (C.41)$$

with α:

$$\alpha = 1 - \frac{1}{2kRf(t)} \quad (C.36)$$

Replacing C.36 in C.41, I get:

$$\beta_{1,2} = 1 - \frac{1}{2kRf(t)} \pm \sqrt{(1 - \frac{1}{2kRf(t)})^2 - 1} \quad \text{(C.42)}$$

$$\beta_{1,2} = 1 - \frac{1}{2kRf(t)} \pm \sqrt{1 - \frac{2}{2kRf(t)} + (\frac{1}{2kRf(t)})^2 - 1} \quad \text{(C.43)}$$

$$\beta_{1,2} = 1 - \frac{1}{2kRf(t)} \pm \sqrt{-\frac{1}{kRf(t)} + (\frac{1}{2kRf(t)})^2} \quad \text{(C.44)}$$

The solution C.37 can be rewritten as:

$$\overline{V_0} = \beta f(t) = (\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \quad \text{(C.45)}$$

To show that C.45 is a solution of C.30, which carry for convenience, I go to make the substitution in the equation:

$$\frac{dV_o}{dt} = \frac{k}{c} V_o^2 - \frac{k}{C} 2\alpha f(t) V_o + \frac{k}{C} f_{(t)}^2 \quad \text{(C.30)}$$

$$0 = \left[(\alpha \pm \sqrt{\alpha^2 - 1}) f(t)\right]^2 - 2\alpha(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) f + f^2 \quad \text{(C.46)}$$

$$0 = (\alpha \pm \sqrt{\alpha^2 - 1})^2 f^2 - 2\alpha(\alpha \pm \sqrt{\alpha^2 - 1}) f^2 + f^2 \quad \text{(C.47)}$$

$$0 = (\alpha^2 \pm 2\alpha\sqrt{\alpha^2 - 1} + \alpha^2 - 1) f^2 - 2\alpha^2 f^2 \mp 2\alpha f^2 \sqrt{\alpha^2 - 1} + f^2 \quad \text{(C.48)}$$

$$0 = \alpha^2 f^2 \pm 2\alpha f^2 \sqrt{\alpha^2 - 1} + f^2 \alpha^2 - f^2 - 2\alpha^2 f^2 \mp 2\alpha f^2 \sqrt{\alpha^2 - 1} + f^2 = 0 \quad \text{(C.49)}$$

The C.45 is therefore a particular solution of the Riccati equation.

C.4 General solution of Riccati eqution

Considering the equation in normal form

$$y' + A(x)y = B(x)y^2 + C(x) \quad \text{(C.50)}$$

For:

B(X)=0, it is reduced to a non-homogeneous linear equation;

B(x)=C(x)=0, becomes a homogeneous linear equation;

B(x)≠0, C(x)=0, it is reduced to a Bernulli equation with n = 2;

B(x)≠0, C(x)≠0, is called the Riccati equation;

The equation under consideration is that obtained in the previous paragraph, 4.30:

$$\frac{dV_o}{dt} = \frac{k}{c}V_o^2 - \frac{k}{C}2\alpha f(t)V_o + \frac{k}{C}f_{(t)}^2 \quad \text{(C.30)}$$

Which is attributable to C.50 with B(x) ≠ 0, C(x) ≠ 0 which is the fourth case, that is, the equation of Riccati. Its integration is possible if its particular integral y(x) = y_1(x) is known. In this case with appropriate changes of the variable, it can be brought back to a Bernoulli equation which in turn becomes a linear equation.

If y_1 is a particular integer of C.50 it satisfies the equation, that is:

$$y_1' + A(x)y_1 = B(x)y_1^2 + C(x) \quad \text{(C.51)}$$

By making the difference between C.50 and C.51, I get:

$$y' - y_1' + (y - y_1)A(x) = (y^2 - y_1^2)B(x) \quad \text{(C.52)}$$

Placing:

$$z = y - y_1 \quad \text{(C.53)}$$

$$z' = y' - y_1' \quad \text{(C.54)}$$

$$y^2 - y_1^2 = (y - y_1)(y + y_1) = (y - y_1)(y - y_1 + 2y_1) = z(z + 2y_1) \quad \text{(C.55)}$$

And going to replace C.53, C.54 and C.55 in C.52, I get:

$$z' + A(x)z = z(z + 2y_1)B(x) \quad \text{(C.56)}$$

$$z' + A(x)z = z^2B(x) + 2y_1B(x)z \quad \text{(C.57)}$$

$$z' + (A(x) - 2y_1B(x))z = B(x)z^2 \quad \text{(C.58)}$$

The C.58 is a Bernoulli equation with n = 2 whose integral is:

$$z = e^{-\int(A-2y_1B)dx}.[-\int B \cdot e^{-\int(A-2y_1B)dx} \cdot dx + k]^{-1} \quad \text{(C.59)}$$

Replacing z with equation C.53, I get:

$$y - y_1 = e^{-\int(A-2y_1B)dx}.[-\int B \cdot e^{-\int(A-2y_1B)dx} \cdot dx + k]^{-1} \quad \text{(C.60)}$$

I can write the C.60 in canonical form:

$$y = y_1 - \frac{e^{-\int(A-2y_1B)dx}}{\int B \cdot e^{-\int(A-2y_1B)dx}.dx+k} = y_1 - \frac{N}{D} \quad \text{(C.61)}$$

For convenience I rewrite the equation I would like to know about the general integral and the comparison with the C.50:

$$\frac{dV_o}{dt} + \frac{k}{C}2\alpha f(t)V_o = \frac{k}{c}V_o^2 + \frac{k}{C}f_{(t)}^2 \quad \text{(C.62)}$$

$$y' + A(x)y = B(x)y^2 + C(x) \quad \text{(C.50)}$$

The comparison shows that:

$$A(x) = \frac{k}{C}2\alpha f(t) \quad \text{(C.63)}$$

$$B(x) = \frac{k}{c} \quad \text{(C.64)}$$

$$C(x) = \frac{k}{C}f_{(t)}^2 \quad \text{(C.65)}$$

$$y_1 = \overline{V_0} = \beta f(t) = (\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \quad \text{(C.66)}$$

For convenience I'm going to break the equation C.61 into three parts, y1, N (numerator) and D (denominator).

$$N = e^{-\int (A - 2y_1 B)dx} \quad \text{(C.67)}$$

$$D = \int B \cdot e^{-\int (A - 2y_1 B)dx} \cdot dx + k \quad \text{(C.68)}$$

I'm going to replace C.63, C.64 and C.66 in C.67:

$$N = e^{-\int \left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) dx} \quad \text{(C.69)}$$

In the case of step signal I can consider f(t)=f(x)=constant and I can rewrite C.69 as:

$$N = e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) \int dx} \quad \text{(C.70)}$$

$$N = e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x} \quad \text{(C.71)}$$

I'm going to replace C.63, C.64 and C.66 in C.68:

$$D = \int \frac{k}{c} \cdot e^{-\int \left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) dx} \cdot dx + k \quad \text{(C.72)}$$

In the case of step signal I can consider f(t)=f(x)=constant and I can rewrite C.72 as:

$$D = \frac{k}{c} \int e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) \int dx} \cdot dx + k \quad \text{(C.73)}$$

$$D = \frac{k}{c} \int e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x} \cdot dx + k \quad \text{(C.74)}$$

The integer of C.74 is:

$$D = -\frac{k}{c} \cdot \frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}} + k \quad \text{(C.75)}$$

By simplifying the numerator and denominator the term k/c, C.75 becomes:

$$D = -\frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t)} + k \quad \text{(C.76)}$$

I'm going to replace the results obtained, C.71 and C.76, in C.61 that I carry for convenience:

$$y = y_1 - \frac{e^{-\int (A - 2y_1 B)dx}}{\int B \cdot e^{-\int (A - 2y_1 B)dx} \cdot dx + k} = y_1 - \frac{N}{D} \quad \text{(C.61)}$$

$$y = y_1 - \frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{-\frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t)} + k} \quad \text{(C.77)}$$

A denominator there is a sign - so the C.77 can write it as:

$$y = y_1 + \frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{\frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t)} + k} \quad \text{(C.78)}$$

$$y = y_1 + \frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{\frac{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x} + k(2\alpha f(t) - 2\left(\alpha \pm \sqrt{\alpha^2 - 1}\right) f(t))}{2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t)}} \quad \text{(C.79)}$$

$$y = y_1 + \frac{(2\alpha f(t) - 2\left(\alpha \pm \sqrt{\alpha^2 - 1}\right) f(t)) e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x}}{e^{-\left(\frac{k}{C} 2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \frac{k}{c}\right) x} + k(2\alpha f(t) - 2\left(\alpha \pm \sqrt{\alpha^2 - 1}\right) f(t))} \quad \text{(C.80)}$$

In C.80 I will also replace y1:

$$y_1 = \overline{V_0} = \beta f(t) = (\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \quad \text{(C.66)}$$

$$y = (\alpha \pm \sqrt{\alpha^2 - 1})f(t) + \frac{(2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2-1})f(t))e^{-\left(\frac{k}{C}2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2-1})f(t)\frac{k}{c}\right)x}}{e^{-\left(\frac{k}{C}2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2-1})f(t)\frac{k}{c}\right)x} + k(2\alpha f(t) - 2(\alpha \pm \sqrt{\alpha^2-1})f(t))} \quad (C.81)$$

C.4.1 Constant integration of the general equation of Riccati

$$y = y_1 - \frac{e^{-\int (A - 2y_1 B)dx}}{\int B \cdot e^{-\int (A-2y_1 B)dx} \cdot dx + k} = y_1 - \frac{N}{D} \quad (C.61)$$

The equation C.61 can be rewritten as:

$$y = y_1 - \frac{e^{-\int T(x)dx}}{\int B \cdot e^{-\int T(x)dx} \cdot dx + k} = y_1 - \frac{N}{D} \quad (C.82)$$

where,

$$T(x) = (A - 2y_1 B) \quad (C.83)$$

For a voltage step I can consider T(x) independent of the x variable, and then take it out of the integral sign. I write the equation C.82 in another form:

$$y = y_1 - \frac{1}{e^{\int T(x)dx}[\int B \cdot e^{-\int T(x)dx} \cdot dx + k]} \quad (C.84)$$

$$y = y_1 - \frac{1}{e^{Tx}[B \cdot \int e^{-Tx} \cdot dx + k]} \quad (C.85)$$

$$y = y_1 - \frac{1}{e^{Tx}[-\frac{B}{T} \cdot e^{-Tx} + k]} \quad (C.86)$$

$$y = y_1 - \frac{1}{[-\frac{B}{T} + ke^{Tx}]} \quad (C.87)$$

Constant integration

$$y_0 = y_1 - \frac{1}{[-\frac{B}{T} + k]} \quad (C.89)$$

$$y_1 - y_0 = \frac{1}{[-\frac{B}{T} + k]} \quad (C.90)$$

$$\frac{1}{y_1 - y_0} = -\frac{B}{T} + k \quad (C.91)$$

$$k = \frac{1}{y_1 - y_0} + \frac{B}{T} \quad (C.92)$$

C.5 Differential equation solution for I-V linear trend

For convenience, carry out the equations in paragraph 4.2 regarding the case study 1, where the current dependence on the differential voltage is linear.

Case 1: $V_{id} < V_{GS} - V_T$

$$I_1 = I_{UP} = K(V_{GS} + V_{id} - V_T)^2 = K(V_{OVQ} + V_{id})^2 \quad \text{(C.4)}$$

$$I_2 = I_{DWN} = K(V_{GS} - V_{id} - V_T)^2 = K(V_{OVQ} - V_{id})^2 \quad \text{(C.5)}$$

$$I_L = I_{UP} - I_{DWN} = K(V_{GS} + V_{id} - V_T)^2 - K(V_{GS} - V_{id} - V_T)^2 =$$
$$= K[(V_{GS} - V_T)^2 + {V_{id}}^2 + 2(V_{GS} - V_T)V_{id}] - K[(V_{GS} - V_T)^2 + {V_{id}}^2 - 2(V_{GS} - V_T)V_{id}] =$$
$$= K[2(V_{GS} - V_T)V_{id}] + K[2(V_{GS} - V_T)V_{id}] =$$
$$= 4K(V_{GS} - V_T)V_{id} = 4K(V_{OVQ})V_{id} \quad \text{(C.6)}$$

Considering "Case 1" ($V_{id} < V_{GS} - V_T$):

$$\mathbf{f(t) = I_1 - I_2 = 4K(V_{OVQ})V_{id}} \quad \text{(C.7)}$$

$$f(t) = 4K(V_{OVQ})V_{id} \quad \text{(C.94)}$$

$$V_{id}(t) = V_i(t) - V_o(t) \quad \text{(C.95)}$$

$$f(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad \text{(C.96)}$$

I replace the (C.95) in (C.94)

$$f(t) = 4K(V_{OVQ})(V_i(t) - V_o(t)) \quad \text{(C.97)}$$

Development the second member of (C.97):

$$f(t) = 4K(V_{OVQ})V_i(t) - 4K(V_{OVQ})V_o(t) \quad \text{(C.98)}$$

For convenience I rewrite (C.96) and go to replace f(t) with the result of (C.98)

$$f(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad \text{(C.96)}$$

$$4K(V_{OVQ})V_i(t) - 4K(V_{OVQ})V_o(t) = \frac{V_o}{R} + C\frac{dV_o}{dt} \quad \text{(C.99)}$$

I try to write (C.99) in canonical order by sorting and grouping some terms:

$$-4K(V_{OVQ})V_o(t) - \frac{V_o}{R} - C\frac{dV_o}{dt} + 4K(V_{OVQ})V_i(t) = 0 \quad \text{(C.100)}$$

$$(4KV_{OVQ} + \frac{1}{R})V_o(t) + C\frac{dV_o}{dt} - 4K(V_{OVQ})V_i(t) = 0 \quad \text{(C.101)}$$

$$C\frac{dV_o}{dt} + \left(4KV_{OVQ} + \frac{1}{R}\right)V_o(t) = 4K(V_{OVQ})V_i \quad \text{(C.102)}$$

$$\frac{dV_o}{dt} + \left(\frac{4KV_{OVQ}}{C} + \frac{1}{CR}\right)V_o(t) = \frac{4K(V_{OVQ})V_i}{C} \quad \text{(C.103)}$$

The equation (C.103) is of the form:

$$\frac{dV_o}{dt} + A(t)V_o = B(t) \quad \text{(C.104)}$$

If:

B(x)=0; the (C.104) is called a homogeneous linear equation

B(x)≠0; the (C.104) is called a not homogeneous linear equation

The general integer is given by the sum of the homogeneous equation solution plus a particular solution.

C.5.1 Not homogeneous equation solution

I rewrite for convenience the C.103, C.104:

$$\frac{dV_o}{dt} + \left(\frac{4KV_{OVQ}}{C} + \frac{1}{CR}\right)V_o(t) = \frac{4K(V_{OVQ})V_i}{C} \quad \text{(C.103)}$$

$$\frac{dV_o}{dt} + A(t)V_o = B(t) \quad \text{(C.104)}$$

The previous equation can be written in the form:

$$dV_o + A(t)V_o dt = B(t)dt \quad \text{(C.105)}$$

I consider the first member of equation C.105: (C.106)

In order to integrate (C.105) we look for a function I(t) such that (C.106) multiplied by this function results in the total differential of y·I(t), that is:

$$I(t)dV_o + I(t)A(t)V_o dt = d[V_o \cdot I(t)] \quad \text{(C.107)}$$

By developing the (C.107), I get:

$$\mathbf{I(t)dV_o} + I(t)A(t)V_o dt = \mathbf{I(t)dV_o} + V_o \cdot d[I(t)] \quad \text{(C.108)}$$

By simplifying some terms, I get:

$$I(t)A(t)\mathbf{V_o}dt = \mathbf{V_o} \cdot d[I(t)] \quad \text{(C.109)}$$

$$I(t)A(t)dt = d[I(t)] \quad \text{(C.110)}$$

The (C.110) can be rewritten in the form:

$$\frac{d[I(t)]}{I(t)} = A(t)dt \quad \text{(C.111)}$$

By integrating both members, I get:

$$\int \frac{d[I(t)]}{I(t)} = \int A(t)dt \quad \text{(C.112)}$$

$$\log(c \cdot I(x)) = \int A(t)dt \quad \text{(C.113)}$$

$$c \cdot I(x) = e^{\int A(t)dt} \quad \text{(C.114)}$$

One of the many functions that verify the (C.107) is:

$$I(x) = e^{\int A(t)dt} \quad \text{(C.115)}$$

Obtained for c = 1. Resuming the starting equation (C.105)

$$dV_o + A(t)V_o dt = B(t)dt \quad \text{(C.105)}$$

And multiplying both members for I (t), you have:

$$I(t)dV_o + I(t)A(t)V_o dt = I(t)B(t)dt \quad \text{(C.116)}$$

Comparing the (C.116) with what is written in (C.107), which carry it for convenience:

$$I(t)dV_o + I(t)A(t)V_o dt = d[V_o \cdot I(t)] \quad \text{(C.107)}$$

The (C.116) can be written:

$$d[V_o \cdot I(t)] = I(t)B(t)dt \quad \text{(C.117)}$$

The (4.117), integrated, provides the general integer of (C.105) and therefore of (C.104):

$$\int d[V_o \cdot I(t)] = \int I(t)B(t)dt \quad \text{(C.118)}$$

$$V_o \cdot I(t) = \int I(t)B(t)dt \quad \text{(C.119)}$$

$$V_o = \frac{\int I(t)B(t)dt}{I(t)} \quad \text{(C.120)}$$

With I(t), given by (C.115). Going to replace the value of I(t) in (C.120), you get:

$$V_o = \frac{\int e^{\int A(t)dt}B(t)dt}{e^{\int A(t)dt}} = \frac{N}{D} \quad \text{(C.121)}$$

Where N and D are respectively:

$$N = \int e^{\int A(t)dt}B(t)dt \quad \text{(C.122)}$$

$$D = e^{\int A(t)dt} \quad \text{(C.123)}$$

By comparing the result of the general equation (4.104) with that (4.103) I want to know the solution, I can determine the terms A(t) and B(t):

$$\frac{dV_o}{dt} + \left(\frac{4KV_{OVQ}}{C} + \frac{1}{CR}\right)V_o(t) = \frac{4K(V_{OVQ})V_i}{C} \quad \text{(C.103)}$$

From the comparison you can write:

$$A(t) = \left(\frac{4KV_{OVQ}}{C} + \frac{1}{CR}\right) \quad \text{(C.124)}$$

$$B(t) = \frac{4K(V_{OVQ})V_i}{C} \quad \text{(C.125)}$$

Considering terms A(t) and B(t) as constants, (C.122) and (C.123) can be rewritten as:

$$N = B \cdot \int e^{A\cdot t}dt = \frac{B}{A}e^{A\cdot t} + c \quad \text{(C.126)}$$

$$D = e^{A\cdot t} \quad \text{(C.127)}$$

The (C.121) can be rewritten as:

$$V_o = \frac{\int e^{\int A(t)dt}B(t)dt}{e^{\int A(t)dt}} = \frac{\frac{B}{A}e^{A\cdot t}+c}{e^{A\cdot t}} = \frac{B}{A} + c \cdot e^{-A\cdot t} \quad \text{(C.128)}$$

C.5.2 Integration constant calculation

In the case of a unit step, at instant t = 0, Vi = 1 and Vo = 0.05:

$$A(t) = \left(\frac{4KV_{OVQ}}{C} + \frac{1}{CR}\right) \quad \text{(C.124)}$$

$$B(t) = \frac{4K(V_{OVQ})V_i}{C} \quad \text{(C.125)}$$

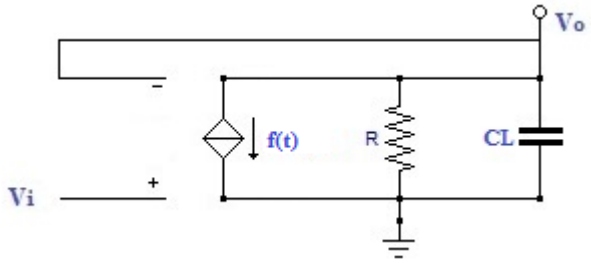
I can rewrite the C.128 as:

$$V_o(t) = \frac{V_2}{1+\frac{1}{4KRV_{OVQ}}} + ce^{-A\cdot t} = \rho V_2 + ce^{-A\cdot t} \quad \text{(C.129)}$$

With "c" such that $V_o(0) = V_i - V_{ovq}$

$$c = V_i(1-\rho) - V_{ovq} < 0 \quad \text{(C.130)}$$

C.6 Calculation of the proposed model's settling time



circuital model

$$f(v_{id}) = \begin{cases} 4kV_{ovq}V_{id} & |V_{id}| < V_{ovq} \\ sgn(V_{id})k(V_{ovq} + V_{id})^2 & |V_{id}| > V_{ovq} \end{cases} \quad \text{(C.131)}$$

The regime output voltage is:

$$4kV_{ovq}(V_i - V_o) = \frac{V_o}{R} \quad \text{(C.132)}$$

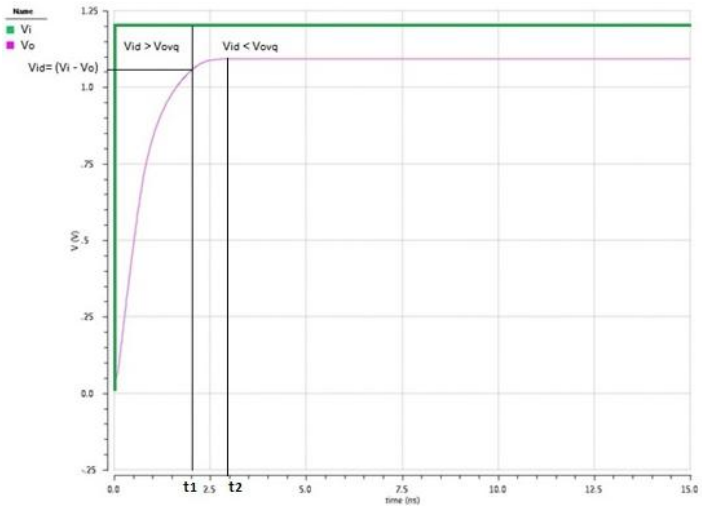
$$V_o = \frac{4kRV_{ovq}}{1+4kRV_{ovq}}V_i \qquad (V_o = V_i \quad per \ R \to \infty) \quad \text{(C.133)}$$

step of input:

$$V_i(0^-) = V_1 \quad \text{(C.134)}$$

$$V_i(0^+) = V_2 = V_1 + \Delta \qquad \Delta > V_{ovq} \quad \text{(C.135)}$$

$$V_{id}(0^+) = V_2 - \frac{4kRV_{ovq}}{1+4kRV_{ovq}}V_1 > V_{ovq} \qquad (V_1 < 0) \quad \text{(C.136)}$$



respnse to input step

The settling time is given by the sum of two contributions:

$t_{set}=t_1+t_2$ (C.137)

Time t_1 is due to the case where the current flowing in the load (I_L) is nonlinear (case 2) while t_2 is due to the case where the current I_L has a linear trend (case 1).

C.6.1 Time calculation t_1

Explaining the connection between input voltage and output voltage, I have

$$V_{id} = V_i - V_0 \quad \text{(C.138)}$$

Taking into account that the final value (maximum value) for the differential input voltage, is when

$$V_{id} = V_{GS} - V_T = V_i - V_0 = V_{ov} \quad \text{(C.139)}$$

By expressing the output voltage Vo in function of Vov and indicating with t_1, the time instant in which the output voltage reaches the final value, it has:

$$V_0(t1) = V_i - V_{ov} \quad \text{(C.140)}$$

For convenience, carry some equations obtained for the calculation of the integral of the Riccati equation

$$(V_i + V_{OVQ}) = f(t)$$

$$\alpha = 1 + \frac{1}{2kRf(t)} \quad \text{(C.141)}$$

The particular integral of Riccati's equation is:

$$y_1 = \overline{V_0} = \beta f(t) = (\alpha \pm \sqrt{\alpha^2 - 1}) f(t) \quad \text{(C.142)}$$

The general integral of Riccati's equation is:

$$y = y_1 - \frac{1}{[-\frac{B}{T} + ke^{Tx}]} \quad \text{(C.143)}$$

$$V(t) = \overline{V_0} - \frac{1}{[-\frac{B}{T} + ke^{Tt}]}$$

The integration constant is:

$$y_0 = y_1 - \frac{1}{[-\frac{B}{T} + k]} \quad \text{(C.144)}$$

$$y_1 - y_0 = \frac{1}{[-\frac{B}{T} + k]} \quad \text{(C.145)}$$

$$\frac{1}{y_1 - y_0} = -\frac{B}{T} + k \quad \text{(C.146)}$$

$$k = \frac{1}{y_1 - y_0} + \frac{B}{T} \quad \text{(C.147)}$$

if consider y_0=0, I have

$$k = \frac{1}{y_1} + \frac{B}{T} \quad \text{(C.148)}$$

$$V(t) = \overline{V_0} - \frac{1}{[-\frac{B}{T} + (\frac{1}{\overline{V_0}} + \frac{B}{T})e^{Tt}]} \quad \text{(C.149)}$$

I'm going to impose the condition that allows me to get t_1:

$$V_0(t1) = V_i - V_{ov} = \overline{V_0} - \frac{1}{[-\frac{B}{T} + (\frac{1}{\overline{V_0}} + \frac{B}{T})e^{Tt}]} \quad \text{(C.150)}$$

$$V_i - V_{ov} - \overline{V_0} = -\frac{1}{[-\frac{B}{T} + (\frac{1}{\overline{V_0}} + \frac{B}{T})e^{Tt}]} \quad \text{(C.151)}$$

$$[-\frac{B}{T} + (\frac{1}{\overline{V_0}} + \frac{B}{T})e^{Tt}] = -\frac{1}{(V_i - V_{ov} - \overline{V_0})} \quad \text{(C.152)}$$

$$(\frac{1}{\overline{V_0}} + \frac{B}{T})e^{Tt} = \frac{B}{T} - \frac{1}{(V_i - V_{ov} - \overline{V_0})} \quad \text{(C.153)}$$

$$e^{Tt} = \frac{\frac{B}{T} - \frac{1}{(V_i - V_{ov} - \overline{V_0})}}{(\frac{1}{\overline{V_0}} + \frac{B}{T})} \quad \text{(C.154)}$$

$$t_1 = \frac{1}{T} \ln \left(\frac{\frac{B}{T} - \frac{1}{(V_i - V_{ov} - \overline{V_0})}}{(\frac{1}{\overline{V_0}} + \frac{B}{T})} \right) \quad \text{(C.155)}$$

If consider yo≠0, I get:

$$t_1 = \frac{1}{T}\ln\left(\frac{\frac{B}{T}-\frac{1}{(V_i-V_{ov}-\overline{V_0})}}{\frac{1}{\overline{V_0}-y_0}+\frac{B}{T}}\right) \quad \text{(C.156)}$$

C.6.2 Time calculation t_2

In the previous section, the general integral of the differential equation in the linear zone was found, which carry over for convenience:

$$V_o(t=0) = \frac{V_2}{1+\frac{1}{4KRV_{OVQ}}} + ce^{-A\cdot t} = \rho V_2 + ce^{-A\cdot t} \quad \text{(C.129)}$$

Where "c" is the integration constant and is given by:

$$c = V_2(1-\rho) - V_{ovq} < 0 \quad \text{(C.130)}$$

The settling time with an error ε is given by t_1+t_2 where t_2 is the time for which:

$$V_o = \rho V_2 - \rho(V_2 - V_1)\varepsilon \quad \text{(C.157)}$$

$$\rho V_2 - \rho(V_2 - V_1)\varepsilon = \rho V_2 + ce^{-At_2} = \rho V_2 - |c|e^{-At_2} \quad \text{(C.158)}$$

$$t_2 = \frac{1}{A} ln \frac{|c|}{\varepsilon\rho(V_2-V_1)} \quad \text{(C.159)}$$

C.6.3Solution of homogeneous associated

$$\frac{dV_o}{dt} + A(t)V_o = 0 \quad \text{(C.160)}$$

$$\frac{dV_o}{dt} = -A(t)V_o \quad \text{(C.161)}$$

$$\frac{dV_o}{V_o} = -A(t)dt \quad \text{(C.162)}$$

For V_0≠0, I have:

$$\log(c_1 y) = -\int A(t)dt \quad \text{(C.163)}$$

$$c_1 y = e^{-\int A(t)dt} \quad \text{(C.164)}$$

For c1=1/c, I have:

$$y = ce^{-\int A(t)dt} \quad \text{(C.167)}$$

Omogeneous equation associated:

$$\frac{dV_o}{dt} + \left(\frac{4KRV_{OVQ}+1}{CR}\right)V_o(t) = 0 \quad \text{(C.168)}$$

The term A(t) in this case, is:

$$A(t) = \left(\frac{4KRV_{OVQ}+1}{CR}\right) \quad \text{(C.169)}$$

So a solution of the homogeneous associated can be written as:

$$y = ce^{-\int\left(\frac{4KRV_{OVQ}+1}{CR}\right)dt} \quad \text{(C.170)}$$

assuming the term A(t) independent of time, I can write:

$$y = ce^{-\left(\frac{4KRV_{OVQ}+1}{CR}\right)\cdot t} \quad \text{(C.171)}$$

C.6.4 Integral calculations

$$\int \frac{dx}{e^x-1} = \int \left(-1+\frac{e^x}{e^x-1}\right)dx = -x+\ln(e^x-1)$$

$$\int \frac{dx}{ae^{bx}-1} = \int \left(-1+\frac{1}{b}\frac{abe^{bx}}{ae^{bx}-1}\right)dx = -x+\frac{1}{b}\ln\left(ae^{bx}-1\right)$$

$$\int \left(\frac{1}{ae^{bx}-1}\right)^2 dx = \int \left(\frac{1+a^2e^{2bx}-2ae^{bx}-a^2e^{2bx}+2ae^{bx}}{(ae^{bx}-1)^2}\right)dx =$$

$$=\int \left(1-\frac{ae^{bx}}{ae^{bx}-1}+\frac{ae^{bx}}{(ae^{bx}-1)^2}\right)dx =$$

$$= x-\frac{1}{b}\ln\left(ae^{bx}-1\right)-\frac{1}{b}\frac{1}{ae^{bx}-1}$$

$$\int \left(a+\frac{b}{ce^{dx}-1}\right)^2 dx = \int [\,a^2+\frac{2ab}{ce^{dx}-1}+\left(\frac{b}{ce^{dx}-1}\right)^2 dx =$$

$$a^2x+2ab\left[-x+\frac{1}{d}\ln\left(ce^{dx}-1\right)\right]+b^2\left[x-\frac{1}{d}\ln\left(ce^{dx}-1\right)-\frac{1}{d}\frac{1}{(ce^{dx}-1)}\right] =$$

$$= (a-b)^2x+\frac{b}{d}(2a-b)\ln\left(ce^{dx}-1\right)-\frac{b^2}{d}\frac{1}{ce^{dx}-1}$$

$$\int e^{-\rho x}dx = -\frac{1}{\rho}e^{-\rho x}$$

$$\int (a+ce^{-gx})^2dx = \int (a^2+2ace^{-gx}+c^2e^{-2gx})dx = a^2x-\frac{2ac}{g}e^{-gx}-\frac{c^2}{2g}e^{-2gx}$$

$$V^* = \overline{V_o}-\frac{\delta}{\delta c_1 e^{t/\tau_{NL}}-1}$$

$$e^{t/\tau_{NL}} = \frac{1}{\delta c_1}\Sigma$$

$$\Sigma = \frac{\delta}{\overline{V_o}-V^*}+1$$

$$\overline{V_o} = (\alpha-\sqrt{\alpha^2-1})\Psi$$

$$\delta = 2\sqrt{\alpha^2-1}\Psi$$

$$V^* = \Psi-2V_{ov}$$

$$\Sigma = 1+\frac{2\sqrt{\alpha^2-1}}{\alpha-\sqrt{\alpha^2-1}-1+2V_{ov}/\Psi} = \frac{(\alpha-1)+2(V_{ov}/\Psi)+\sqrt{\alpha^2-1}}{(\alpha-1)+2(V_{ov}/\Psi)-\sqrt{\alpha^2-1}}$$

$$\delta c_1 = 1+\frac{\delta}{\overline{V_o}-V_o(0)} = 1+\frac{2\sqrt{\alpha^2-1}}{\alpha-\sqrt{\alpha^2-1}-(V_o(0)/\Psi)} = \frac{\alpha-V_o(0)/\Psi+\sqrt{\alpha^2-1}}{\alpha-V_o(0)/\Psi-\sqrt{\alpha^2-1}}$$

$$\frac{\Sigma}{\delta c_1} = \frac{(\alpha-1)+2V_{ov}/\Psi+\sqrt{\alpha^2-1}}{(\alpha-1)+2V_{ov}/\Psi-\sqrt{\alpha^2-1}}\frac{\alpha-V_o(0)/\Psi-\sqrt{\alpha^2-1}}{\alpha-V_o(0)/\Psi+\sqrt{\alpha^2-1}}$$

$$h = \sqrt{\alpha^2-1}$$

$$\Sigma = \frac{a+h}{a-h}$$

$$\delta c_1 = \frac{b+h}{b-h}$$

$$\frac{\Sigma}{\delta c_1} = \frac{a+h}{a-h}\frac{b-h}{b+h} = \frac{(ab-h^2)+h(b-a)}{(ab-h^2)-h(b-a)} = \frac{m+hn}{m-hn}$$

$$m = ab-h^2 = \left[(\alpha-1)+2\frac{V_{ov}}{\Psi}\right]\left(\alpha-\frac{V_o(0)}{\Psi}\right)-(\alpha^2-1) =$$

$$= (1-\alpha)\left(1+\frac{V_o(0)}{\Psi}\right)+2\frac{V_{ov}}{\Psi}\left(\alpha-\frac{V_o(0)}{\Psi}\right) =$$

$$\frac{1}{\Psi^2} = \left[2V_{ov}\alpha\Psi-2V_{ov}V_o(0)-\frac{1}{2KR}\left(\Psi+V_o(0)\right)\right] =$$

$$= \frac{A_v\alpha\Psi-A_vV_o(0)-\Psi-V_o(0)}{2KR\Psi^2} =$$

$$= \frac{\theta}{\Psi}\left[A_v\left(\alpha\Psi-\frac{A_v}{1+A_v}V_1\right)-\left(\Psi+\frac{A_v}{1+A_v}V_1\right)\right] =$$

$$= \frac{\theta}{\Psi(1+A_v)}\{A_v[\alpha\Psi(1+A_v)-A_v-1]-[\Psi(1+A_v)+A_vV_1]\}$$

$$n = \alpha-\frac{V_o(0)}{\Psi}-(\alpha-1)-2\frac{V_{ov}}{\Psi} = 1-\frac{V_o(0)+2V_{ov}}{\Psi} =$$

$= 1 - \frac{A_{vF}V_1+2V_{ov}}{V_2+V_{ov}} = \frac{1}{\Psi}\left(\frac{V_1}{1+A_v} + \Delta V - V_{ov}\right) =$

$= \frac{1}{\Psi(1+A_v)}[V_1 + (1+A_v)(\Delta V - V_{ov})]$

$\theta = \frac{1}{2KR\Psi}$

$\theta A_v = \frac{2V_{ov}}{\Psi} = 2\eta$

$m \pm hn = \frac{1}{\Psi(1+A_v)}\{2\eta[\alpha\Psi(1+A_v) - A_vV_1] - \frac{2V_{ov}}{A_v}(1+A_v) - 2\eta V_1 \pm$

$\pm\sqrt{\alpha^2-1}[V_1 + (1+A_v)(\Delta V - V_{ov})]\} =$

$= \frac{1}{\Psi(1+A_v)}\{2(1+A_v)[V_{ov}\left(\alpha - \frac{1}{A_v}\right) - \eta V_1] \pm$

$\pm\sqrt{\alpha^2-1}[V_1 + (1+A_v)(\Delta V - V_{ov})]\} =$

$= \frac{1}{\Psi}\{2\left[V_{ov}\left(1 - \frac{1}{A_v}(1-2\eta) - \eta V_1\right] \pm \sqrt{\alpha^2-1}\left(\frac{V_1}{(1+A_v)} + \Delta V - V_{ov}\right)\right\}$

C.6.5 Matlab code to estimate settling time and energy

```
%I have been selected Kota1 and VthO1
%Data taken from file "fitting.mat"
load fitting.mat
Kx=Kota1;
Vgs=0.5498;
Vovx=Vgs-VthO1;
Vdd=2.5;
Ib0=5.4e-6;
CL=1e-12;
% Input step
V1=-0.2;
V2=0.2;
% Settling precision
eps=0.001;
% Model parametres
R0=1e6;
Ncm=1;
mm=1;
alpha=1;
K=Kx*mm;
Vov=alpha*Vovx;
R=R0/Ncm/mm/alpha;
Ib=Ib0*alpha*alpha;
% Circuit coefficients for power
if V1<V2
   h1=1+Ncm;
   h2=1;
else
   h1=1;
   h2=1+Ncm;
end
I0=2*Ib+Vdd/R;
% Small signal
Gm=4*K*Vov*Ncm;
Av=Gm*R;
Avdb=20*log10(Av);
GBW=Gm/CL/2/pi;
% Preliminary calculations
Avf=Av/(Av+1);
Vlim=Vov-(1-Avf)*V1;
V0=Avf*V1;
psi=Vov+V2;
% Not linear settling
if V2-V1<Vlim
   T1=0;
   Vx=V0;
   J1=0;
else
   aa=1+1/(2*K*R*psi);
```

```
    hh=sqrt(aa*aa-1);
    gg=aa-hh;
    VL=gg*psi;
    dd=2*hh*psi;
    Vx=V2-Vov;
    TNL=CL/K/dd;
    c1=1/dd+1/(VL-V0);
    SS=dd/(VL-Vx)+1;
    pp=dd*c1;
    T1=TNL*log(SS/pp)
    ex=exp(T1/TNL);
    cj1=dd*dd*TNL;
    cj2=dd*TNL*(2*(1-gg)*psi-dd);
    J1=cj1/(1-pp*ex)+(((1-gg)*psi-dd)^2)*T1+cj1/(pp-1)-cj2*log(pp-1)+cj2*log(pp*ex-1);
end
% Linear settling
    Vfin=Avf*V2;
    Vin=Avf*V1;
    Q=Vfin-Vx;
    tau=CL/(Gm+1/R);
    T2=tau*log(Q/eps/(Vfin-Vin))
    aj=psi-Vfin;
    cj=Vfin-Vx;
    dj=Vfin-V2*Vov;
    ej1=exp(-T2/tau);
    ej2=exp(-2*T2/tau);
    J2=cj*cj*(1-ej2)+4*aj*cj*(1-ej1)+2*aj*aj*T2/tau;
    J2=J2*tau/2;
    J3=cj*cj*(1-ej2)-4*dj*cj*(1-ej1)+2*dj*dj*T2/tau;
    J3=J3*tau/2;

% Final accounts
Tsettl=T1+T2
Qalim=K*(h1*J1+h1*J2+h2*J3)+I0*Tsettl
Ealim=Vdd*Qalim
Econd=CL*Avf*Avf*(V2^2-V1^2)/2
Ediss=Ealim-Econd
Pavg=Ediss/Tsettl
```

C.6.6 Matlab code to plot settling time and energy as function of K and Vov

```
%Kota1 and Vtho1
load fitting.mat
%Kx=Kota1;
Vgs=0.5498;
%Vovx=Vgs-VthO1;
Vdd=2.5;
Ib0=5.4e-6;
CL=1e-12;
 % Input step
V1=-0.2;
V2=0.2;
 % Settling precision
eps=0.001;
%Cycle for
KK=linspace(1e-04,5e-04,100);
VV=linspace(0.1,0.5,500);
 for i=1:length(KK);
    for j=1:length(VV);
Kx=KK(i);
Vovx=Vgs-(Vgs-VV(j));
% Model parameters
R0=1e6;
Ncm=1;
mm=1;
alpha=1;
K=Kx*mm;
Vov=alpha*Vovx;
R=R0/Ncm/mm/alpha;
Ib=Ib0*alpha*alpha;
 % Circuit coefficients for power
if V1<V2
    h1=1+Ncm;
    h2=1;
else
    h1=1;
    h2=1+Ncm;
end
I0=2*Ib+Vdd/R;
 % Small signal
Gm=4*K*Vov*Ncm;
Av=Gm*R;
Avdb=20*log10(Av);
GBW=Gm/CL/2/pi;
 % Preliminary calculations
Avf=Av/(Av+1);
Vlim=Vov-(1-Avf)*V1;
V0=Avf*V1;
psi=Vov+V2;
```

```
% Not linear settling
if V2-V1<Vlim
   T1(i,j)=0;
E1(i,j)=0;
   Vx=V0;
   J1(i,j)=0;
else
   aa=1+1/(2*K*R*psi);
   hh=sqrt(aa*aa-1);
   gg=aa-hh;
   VL=gg*psi;
   dd=2*hh*psi;
   Vx=V2-Vov;
   TNL=CL/K/dd;
   c1=1/dd+1/(VL-V0);
   SS=dd/(VL-Vx)+1;
   pp=dd*c1;
   T1(i,j)=TNL*log(SS/pp);
   ex=exp(T1(i,j)/TNL);
   cj1=dd*dd*TNL;
   cj2=dd*TNL*(2*(1-gg)*psi-dd);
J1(i,j)=cj1/(1-pp*ex)+((1-gg)*psi-dd)^2*T1(i,j)+cj1/(pp-1)-cj2*log(pp-1)+cj2*log(pp*ex-1);
end
 % Linear settling
   Vfin=Avf*V2;
   Q=Vfin-Vx;
   Vin=Avf*V1;
   tau=CL/(Gm+1/R);
   T2(i,j)=tau*log(Q/eps/(Vfin-Vin));
  aj=psi-Vfin;
  cj=Vfin-Vx;
  dj=Vfin-V2*Vov;
  ej1=exp(-T2(i,j)/tau);
  ej2=exp(-2*T2(i,j)/tau);
  J2(i,j)=cj*cj*(1-ej2)+4*aj*cj*(1-ej1)+2*aj*aj*T2(i,j)/tau;
  J2(i,j)=J2(i,j)*tau/2;
  J3(i,j)=cj*cj*(1-ej2)-4*dj*cj*(1-ej1)+2*dj*dj*T2(i,j)/tau;
  J3(i,j)=J3(i,j)*tau/2;
   % Final calculations
Tsettl(i,j)=T1(i,j)+T2(i,j);
Qalim(i,j)=K*(h1*J1(i,j)+h1*J2(i,j)+h2*J3(i,j))+I0*Tsettl(i,j);
Ealim(i,j)=Vdd*Qalim(i,j);
Econd=CL*Avf*Avf*(V2^2-V1^2)/2;
Ediss(i,j)=Ealim(i,j)-Econd;
Pavg(i,j)=Ediss(i,j)/Tsettl(i,j);
end
end
figure, mesh(VV,KK,Tsettl), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'),
title('Tsett 3D')
```

```
figure, surf(VV,KK,Tsettl), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett 3D')
figure, contour3(VV,KK,Tsettl), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett 3D')
figure, contour(VV,KK,Tsettl), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett')

figure, contour(VV,KK,Ediss), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis')
figure, mesh(VV,KK,Ediss), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis 3D')
figure, surf(VV,KK,Ediss), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis 3D')
figure, contour3(VV,KK,Ediss), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis')
figure(9)
hold on, contour(VV,KK,Tsettl), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett & Edis')
hold on, contour(VV,KK,Ediss), grid on, xlabel('Vov [V]'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Tsett & Edis')
```

C.6.7 Matlab code to plot settling time and energy as function of K and Ncm

```
load fitting.mat
%Kx=Kota1;
Vgs=0.5498;
Vovx=Vgs-VthO1;
Vdd=2.5;
Ib0=5.4e-6;
CL=1e-12;
 % Input step
V1=-0.2;
V2=0.2;
 % Settling precision
eps=0.001;
% Cycle for
KK=linspace(1e-04,5e-04,100);
VV=linspace(1,4,30);
 for i=1:length(KK);
    for j=1:length(VV);
Kx=KK(i);
          %Vovx=Vgs-(Vgs-VV(j));
% Model parameters
R0=1e6;
Ncm=VV(j);
mm=1;
alpha=1;
K=Kx*mm;
Vov=alpha*Vovx;
R=R0/Ncm/mm/alpha;
Ib=Ib0*alpha*alpha;
 % Circuit coefficients for power
if V1<V2
    h1=1+Ncm;
    h2=1;
else
    h1=1;
    h2=1+Ncm;
end
I0=2*Ib+Vdd/R;
 % Small signal
Gm=4*K*Vov*Ncm;
Av=Gm*R;
Avdb=20*log10(Av);
GBW=Gm/CL/2/pi;
 % Preliminary calculations
Avf=Av/(Av+1);
Vlim=Vov-(1-Avf)*V1;
V0=Avf*V1;
psi=Vov+V2;

% Non-linear settling
```

```
if V2-V1<Vlim
   T1(i,j)=0;
E1(i,j)=0;
   Vx=V0;
   J1(i,j)=0;
else
   aa=1+1/(2*K*R*psi);
   hh=sqrt(aa*aa-1);
   gg=aa-hh;
   VL=gg*psi;
   dd=2*hh*psi;
   Vx=V2-Vov;
   TNL=CL/K/dd;
   c1=1/dd+1/(VL-V0);
   SS=dd/(VL-Vx)+1;
   pp=dd*c1;
   T1(i,j)=TNL*log(SS/pp);
   ex=exp(T1(i,j)/TNL);
   cj1=dd*dd*TNL;
   cj2=dd*TNL*(2*(1-gg)*psi-dd);
J1(i,j)=cj1/(1-pp*ex)+((1-gg)*psi-dd)^2*T1(i,j)+cj1/(pp-1)-cj2*log(pp-1)+cj2*log(pp*ex-1);
end
 % Linear settling
   Vfin=Avf*V2;
   Q=Vfin-Vx;
   Vin=Avf*V1;
   tau=CL/(Gm+1/R);
   T2(i,j)=tau*log(Q/eps/(Vfin-Vin));
  aj=psi-Vfin;
  cj=Vfin-Vx;
  dj=Vfin-V2*Vov;
  ej1=exp(-T2(i,j)/tau);
  ej2=exp(-2*T2(i,j)/tau);
  J2(i,j)=cj*cj*(1-ej2)+4*aj*cj*(1-ej1)+2*aj*aj*T2(i,j)/tau;
  J2(i,j)=J2(i,j)*tau/2;
  J3(i,j)=cj*cj*(1-ej2)-4*dj*cj*(1-ej1)+2*dj*dj*T2(i,j)/tau;
  J3(i,j)=J3(i,j)*tau/2;
   % Final calculations
Tsettl(i,j)=T1(i,j)+T2(i,j);
Qalim(i,j)=K*(h1*J1(i,j)+h1*J2(i,j)+h2*J3(i,j))+I0*Tsettl(i,j);
Ealim(i,j)=Vdd*Qalim(i,j);
Econd=CL*Avf*Avf*(V2^2-V1^2)/2;
Ediss(i,j)=Ealim(i,j)-Econd;
Pavg(i,j)=Ediss(i,j)/Tsettl(i,j);
end
end
figure, mesh(VV,KK,Tsettl), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'),
title('Tsett 3D')
figure, surf(VV,KK,Tsettl), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett
3D')
```

```
figure, contour3(VV,KK,Tsettl), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett 3D')
figure, contour(VV,KK,Tsettl), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett')

figure, contour(VV,KK,Ediss), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis')
figure, mesh(VV,KK,Ediss), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis 3D')
figure, surf(VV,KK,Ediss), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis 3D')
figure, contour3(VV,KK,Ediss), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Edis')
figure(9)
hold on, contour(VV,KK,Tsettl), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Tsett [s]'), title('Tsett & Edis')
hold on, contour(VV,KK,Ediss), grid on, xlabel('Ncm'), ylabel('K [A/V^2]'), zlabel('Edis [J]'), title('Tsett & Edis')
```

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