RESEARCH ARTICLE

Rail to Rail ICMR and High Performance ULV Standard-Cell-Based Comparator for Biomedical and IoT Applications

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ABSTRACT In this paper a novel ultra-low voltage (ULV) standard-cell-based comparator which provides rail-to-rail input common-mode range (ICMR) is presented. The topology, unlike the others in the literature, uses only 2-inputs NAND gates and is able to operate with supply voltages as low as 0.15V. A detailed theoretical analysis based on transistor level modeling is provided to explain the operating principle and highlight the performance advantages of the proposed comparator. The circuit has been tested through several simulations, including corner analysis and Monte Carlo runs, by using three different technologies: 180 nm, 130 nm and 28 nm for both a supply voltage of 0.3 V and 0.15 V. The results found not only confirm the robustness of the proposed comparator, but also demonstrate very advantageous performances. Indeed, for the same technology node it exhibits the highest speed and the lowest EDP (about ten times lower than the one of the others standard-cell-based comparators in the literature). It exhibits also the lowest power consumption and silicon area.

I. INTRODUCTION

In the modern era, the Internet of Things (IoT) has become pervasive, simplifying our daily lives through the use of smart devices. These devices enable us to effortlessly perform routine tasks such as banking, booking, traveling, and more. Additionally, the field of biomedical devices [1] has experienced significant advancements with the emergence of nano-technology, particularly in the treatment of nervous system disorders [2], [3], [4], [5].

One of the most effective yet intricate techniques utilized for the treatment of neural system disorders is Deep Brain Stimulation (DBS) [6], [7]. DBS systems are employed in the management of various neural disorders, including but not limited to Parkinson's disease, essential tremors, and dystonia [8]. The DBS system is based on an acquisition chain consisting of multiple components operating within

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a complex architecture tailored to control and stimulate specific brain areas, depending on the neural disorder under treatment. The conventional acquisition chain encompasses electrodes, a signal conditioning chain, an analog-to-digital converter (ADC) followed by digital processing units, data transmission components, and in certain cases, a stimulation generator to implement a closed-loop system, all powered by a battery. An example of such a system's architecture is depicted in Figure 1. The primary purpose of the surgically implanted electrodes, located beneath the scalp, is to capture and detect electrical signals within the brain region associated with the neural disorder. These electrical signals, once captured, undergo amplification by a front-end amplifier that filters and enhances specific frequencies. Subsequently, the amplified signal is converted into a digital format through an ADC and further processed via a digital signal processing block (DSP). The processed data may then be transmitted, either through wired or wireless communication, to an external control unit (CU), which establishes communication
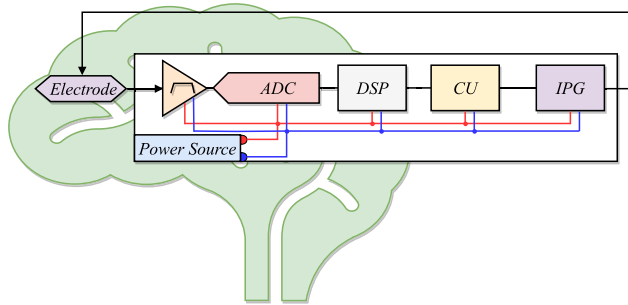
FIGURE 1. Closed loop scheme of the deep brain stimulation system.

with the implanted pulse generator (IPG). The IPG is responsible for stimulating the electrodes within the brain region linked to the neural disorder, with the objective of mitigating or suppressing the symptoms, particularly in the case of Parkinson's disease.

Given the intricate nature of these systems, there exist several blocks that can be optimized to enhance the efficiency of the implant. A critical concern in this context is power consumption. As the system relies on battery power [9], the efficiency of the acquisition chain significantly influences the device's autonomy and the lifespan of the battery [10]. When the battery reaches its end of life, it necessitates a surgical procedure to replace it, which poses challenges given the implant's location beneath the patient's scalp. In addition, recent studies have demonstrated that biomedical devices can be powered through energy harvesting systems, thus increasing the need for very low power consumption building blocks [11], [12], [13].

This challenge has spurred researchers to aggressively reduce the supply voltage and current consumption of conventional building blocks in these devices. This trend has paved the way for a new field of application that emphasizes ultra-low voltage (ULV) and ultra-low power (ULP) devices [14], [15], [16], [17]. ULV and ULP building blocks are favored in contemporary applications because they extend device autonomy, reduce heat generation, and facilitate energy-harvesting systems.

A fundamental building block employed in biomedical systems is the latched comparator, which plays a pivotal role in analog-to-digital converters (ADCs) [18], [19] and Low Dropout Regulators (LDOs) [20], [21], [22], [23], [24], [25]. Typically, this comparator consists of an input preamplifier followed by a latch, and it can be configured in various topologies such as StrongARM, double-tail, or Current-Mode Logic (CML) [26]. However, the design of such analog components, including schematic and layout, is traditionally a manual process involving iterative adjustments to meet specifications while ensuring robustness under process, supply voltage, temperature (PVT), and mismatch variations. This analog design process is notably more time-consuming than the semi-automatic digital design process, despite analog blocks constituting a relatively small part of the overall system. Therefore, alongside the motivation to reduce supply

voltage and power consumption, there is a strong impetus to modernize the analog design process, making it compatible with automatic place-and-route CAD tools and potentially enabling automatic device sizing.

In light of this context, current research trends are leaning toward designing analog blocks using digital standard cells [27]. This approach can either emulate the behavior of analog building blocks or implement analog functions within the digital domain [28]. The adoption of standard-cell-based analog functions enhances design portability across different technologies and allows for the reconfiguration of speed versus supply voltage [29], [30]. This standard-cell-based approach is particularly well-suited for ultra-low voltage (ULV) scenarios, where the stacking of multiple devices becomes challenging, thereby limiting the feasibility of traditional analog design techniques like cascoding.

Digital standard-cells have been explored as potential solutions to lower the minimum supply voltage into the deep sub-threshold range [31]. This approach reduces the human design effort required and ultimately lowers costs and time to market.

Several standard-cell-based circuits, such as Operational Transconductance Amplifiers (OTAs) [32], [33], [34], [35], [36], [37], [38], comparators [39], [40], [41], [42], [43], [44], [45], [46], [47], and filters [48], [49], have been proposed in the literature, demonstrating the effectiveness of the standard-cell approach in increasingly constrained analog and mixed signal integrated circuits operating in ULV conditions. Despite the ability of standard-cell-based topologies to operate at supply voltages as low as 0.15 V [36], [41], it is important to note that their performance is greatly affected by PVT variations. Consequently, they may be considered less robust when compared to analog counterparts, which, however, require increased design time and effort, and cannot achieve ULV operation using the conventional topologies and design approaches [36], [37].

Several standard-cell-based comparators have been recently proposed in the literature, demonstrating state-of-the-art performance in terms of power consumption and delay [39], [40], [41], [42], [43], [44], [50]. For example, in [39], a fully synthesizable comparator based on 3-inputs NAND gates (NAND-3) was proposed. The main limitation of this comparator is its non-rail-to-tail input common-mode range (ICMR), which, due to the usage of NAND-3 gates, is not able to operate for low input common-mode voltages, and starts to degrade its performances for input common-mode voltages lower than $V_{DD}/2$. To address this limitation, a comparator based on the same design, but with a symmetric part based on NOR-3 gates has been proposed in [44]. To optimize performance with respect to the input common-mode voltage, a MUX was added to select either the NAND-3 or NOR-3 path.

In an effort to achieve a rail-to-rail input common-mode range, a comparator utilizing both the NAND-3 and NOR-3 paths was presented in [40] and [41]. Finally, a standard-cell-based comparator that utilized And-Or-Invert (AOI) gates to
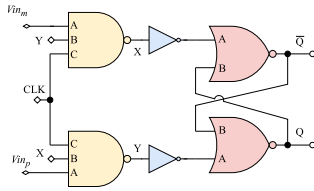
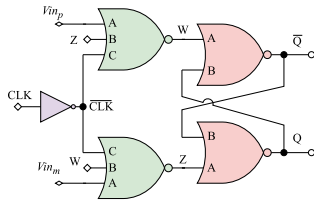**FIGURE 2.** *NAND₃* based comparator, proposed in [39].

FIGURE 3. *NOR₃* based comparator, proposed in [39].

improve upon the power consumption of [40] and [41] has been presented in [42].

In this paper we propose a novel ULV, rail-to-rail ICMR, fully synthesizable comparator topology, which avoids the usage of 3-inputs logic gates exploited in previous topologies and is made up of only 2-inputs NAND gates. The proposed topology aims at overcoming the limitations in terms of ICMR and propagation delay of previous fully synthesizable comparators. Since the proposed topology relies on 2-inputs standard cells, it exhibits an increased peak current in evaluation phase with respect to previous topologies, thus allowing a reduction of the propagation delay and an increment of the comparison speed. In addition, the adoption of 2-inputs gates, together with the proposed design strategy, result also in improved ICMR, reaching real rail-to-rail performance at supply voltages from 0.3 V down to 0.15 V.

A detailed theoretical analysis based on transistor-level modeling for different input common-mode voltages is provided to explain the operating principle and highlight the performance advantages of the proposed comparator. Extensive simulations in a commercial 180nm CMOS technology are presented to demonstrate state-of-the-art propagation delay and power-delay-product (PDP), with good overall performance. Additional simulations in 28nm and 130nm technologies are reported to confirm the portability of the proposed comparator topology across different technology nodes.

In the following, a review of previous standard-cell-based comparators is reported in Section II, the proposed topology and its detailed theoretical analysis are reported in Sections III and IV. The detailed analysis of the comparator behavior for different input common-mode voltages and its design strategy are described in Section V, simulation results are presented in Section VI, a comparison against the state of the art of ULV comparators is discussed in Section VII, and finally, some conclusions are drawn in Section VIII.
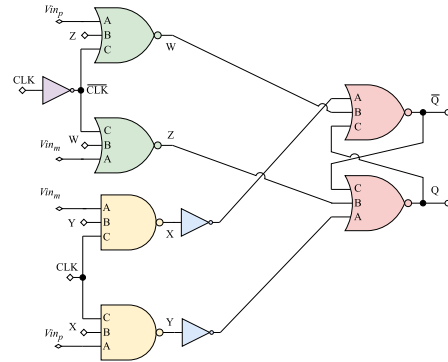

FIGURE 4. *NAND₃ + NOR₃* based comparator, proposed in [41].

II. PREVIOUS WORKS

The first standard-cell-based comparator has been introduced in [39] and is depicted in Figure 2 (referred to as the "*NAND₃* based comparator"). This design consists of a primary stage comprising two *NAND₃* cells, followed by a second stage that employs a *NOR* latch to sample and retain the output from the first stage. Both input terminals of the comparator are linked to the *A* input of the two *NAND₃* gates. Consequently, the differential input signal is amplified by the *NAND₃* gates and the subsequent *NOT* gates. The "*NOR₃* based comparator," an alternative version of the standard-cell-based comparator as proposed in [39], is displayed in Figure 3. In this configuration, the two input terminals of the comparator are connected to the *A* input of the two *NOR₃* gates. Here, the differential input signal is solely amplified by the *NOR₃* gates, resulting in lower gain compared to the *NAND₃* based comparator. While these comparators exhibit satisfactory performance under certain input voltage conditions, they exhibit shortcomings under specific stimulus scenarios in ULV conditions. In the case of the *NAND₃* based comparator, during the reset phase, its internal nodes are set to V_{DD}. Consequently, when an input signal with a common voltage below $V_{DD}/2$ is considered, the current path towards ground of the *NAND₃* architecture is interrupted. As a result, the input stage of the amplifier experiences significantly reduced or even absent gain, rendering the comparator unbalanced for certain input differential voltage levels. This issue becomes particularly critical when the input common-mode voltage falls below $V_{DD}/2$, and the input differential signal is small.

Conversely, the *NOR₃* based comparator depicted in Figure 3 faces a dual limitation, as its ICMR is constrained to voltages lower than $V_{DD}/2$".

To circumvent these ICMR limitations observed in the comparators of Figure 2 and Figure 3, a solution is presented in [40] and [41], illustrated in Figure 4 (referred to as the "rail-to-rail comparator" hereafter). This comparator combines the digital outputs of the *NAND₃* and *NOR₃* based comparators in a complementary manner, similar to rail-to-rail analog operational amplifiers.
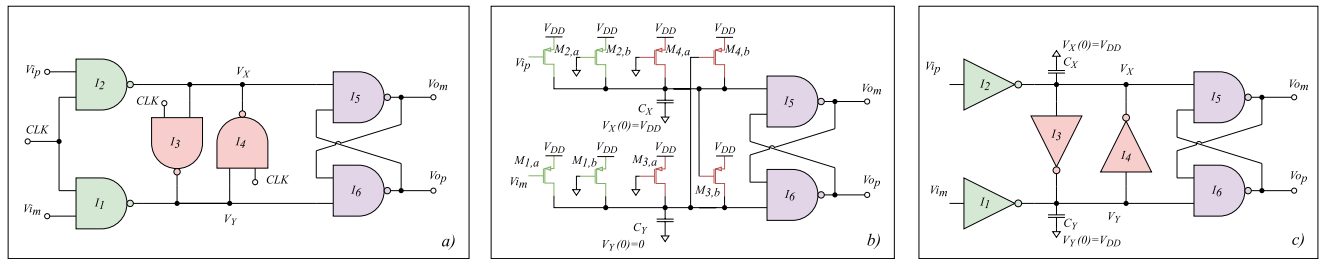
FIGURE 5. Proposed rail-to-rail comparator circuit a), equivalent circuit during the reset phase (CLK=0) b) and equivalent circuit during the evaluation phase (CLK=V_{DD}) c).

Another approach to achieve rail to rail ICMR is exploited in the comparator proposed in [42], which, however, relies on the specific schematic-level implementation of *AOI* and *OAI* gates, which may differ across standard-cell libraries. Since this paper primarily focuses on comparators which can be implemented using all digital standard-cell libraries and that do not rely on specific gates with varying schematic-level implementations, we will not include the comparator in [42] in the comparisons.

III. PROPOSED TOPOLOGY OF RAIL-TO-RAIL ICMR STANDARD-CELL-BASED COMPARATOR

Unlike the previous topologies [39], [40], [41], the input stage of the proposed comparator avoids 3-input gates, and it is split into two parts using only 2-inputs gates. In particular, according to the topology depicted in Fig. 5a), the first two NAND gates, namely I_1 and I_2, have the purpose to pre-amplify the input signal when the clock is high. On the other hand, when the clock is low this couple of NAND gates makes the structure opaque to the input signal and also cut-off the current path from V_{DD} to *GND*, thus avoiding static power consumption. The second NAND couple, I_3 and I_4 is in a positive feedback configuration, thus, when the clock is high, it is equivalent to the static storage element and works like the sense amplifier typically used in DRAMs, whereas, when the clock is low, it works like the previous couple. Finally, the last couple, composed by gates I_5 and I_6, is a NAND-based SR sequential circuit which has been exploited as final output stage to retain the result of the comparison.

A. OPERATING PRINCIPLES

To better explain and analyze the behavior of the proposed ULV dynamic comparator, we can divide the analysis into the two phases: pre-charge and evaluation phases, as reported in Fig. 5b) and Fig. 5c), respectively.

The analysis of the two phases is as follows:

- pre-charge phase: during the pre-charge, when the clock is low (CLK ≡ *GND*), the two NAND couples, I_1-I_2 and I_3-I_4 set the voltages at inner nodes X and Y to the power supply. More specifically, at least one PMOS of the NAND of the two couples (i.e., at least two PMOS for each branch) pre-charge to V_{DD} the parasitic internal nodes of the comparator. Note that, since during the

previous comparison one of the two nodes X or Y was discharged to *GND*, the overall power consumption in this pre-charge phase is given by the charge required to pre-charge this node.

- evaluation phase: in the next evaluation phase, when the clock is high (CLK ≡ V_{DD}), all the four NAND-gates in the two couples, I_1-I_2 and I_3-I_4, behave like four inverters (see Fig. 5c). In particular, the equivalent inverters due to I_1 and I_2 pre-amplify the input, forcing the nodes X or Y to be charged or discharged depending on the sign of the input differential signal. These voltages at nodes X and Y are then re-generated thanks to the positive feedback provided by I_3 and I_4 until the two nodes reach *GND* and V_{DD}. To maintain the output voltage during the pre-charge phase and to speed up the evaluation process, the SR sequential circuit implemented by I_5-I_6 is added as last stage. It reads the voltage at nodes X and Y and gives the final output.

The ULV comparator topology regardless its sizing has a very large ICMR, but to guarantee a rail-to-rail ICMR a proper sizing strategy has to be implemented. In particular, the sizing of I_3 and I_4 with respect to I_1 and I_2 has to be accurately considered. At this purpose, referring to Fig. 5c, since I_1 and I_3 (I_2 and I_4) drive the same net, I_3-I_4 have to be sized with an adequate strenght with respect to I_1-I_2, to guarantee the full charge (discharge) of nodes X and Y, even when the input common-mode voltage approaches V_{DD} or *GND*, as will be better shown in the next sections.

It has to be pointed out that, with respect to the topology in [40] and [41], the comparator proposed in this work exploits a different approach to reach the rail-to-rail ICMR. Indeed, the topology in [40] and [41] exploits two complementary subsections (one PMOS and one NMOS) inspired to the comparator of [39], whose digital outputs are combined similarly to rail-to-rail analog operational amplifiers. Thus, on the upper half of the ICMR only the NMOS part of the comparator is active, whereas for the lower half only the PMOS counterpart is active. Another important aspect is that, being the feedback of [39], [40] and [41] applied to one of the inputs of the $NAND_3$ or NOR_3 of the input gates, the whole circuit or part of it is not active on one half of the ICMR. The comparator here proposed exploits a current-mode driving of the positive feedback at
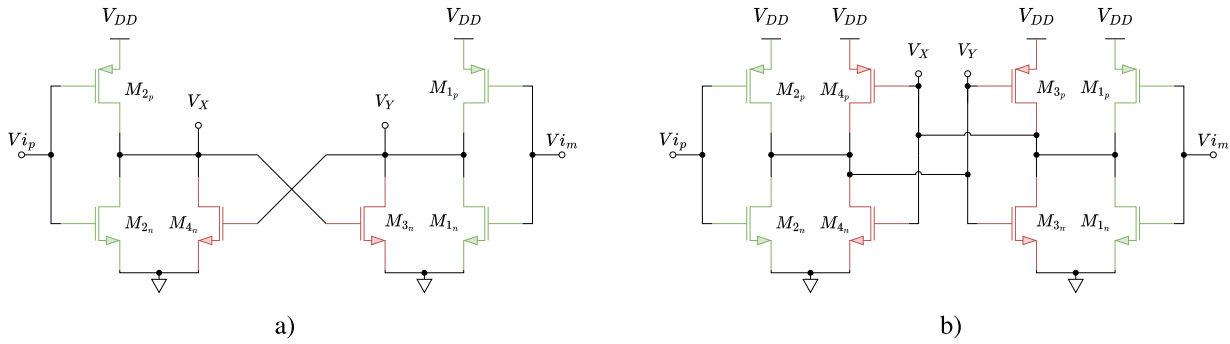
FIGURE 6. Comparator in the preamplification phase a), comparator in the regeneration phase b).

the output nodes of $I_{1,2}$, which allows to regenerate the differential signal with an extra degree of freedom. Indeed, the introduction of a current-mode positive feedback results in the possibility to optimize the driving strength of $I_{1,2}$ with respect to $I_{3,4}$ to achieve rail-to-rail ICMR.

It has also to be remarked that, even if the comparator presented in the conference paper [47] is standard-cell-based and exploits 2-inputs NAND gates, it exhibits substantial differences in both topology and operational principles with respect to the comparators presented in this paper. More specifically, reference [47] presents a fast comparator utilizing only NAND$_2$ gates from the standard-cell library, and the main claim is in highly optimized area consumption, at the expense of the input common-mode range (ICMR), which is very limited compared to the rail-to-rail ICMR of the comparator proposed in this paper.

IV. DETAILED ANALYSIS OF THE PROPOSED COMPARATOR IN THE EVALUATION PHASE

In order to provide an in depth analysis of the proposed comparator, its behavior during the evaluation phase has to be studied by focusing on two further sub-phases of the evaluation phase: preamplification and regeneration, as detailed in the following.

- Preamplification: in this phase, as the clock signal goes high after the precharge phase, the two nodes V_X and V_Y are at V_{DD}. Referring to schematic in Fig. 5c), it can be inferred that, at the beginning of the evaluation phase, the two *PMOS* transistors, M_{p3} and M_{p4} of the equivalent inverters I_3 and I_4, are in cut-off, because their gate voltage is approximately equal to V_{DD}, resulting in the equivalent circuit shown in Fig. 6a). Denoting with V_{XY_c} and V_{XY_d}, the common-mode and differential-mode components of the voltages V_X and V_Y, it can be observed that V_{XY_c} starts to decrease in the preamplification phase, due to the current drawn from M_{n3} and M_{n4} whose gate voltage is approximately equal to V_{DD}. The effect of M_{n1}, M_{p1}, M_{n2}, and M_{p2} on the variation of V_{XY_c} depends on the input common-mode voltage Vi_c of the comparator, which determines the
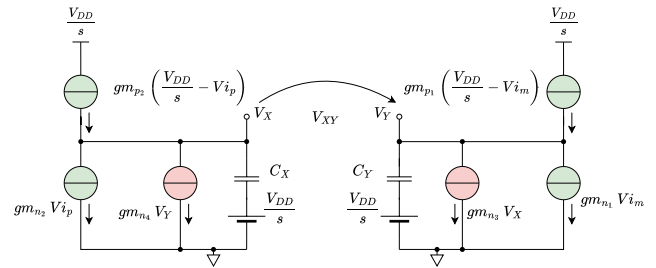

FIGURE 7. Simplified model of the proposed comparator in the preamplification sub-phase of the evaluation phase.

current sourced by M_{p1} (M_{p2}) and the current sinked by M_{n1} (M_{n2}). Assuming that transistors are sized so that the current drawn from M_{n3} and M_{n1} (M_{n4} and M_{n2}) is greater than the current sourced by M_{p1} (M_{p2}) for all the considered input common-mode voltages, the internal nodes V_X and V_Y discharge until V_{XY_c} reaches $V_{XY_{cLIM}}$, which is here defined as the value of common-mode voltage V_{XY_c} required to turn on the two PMOS transistors M_{p3} and M_{p4} in the positive feedback loop formed by the two NAND cells, I_3 and I_4. Focusing on the differential-mode voltage, it can be observed that V_{XY_d} results from the inverting amplification of the differential input voltage Vi_d. In this phase, the positive feedback provided by I_3 and I_4 accelerates the evaluation of the differential signal, helping the comparator to generate an initial difference in the internal node voltages at the end of the preamplification phase defined as $V_{XY_{dpre}}$.

- Regeneration: this phase starts when V_{XY_c} is equal to $V_{XYc_{LIM}}$ and can be analyzed referring to the equivalent circuit in Fig. 6b). During this phase, both the NMOS and PMOS of the NAND cells either source or sink current depending on the sign of the input signal. Consequently, the internal nodes V_X and V_Y are charged or discharged until $|V_{XY_d}| = |V_{DD}|$ based on the input differential voltage polarity. The positive feedback provided by $I_{3,4}$ accelerates the evaluation of the differential signal until nodes V_X and V_Y are completely charged to V_{DD} or discharged to *GND*.

In the following, the behavior of the comparator is analyzed in the Laplace domain using a linearized circuit, and the primary equations for assessing the performance of the comparator during the preamplification and regeneration phases are derived. For the following analysis the output resistances of MOS devices are neglected, whereas the initial conditions on the parasitic capacitances C_X and C_Y are taken into account. Furthermore, the transconductance of I_1 is assumed equal to that of I_2, and the transconductance of I_3 is assumed equal to that of I_4.

A. ANALYSIS OF THE BEHAVIOR OF THE COMPARATOR DURING THE PREAMPLIFICATION PHASE

Starting from the schematic in Fig. 6a), the equivalent circuit for the preamplification phase can be described by the model in the Laplace domain reported in Fig. 7, where MOS transistors are represented by voltage-controlled current sources, and usual notation for MOS transcondactances is used.

Referring to the model in Fig. 7, the node equations during the preamplification phase can be written as:

$$\begin{cases} gm_{p2}(V_{DD}/s - Vi_p) = gm_{n2}Vi_p + \\ \qquad\qquad + gm_{n4}V_Y + (V_X - V_{DD}/s)sC_X \\ gm_{p1}(V_{DD}/s - Vi_m) = gm_{n1}Vi_m + \\ \qquad\qquad + gm_{n3}V_Y + (V_Y - V_{DD}/s)sC_Y \end{cases} \quad (1)$$

Now, considering that:

$$\begin{cases} Vi_p = Vi_d/2 + Vi_c & Vi_m = -Vi_d/2 + Vi_c \\ V_X = V_{XY_d}/2 + V_{XY_c} & V_Y = -V_{XY_d}/2 + V_{XY_c} \end{cases} \quad (2)$$

it can be derived that:

$$\begin{cases} V_{XY_c}(s) = V_{DD}\dfrac{gm_{p2}}{gm_{n4}}\dfrac{1 + sC_X/gm_{p2}}{s(1 + sC_X/gm_{n4})} \\ \quad - \dfrac{gm_{p2} + gm_{n2}}{gm_{n4}}\dfrac{Vi_c}{1 + sC_X/gm_{n4}} \\ V_{XY_d}(s) = \dfrac{gm_{p2} + gm_{n2}}{gm_{n4}}\dfrac{1}{s(1 - sC_X/gm_{n4})} \end{cases} \quad (3)$$

from which, by antitrasforming, the common-mode voltage $V_{XY_c}(t)$ can be expressed as:

$$V_{XY_c}(t)$$
$$= V_{DD}\frac{gm_{p2}}{gm_{n4}}\left[1 + \frac{C_X}{gm_{p2}}\left(1 - \frac{gm_{p2}}{gm_{n4}}\right)e^{-t\,gm_{n4}/C_X}\right]$$
$$- Vi_c\frac{gm_{p1} + gm_{n1}}{gm_{n3}}e^{-t\,gm_{n4}/C_X} \quad (4)$$

and the differential-mode voltage $V_{XY_d}(t)$ as:

$$= Vi_d\frac{gm_{p2} + gm_{n2}}{gm_{n4}}\left(1 + \frac{C_X}{gm_{n4}}e^{gm_{n4}/C_X\,t}\right) \quad (5)$$

The time duration t_{pre} of the preamplification phase is set by the time needed by the common-mode voltage V_{XY_c} to reach
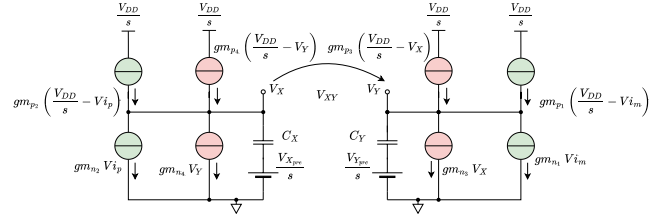

FIGURE 8. Simplified model of the proposed comparator in the regeneration phase of the evaluation.

the value $V_{XY_{cLIM}}$ and can be derived from Eq. 4 as follows:

$$t_{pre} = \frac{C_X}{gm_{n4}}\,ln\left(\frac{V_{DD}\frac{C_X}{gm_{n4}}\left(1 - \frac{gm_{p2}}{gm_{n4}}\right) - Vi_c\frac{gm_{p1} + gm_{n1}}{gm_{3n}}}{V_{XY_{cLIM}} - V_{DD}\,gm_{p2}/gm_{n4}}\right)$$
$$(6)$$

The differential voltage V_{XY_d} at time t_{pre} can then be expressed as:

$$V_{XY_{dpre}} = Vi_d\frac{gm_{p2} + gm_{n2}}{gm_{n4}}\left(1 + \frac{C_X}{gm_{n4}}e^{t_{pre}\frac{gm_{n4}}{C_X}}\right) \quad (7)$$

From Equation 6, it is evident that as Vi_c increases, the preamplification duration also increases. The first term in the numerator, "$V_{DD}\frac{C_X}{gm_{n4}}(1 - \frac{gm_{p2}}{gm_{n4}})$," is associated with the sizing of $I_{1,2}$ and $I_{3,4}$, and it becomes smaller as the size of $I_{3,4}$ increases. Additionally, the ratio of $I_{1,2}$ to $I_{3,4}$ impacts the Vi_c term in the numerator, causing it to decrease with larger $I_{3,4}$. Regarding the denominator, it depends again on the $I_{1,2}$ to $I_{3,4}$ ratio. It is worth noting that the denominator's value in the logarithmic argument is technology-dependent because $V_{XY_{cLIM}}$ is influenced by the threshold voltage (V_{th_p}) of the technology. Clearly, the time constant that multiplies the logarithmic equation is determined by the parasitic capacitance at node X and the two NMOS transistors in $I_{3,4}$, which discharge the X and Y nodes until $V_{XY_{cLIM}}$ is reached.

From Equation 7, we can see that the initial gain of the differential voltage at the X and Y nodes is influenced by the ratio of $I_{1,2}$ and $I_{3,4}$. Conversely, due to the positive feedback from $I_{3,4}$, there is an observable exponential growth in the differential output voltage at t=0. This growth would be even faster with an increase in the size of $I_{3,4}$, which raises gm_{n4}. However, it's important to note that C_X is also related to the size of I_4, and therefore, the time constant of the positive feedback for the differential signal increases during the preamplification phase in proportion to $1/L_{M_{n3,4}}^2$ since $gm_{n4} \propto W_{M_{n3,4}}/L_{M_{n3,4}}$ and $C_X \propto W_{M_{n3,4}} \cdot L_{M_{n3,4}}$. This implies that a minimum-size $I_{3,4}$ corresponds to a higher differential gain in the preamplification phase.

B. ANALYSIS OF THE BEHAVIOR OF THE COMPARATOR DURING THE REGENERATION PHASE

Starting from the schematic in Fig. 6b), the equivalent circuit for the regeneration phase can be described by the model in the Laplace domain reported in Fig. 8, where MOS transisors are represented by voltage-controlled current sources, usual
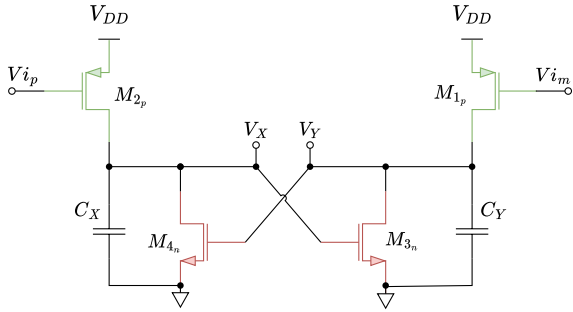
FIGURE 9. Equivalent circuit of the proposed comparator during the preamplification phase when the input common-mode voltage is equal to *GND*.

notation is used for MOS transcondactances, and the initial voltage at the two nodes V_X and V_Y is equal to $V_{XY_{cLIM}} \pm V_{XY_{dpre}}/2$.

Referring to the model in Fig. 8, the differential voltage V_{XY_d} can be expressed as:

$$V_{XY_d}(s) = \frac{1}{gm_{n_4} + gm_{p_4}} \frac{V_{XY_{dpre}} C_X + Vi_d(gm_{p_2} + gm_{n_2})}{1 - s\,C_X/(gm_{n_4} + gm_{p_4})} \tag{8}$$

which antitransformed results in:

$$V_{XY_d}(t) = \frac{V_{XY_{dpre}} C_X + Vi_d(gm_{p_2} + gm_{n_2})}{gm_{n_4} + gm_{p_4}} e^{t\,\frac{gm_{n_4} + gm_{p_4}}{C_X}} \tag{9}$$

From the above equation, assuming $\frac{V_{DD}}{2}$ as logic threshold, the regeneration time can be expressed as:

$$t_{reg} = \frac{C_X}{gm_{n_4} + gm_{p_4}} \ln\left(\frac{V_{DD}/2(gm_{n_4} + gm_{p_4})}{V_{XY_{dpre}} C_X + Vi_d(gm_{p_2} + gm_{n_2})}\right) \tag{10}$$

The delay of the proposed comparator can be therefore expressed as:

$$Delay = t_{pre} + t_{reg} \tag{11}$$

and considering that the duration of the reset phase is always lower than the duration of the evaluation (preamplification and regeneration) phase, the maximum clock frequency of the proposed comparator can be approximated as:

$$f_{max} = \frac{1}{2(t_{pre} + t_{reg})} \tag{12}$$

It is evident that increasing the size of $I_{3,4}$ can reduce the regeneration time, while increasing $I_{1,2}$ leads to a decrease in the argument of the logarithm, thus reducing the duration of the regeneration phases. This analysis allows us to determine the optimal design strategy for achieving specific performance goals in a given application.

V. ANALYSIS OF DIFFERENT INPUT COMMON-MODE VOLTAGES AND DESIGN STRATEGY

In this Section, our focus is on examining the behavior of the comparator under various input common-mode voltage conditions. Specifically, we investigate scenarios where the

input common-mode voltage is either *GND* or V_{DD}, as these represent the worst-case scenarios for achieving a rail-to-rail ICMR.

A. COMMON-MODE VOLTAGE = GND

1) PREAMPLIFICATION PHASE

Starting from the schematic in Fig. 6a), and considering an input common-mode voltage $Vi_c = GND$, the equivalent circuit for the preamplification phase can be redrawn as in Fig. 9. As it can be observed, in this condition both the NMOS transistors of $I_{1,2}$ are in cut-off. The equations which govern the behavior of this circuit in the preamplification phase are the following:

$$\begin{cases} \dfrac{kp_2(V_{DD} - Vi_p - |Vth_{p_2}|)^2}{C_X} - \dfrac{kn_4(V_Y - Vth_{n_4})^2}{C_X} = \dfrac{dV_X}{dt}; \\ \dfrac{kp_1(V_{DD} - Vi_m - |Vth_{p_1}|)^2}{C_Y} - \dfrac{kn_3(V_X - Vth_{n_3})^2}{C_Y} = \dfrac{dV_Y}{dt}; \end{cases} \tag{13}$$

with usual notation for MOS devices parameters.

For the common-mode voltage, the above equations result in a Riccati equation of the form $a - bx^2 = \frac{dx}{dt}$, whose solution is:

$$V_{XY_c}(t) = Vth_{n_4} + \sqrt{\frac{kp_2}{kn_4}}(V_{DD} - |Vth_{p_2}|) \\ \cdot \tanh\left\{\frac{\sqrt{kp_2 kn_4}(V_{DD} - |Vth_{p_2}|)}{C_X}(c_1 + t)\right\} \tag{14}$$

in which the constant term c_1 can be derived by considering the initial condition $V_{XY_c}(t)\Big|_{t=0} = V_{DD}$:

$$c_1 = \frac{C_X}{\sqrt{kn_4 kp_2}(V_{DD} - |Vth_{p_2}|)} \\ \cdot \operatorname{arctanh}\left\{\sqrt{\frac{kp_2}{kn_4}}\frac{V_{DD} - Vth_{n_4}}{V_{DD} - |Vth_{p_2}|}\right\} \tag{15}$$

The preamplification time can be thus written as:

$$t_{pre} = \frac{C_X}{\sqrt{kn_4 kp_2}(V_{DD} - |Vth_{p_2}|)} \\ \cdot \left[\operatorname{arctanh}\left\{\sqrt{\frac{kp_2}{kn_4}}\frac{V_{XY_{cLIM}} - Vth_{n_4}}{V_{DD} - |Vth_{p_2}|}\right\} \\ - \operatorname{arctanh}\left\{\sqrt{\frac{kp_2}{kn_4}}\frac{V_{DD} - Vth_{n_4}}{V_{DD} - |Vth_{p_2}|}\right\}\right] \tag{16}$$

Considering the preamplification time, also the preamplified differential voltage can be evaluated, starting by the node equation for the differential mode:

$$\frac{kp_2}{C_X}(V_{DD} - Vi_d - |Vth_{p_2}|)^2 - \frac{kn_4}{C_X}(V_{XY_d} - Vth_{n_4})^2 = \frac{dV_{XY_d}}{dt} \tag{17}$$
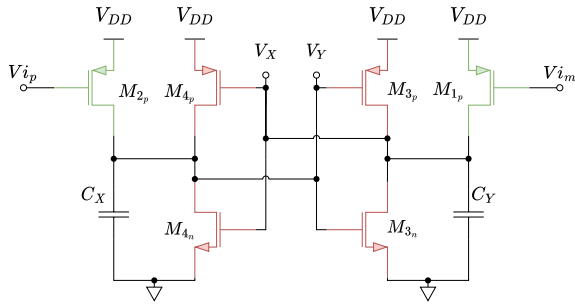
FIGURE 10. Equivalent circuit of the proposed comparator during the regeneration phase when the input common-mode voltage is equal to GND.
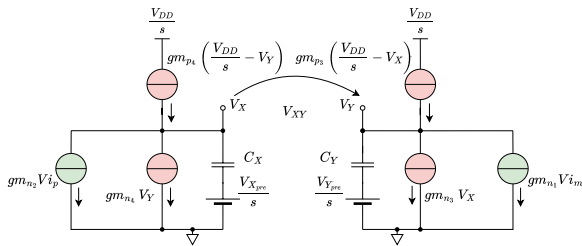

FIGURE 11. Simplified model of the proposed comparator during the regeneration phase when the input common-mode voltage is equal to GND.

which again can be reconduced to a Riccati equation, whose solution is here reported:

$$
V_{XY_d}(t) = Vth_{n_4} + \sqrt{\frac{kp_2}{kn_4}}(V_{DD} - Vi_d - |Vth_{p_2}|) \cdot
$$
$$
\cdot \tanh\left\{\frac{\sqrt{kp_2 kn_4}(V_{DD} - Vi_d - |Vth_{p_2}|)}{C_X}(c_1 + t)\right\} \quad (18)
$$

By imposing the initial condition: $V_{XY_d}(t)\Big|_{t=0} = 0$ the constant term c_2 can be derived:

$$
c_2 = \frac{C_X}{\sqrt{kn_4 kp_2}(V_{DD} - Vi_d - |Vth_{p_2}|)}
$$
$$
\cdot arctanh\left\{\sqrt{\frac{kn_4}{kp_2}}\frac{-Vth_{n_4}}{V_{DD} - Vi_d - |Vth_{p_2}|}\right\} \quad (19)
$$

and thus the preamplified differential voltage at nodes X, Y can be computed as:

$$
V_{XY_{dpre}} = Vth_{n_4} + \sqrt{\frac{kn_4}{kp_2}}(V_{DD} - Vi_d - |Vth_{p_2}|)
$$
$$
\cdot \tanh\left\{\frac{\sqrt{kp_2 kn_4}(V_{DD} - Vi_d - |Vth_{p_2}|)}{C_X}(c_2 + t_{pre})\right\} \quad (20)
$$

As can be seen from the above equations, when the input common-mode voltage is set to *GND*, the comparator continues to operate effectively without losing its capability to amplify the differential signal.
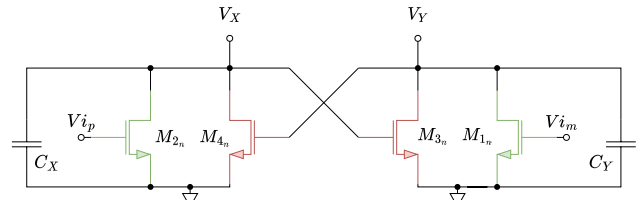
FIGURE 12. Equivalent circuit of the comparator during the preamplification phase when the input common-mode voltage is equal to V_{DD}.

2) REGENERATION PHASE

Starting from the schematic in Fig. 6b), and considering an input common-mode voltage $Vi_c = GND$, the equivalent circuit for the regeneration phase can be redrawn as in in Fig. 10, resulting in the linearized model depicted in Fig. 11.

Referring to the model in Fig. 11, the regeneration time can be evaluated by considering that the differential voltage at nodes X,Y can be written as:

$$
V_{XY_d}(t) = \frac{V_{XY_{dpre}} C_X + Vi_d gm_{p_2}}{gm_{n_4} + gm_{p_4}} e^{t\frac{gm_{n_4} + gm_{p_4}}{C_X}} \quad (21)
$$

Now, considering that the output is valid when $V_{XY_d} = V_{DD}/2$ (logic threshold equal to $V_{DD}/2$), the regeneration time can be evaluated as:

$$
t_{reg} = \frac{C_X}{gm_{n_4} + gm_{p_4}} ln\left(\frac{V_{DD}/2(gm_{n_4} + gm_{p_4})}{V_{XY_{dpre}} C_X + Vi_d gm_{p_2}}\right) \quad (22)
$$

Again, in this scenario as well, the reduction in regeneration time is optimized as the size of the NAND cells $I_{3,4}$ increases, resulting in an increase in gm_{n_4,p_4}. Additionally, it's important to note that the input common-mode voltage during this phase is not critical at all. The only difference, in fact, compared to the nominal case where $Vi_c = V_{DD}/2$, is the preamplified voltage at the X and Y nodes, along with the equivalent gm that amplifies Vi_d, which results reduced by a factor equal to gm_{n_2}.

B. COMMON-MODE VOLTAGE = VDD

Starting from the schematic in Fig. 6a), and considering an input common-mode voltage $Vi_c = V_{DD}$, the equivalent circuit for the preamplification phase can be redrawn as in Fig. 12. As it can be observed, in this condition both the PMOS transistors of $I_{1,2}$ are in cut-off. As a result, the nodes X and Y discharge through the NMOS transistors of cells $I_{1,2}$ and $I_{3,4}$ until the voltage $V_{X,Y}$ reaches the common-mode voltage $V_{XY_c} = V_{XY_{cLIM}}$. It's important to note that during this phase, depending on the polarity of the input differential voltage, the two nodes X and Y produce a differential voltage through the NMOS transistors of $I_{1,2}$ effectively amplifying the differential signal due to their operation in the saturation region.

1) PREAMPLIFICATION PHASE

In order to deeply understand the behavior of the circuit in this working condition, we can start from the equation at

nodes X, Y:

$$\begin{cases} \dfrac{kn_2(Vi_p - Vth_{n_2})^2}{C_X} + \dfrac{kn_4(V_Y - Vth_{n_4})^2}{C_X} + \dfrac{dV_X}{dt} = 0; \\ \dfrac{kn_1(Vi_m - Vth_{n_1})^2}{C_Y} + \dfrac{kn_3(V_X - Vth_{n_3})^2}{C_Y} + \dfrac{dV_Y}{dt} = 0; \end{cases}$$
(23)

and considering that in the common-mode equivalent circuit $Vi_p = Vi_m = V_{DD}$, the node equation can be written as:

$$\frac{kn_2(V_{DD} - Vth_{n_2})^2}{C_X} + \frac{kn_4(V_{XY_c} - Vth_{n_4})^2}{C_X} + \frac{dV_{XY_c}}{dt} = 0$$
(24)

which is a Riccati equation in the form $\frac{dx}{dt} = -bx^2 - a$ whose solution is:

$$V_{XY_c}(t) = Vth_{n_4} - \sqrt{\frac{kn_2}{kn_4}}(V_{DD} - Vth_{n_2})$$
$$\cdot tg\left\{ \frac{\sqrt{kn_2 kn_4}(V_{DD} - Vth_{n_2})}{C_X}(c_3 + t) \right\}$$
(25)

and the initial condition $V_{XY_c}(t)\big|_{t=0} = V_{DD}$, can be imposed to find c_3 as:

$$c_3 = \frac{C_X}{\sqrt{kn_2 kn_4}(V_{DD} - Vth_{n_2})}$$
$$\times \left\{ arctan\left(\sqrt{\frac{kn_4}{kn_2}} \frac{-V_{DD} + Vth_{n_4}}{V_{DD} - Vth_{n_2}} \right) \right\}$$
(26)

Finally the preamplification time can be derived as:

$$t_{pre} = \frac{C_X}{\sqrt{kn_2 kn_4}(V_{DD} - Vth_{n_2})}$$
$$\cdot \left\{ arctan\left(\sqrt{\frac{kn_4}{kn_2}} \frac{V_{XY_{cLIM}} - Vth_{n_4}}{V_{DD} - Vth_{n_2}} \right) \right.$$
$$\left. - arctan\left(\sqrt{\frac{kn_4}{kn_2}} \frac{Vth_{n_4} - V_{DD}}{V_{DD} - Vth_{n_2}} \right) \right\}$$
(27)

The differential voltage V_{XY_d} at X, Y nodes can then be computed by considering Eq. 23 resulting in:

$$\frac{kn_2}{C_X}\left(Vi_d - Vth_{n_2} \right)^2 + \frac{kn_4}{C_X}\left(V_{XY_d} - Vth_{n_4} \right)^2 + \frac{dV_{XY_d}}{dt} = 0$$
(28)

which is again a Riccati equation in the form $a + b\,x^2 + dx/dt = 0$ whose solution is:

$$V_{XY_d}(t) = -Vth_{n_4} - \sqrt{\frac{kn_2}{kn_4}}(V_{idc} - Vth_{n_2})$$
$$\cdot tan\left\{ \frac{\sqrt{kn_2 kn_4}(V_{id} - Vth_{n_2})}{C_X}(c_4 + t) \right\}$$
(29)
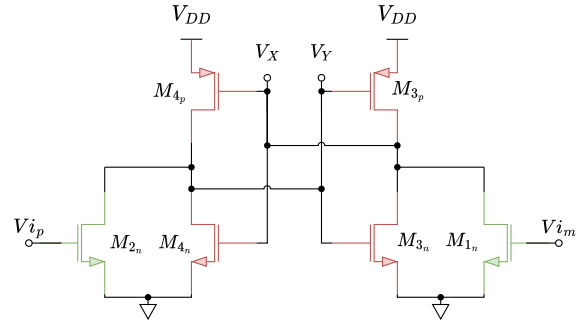
FIGURE 13. Equivalent circuit of the comparator during the regeneration phase when the input common-mode voltage is equal to V_{DD}.
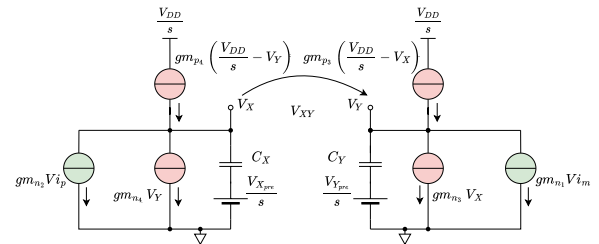
FIGURE 14. Simplified model of the comparator during the regeneration phase when the input common-mode voltage is equal to V_{DD}.
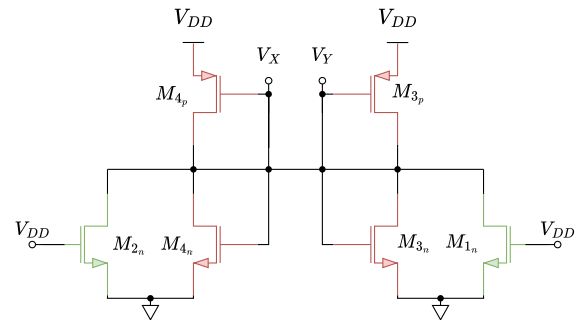
FIGURE 15. Equivalent transistor level circuit for the common-mode voltage of the comparator during the regeneration phase.

and by imposing the initial condition $V_{XY_d}(t)\big|_{t=0} = 0$, c_4 can be computed as:

$$c_4 = \frac{C_X}{\sqrt{kn_2 kn_4}(V_{id} - Vth_{n_2})}$$
$$\cdot arctan\left(-\sqrt{\frac{kn_4}{kn_2}} \frac{Vth_{n_4}}{V_{id} - Vth_{n_2}} \right)$$
(30)

and thus the differential voltage accumulated during the preamplification phase when the input common-mode voltage is equal to V_{DD} can be derived as:

$$V_{XY_{dpre}} = -Vth_{n_4} - \sqrt{\frac{kn_2}{kn_4}}(V_{id} - Vth_{n_2})$$
$$\cdot tg\left\{ \frac{\sqrt{kn_2 kn_4}(V_{id} - Vth_{n_2})}{C_X}(c_4 + t_{pre}) \right\}$$
(31)

2) REGENERATION PHASE

The transistor level circuit in the regeneration phase is depicted in Fig. 13. As it can be observed, both the PMOS of the logic gates $I_{3,4}$ are on. The linearized equivalent circuit of the comparator during the regeneration phase is depicted in Fig. 14. By considering the V_{XY_d}:

$$V_{XY_d}(t) = \frac{gm_{n_2}Vid - V_{XY_{dPRE}}C_X}{gm_{p_4} + gm_{n_4}} e^{t(gm_{p_4}+gm_{n_4})/C_X} \quad (32)$$

the regeneration time for the circuit in Fig. 14 can be evaluated as:

$$t_{reg} = \frac{C_X}{gm_{p_4} + gm_{n_4}} \ln\left(\frac{V_{DD}/2(gm_{p_4} + gm_{n_4})}{gm_{n_2}Vid - V_{XY_{dPRE}}C_X}\right) \quad (33)$$

It has to be noted that, during this phase, a potential issue may arise concerning the sizing of $I_{1,2}$ and $I_{3,4}$. More specifically, the common-mode voltage V_{XY_c} could decrease more rapidly than the time required to regenerate the differential signal. To better understand this point, the transistor-level equivalent circuit for the common-mode voltage during the regeneration phase reported in Fig. 15, can be analyzed. According to Fig. 15, in the regeneration phase the PMOS transistors M_{4_p} and M_{3_p} are on, and source a current which tends to charge the capacitances C_X and C_Y. In the same phase, the four NMOS devices M_{4_n}, M_{3_n}, M_{2_n} and M_{1_n}, which all exhibit an high value of the gate-source voltage, sink a current which is higher than the current sourced by M_{4_p} and M_{3_p}, and the common-mode voltage tends to decrease very quickly until the currents drawn by NMOS transistors in $I_{3,4}$ become negligible compared to those drawn by $I_{1,2}$. After this phase, the influence of M_{4_n} and M_{3_n} can be disregarded when compared to M_{2_n} and M_{1_n} which remain the dominant discharging devices. The time it takes to reach this condition is referred to as t^*. We can derive its value by considering the time to reach $V_{XY_c} = Vth_{n_{4,3}}$, which places the two NMOS transistors of $I_{3,4}$ in weak inversion. Subsequently, the dominant effects are governed by the NMOS transistors in $I_{1,2}$ and PMOS transistors M_{4_p} and M_{3_p}.

The equations for the common-mode voltage circuit in this phase are as follows:

$$\begin{cases} -\dfrac{(V_{DD} - Vth_{n_2})^2}{C_X}kn_2 + \\ -\dfrac{(V_{XY_c} - Vth_{n_4})^2}{C_X}kn_4 + \\ +\dfrac{(V_{DD} - V_{XY_c} - |Vth_{p_4}|)^2}{C_X}kp_4 = \dfrac{dV_{XY_c}}{dt} \\ \quad \text{if } t_{pre} < t < t^*; \\ \\ -\dfrac{(V_{DD} - Vth_{n_2})^2}{C_X}kn_2 + \\ +\dfrac{(V_{DD} - V_{XY_c} - |Vth_{p_4}|)^2}{C_X}kp_4 = \dfrac{dV_{XY_c}}{dt} \\ \quad \text{if } t > t^* \end{cases} \quad (34)$$

Both these equations can be re-conduced to a Riccati equation, the most interesting one is the one at $t > t^*$. If we

consider the solution for that Riccati equation, in the form of: $-a + bx^2 = \frac{dx}{dt}$ it can be derived that:

$$V_{DD} - V_{XY_c} - Vth_{p_4}$$
$$= \sqrt{\frac{kn_2}{kp_4}}(V_{DD} - Vth_{n_2})$$
$$\cdot \tanh\left\{\frac{\sqrt{kn_2 kp_4}(V_{DD} - Vth_{n_2})}{C_X}(c_5 + t)\right\} \quad (35)$$

where c_5 can be derived by imposing that $V_{XY_c}(t)\Big|_{t=t^*} = Vth_{n_4}$ as:

$$c_5 = \frac{C_X}{\sqrt{kn_2 kn_4}(V_{DD} - Vth_{n_2})}$$
$$\cdot \operatorname{arctanh}\left\{\sqrt{\frac{kp_4}{kn_2}} \cdot \frac{V_{DD} - Vth_{n_4} - |Vth_{p_4}|}{V_{DD} - Vth_{n_2}}\right\} - t^* \quad (36)$$

and by imposing the $V_{XY_c}(t_{cm_{GND}}) = 0$, the $t_{cm_{GND}}$ time can be derived as:

$$t_{cm_{GND}} = t^* + \frac{C_X}{\sqrt{kn_2 kn_4}(V_{DD} - Vth_{n_2})}$$
$$\cdot \left[\operatorname{arctanh}\left\{\sqrt{\frac{kp_4}{kn_2}} \cdot \frac{V_{DD} - |Vth_{p_4}|}{V_{DD} - Vth_{n_2}}\right\}\right.$$
$$\left. + -\cdot \operatorname{arctanh}\left\{\sqrt{\frac{kp_4}{kn_2}} \cdot \frac{V_{DD} - Vth_{n_4} - |Vth_{p_4}|}{V_{DD} - Vth_{n_2}}\right\}\right] \quad (37)$$

which depends on technology parameters (threshold voltages) and on the ratio $\frac{kp_4}{kn_2}$, which is present on both the *arctan* members.

To guarantee that the proposed comparator behaves correctly also for an input common-mode voltage equal to V_{DD} it is therefore very important to guarantee that the condition $t_{reg} < t_{cm_{GND}}$ is fulfilled also for an input common-mode voltage equal to V_{DD} which represents the worst case. At this purpose, the designer's only viable option, especially considering the restriction imposed by a standard-cell-based design approach, is to increase the multiplicity (i. e., the number of instances in parallel) of $I_{3,4}$, because this increases the current sourced by M_{4_p} and M_{3_p} with respect to the current sinked by M_{2_n} and M_{1_n}, thus slowing the decreasing of V_{XY_c} and increasing the value of $t_{cm_{GND}}$.

This relationship can be seen from Equation 33, where it is evident that increasing the size of $I_{3,4}$ will lead to a reduction in the regeneration time t_{reg}, and from Equation 37 which shows how increasing the size of $I_{3,4}$ will result in increased $t_{cm_{GND}}$. In the following, the design strategy will be clearly presented with considering three different CMOS technology nodes.

C. POWER CONSUMPTION AND ENERGY CONSUMPTION CONSIDERATIONS

In this Section we compute the energy consumption of the proposed comparator topology considering both the energy

needed for charging the parasitic capacitors at the internal nodes X and Y, and the energy dissipation due to short-circuit currents in the different phases of operation. For the following analysis we assume that the two parasitic capacitances at nodes X and Y are identical to each other: $C_X = C_Y$.

Since in the reset phase just one of the two output nodes is charged to V_{DD}, and no short-circuit current contributions are present, the dissipated energy in this phase is:

$$E_{res} = \frac{1}{2} C_X V_{DD}^2 \qquad (38)$$

During the preamplification phase the energy consumption is given by:

$$E_{pre} = \frac{1}{2} C_X \left[2V_{DD}^2 - (V_{XY_{c_{LIM}}} + V_{XY_{d_{PRE}}})^2 \right.$$
$$\left. - (V_{XY_{c_{LIM}}} - V_{XY_{d_{PRE}}})^2 \right]$$
$$+ V_{DD} \int_0^{t_{pre}} (I_{2_p} + I_{1_p}) dt \qquad (39)$$

where the last term represents the contribution due to the short-circuit current which flows from M_{2_p} and M_{1_p} to ground.

Finally, during the regeneration phase, in which one capacitor is discharged to ground and the other one is charged to V_{DD}, the energy consumption can be computed as:

$$E_{reg} = V_{DD} \int_0^{t_{reg}} (I_{2_{p(n)}} + I_{4_{p(n)}}) dt$$
$$+ V_{DD} \int_0^{t_{reg}} (I_{3_{n(p)}} + I_{1_{n(p)}}) dt$$
$$+ \frac{1}{2} C_X \left[V_{DD}^2 - (V_{XY_{c_{LIM}}} \right.$$
$$\left. + +V_{XY_{d_{PRE}}})^2 + (V_{XY_{c_{LIM}}} - V_{XY_{d_{PRE}}})^2 \right] \qquad (40)$$

where the first two terms are due to the short-circuit currents of the respective transistors. The overall energy dissipation is therefore given by:

$$E_{tot} = E_{res} + E_{pre} + E_{reg} \qquad (41)$$

and the power consumption for a given clock frequency f_{clk} can be written as:

$$P_{tot} = f_{clk} E_{tot} = f_{clk}[E_{res} + E_{pre} + E_{reg}] \qquad (42)$$

According to the above equations, both the energy dissipation and the power consumption depends on the input common-mode voltage and also on the input differential voltage. By looking at Eq. 39 and Eq. 40 the effect of the input differential voltage can be found in the term $V_{XY_{d_{PRE}}}$. Furthermore the dependence of the energy and power consumption is clearly related to the active transistor which play a role in the comparison phase. Indeed, for a very low or very high input common-mode voltage, some transistors are switched off and do not contribute to the overall energy consumption. For example, for input common-mode voltage
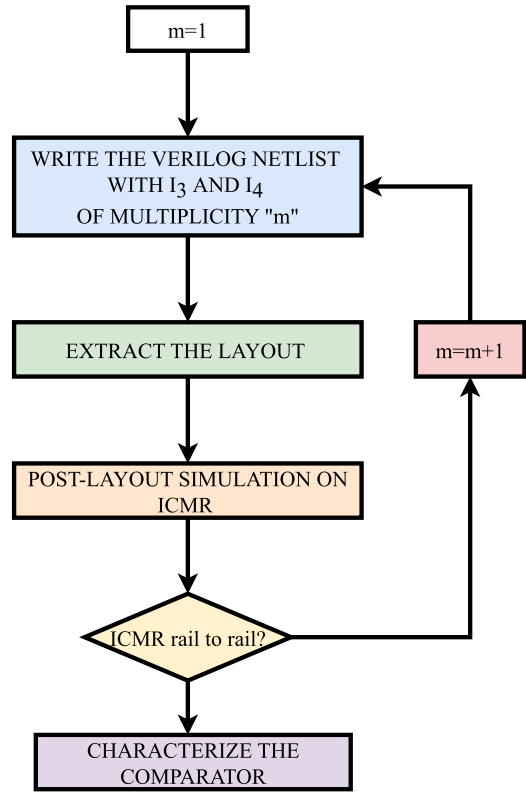

FIGURE 16. Design flow for the proposed comparator.

equal to V_{DD}, the terms I_{2_p} and I_{1_p} of Eq. 39 are equal to 0, and these two terms are not present also in Eq. 40. However, in the same case of input common-mode voltage equal to V_{DD}, the contributions of $I_{1,2_n}$ becomes dominant due to the high V_{gs_n}. Similar considerations can be done for very low input common-mode voltages.

The energy and power consumption are also related to the parasitic capacitance seen at nodes X and Y. These two parasitic capacitances increase with the increasing of the size of $I_{3,4}$, thus there is a trade-off between energy (power) consumption and input common-mode range.

D. DESIGN STRATEGY
Since we are proposing a standard-cell based, fully synthesizable comparator topology, the basic gate assumed for the design is the minimum-sized 2-inputs NAND gate, taken from the standard-cell library of the target technology (I_1-I_2 and I_5-I_6 are therefore implemented as a single instance of the minimum-sized 2-inputs NAND gate). Then, the effect of varying the multiplicity m (i. e., the number of instances in parallel) of I_3-I_4 on the ICMR of the comparator has been investigated according to design flow illustrated in Fig. 16. The goal of the proposed design strategy is to assure a rail-to-rail ICMR, and we consider as a first design point a multiplicity m for $I_{3,4}$ of 1. Starting from the verilog netlist of the comparator, an automatic layout flow within the Cadence Innovus tool is carried out, and post-layout simulations with the extracted netlist are performed. It has to be remarked

```
module SC_Rail_to_Rail ( CLK, Out1, Out2, Vinm, Vinp );

inout  CLK, Out1, Out2, Vinm, Vinp;

ND2D0BWP7T I1 ( .ZN(y), .A2(CLK), .A1(Vinm));
ND2D0BWP7T I2 ( .ZN(x), .A2(CLK), .A1(Vinp));
ND2D0BWP7T I3_0 ( .A1(CLK), .A2(y), .ZN(x));
ND2D0BWP7T I3_1 ( .A1(CLK), .A2(y), .ZN(x));
ND2D0BWP7T I3_2 ( .A1(CLK), .A2(y), .ZN(x));
ND2D0BWP7T I3_3 ( .A1(CLK), .A2(y), .ZN(x));
ND2D0BWP7T I4_0 ( .A1(CLK), .A2(x), .ZN(y));
ND2D0BWP7T I4_1 ( .A1(CLK), .A2(x), .ZN(y));
ND2D0BWP7T I4_2 ( .A1(CLK), .A2(x), .ZN(y));
ND2D0BWP7T I4_3 ( .A1(CLK), .A2(x), .ZN(y));
ND2D0BWP7T I5 ( .ZN(Out2), .A2(Out1), .A1(y));
ND2D0BWP7T I6 ( .ZN(Out1), .A2(Out2), .A1(x));

endmodule
```

FIGURE 17. Verilog netlist of the comparator referring to the 180 nm standard-cell library.

TABLE 1. Input common-mode range in percentage of V_{DD} when the multiplicity of I_3-I_4 is changed in different technologies.

		Technology		
		28 nm	130 nm	180 nm
Multiplicity	1	77.67	88.67	77.67
	2	88.67	100	88.67
	3	88.67	100	94.33
	4	100	100	100

that the automatic layout flow is allowed for the proposed comparator topology, due to the fact that only standard-cells taken from the digital library are used.

Simulations are then carried out in the Cadence Virtuoso environment using a testbench designed to allow the derivation of the ICMR when the multiplicity of I_3-I_4 is varied, and assuming a supply voltage V_{DD} of 300mV, an input differential amplitude of 10 mV and a 10 Hz clock frequency.

This study has been conducted on three different technology nodes (28nm, 130nm, and 180 nm), referring to the standard-cell library provided by the IC manufacturer, and results of this analysis are reported in Tab. 1, where the ICMR in percentage of the supply voltage is reported for different values of the multiplicity. As it can be observed, the 130nm technology requires a multiplicity of just 2 NAND gates, whereas both the 28nm and 180nm require a multiplicity of 4 to provide a fully rail-to-rail ICMR. According to these results, a multiplicity of 4 is enough to guarantee on all the tested nodes a rail-to-rail ICMR, and thus we assume 4 for our design.

The Verilog netlist of the proposed comparator topology using the standard-cell library of the 180nm CMOS process is reported in Fig. 17, confirming that the comparator discussed in this work can be coded in Verilog or VHDL language and can be therefore considered as a fully synthesizable circuit, whose layout can be automatically generated by an automatic place and route flow for digital circuits.

The layout of the proposed comparator implemented in the three technology nodes with $m = 4$ are reported in Fig. 18.

To gain a deeper understanding of the trade-offs that were considered, we here reported the transient response of the proposed comparator designed for the 180 nm technology. We conducted this analysis using the minimum-sized NAND

gates $I_{1,2,3,4}$. In Figure 19, we illustrate the two most challenging scenarios. We applied a 10 mV input differential voltage to evaluate the comparator's performance, with a reference clock frequency of 71.5 kHz, a supply voltage of 300 mV, and an input common-mode set to *GND* as shown in Figure 19(a), and $V_{DD} = 300\,mV$ as depicted in Figure 19(b).

In agreement with the theoretical study in Section VA, when the input common-mode voltage is set to *GND*, the comparator operates successfully, providing output imbalances based on the input differential voltage's sign even without increasing the multiplicity of $I_{3,4}$. When the input common-mode voltage is set to V_{DD}, it can be observed a very fast preamplification process, because both *NMOS* transistors in $I_{1,2}$ and $I_{3,4}$ are discharging nodes X and Y, according to Fig. 12. On the other hand, during the regeneration phase, it's notable the rapidity with which the common-mode voltage at nodes X and Y (V_{XY_c}) approaches *GND* compared to the time to regenerate the differential signal. As a consequence, the regeneration condition ($V_{XY_d} = V_{DD}/2$) is not achieved before the common-mode voltage at nodes X and Y reaches *GND*. Consequently, the correct operation of the comparator is not assured, and the output differential voltage is not regenerated since the condition $t_{cm_{GND}} > t_{reg}$ has not been respected as pointed out in in Section VB. In order to fulfill the condition $t_{cm_{GND}} > t_{reg}$, the multiplicity of $I_{3,4}$ has been increased at 4 according to Tab. 1. In Fig. 20 it has been depicted the transient behavior of the proposed comparator with $I_{3,4}$ of multiplicity 4 and $I_{1,2}$ of minimum size, considering an input differential voltage of 10 mV, a clock frequency of 71.5kHz, a supply voltage of 300mV and an input common-mode voltage of 0V (a) and 300mV (b). It can be observed that in both cases the comparator is able to properly regenerate the differential signal. As a consequence, it can be concluded that, the given sizing gives to the proposed comparator a reliable rail-to-rail ICMR behavior.

VI. SIMULATION RESULTS AND COMPARISONS

In order to provide a fair comparison between the proposed topology and previously reported ones, the standard-cell library of the TSMC 180nm process has been considered as the target library. In particular, the topology presented in [40] and [41], which is the only standard-cell-based comparator with a rail-to-rail ICMR reported in the technical literature, has been re-simulated on the 180nm CMOS process and compared with the proposed comparator referring to the same testbench.

A. POWER CONSUMPTION AND DELAY OF THE PROPOSED COMPARATOR

The power consumption P_D and the propagation delay (Delay) of the comparator have been tested in ULV conditions with considering two values of the supply voltage V_{DD} (0.15 V and 0.3 V), with an input differential voltage of 10 mV, an input common-mode voltage equal to $V_{DD}/2$ and an operating frequency of 10 Hz as done in [40] and [41]. In order to overcome the effects of the initial power
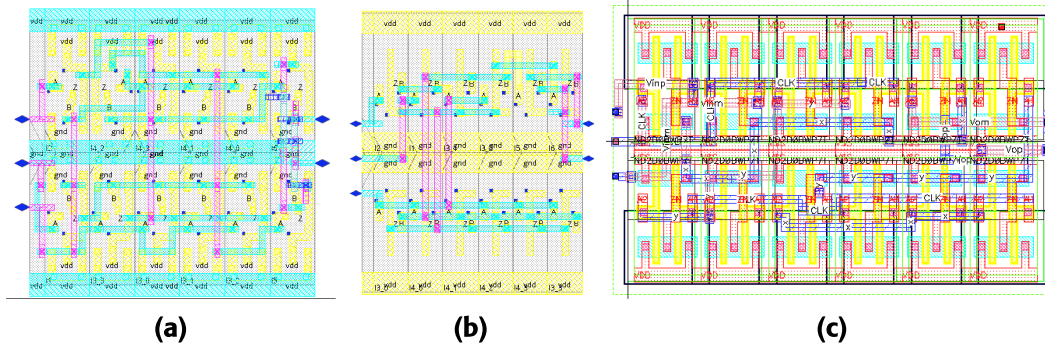
FIGURE 18. Automatically implemented layout of the proposed comparator in 28 nm with an area consumption of 6.6μm^2 a), 130 nm with an area consumption of 81.67μm^2 b) and 180 nm with an area consumption of 140.84μm^2 c).
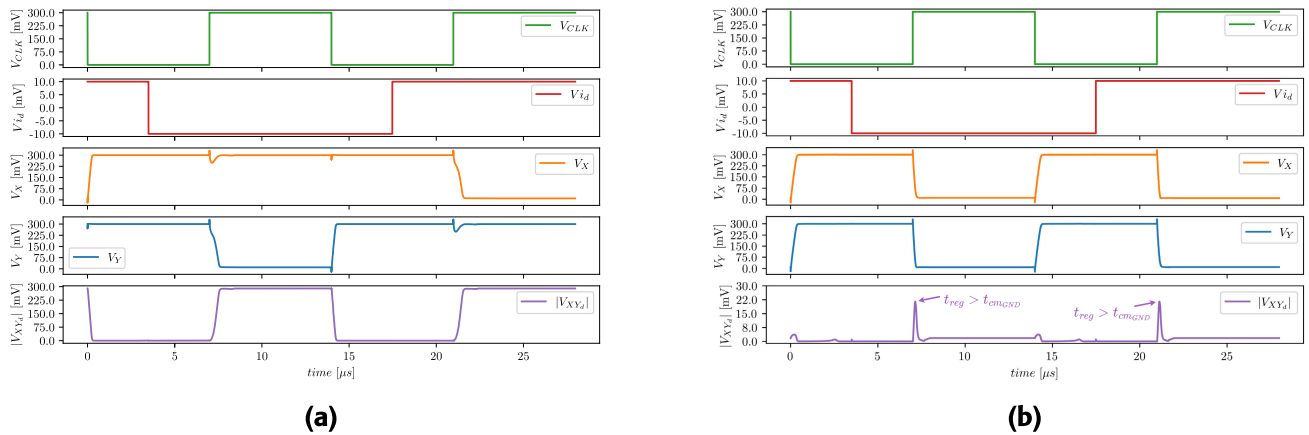
FIGURE 19. Transient behavior of the proposed comparator with $I_{1,2,3,4}$ of minimum size, considering an input differential voltage of 10 mV, a clock frequency of 71.5kHz, a supply voltage of 300mV and an input common-mode voltage of 0V (a) and 300mV (b).
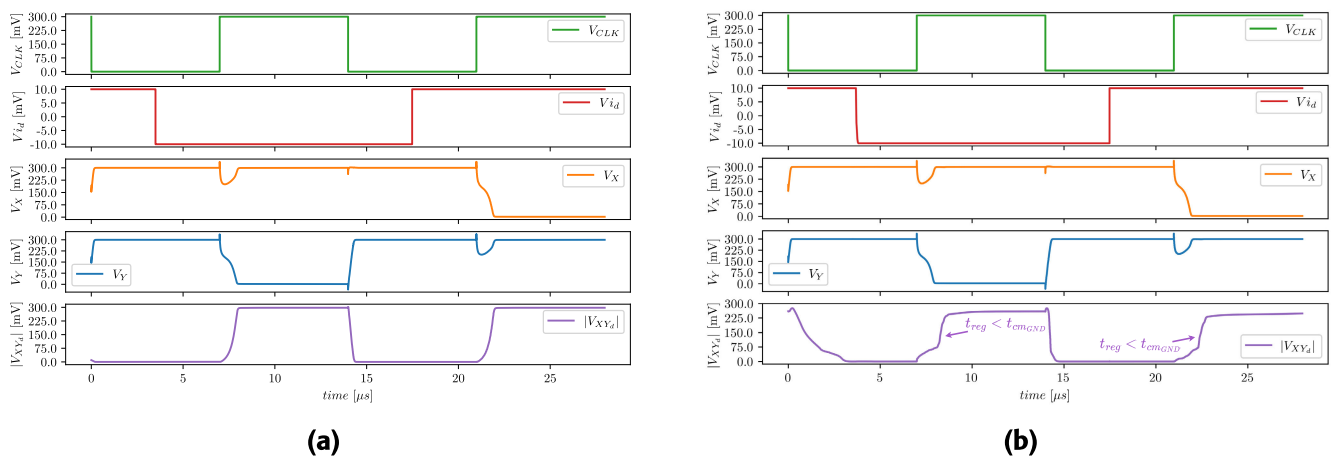
FIGURE 20. Transient behavior of the proposed comparator with $I_{3,4}$ of multiplicity 4 and $I_{1,2}$ of minimum size, considering an input differential voltage of 10 mV, a clock frequency of 71.5kHz, a supply voltage of 300mV and an input common-mode voltage of 0V (a) and 300mV (b).

consumption transitory, the values of power consumption and delay have been collected at the end of a long transient simulation involving 200 comparisons, and results of the analysis are reported in Tab. 2.

The propagation delay and the power consumption of the proposed comparator have been reported also as a function of the input common-mode voltage V_{icm} in Fig. 21. As it can be observed in Fig. 21, the proposed comparator is

FIGURE 21. Delay a) and power consumption b), of the proposed comparator for different input common-mode voltages Vi_{CM} for $V_{DD} = 0.15V$ (green trace) and $V_{DD} = 0.3V$ (red trace).

FIGURE 22. Power consumption and delay of other standard-cell based comparators taken from literature for different input common-mode voltages Vi_{CM} and for $V_{DD} = 0.3V$. The delay and the power consumption vs Vi_{cm} for the comparator in [40], [41] are depicted in purple, whereas the delay and the power consumption for the comparator in [39] are depicted in blue.

TABLE 2. Power consumption and Delay of the proposed comparator for two different values of the supply voltage.

	This Work		Previous works [40], [41]	
V_{DD} [V]	0.15	0.3	0.15	0.3
Delay [µs]	39.307	3.411	75.234	6.728
P_D [pW]	9.127	76.096	7.714	63.697
ICMR [% of V_{DD}]	100	100	90	92
PDP [a J]	358.755	259.563	580.355	428.553

TABLE 3. Performance of the proposed comparator at the maximum operating frequency.

V_{DD} [V]	0.15	0.3
f_{max} [kHz]	6.21	71.5
ICMR [% of V_{DD}]	100	100
Delay [µs]	39.29	3.39
P_D [pW]	17.23	409.83
PDP [a J]	676.967	1389.324
EDP [a J/ kHz]	109.012	19.431

TABLE 4. Offset of the comparators considering mismatch variations in the typical PVT corner.

		This work		[40], [41]	
	V_{DD} [V]	0.15	0.3	0.15	0.3
Typical	[mV]	-1.5	-1	-0.5	-1
Mismatch	μ [mV]	0.5	1.2	-0.57	-1.1
	σ [mV]	10.99	11.11	10.52	11.19

able to work over the whole input common-mode range considering both a 0.15 V and a 0.3 V supply voltage. Indeed

even with a 150 mV supply voltage, the proposed circuit is able to operate with an input common-mode voltage of 0 or V_{DD}. This remarkable result has been achieved thanks to the simplicity of the topology and to the adopted sizing strategy. For the sake of comparison, Fig. 22 reports the power consumption and the delay of other standard-cell based comparators taken from literatures [39], [40] and [41], for a supply voltage $V_{DD} = 0.3V$, and with considering an input differential voltage of 10mV, a clock frequency of 10 Hz and a variable input common-mode range. The delay and the power consumption vs $Vi_{cm}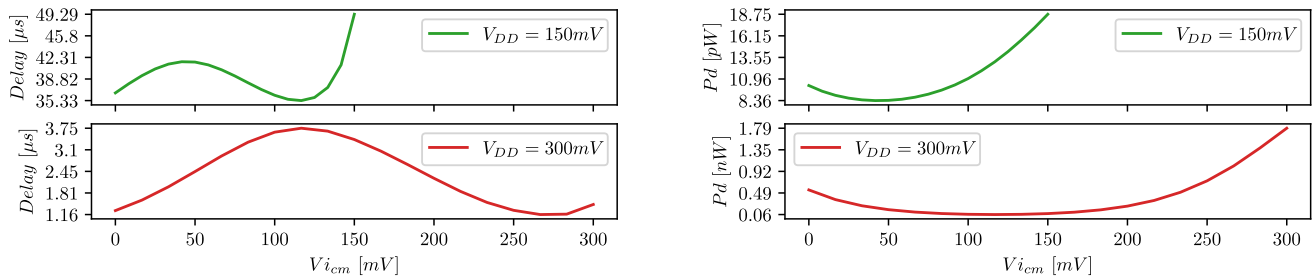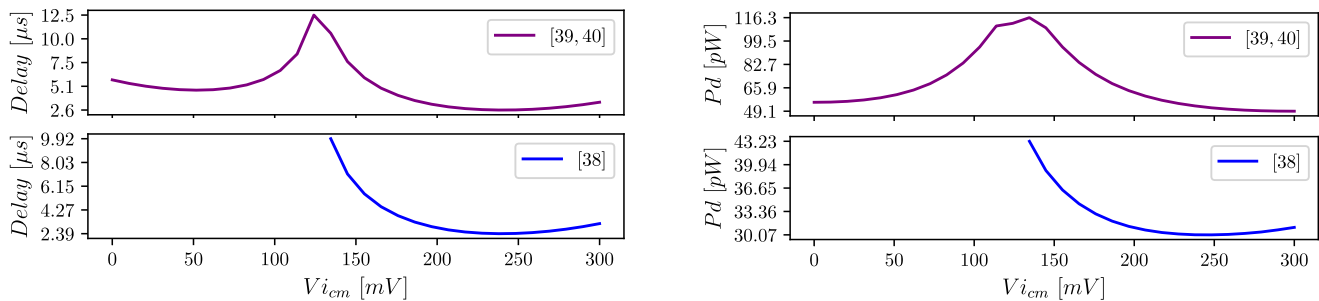$ of the comparator in [40] and [41] are depicted in purple, whereas the delay and the power consumption of the comparator in [39] are depicted in blue. As it can be observed, the comparator presented in [39] doesn't present a rail-to-rail behavior with respect to the input common-mode voltage. The comparator presented in [40] and [41] presents a rail-to-rail ICMR, however, its mode of operation drastically differs from the one of the comparator here proposed. Indeed, while the comparator in [40] and [41] is composed by two complementary parts which work one on the half upper input common-mode range and one on the half lower input common-mode range, the comparator here presented works in the whole input common-mode range without compromising the working condition of any cell instance. This results in a much lower variation of the delay vs Vi_c of the proposed comparator with respect to the comparators in [39], [40] and [41]. On the other hand, for what concerns the power consumption, while for low or

TABLE 5. Power consumption and Delay of the proposed comparator under temperature and supply voltage variations.

Alim,Temp [V,°C]	0.3,27	0.3,0.0	0.3,80.0	0.33,27	0.27,27.0
Delay [µs]	3.412	11.44	0.562	2.16	5.43
P_D [pW]	76.096	20.806	620.91	123.03	47.78
ICMR [mV]	300	300	300	300	300
PDP [a J]	259.64	238.021	348.951	265.745	259.445
f_{max} [kHz]	73.271	21.853	444.84	115.741	46.041
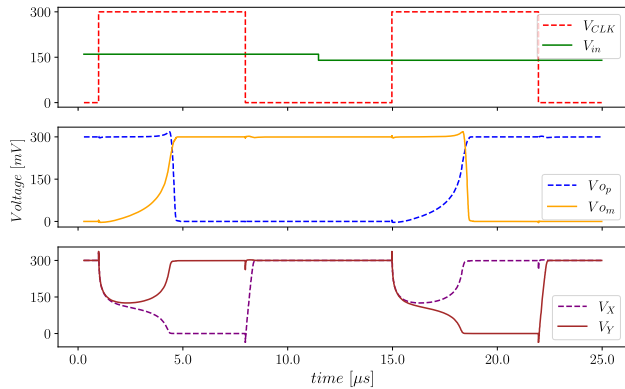
FIGURE 23. Transient waveforms of the proposed comparator at the maximum operating frequency.

TABLE 6. Power consumption and Delay of the proposed comparator in the different technology corners.

Corner	TYP	FF	SS	SF	FS
V_{DD} [V]	0.3	0.3	0.3	0.3	0.3
Delay [µs]	3.412	0.79	17.42	2.99	3.67
P_D [pW]	76.096	281.37	76.096	69.44	159.099
ICMR [mV]	300	300	300	300	300
PDP [a J]	259.64	222.282	1325.592	207.626	583.893
f_{max} [kHz]	73.271	316.456	14.351	83.612	68.12

high input common-mode voltage the power consumption of [40] and [41] decreases due to the fact that half circuit is not active, the proposed comparator exhibits an increased power consumption, due to the fact that transistors of $I_{1,2}$ are biased with an higher $|V_{gs}|$. As a further assessment of the proposed comparator we have characterized its performances when high clock frequencies are considered. More specifically, the maximum operating frequency f_{max} has been evaluated with considering the delay of the comparator extracted when stimulated with an input differential signal amplitude of 10mV, a common-mode input voltage of $V_{DD}/2$, a 90% of the power supply voltage and a temperature of 0°C. Obviously, for each one of the two considered supply voltages (i.e. 0.15 V and 0.3 V), a value of the maximum operating frequency has been computed. Results of the high frequency carachterization are reported in Tab. 3, where EDP denotes the energy-delay-product as usual.

The transient waveforms of the proposed comparator are reported in Fig. 23 for a supply voltage of 300mV, an input common-mode voltage set at $V_{DD}/2$, an input differential voltage amplitude of 10mV and a clock frequency of 71.5 kHz. As it can be observed, the voltages V_X and V_Y at

the two internal nodes X, Y and the output voltages V_{O_p} and V_{O_m} follow the trend described in Section III-A.

B. OFFSET OF THE PROPOSED COMPARATOR
This Section presents the characterization of the offset of standard-cell-based, rail-to-rail ICMR comparators considering mismatch variations in the typical PVT corner. Table 4 summarizes the results of 200 Monte Carlo simulations focused solely on mismatch. It has been reported the nominal value of the input-referred offset voltage as well as the mean value and standard deviation.

As it can be observed, both the topology proposed in this work and the one presented in [40] and [41] result in a similar offset behavior, with a mean value close to 0 mV and a standard deviation in the range of 10 mV. It has to be remarked that the standard deviation of the offset can be reduced in accordance to the Pelgrom law [51] by increasing the size of instances $I_{1,2,3,4}$, which mainly contribute to the offset voltage.

C. INPUT-REFERRED NOISE OF THE PROPOSED COMPARATOR
The noise analysis of the proposed comparator has been carried out according to [52]. In particular the comparator noise has been evaluated in the Cadence Virtuoso environment through a transient noise simulation. Simulation results have shown that, for a supply voltage of 300mV and a clock frequency of 71.5kHz the input-referred noise is about 120μV, whereas for a supply voltage of 150mV and a clock frequency of 6.21kHz it results about 240μV. These results show that noise of the comparator is much lower than its offset voltage.

D. PERFORMANCES UNDER PVT VARIATIONS
To quantify the robustness of the proposed comparator with respect to PVT variations, simulations in the same conditions adopted in Section VI-A and considering a ±10% variation of the supply voltage (around the nominal supply voltage of 0.3 V), and a temperature range from 0°C to 80°C have been carried out. Main performance parameters under supply voltage and temperature variations are summarized in Tab. 5, whereas performances in the different technology corners are reported in Tab. 6. These results confirm the robustness of the proposed circuit.

E. PERFORMANCES ACROSS DIFFERENT TECHNOLOGY NODES
To highlight the portability of the proposed comparator topology across different technology nodes, additional simulations

TABLE 7. Performance of the proposed comparator in three different technology nodes.

Node [nm]	28		130		180	
V_{DD} [V]	0.15	0.3	0.15	0.3	0.15	0.3
f_{max} [kHz]	900	11510	50	2000	6.21	71.5
ICMR [mV]	150	300	150	300	300	300
Delay [µs]	0.271	0.021	0.631	0.06	39.29	3.39
P_D [pW]	616.84	13850	251.1	6491	17.23	409
PDP [aJ]	167.164	290.85	158.444	389.46	676.967	1386.51
EDP [aJ/kHz]	0.186	0.025	3.169	0.195	109.012	19.392
σ_{off} [mV]	31.91	31.2	30.1	31.2	10.99	11.11

TABLE 8. Comparison with the state-of-the-art of ultra-low voltage comparators.

	Simulated				Simulated		Simulated	Simulated	Measured		Simulated
	This Work				[46]		[53]	[54]	[41]		[42]
V_{DD} [V]	0.15	0.3	0.15	0.3	0.15	0.3	0.3	0.35	0.15	0.3	0.35
Technology [nm]	28	28	180	180	130	130	180	90	180	180	45
Area [μm^2]	80.7	80.7	167.7	167.7	670	670	-	-	900	900	59
ICMR [mV]	150	300	150	300	150	300	300	350	135	275	350
ICMR-range %	100	100	100	100	100	100	100	100	90	91.667	100
Delay [ns]	631	57.8	39290	3390	2200	59.27	980	2.22	442000	34700	2100
Vid [mV]	10	10	10	10	1	1	0.5	-	10	10	10
f_{ck} [kHz]	50	2000	6.21	71.5	80	2000	62.5	50	10	10	10
Offset (σ_{off}) [mV]	30.1	31.2	10.99	11.11	18.74	17.98	-	-	31	8	4.73
$\frac{\sigma_{off}}{V_{DD}}$ [%]	20.067	10.4	7.327	3.703	12.493	5.993	-	-	20.667	2.667	1.351
P_d [nW]	0.251	6.491	0.017	0.409	0.856	52.5	0.1	184	0.027	0.024	0.244
PDP [aJ]	158.381	375.18	667.93	1386.51	1883.2	3111.675	98	408.48	11934	832.8	512.4
EDP [aJ/kHz]	3.168	0.188	107.557	19.392	23.54	1.556	1.568	8.17	1193.4	83.28	51.24
	STD-CELL				BD-SA				STD-CELL		

BD-SA: Body-Driven StrongARM; STD-CELL: Standard-Cell-Based.

referring to the standard-cell library of a 28nm and of a 130nm CMOS technology have been carried out within the Cadence Virtuoso environment, and results are summarized in Tab. 7.

The area footprint of the proposed topology has been estimated for all the three considered CMOS technologies by performing an automatic layout flow within the Cadence Innovus environment. The area has resulted to be $140.8\mu m^2$, $81.7\mu m^2$, and $6.6\mu m^2$ for the 180nm, 130nm and 28nm technology respectively.

VII. COMPARISON

The proposed comparator topology has been compared against the state of the art of ULV comparators (i.e. $V_{DD} \leq 350mV$), and results are summarized in Tab. 8. The proposed comparator exhibits the best EDP among the standard-cell-based comparators in the literature (referring to both the 180nm and 130 nm implementations). The 130nm implementation of the proposed topology results in the best EDP also with respect to ULV full custom comparators, reaching a EDP of only 0.188 aJ/kHz which is about 10 times lower than [46] which resulted in the lowest EDP in the recent literature. The area footprint of the proposed topology results much lower than the area of all other ULV comparators and it results about 5 times more compact than previously presented rail-to-rail ICMR standard-cell-based comparators considering the same technology node.

VIII. CONCLUSION

In this paper we have presented a novel ULV standard-cell-based comparator with rail-to-rail ICMR. The topology, unlike the previous ones, is made up of only 2-inputs NAND gates. An in-depth theoretical analysis has been carried out to confirm the reliability of the proposed comparator even for the extreme values of the ICMR and to determine a suitable sizing strategy for the standard-cells multiplicity. Performances have been assessed through corner analysis and Monte Carlo simulations in three technology nodes, showing state of the art performances.

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