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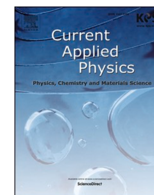

Analytical model of the drain current in amorphous silicon junction field effect transistors

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A R T I C L E I N F O

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A B S T R A C T

This paper presents an analytical model of a hydrogenated amorphous silicon (a-Si:H) junction field effect transistor (JFET) based on a p-type/intrinsic/n-type stacked structure. The p-doped layer is connected to the transistor gate electrode, while the n-layer acts as the device channel. The analysis shows the effect of the geometrical and physical parameters of the intrinsic and n-doped layers on the transistor characteristics. In particular, the intrinsic layer thickness plays a central role in determining the depletion region of the n-channel and, as a consequence, the device threshold voltage. The drain current behavior achieved with a modeled parametric analysis is in very good agreement with the experimental drain current measured on fabricated JFET, both in triode and pinch-off regions. This demonstrates the model feasibility as an effective tool to design thin film electronic circuit as a sensor signal amplifier based on a-Si:H p-i-n junction.

1. Introduction

The success of hydrogenated amorphous silicon (a-Si:H) [1] relies on its low deposition temperature (below 250 °C), which permits deposition on different kind of substrates (such as plastic, metal and glass) and low thermal budget, on its high absorption coefficient in the visible range (ranging between 10^6 and 10^4 cm^{-1} for blue and red wavelengths, respectively), which allows the use of thin film layers, on its high energy gap (around 1.75 eV), which leads to a very low dark current [2].

Thanks to these features, photovoltaics [3,4] and flat panel displays [5,6] constitute the two main applications of hydrogenated amorphous silicon (a-Si:H) materials. In flat panel displays (FPD), bottom gate thin film transistor with amorphous silicon nitride/intrinsic amorphous silicon/n-type amorphous silicon stacked structures [7] are utilized as a switching device, while in photovoltaics, amorphous silicon carbide p-type/intrinsic amorphous silicon/n-type amorphous silicon or crystalline/amorphous silicon heterojunction structures [8] are used as a solar cell.

In FPD applications, even though gate driver based on low-temperature polycrystalline silicon TFT integrated on glass [9–11] have been chosen as a low cost and compact solution with respect to IC based crystalline silicon, different research groups have developed peripheral gate driver based on a-Si:H taking advantage of to its low-fabrication costs and uniform device characteristics over a large area [12–14].

Recently, p-i-n structures have been fabricated on a single glass substrate and used as both photosensors and temperature sensors in lab-on-chip applications where thermal control and light detection are simultaneously needed [15]. In order to increase the system performance, an electronic circuit able to amplify the sensor signal should be integrated. In this way, an edge computing-like system can be achieved. Within this framework, here we present an analytical model useful to design a Junction Field Effect Transistor (JFET) based on an amorphous silicon p-i-n structure. This allows for a sensor signal pre-treatment by utilizing a thin film electronic circuit, fabricated on the same glass substrate where the detection occurs. With respect to the previous papers published by the authors [16,17], the model presented here offers a simple and fast way for designing the device, taking into account the role of the geometrical and physical parameters of the structure. In particular, in the previous works we used a numerical simulator which solves the coupled Poisson and continuity equations inside the structure, taking into account not only the geometrical features and doping of the amorphous silicon layers, but also the defect density distribution and related parameters (energy level of dangling bonds, band tails distributions and capture cross sections for electrons and holes). Of course, while a numerical model can be more precise in fitting the experimental curves, an analytical model is a tool for providing a simple support for understanding the device behavior and a first order device design.

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The work is structured as follows: Section II presents the working operation of the device and its equivalent electrical model section III describes the analytical model and a parametric analysis of the transistor's characteristics, section IV specifies the technological steps for the transistor fabrication, while section V presents the experimental characterization of the fabricated devices and the discussion. Finally, Section VI draws the conclusions.

2. Device structure and operation

The qualitative device structure is reported in Fig. 1. It consists of a metal gate/p-type/intrinsic region/n-doped stacked structure. On the n-doped layer a patterned metal layer defines the drain and source contacts. L and W specify length and width of the channel.

As for the crystalline case, the operation is based on the depletion of the channel, the active region of the transistor [18], that in our device is the n-doped layer. If both drain and source are connected to ground, a negative voltage applied to the gate causes a uniform depletion of the channel. If, instead, the source contact is connected to ground and the drain is connected to a positive voltage (V_{DS}), the voltage applied to the gate (V_{GS}) controls the current flowing between source and drain (I_D), through the not depleted zone of the n-doped layer.

The device is "normally-on", and a threshold voltage (V_t) can be defined as the voltage applied to the gate to completely depletes the n channel, bringing the transistor to the off condition. With the devices in on-condition, a triode or a pinch-off current regime is achieved, depending on the relation between V_{DS} and V_{GS}. From an electrical point of view, the device can be modeled as in Fig. 2, where we notice the presence of the channel modulated current and of the gate-drain and gate-source reverse saturation currents. For a correct operation, the gate current needs to be negligible with respect to the channel current.

3. Analytical model of the JFET characteristics

The main difference with respect to c-Si case is the presence of the intrinsic layer, which ensures a depletion region depth allowing the rectified characteristic of the p-i-n junction [2]. In particular, the intrinsic thickness (W_i) determines the threshold voltage (V_t) and the drain current (I_D), as well as with p-layer and n-layer doping and thicknesses. In order to highlight the effect of W_i on the depletion layer, we carried out the following analysis. Fig. 3 shows the electric field distribution in the neutral zone of the doped layers and in the intrinsic region.

This distribution is valid under the following ideal conditions:

a. Absence of defects in the a-Si:H layers;
b. Absence of electronic defects at the interfaces;
c. Uniform doping of the p-type and n-type zones.

While the first hypothesis is far from being satisfied, due the well known presence of dangling bonds in amorphous material [19,20], the last two assumptions can be considered well satisfied due to the deposition technique of the a-Si:H layers, performed in a PECVD system with three UHV chambers, without interrupting the vacuum between the depositions of the three layers [21].

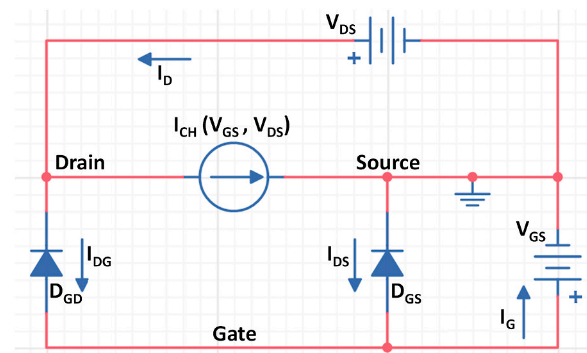

Fig. 2. Electrical model of the a-Si:H JFET.

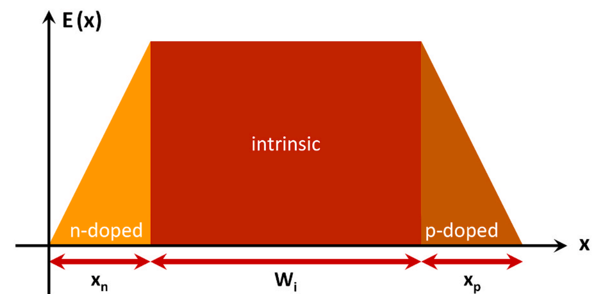

Fig. 3. Electric field distribution in the device assuming ideal conditions. x_n and x_p indicate the depletion region in the n- and p-doped regions, respectively.

Therefore, the following calculation can be considered as a first order approximation of the exact solution. Starting from the Poisson's equation in the depleted regions and imposing the continuity of the electric field at the n-i and i-p interfaces, we obtain:

$$x_d = x_n + x_p = W_i\left[\sqrt{1+\frac{2\varepsilon_s}{qW_i^2}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)(V_{bi}-V_r)}-1\right] \tag{1}$$

where x_n and x_p are the thicknesses of the depletion regions, N_a and N_d are doping concentrations of the n-doped and p-doped layers respectively. Moreover, V_{bi} is the built-in potential of the p-i-n junction, while V_r is the reverse applied voltage. If $N_a = N_d$, then $x_p = x_n = x_d/2$, while if N_a is much greater than N_d, the total depletion region x_d coincides with x_n.

Fig. 4 shows the behavior of x_d (as derived from Eq. (1)) as a function of doping concentration at different intrinsic layer thickness. Data refer

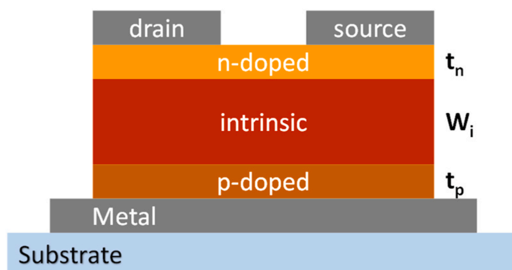

Fig. 1. Cross section (left) and top view (right) of the amorphous silicon JFET. t_p, W_i and t_n are the thicknesses of the p-type, intrinsic and n-type layers, respectively, while L and W are the length and width of the channel. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

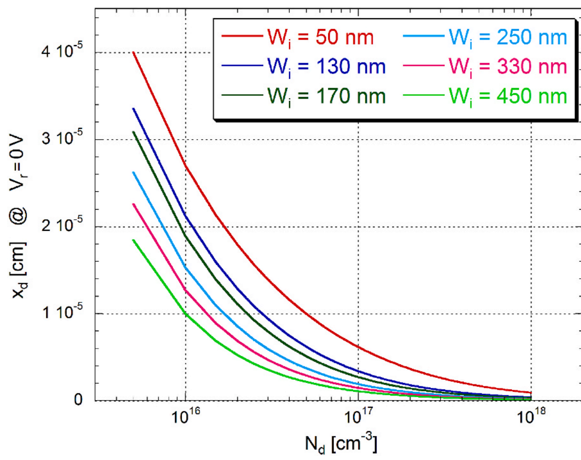

Fig. 4. Width of the depletion region in the n-layer channel as a function of n-layer doping at different i-layer thickness.

to the case $N_a \gg N_d$. To carry out the simulations we considered $V_{bi} = 0.8$ V, $\epsilon_s = 10^{-12}$ F cm^{-1} and $q = 1.6\ 10^{-19}$ C. As expected, x_d decreases with increasing N_d and W_i. This means that a thinner i-layer eases the channel modulation leading to a lower threshold voltage. However, the high defect density in the doped layers and the probability of hopping conduction through defects in a thin intrinsic layer set a lower limit for the i-layer thickness. A careful design of the i-layer thickness is necessary in order to achieve at the same time a low threshold voltage and low reverse saturation current of the gate/p-i-n/source and gate/p-i-n/drain junctions.

Taking into account that an increase of dopant atoms always leads to an increase of defects in a-Si:H materials, the optimal n-layer doping has to satisfy two opposite requirements: ease modulation achieved with low doping and high conductivity achieved with high doping. Therefore, also in this case a trade-off has to be considered in order to get low threshold voltage and high conductivity. These concepts are illustrated in Fig. 5, which reports the depletion region of the channel versus the doping concentration at different voltages applied to the junction: at fixed voltage, the depletion region decreases as the doping increases.

Assuming that the depletion region extends almost completely into the n-channel, the threshold voltage V_t can be derived from Eq. (1), imposing $x_d = t_n$ (the n-doped thickness):

$$V_t = V_{bi} - \frac{t(t+2W_i)qN_d}{2\varepsilon_s} \tag{2}$$

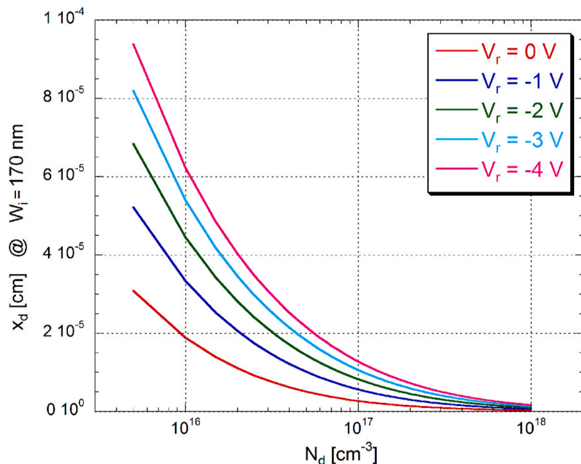

Fig. 5. Width of the depletion region in the n-layer channel as a function of n-layer doping at different reverse voltages (V_r).

where V_{bi} is the built-in voltage and ϵ_s is the dielectric constant of the a-Si:H layer.

With reference to Fig. 6, biasing with a positive voltage (V_{DS}) the drain contact, the depletion region will assume a trapezoidal shape into the n-layer depending on the voltage drop V(y) along the channel axis (y) as reported in the following Eq. (3):

$$x_n(y) = \sqrt{W_i^2 + \frac{2\varepsilon_s}{qN_d}[V_{bi} - V_G + V(y)]} - W_i \tag{3}$$

where we can note the effect of the intrinsic layer thickness. Applying the charge control mode of the MOSFET, we can derive Eq. (4) and Eq. (5) for the drain current in the triode and pinch-off region, respectively:

$$\begin{aligned} I_{D,trd} = \; & q\mu_n N_d \frac{W}{L}\left\{(t+W_i)V_D - \frac{2}{3}\frac{qN_d}{2\varepsilon_s}\right. \\ & \left[\left(W_i^2 + \frac{2\varepsilon_s}{qN_d}(V_{bi} - V_G + V_D)\right)^{3/2} + \right. \\ & \left.\left. - \left(W_i^2 + \frac{2\varepsilon_s}{qN_d}(V_{bi} - V_G)\right)^{3/2}\right]\right\} \end{aligned} \tag{4}$$

$$\begin{aligned} I_{D,sat} = \; & q\mu_n N_d \frac{W}{L}\left\{(t+W_i)\left[\frac{qN_d}{2\varepsilon_s}\right.\right. \\ & \left.\left[t(t+2W_i) - \frac{2}{3}(t+W_i)^2\right] - (V_{bi} - V_G)\right] + \\ & \left. + \frac{2}{3}\frac{qN_d}{2\varepsilon_s}\left(W_i^2 + \frac{2\varepsilon_s}{qN_d}(V_{bi} - V_G)\right)^{3/2}\right\} \end{aligned} \tag{5}$$

Equations (4) and (5) can be utilized to draw the output characteristics of the a-Si:H JFET. Fig. 7 reports the drain current (I_D) as a function of V_{DS} at $V_{GS} = 0$ V achieved with the values of W_i, t_n and N_d reported in Table 1. The electron mobility μ_n has been taken equal to 0.3 cm^{2}V^{-1}s^{-1}, while the other parameters are the same with respect to the simulations carried out to obtain Figs. 4 and 5.

Considering the red curve as a reference and comparing two structures with only one different parameter (see Fig. 7 and Table 1), we note that:

Case A) a decrease of Wi (blue curve) leads to a decrease of I_D due to the larger depletion layer;
Case B) an increase of n-layer thickness (green curve) causes an increase of I_D due to larger conductance;

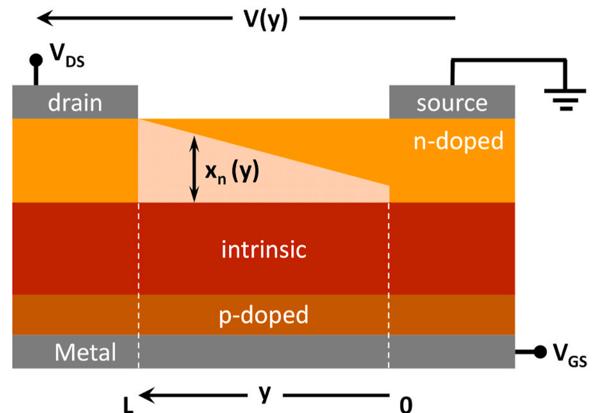

Fig. 6. Cross section of the device in pinch-off condition. The light pink region represents the depletion region of the device. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

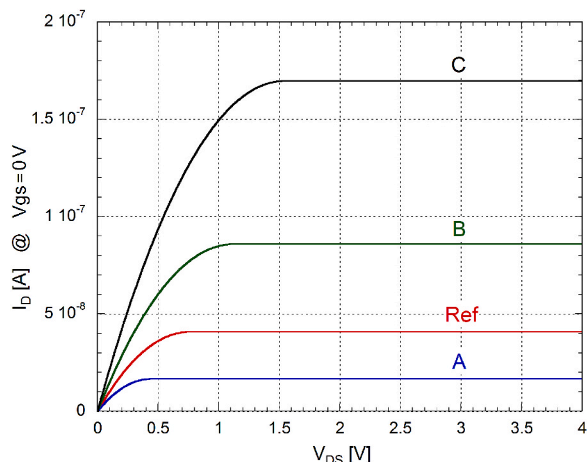

Fig. 7. Modeled output characteristics of an a-Si:H JFET for different values of W_i, t_n and N_d.

Table 1
Geometrical and physical parameters of the modeled JFET output characteristics reported in Fig. 7.

	W_i [nm]	t_n [nm]	N_d [cm^{-3}]
Ref	170	50	1 10^{17}
A	130	50	1 10^{17}
B	170	60	1 10^{17}
C	170	50	1.5 10^{17}

Case C) a doping increase (black curve) induces both a greater current and threshold voltage.

4. Fabrication of the JFET device

The a-Si:H JFET fabrication has been carried out on a glass substrate using standard microelectronic technologies including Plasma Enhanced Chemical Vapor Deposition (PECVD) in UHV three chambers system for the growth of the a-Si:H layers. In particular, five lithographic masks have been used for the whole process as follows:

a. Deposition by vacuum evaporation of a metal stack of Cr (300 Å)/Al (1500 Å)/Cr (300 Å) and its patterning by wet etching for the definition of the bottom gate contact (mask #1);
b. Deposition of the a-Si:H layers by PECVD and of a 50 nm-thick Cr layer by vacuum evaporation. Subsequent patterning by wet etching of the Cr layer and Reactive Ion Etching (RIE) of the a-Si:H materials for the definition of the device area (mask #2);
c. Additional etching of the Cr layer for the definition of the drain and source contacts (mask #3);
d. Deposition by spin coating and subsequent curing and pattering of a 5 μm-thick SU-8 negative photoresist acting as passivation and protective layer (mask #4);
e. Deposition by sputtering of a 200 nm-thick TiW alloy layer and its pattering for the definition of the electrical contacts of drain and source (mask #5).

A schematic 3D illustration of the complete device and of the mask #3 are reported in Fig. 8, while Fig. 9 and its inset show a picture of the glass substrate hosting 12 JFET and a zoom of one JFET, respectively.

The ratio between the channel width (W) and channel length (L) has been kept equal to 10 in all the fabricated transistors.

5. Results and discussion

The fabricated JFETs have been characterized by measuring the output current-voltage characteristics and the gate current curves. The experimental set-up for these measurements includes two Source Measure Unit (SMU) Keithley 236. The two instruments are able to provide the voltages V_{GS} and V_{DS} for the biasing of the device and for the current read-out. Fig. 10 shows the measured I_D-V_{DS} (left) and I_G-V_{DS} (right) curves at different V_{GS} for the device with $W_i = 170$ nm and $t_n = 50$ nm.

Taking into consideration that the reported channel current is net of the gate current and comparing the current values of the two graphs of Fig. 10, it appears that the JFET works correctly in the investigated voltage range: the output current is much higher that the gate current, the characteristics are those typical of a transistor, the gate currents are those representative of a diode.

However, it is important to note that even though an increase of the reverse voltage applied to the drain drives the device in the pinch-off region, at the same time it causes an increase of the gate current and imposes a limit in the voltage applied to the drain. On the other hand,

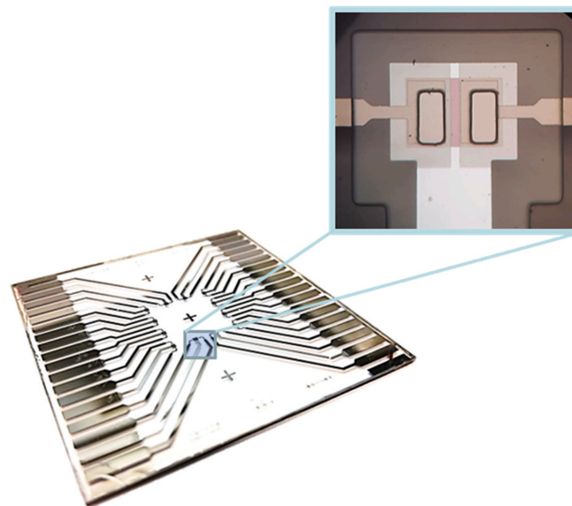

Fig. 9. Picture of the fabricated device. The zoom highlights the gate contact (white region), the a-Si:H layers (pink area) and the drain and source contacts (light brown regions). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

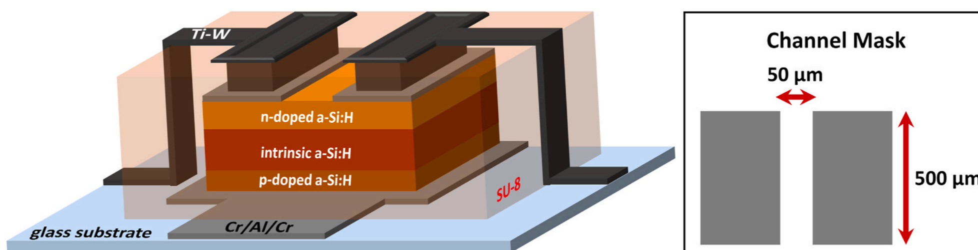

Fig. 8. Schematic 3D view of the fabricated device (left) and mask for the channel definition (right).

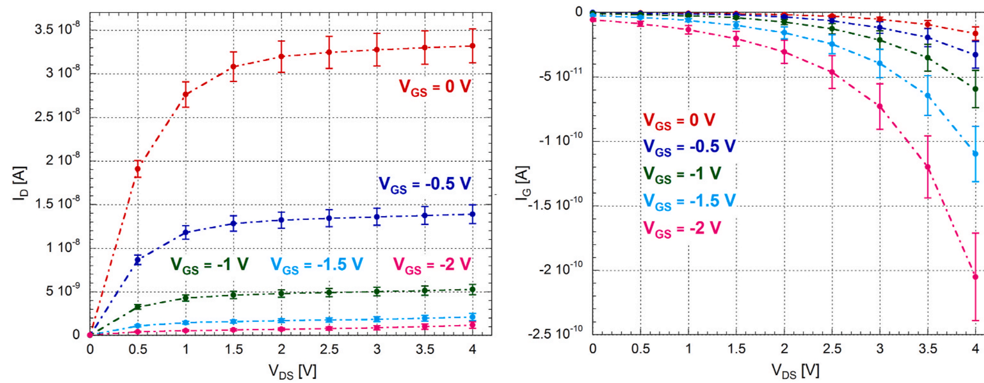

Fig. 10. Measured a-Si:H JFET characteristics. The output curves (left part) are those typical of a transistor, while the I_G-V_{DS} curves (right part) reproduce the typical current-voltage curves of a diode. Symbols represent the average current value for five transistors, while the vertical bars represent the standard deviations.

V_{GS} imposes an even more limiting range of working operation. Indeed, as it can be seen in Fig. 10, an increase in the absolute value of V_{GS} reduces the drain current and simultaneously rises the gate current. Therefore, the achievement of the threshold voltage could be inhibited by the increase in the reverse saturation current of the reverse biased p-i-n gate/drain junction. Therefore, a careful design of the p-i-n junction has to be accomplished. In particular, the thickness of the intrinsic layer has to satisfy two conflicting needs: a decrease in the thermal generated current, which requires a thin i-layer, and a decrease in the hopping current, which calls for a thick region [2].

Besides these considerations, in order to prove the validity of the developed analytical model, we fabricated a-Si:H JFETs by varying the i-layer and the n-layer thickness. Fig. 11 shows the output characteristics I_D-V_{DS}, measured at $V_{GS} = 0$ V, for different geometrical features of the transistor structure.

Using the blue curve as reference, we see that:

1. An increase of the i-layer thickness leads to an increase of the drain current due to a decrease of the induced depletion region. This experimental behavior confirms the initial hypothesis of low defect density at n-i and i-p interfaces. As a matter of fact, a high defect density could have shielded the electric field at the junction, hampering the depletion region in the n-doped channel;
2. An increase in the n-layer thickness causes an increase of the drain current due to its increased conductance.

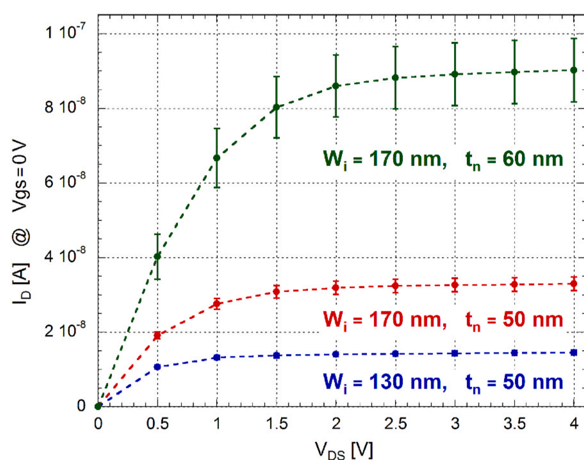

Fig. 11. Measured output characteristics of the fabricated JFETs for different values of the geometrical parameters W_i and t_n. Symbols represent the average current value for five transistors, while the vertical bars represent the standard deviations.

Even though a fitting procedure has not been carried out in this work, data shown in Fig. 11 are well represented by the modeled results reported in Fig. 7. In particular, the investigated devices show measured output characteristics comparable with the simulated ones in the pinch-off region. Indeed, for both modeled and experimental curves, an increase of 30% in the intrinsic-layer thickness increases the drain current about three times, while an increase of 20% in the n-layer thickness increases the drain current of a factor 2.5. In the triode region, instead, differences between modeled data and experimental measurements are present. This can be ascribed to the defect states inside the doped layer that reduce the modulation of the depletion region in the n-channel, leading to different threshold voltages. Once the channel is completely depleted (pinch-off), defect effect is strongly reduced.

However, the obtained results highlight the role of the intrinsic layer in controlling the working operation of the device and that the model can work as a successful tool for designing the device performance.

Taking into account that the a-Si:H p-i-n structure has been extensively used as photodiode and temperature sensors in lab-on-chip systems for biomolecular recognition [22–25] and DNA amplification [26, 27] the presented results open the possibility to integrate a thin film electronic amplifier of sensor signal on the same glass substrate.

6. Conclusions

An analytical model of the channel depletion region and of the drain current of an a-Si:H JFET based on a p-i-n junction has been reported in this work. To our knowledge, it is the first time that the intrinsic layer is taken into account in determining the depletion region of the n-type channel and the threshold voltage of the device. In particular, a parametric analysis shows that (i) a thinner i-layer eases the channel modulation leading to a lower threshold voltage and to a lower drain current in the triode and pinch-off regions, (ii) a thicker n-type layer hinders the channel depletion increasing both threshold voltage and drain current.

The model results are very well reproduced by the drain currents measured on JFET fabricated with the same geometrical parameters used in the simulations. This agreement demonstrates that the developed model can be effectively used as a tool for designing thin film electronic amplifiers based on a p-i-n structure.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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