80dB Tuning Range Transimpedance Amplifier Exploiting the Switched-Resistor Approach

Francesco Centurelli, Alessandro Fava, Giuseppe Scotti, Alessandro Trifiletti

DIET Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni

Università di Roma La Sapienza, Roma, ITALY

Contact Author: Francesco Centurelli

francesco.centurelli@uniroma1.it

Abstract

This paper presents the design of a low-noise, low-power transimpedance amplifier (TIA) for biomedical applications. The proposed TIA exploits for the first time in the literature a Switched-Resistor (SR) as the feedback element in order to achieve a digitally tunable transimpedance gain with an extremely large tuning range (higher than 80 dB) and a maximum value as high as 10 GΩ. Another important feature which comes with the adoption of the SR technique is that the output voltage is already sampled with the SR clock signal and this simplifies the design of the following digitizer block. The circuit has been designed in a commercial 130nm CMOS technology and simulation results show a minimum IRCSN (input-referred current spectrum noise) of 1.67 fA/√Hz and a total power consumption of 0.9 µW with a 0.6 V supply voltage. Extensive parametric and Monte Carlo simulations have confirmed a good robustness against PVT and mismatch variations.

Keywords

Bio-transimpedance, Switched-Resistor, low-noise, gain control, low-power CMOS, sensor interface.

1. Introduction

Integrated current measurement systems are gaining more and more importance for the research and understanding of biological physical phenomena and for biomedical instrumentation and research in general. In all these research areas, the current measurement systems require a compact front-end with very low input noise and a widely tunable transimpedance gain. In particular, referring to biological studies involving the measurement of ion channel and membrane protein currents, an input current resolution of ±5 pA and a recording bandwidth ranging from 1 to 10 kHz are required. Other applications such as DNA sequencing have to cope with input currents in the range of 10-50 pA due to nanopore sensors [1][2].

If we look at wearable biomedical devices, which are nowadays utilized in a lot of health-care applications, such as pulse oximetry, photoplethysmogram (PPG), blood glucose measurements and near infrared spectroscopy (NIRS) [3][4][5][6], again we find that they require a front-end implemented by a transimpedance amplifier (TIA), as shown in Figure 1. By looking at Figure 1 it is evident that the feedback element which determines the transimpedance gain can be realized by different approaches. The polysilicon resistor array is the conventional solution adopted to implement TIAs with a programmable gain [7][8].

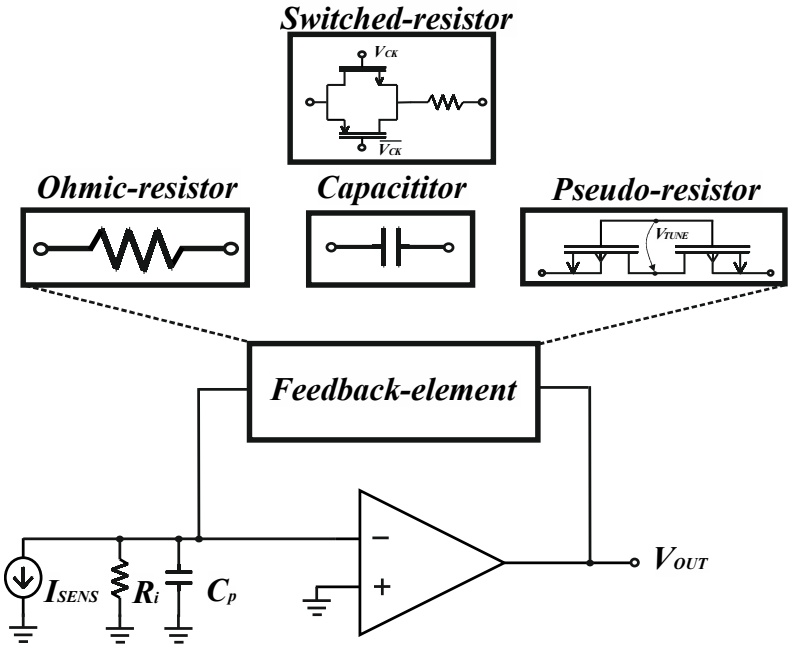


Figure 1: Transimpedance amplifier with different feedback elements.

Other solutions provide capacitive feedback elements [9][10] and pseudo-resistor feedback elements [11][12][13] to improve the trade-off between input noise, programmable gain, bandwidth, and linearity. However solutions based on capacitive feedback elements require more than one stage and therefore exhibit higher power consumption and larger area footprint than other approaches. On the other hand, TIAs based on pseudo-resistor feedback elements are typically much sensitive to process and temperature variations, and may require complex calibration circuits to achieve high production yield.

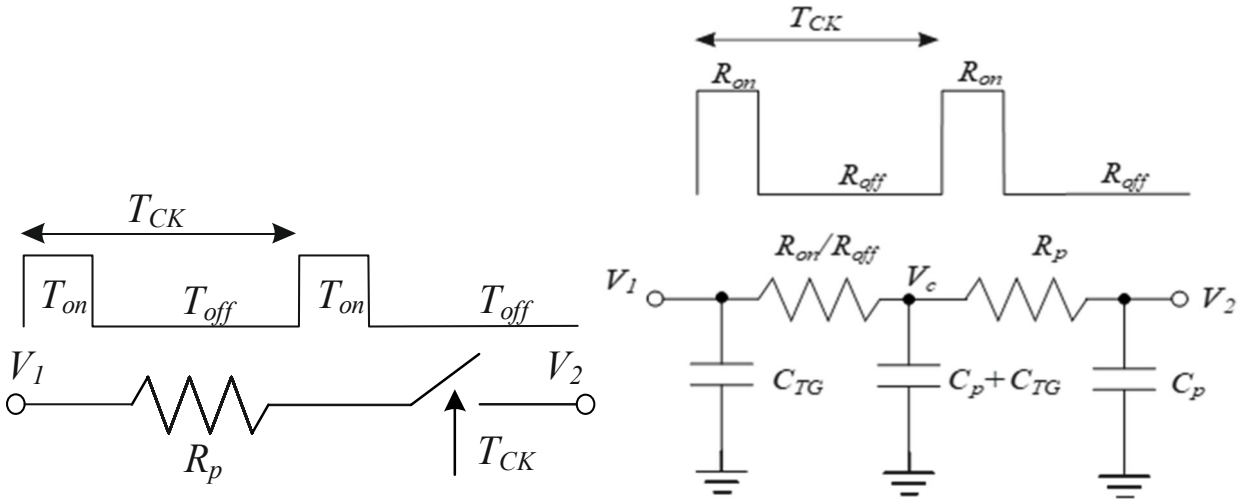
A novel approach to implement digitally tunable and high-valued resistors is represented by the Switched-Resistor (SR) technique [14][15][16], which is gaining popularity among designers of integrated circuits for biomedical applications [17][18][19]. A digital tuning of the equivalent resistance is achieved by a duty cycle controlling unit which adjusts the clock signal driving the SR. Another important feature of the SR technique is that it provides an output voltage which is already sampled with the SR clock signal and this simplify the design of the following digitizer block if the SR clock is used also for the digitizer section. At this purpose, it has to be remarked that the SR technique allows to tune the value of the equivalent resistance without changing the clock frequency. The same is not true for the switched capacitor approach in which the value of the equivalent resistance is tuned by changing the clock frequency.

In this paper we present a TIA for biomedical applications in which we exploit the SR technique to maximize the tuning range of the transimpedance gain while guaranteeing a maximum transimpedance value as high as 10 GΩ. The amplifier in the feedback loop is designed as a single-stage OTA, composed by a p-MOS differential pair with active load, to improve the input noise, and has been optimized to reduce power consumption and area while operating with a supply voltage of 0.6V.

In the following, Section 2 describes the SR technique and discusses the parasitic effects involved. Section 3 presents the design of the proposed TIA. The simulated results and the performance comparisons are reported in Section 4. Finally conclusions are drawn in Section 5.

2. Review of the Switched-Resistor technique

The principle of operation of the SR technique can be described referring to Figure 2a: a MOSFET switch is placed in series with a polysilicon resistor and is driven by a clock signal whose duty cycle δ can be digitally adjusted. The equivalent conductance, that depends on the average current that flows in the series, is proportional to the duty cycle of the clock signal. A detailed model of the switched resistor which accounts for the main parasitic phenomena involved in the SR technique has been recently proposed by the authors in [20].



a) b)

Figure 2: SR technique: a) scheme; b) circuit model.

The detailed model reported in Figure 2b emphasizes the parasitic elements showing the parasitic resistances of the transmission gate switch (TG) in both the on and the off phases of the TG denoted as (R_{on}, R_{off}), the substrate parasitic capacitances of the polysilicon resistor C_p and the parasitic capacitances of the MOS switch C_{TG}.

For applications requiring a very small duty cycle in order to get a very high resistance multiplication factor, the parasitic elements become dominant, and an accurate model is required to determine the exact value of the duty cycle needed to obtain a specific value of the equivalent resistance. The equivalent resistance R_{SR} can be expressed as [20]:

$$R_{SR} = \frac{V_s}{I_{avg}} = R_{SR_{on}} || R_{SR_{off}} \tag{1}$$

where:

$$R_{SR_{on}} = \frac{R_p}{\delta\ \alpha_{on} + F_{ck}[(\tau_{on} - C_p R_p)(V_{an_c}(0) - \alpha_{on})]\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)} \tag{2}$$

$$R_{SR_{off}} = \frac{R_p}{(1-\delta)\ \alpha_{off} + F_{ck}[(\tau_{off} - C_p R_p)(V_{an_c}(\delta T_{ck}) - \alpha_{off})]\left(1 - e^{-\frac{(1-\delta) T_{ck}}{\tau_{off}}}\right)} \tag{3}$$

with $\alpha_{on} = \frac{R_p}{R_p + R_{on}}$; $\alpha_{off} = \frac{R_p}{R_p + R_{off}}$; $\tau_{on} = C_p(R_{on} || R_p)$; $\tau_{off} = C_p(R_{off} || R_p)$; $V_{an_c}(t) = V_c(t)/V_1$. When the duty cycle is reduced beyond a certain value, the $R_{SR_{on}}$ becomes greater than the $R_{SR_{off}}$ and the R_{SR} exhibits the maximum achievable value which is determined by the value of R_{off}.

3. Architecture and design of the proposed TIA

The architecture of the proposed TIA is depicted in Figure 3. The core of the circuit is a conventional single-stage Operational Transconductance Amplifier (OTA), and the shunt feedback resistor is implemented through the SR technique.

Referring to the TIA architecture reported in Figure 3, the closed-loop transfer function can be easily computed as follows:

$$\frac{V_{out}}{I_{in}} = -\frac{R_P * K_{OTA}}{S^2 C_{in} * \tau_{OTA} * R_p + S(C_{in} * R_p + \tau_{OTA} * \delta) + \delta(K_{OTA} + 1)} \tag{4}$$

where C_{in} is the input parasitic capacitance (see Figure 3), τ_{OTA} is the time constant corresponding to the OTA dominant pole, K_{OTA} is the open-loop gain of the OTA, and the conventional model $R_{SR} \cong \frac{R_p}{\delta}$ has been assumed for the switched resistor to keep the expression as simple as possible.

Considering the closed-loop poles, the maximum bandwidth without overshoot in the frequency response is obtained with two real and coincident poles. For the second-order equation to give two real and coincident poles, its discriminant Δ can be equated to zero obtaining the follow condition:

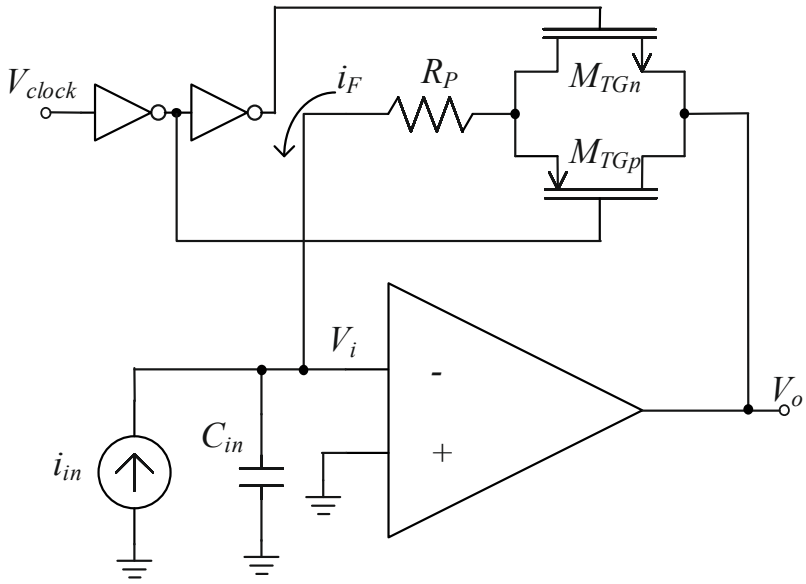


Figure 3: Architecture of the proposed SR TIA.

$$\frac{C_{in}R_p}{\delta\tau_{OTA}} + \frac{\delta\tau_{OTA}}{C_{in}R_p} = 2(2 \cdot K_{OTA} + 1). \quad (5)$$

For small values of δ, the open loop gain K^*_{OTA} corresponding to real coincident poles can be derived as follows:

$$K^*_{OTA} \cong \frac{1}{4}\frac{C_{in}R_p}{\delta\tau_{OTA}} - 2. \quad (6)$$

For $K_{OTA} < K^*_{OTA}$ we have improved stability with reduced bandwidth.

The worst case in terms of stability is reached when $\delta = 1$ (corresponding to the minimum value of the feedback resistor); to guarantee stability without overshoot in this condition, the open loop gain K_{OTA} has to be set equal or smaller than K^{**}_{OTA}

$$K^{**}_{OTA} = \frac{1}{4}\frac{C_{in}R_p}{\tau_{OTA}} + \frac{1}{4}\frac{\tau_{OTA}}{C_{in}R_p} - 2. \quad (7)$$

To guarantee stability and maximum bandwidth when the feedback resistor value is tuned over a wide range, a programmable gain amplifier could be exploited. However, since in most biomedical applications the bandwidth is not a primary design goal, we have adopted a fixed gain amplifier, and a relatively small open-loop gain of the OTA has been chosen in order to guarantee stability for all the feedback resistors settings.

The TIA has been designed referring to a commercial 130nm CMOS technology from STMicroelectronics and Cadence Virtuoso with the Spectre simulator have been used for schematic entry and simulations.

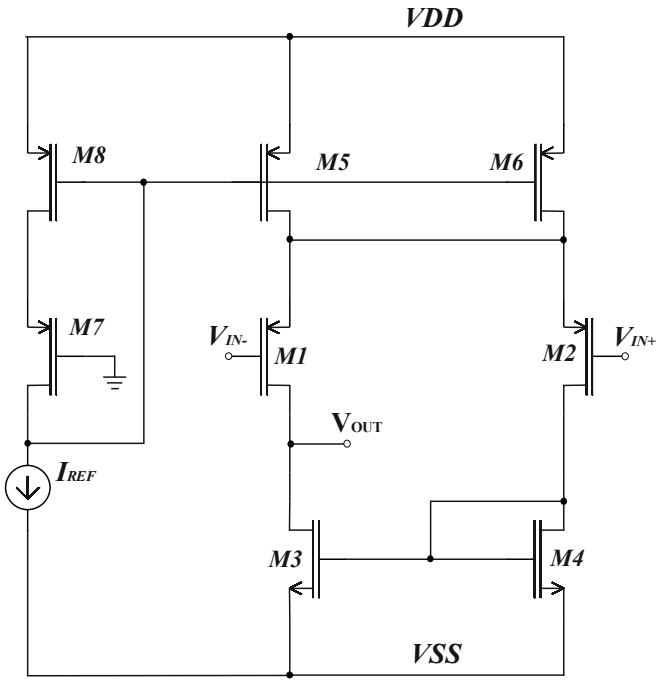


Figure 4: Schematic of the single-stage OTA employed in the TIA.

3.1 OTA design

The schematic of the single-stage OTA adopted in the TIA is reported in Figure 4. Referring to Figure 4, the supply voltage V_{DD} has been set to 0.6V, V_{SS} is 0V, and the ground symbol (in Figure 3 and Figure 4) denotes the analog ground equal to $(V_{DD} + V_{SS})/2$. The amplifier has been optimized to reduce the input current noise. The bias current I_{REF} has been set to 500 pA, M1-M2-M7 have been sized with W=38.5 μm and L = 0.2 μm, M5-M6-M8 with W =2 μm and L =0.13 μm, M3-M4 with W =1 μm and L =15 μm.

The OTA exhibits a DC gain of 30 dB with a common mode rejection ratio (CMRR) of 57 dB and a unity-gain frequency higher than 2 MHz, with a power consumption of about 0.9 μW. The open-loop gain of the OTA has been kept low in order to guarantee the closed-loop stability of the TIA for a very wide range of transimpedance gain settings. Obviously, the low open-loop gain results in higher closed-loop input impedance and limited bandwidth for a specific input capacitance.

3.2 Switched-Resistor design

The SR contributes to overall noise both through the poly resistor and through the switches; on the other hand, these elements, together with the duty cycle, determine the transimpedance gain, taking also into account the parasitic effects, as shown by (1)-(3). A tradeoff has thus to be found between the different contrasting requirements. The TIA being a low-noise front-end, a significant effort has been devoted to the noise optimization, and in particular to the minimization of the noise generated by the TG switches employed in the switched resistor used as feedback element. At this purpose, both the n-MOS and p-MOS transistors used in the TG have been sized with $W/L = 1\,\mu m/10\,\mu m$, resulting in R_{on}/R_{off} equal to $451\ k\Omega/165\ G\Omega$ respectively and C_{TG} about equal to $1\ fF$. In order to maximize the transimpedance gain, the value of the polysilicon resistor has been set to $R_p = 1M\Omega$, as a tradeoff between area and minimum value of the duty cycle for a target transimpedance gain of $10\ G\Omega$, resulting in a parasitic capacitance C_p about equal to $90\ fF$.

The clock frequency for the switched resistors has been set to $F_{CK} = 100\ kHz$, that for the (minimum) duty cycle corresponding to an equivalent resistance of $10\ G\Omega$ results in a minimum T_{on} of 710 ps, that results compatible with the rise/fall times allowed by the inverters driving the switch. The SR feedback resistor is driven by two minimum size CMOS inverters, taken from the standard-cell library of the adopted $130nm$ CMOS technology. The supply voltage of the digital section driving the inverters is $1.2\ V$.

4. Simulation results

The layout of the proposed SR-TIA is reported in Figure 5 showing an area footprint of $102\mu m\ x\ 71\mu m$. The total capacitance C_{in} at the input of the TIA in Figure 3 depends on the application and more specifically on the parasitic capacitance of the sensor. As an example, for a general avalanche photodiode (APD) the parasitic capacitance typically ranges from 1 pF up to 10 pF [21][22]. In our simulations we have assumed $C_{in} = 5\ pF$.

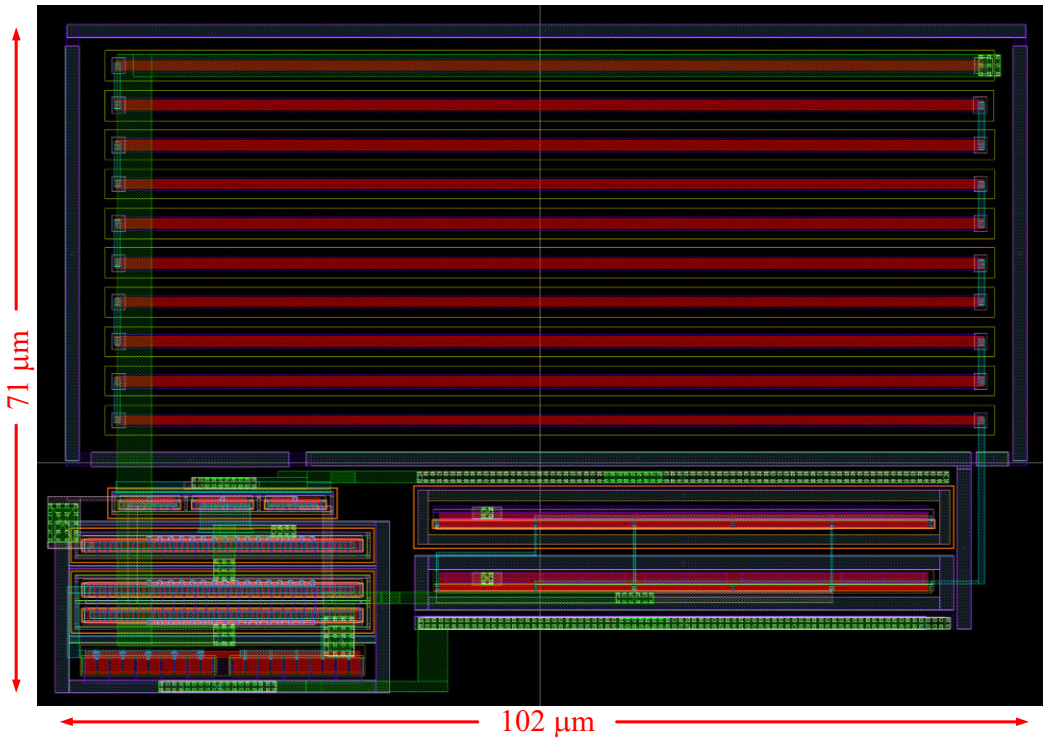


Figure 5. Layout of the proposed SR TIA.

Figure 6a reports the frequency response of the transimpedance gain TZ for different settings of the duty cycle δ from 0.007% to 100%, demonstrating a maximum gain in excess of 10 $G\Omega$ and 80 dB of tuning range with a closed-loop bandwidth ranging from 67 Hz up to 500 kHz. Figure 6b shows the transimpedance gain at low frequency as a function of the duty cycle; the observed non-linear relationship is due to the parasitic capacitances of the SR and is in agreement with the accurate model in [20].

The input-referred current noise spectrum is reported in Figure 7, in which we have also added the theoretical value of the current noise spectrum:

$$PSD_{thermal} = \frac{4K_bT}{R_{eq}} \tag{8}$$

where R_{eq} has been assumed equal to the transimpedance gain TZ.

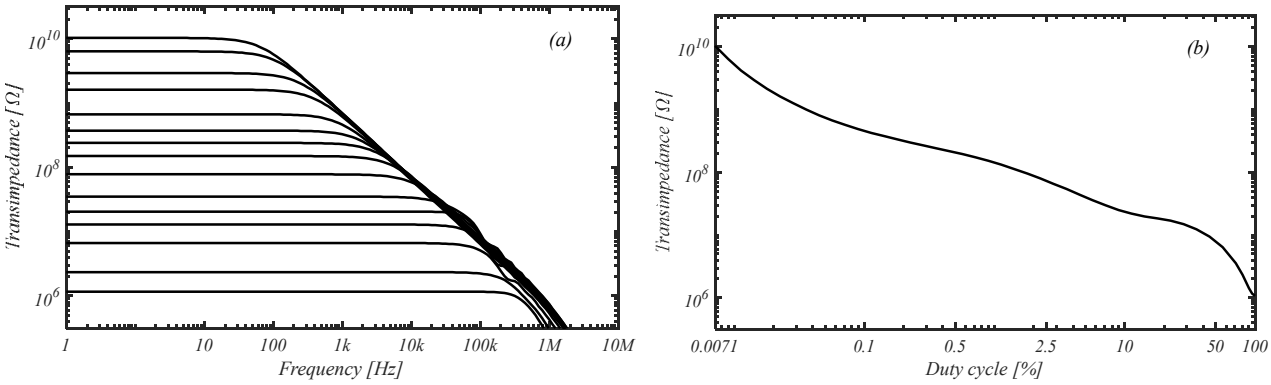


Figure 6: Transimpedance Gain computed with PSS+PAC simulation: (a) frequency responses for different values of duty cycle; (b), low frequency Transimpedance Gain for different values of duty cycle.

It can be noted that the current noise spectrum traces in Figure 7 are not in agreement with the theoretical values and this is due to the additional noise sources in the TG switch and in the OTA. Anyway for a 10 $G\Omega$ transimpedance gain the input-referred current noise spectrum has a minimum spot value of 1.67 $fA/\sqrt{Hz}$ and the input-referred noise (IRN) integrated in the -3dB bandwidth of the TIA results in an input noise of only 10.6 fA_{RMS}.

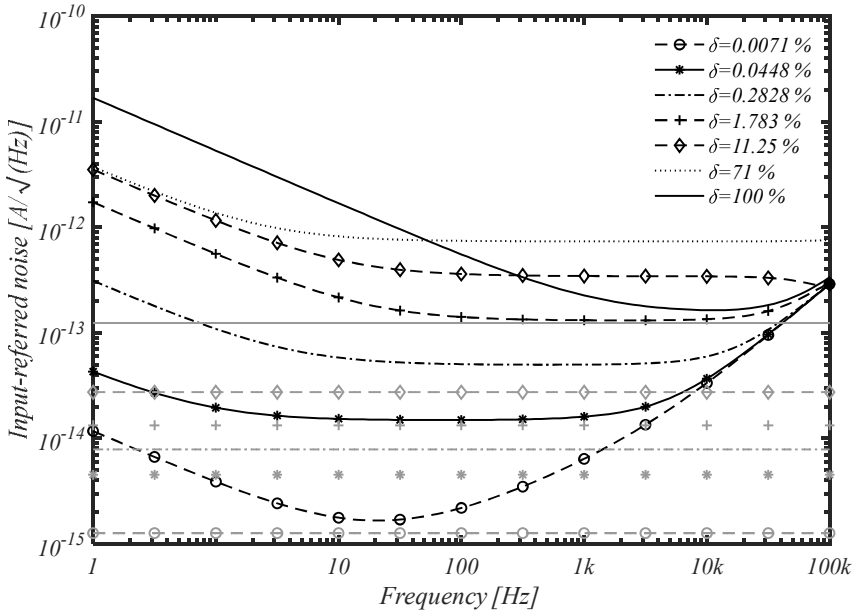


Figure 7: Input-Referred Current Noise Spectrum computed with PSS+PNOISE simulation; traces in grey represent the corresponding ideal current noise spectrum in Eq. 8.

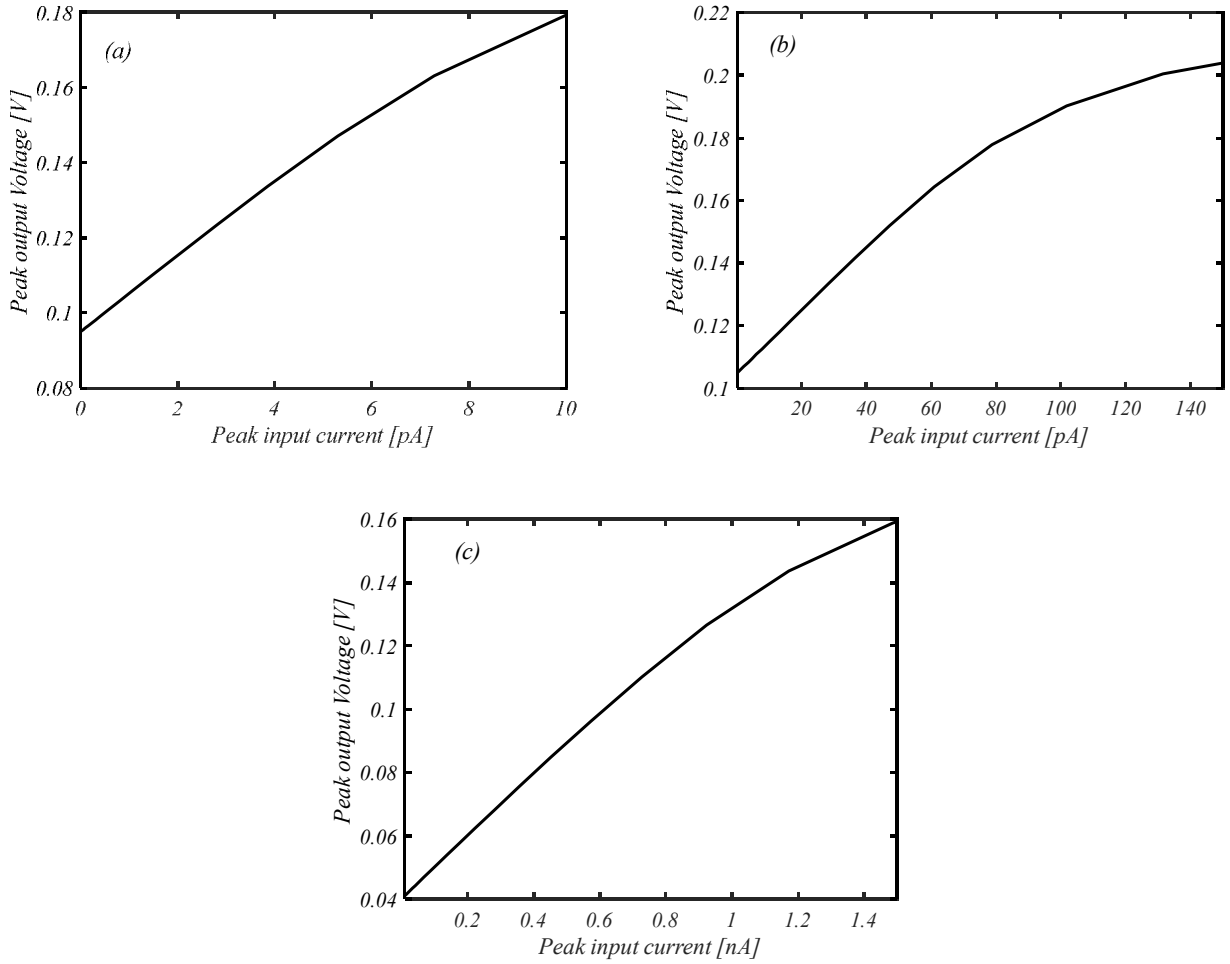


Figure 8 I-V curves at different transimpedance gain: a)10GΩ b) 1GΩ c) 100MΩ

The linearity of the TIA front-end has also to be considered to evaluate its dynamic range. The I-V curves at different transimpedance gains are reported in Figure 8, and show a linear behavior up to a peak output voltage in the order of about 0.17 V for $TZ=10\ G\Omega$.

These data are reported more clearly in Table 1, where for different gain settings the maximum input current for a 1% THD together with the corresponding amplitudes of first harmonic of the output voltage are reported; the distortion simulations have been carried out exploiting the QPSS analysis in the Cadence Virtuoso environment. For the case of a 10 $G\Omega$ gain, an input current of 4.5 pA is obtained; combining it with the input-referred noise data reported in Table 1, a dynamic range of about 49.5 dB has been computed for the proposed TIA.

Table 1
Total Harmonic Distortion (THD) of the proposed TIA

Transimpedance Gain TZ [Ω]	Peak input current @ 1% THD [A]	Amplitude of 1st harmonic @ 1% THD [V]
10G	4.5p	46.14m
1G	60p	62.29m
100M	400p	40.04m
1M	35n	37.55m

4.1 Analysis of the distortions

Three main sources of distortion are present in a SR transimpedance amplifier: the nonlinearity of the OTA, the nonlinearity of the feedback element and the periodically time-varying nature of the system, where the clock signal switches the feedback element between two values ($R_p + R_{on}$ and $R_p + R_{off}$). In the limit of infinite loop gain, this latter effect results in a periodically varying gain and thus yields intermodulation products between the input signal and the clock signal with its harmonics.

For what concerns the other two effects, a simplified model, presented in the Appendix, shows that the nonlinearities of the feedback element are the main sources of distortion. The nonlinearity in the SR is due to the switch resistance, that depends on the drain-source voltage of the devices, and a high value of R_{on} with respect of R_p makes this effect not negligible. This nonlinearity could be reduced by changing the dimensions of the MOS transistors in the TG, but this would result in an increased noise contribution coming from the TG itself. Simulations using ideal switches with the same values of on and off resistances, reported in Table 2 , verify that the TG is the main limitation to the linearity.

Table 2
Total Harmonic Distortion (THD) of the proposed TIA with ideal switch

Transimpedance Gain TZ [Ω]	Peak input current @ 1% THD [A]	Amplitude of 1st harmonic @ 1% THD [V]
10G	14.5p	145.8m
1G	165p	169.8m
100M	810p	80.7m
1.3M	130n	171m

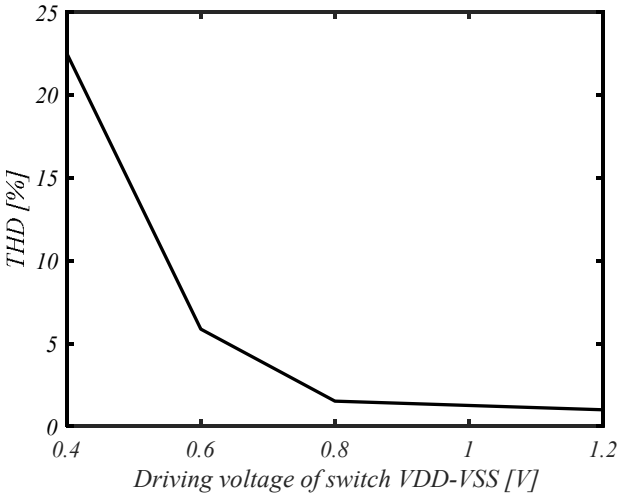


Figure 9 Harmonic distortion in function of transmission gate drive voltage considering 1 GΩ of transimpedance gain

In order to improve the distortions without degrading the noise performance, the amplitude of the clock signal driving the TG can be changed. To better highlight this point, the total harmonic distortion (THD) of the TIA vs. the transmission gate drive amplitude is reported in Figure 9 that shows how the THD is dramatically reduced by increasing the driving voltage, we have therefore chosen 1.2 V as supply voltage for the inverters driving the switch.

4.2 Robustness against PVT variations

Parametric and corner simulations have been carried out in order to assess the robustness of the transimpedance amplifier to process, supply voltage and temperature (PVT) variations. The temperature range assumed for the variation goes from *-20°* to *120°C* while the supply voltage V_{DD} has been varied in a range larger than the typically considered *±10%* of the nominal one to evaluate the possibility of operation at reduced supply voltage (0.5 V to 0.7 V variation has been considered). Figure 10a and Figure 10b show the transimpedance gain at low frequency as a function of temperature and supply voltage respectively, showing in both cases the excellent robustness of the circuit to temperature and supply voltage variations. In particular, Figure 10b shows that the TIA may be supplied with a smaller voltage than the nominal one, in order to reduce the power consumption.

As a further validation of circuit robustness, we have considered the simulations in the extreme PVT corners: TIA performance results somehow sensitive to corner variations, however the possibility of tuning the feedback resistance value by changing the clock duty cycle allows restoring the required gain value. Figure 11 reports the frequency response of the transimpedance gain in the extreme PVT corners before and after the tuning (process variations, temperature variations in the 0-*70°* range and *±10%* supply variations are considered). Table 3 reports the low frequency transimpedance gains in the extreme corners before and after the tuning, including the value of the duty cycle used to compensate the variation. The results in Figure 11 and Table 3 clearly show that, even in the extreme PVT corners, the proposed TIA confirms about 80 dB of tuning range.

The linearity and noise performance under temperature variations are summarized in Table 4. It is evident from Table 4 that linearity performance is worst at high temperatures. Probably a proportional to absolute temperature (PTAT) biasing would allow to improve linearity at high temperatures, but this has not been taken into account in this work.

The linearity and noise performance under supply voltage variations are reported in Table 5, showing limited variations of distortion and noise performance with the supply voltage.

Finally, the linearity and noise performance across the extreme PVT corners are summarized in Table 6, showing reasonable performance also in the extreme corners.

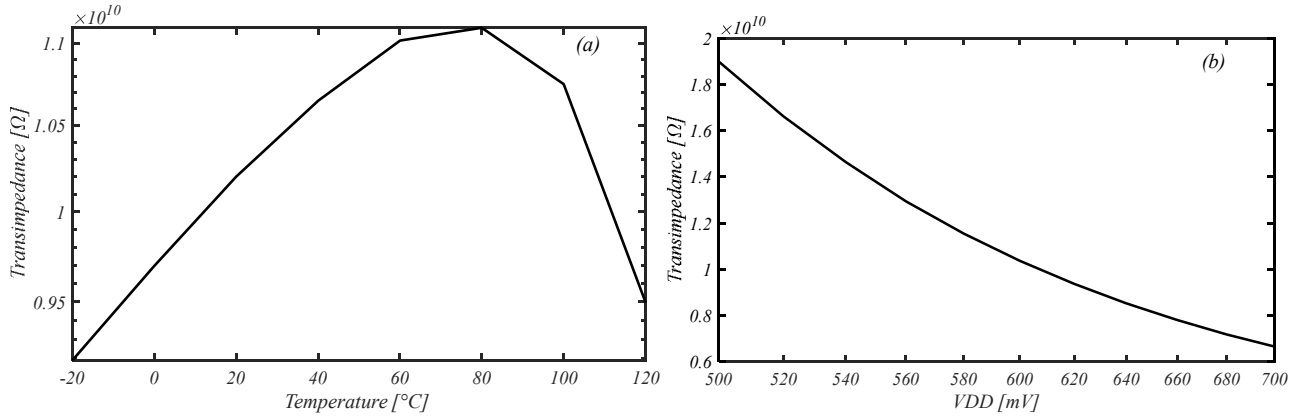


Figure 10: Variations of the transimpedance gain (maximum gain setting) vs: a) temperature (-20 to 120 °C); b) supply voltage (500 to 700 mV).

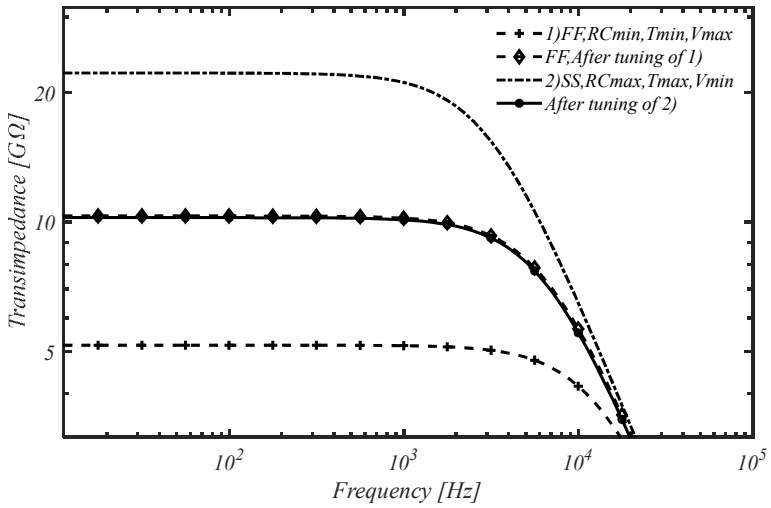


Figure 11: Transimpedance gain (maximum gain setting) under extreme PVT variations, before and after tuning

Table 3
Transimpedance Gain under extreme PVT variations, before and after tuning

PVT Extreme Corners	TZ_{max} $[G\Omega]$	δ $[\%]$	TZ_{min} $[M\Omega]$	δ $[\%]$
TYP	10.150	0.0071	1.071	100
FF+RminCmin+Tmin+Vddmax (no tuning)	5.176	0.0071	0.824	100
FF+RminCmin+Tmin+Vddmax (after tuning)	10.339	0.0047	1.049	92
SS+RmaxCmax+Tmax+Vddmin (no tuning)	22.233	0.0071	1.347	100
SS+RmaxCmax+Tmax+Vddmin (after tuning)	10.256	0.0117	1.347	100

Table 4
THD and IRN of the proposed TIA for different operating temperatures

$Temp$ $[°C]$	δ $[\%]$	Peak input current @ 1% THD *[A]*	Amplitude of 1st harmonic @ 1% THD *[V]*	IRN $[A_{RMS}]$
-20	0.0068	9p	89.07m	15.97f
27	0.0071	4.5p	46.16m	16.05f
60	0.0074	2p	19.97m	14.92f
80	0.0074	800f	8.057m	12.76f
120	0.0069	190f	1.834m	8.69f

Table 5
THD and IRN of the proposed TIA for different supply voltages

V_{DD} $[V]$	δ *[%]*	Peak input current @ 1% THD *[A]*	Amplitude of 1st harmonic @ 1% THD *[V]*	IRN $[A_{RMS}]$
500m	0.0096	6.5p	64.21m	16.80f
600m	0.0071	4.5p	46.16m	16.05f
700m	0.0059	2.5p	24.77m	15.83f

Table 6
THD and IRN of the proposed TIA in the extreme PVT corners

Process	δ *[%]*	Peak input current @ 1% THD *[A]*	Amplitude of 1st harmonic @ 1% THD [V]	IRN $[A_{RMS}]$
FF+RminCmin+Tmin+ Vddmax	0.0051	7p	70.17m	15.34f
SS+RmaxCmax+Tmax +Vddmin	0.0103	3.5p	35.55.m	17.08f

4.3 Monte Carlo analysis: mismatch variations

To validate the robustness of the transimpedance to mismatch variations, Monte Carlo simulations referring to the statistical models provided by STMicroelectronics have been carried out. Histograms of the low frequency transimpedance gain for the maximum and minimum gain settings respectively are reported in Figure 12a and Figure 12b. Mean values and standard deviations are reported in the figures showing moderate variations under device mismatches.

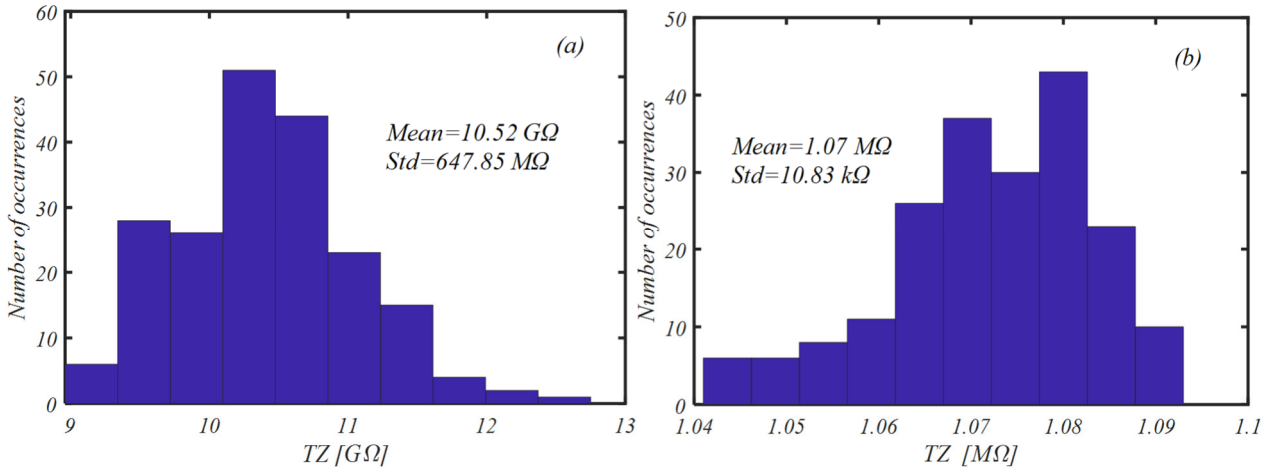


Figure 12: Mismatch variations: (a) maximum Transimpedance Gain case (b); minimum Transimpedance Gain case.

4.4 Post layout simulations

After the implementation of the layout, post layout simulations have been carried out. Results from post layout simulations have been found in reasonable agreement with schematic level simulations: the same TZ values are obtained in post layout simulations with respect to schematic level simulations, with a variation in the duty cycle in the order of 10 to 15%. The main parasitic effect due to the layout has been found to be the parasitic capacitance of the wires connecting the clock driver inverters to the TG switch. To compensate this layout effect the driving capability of the clock driver inverters has been increased of about 10%. After this adjustment, results from post layout simulations have been found in very close agreement with schematic level simulations: the same TZ values are obtained in post layout simulations with respect to schematic level simulations, with a very small variation in the duty cycle and with no relevant differences in noise and distortion performances.

In order to estimate the power consumption of the TIA, we have measured (referring to post layout simulations) the dynamic power of the clock driving inverters and we have found that it is about two orders of magnitude lower than the power consumption of the OTA, and it is therefore negligible as expected. Since the adjustment of the duty cycle can also be implemented through

fully digital circuits (delay and XOR), also the dynamic power of duty cycle tuning circuits is expected to be negligible. For what concerns the clock generator, we consider it as a conventional block always available on chip and we have therefore neglected its power consumption.

Table 7

Comparison against the state of the art

Ref.	[23]	[24]	[12]	[25]	[26]	[27]	This work
Year	2020	2019	2018	2017	2020	2021	2021
Technol. (μm)	0.18	0.35	0.18	0.35	0.18	0.18	0.13
V_{DD} (V)	1.4	6.6	1.8	3.3	1.8	1.8	0.6
Power (μW)	52	330	9500	30000	183	5600	0.9
TZ (Ω)	1.72G	1M	1M-1G	330M	100M-100G	100M	1M-10G
BW (Hz)	180k	8.2M	8k-2M	2M	21k-2.75M	1.3M	67-500k
IRCSN ($A/\sqrt{Hz}$)	18f	3.5p	5.5f-140f	5.6f	42f	15.5f	1.67f
Area (mm^2)	0.0154	-	0.07	0.2	-	0.126	0.0072
FOM	$3.3*10^{32}$	$7*10^{27}$	$1.53*10^{29}$	$3.9*10^{30}$	$2.7*10^{32}$	$1.49*10^{30}$	$4.46*10^{32}$
Tunable	no	no	yes	no	yes	no	yes
results	simulated	simulated	measured	measured	simulated	simulated	simulated

4.5 Comparison with the literature

In order to compare different TIAs designs, we refer to a widely adopted figure of merit (FOM) [23] for the TIA performance:

$$FOM = \frac{TZ*BW}{P_D*IRCSN} \quad (9)$$

where TZ is the transimpedance gain, BW is the 3 dB bandwidth, P_D is the average power dissipation and $IRCSN$ is the input-referred current spectrum noise. Table 7 compares the TIA design proposed in this work against several CMOS TIAs for biosensors applications available in the literature. The designed TIA circuit has a significant improvement in performance showing low noise, widely tunable gain, less power dissipation, better figure of merit (FOM) and reduced footprint compared to conventional CMOS based TIAs.

5. Conclusions

In this paper we report for the first time a transimpedance amplifier for biomedical applications that exploits a switched resistor as the feedback element. This allows achieving a very wide tuning range and compensation of process variations, by varying the duty cycle of the clock signal. As an additional advantage, the proposed TIA provides an output voltage which is already sampled with the SR clock signal and whose value can be easily held exploiting parasitic or small explicit capacitances, thus avoiding the design of an additional sample and hold circuit and simplifying the design of the analog to digital converter.

Simulations show that the proposed approach allows the implementation of TIAs with lower input noise and lower power consumption with respect to TIAs based on pseudo-resistor feedback elements. The low input noise has been achieved by optimizing both the OTA and TG switch, managing also the trade-off between linearity and power consumption. A 1MΩ polysilicon resistor has been exploited to obtain a very wide tuning range and a maximum transimpedance gain as high as 10 $G\Omega$, while guaranteeing an excellent robustness to PVT variations. With the use of only 10 MOS devices (for both OTA and SR), a TIA with excellent performance and insensitive to PVT variations has been designed, minimizing also area footprint.

Appendix

In this Appendix we analyze the distortion of a transimpedance amplifier that exploits a nonlinear OTA and a nonlinear feedback element R_F. We refer to Figure 3, where the transfer functions of the OTA and of the feedback element can be expressed as

$$V_o \cong -\alpha_1 V_i - \alpha_2 V_i^2 - \alpha_3 V_i^3 \tag{10}$$

$$i_F \cong \frac{1}{R_F}(V_R + \gamma_2 V_R^2 + \gamma_3 V_R^3) \tag{11}$$

where V_R=V_o-V_i.

Assuming infinite input impedance for the OTA, current equilibrium at the input node provides

$$i_{in} + i_F = C_{in}\frac{dV_i}{dt}. \tag{12}$$

Let i_{in} be a sinusoidal signal

$$i_{in} = I_{pk} sin(\omega t); \tag{13}$$

due to the nonlinear transfer functions, the voltages V_i and V_o will contain harmonic components and can be expressed in the form

$$V_i = \sum A_i \, sin(i\omega t + \varphi_i) \quad V_o = \sum B_i \, sin(i\omega t + \theta_i) \tag{14}$$

where the A_i and B_i are related through (10).

Eq. (12) thus becomes a set of equations for each harmonic component; considering only the first three harmonics, moderate distortion levels and low frequency, so that the effect of capacitor C_{in} can be neglected, we obtain for the harmonic components of the output voltage:

$$B_1 \cong -R_F I_{pk} \tag{15a}$$

$$B_2 \cong \frac{\gamma_2}{2} B_1^2 \tag{15b}$$

$$B_3 \cong -\frac{1}{2}\left(\frac{\gamma_3}{2} + \gamma_2^2\right) B_1^3. \tag{15c}$$

Eqs. (15) show that the distortion on the output voltage is mainly due to the nonlinearity of the feedback element.

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