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A New Fully Closed-Loop, High-Precision, Class-AB CCII for Differential Capacitive Sensor Interfaces

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Abstract: The use of capacitive sensors has advantages in different industrial applications due to their low cost and low-temperature dependence. In this sense, the current-mode approach by means of second-generation current conveyors (CCIIs) allows for improvements in key features, such as sensitivity and resolution. In this paper, a novel architecture of CCII for differential capacitive sensor interfaces is presented. The proposed topology shows a closed-loop configuration for both the voltage and the current buffer, thus leading to better interface impedances at terminals *X* and *Z*. Moreover, a low power consumption of 600 µW was obtained due to class-AB biasing of both buffers, and the inherent drawbacks in terms of linearity under the mismatch of class-AB buffering are overcome by its closed-loop configuration. The advantages of the novel architecture are demonstrated by circuit analysis and simulations; in particular, very good robustness under process, supply voltage and temperature variations and mismatches were obtained due to the closed-loop approach. The CCII was also used to design a capacitive sensor interface in integrated CMOS technology, where it was possible to achieve a sensitivity of 2.34 nA/fF, with a full-scale sensor variation of 8 pF and a minimum detectable capacitance difference of 40 fF.

Keywords: CCII; class-AB; sensor applications; low-power circuits

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1. Introduction

Nowadays, capacitive sensors can be considered a leading technology since they show inherent benefits for different kinds of measurements [1,2]. They are extremely versatile and can be realized in different ways, allowing their use in many applications [3–7]. In fact, capacitance variation can be obtained either by changing the capacitor geometry acting on the surface of the plates, or by shifting them, changing the overlapping area, or modifying the plates' distance. Another solution may rely on the modification of the permittivity of the considered dielectric material, and this, for instance, also allows chemical changes in material compositions or physical parameters to be sensed [8].

Further advantages are the integration capability, the low-temperature dependance and the low cost, which make these kinds of sensors suitable for different industrial applications and uses. They can be employed, for instance, as accelerometers [9,10], pressure or moisture sensors [11,12], movement sensors [13] and concentration sensors [14]. Furthermore, no particular constraints can be found on sensor dimensions since, in principle, custom geometries and structures can be used for each application. However, miniaturization is a straightforward alternative, especially in many modern systems, in the form of integrated on-chip solutions. Moreover, capacitance variation, and so the dynamics of

the sensor, can be easily defined and managed for the considered applications without particular criticism.

Among capacitive sensors, it is important to consider the differential ones, which are of particular interest since they show improved performance when used for the detection of low capacitance variations or in critical systems with interferences, providing even more robust sensing [15–18].

It is evident that, in this context, a critical role is played by the sensor interface, which should be easily integrated with the capacitive sensor and should be able to exploit sensor performance [19–28]. Different solutions have been provided in the literature, especially in recent years. Two main categories can be defined among capacitive sensor interfaces: the first one is represented by standard interfaces, without any compensation, which simply transduce the sensing parameter [19–21,25,26,28], while the second one collects interfaces that are able to compensate for parasitics by reducing the measurement error [22–24,27]. Moreover, an additional classification can be defined by considering the design approach, and, in particular, we can take into account both current-mode (CM) [23,25,27,28] and voltage-mode (VM) solutions [19–22,24,26,29].

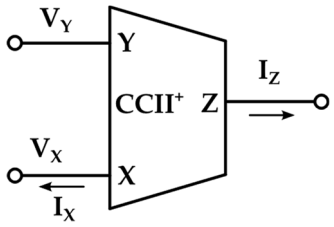
One of the main drawbacks when considering a VM approach is that, especially in highly integrated low-pitch technologies, it is difficult to achieve good sensitivity, resolution and signal-to-noise ratios due to the narrow supply voltage rail, hence the intrinsically reduced voltage swing per variation that is to be measured. However, the current-mode approach could easily overcome this limitation; therefore, it represents an increasingly attractive methodology. One of the most famous CM active building blocks (ABBs) is the second-generation current conveyor (CCII), which inherits and expands the functionalities of its predecessor, the first-generation current conveyor (CCI) [30–39].

In this paper, we propose a completely novel architecture that implements a CCII especially designed for sensor interfacing applications. Favorably, the ABB uses a double IC-level feedback path, both for the voltage and the current subsections of the CCII, which allows for an improvement in the performance of the current buffer section and its robustness to process, supply voltage and temperature (PVT) variations and mismatches. In particular, the closed-loop configuration desensitizes circuit behavior from variations in component parameters, allowing stable performance under the variations, and mitigates the inherent drawbacks in terms of the linearity of the class-AB current buffer, allowing both low power and good linearity even under device mismatches. The proposed CCII was tested in a differential capacitive sensor exploiting the CM approach, and a sensitivity of 2.34 nA/fF with a full-scale sensor variation of 8 pF was achieved.

This manuscript is structured as follows: Section 2 introduces the proposed topology and shows its high-level working principle. Section 3 shows the IC-level in-depth analysis of the circuit, offering specific considerations for the differential capacitive sensor application. Section 4 presents the main simulation results and a comparison with the literature. In Section 5, conclusions are drawn.

2. The Proposed Topology

The CCII is a three-port network, as shown in Figure 1, and in the ideal case, it is characterized by the equations $V_X = \alpha\ V_Y$, with $\alpha = 1$, and $Iz = \beta\ Ix$, with $\beta = 1$; i.e., it is ideally composed of a voltage buffer between terminals Y and X and a current buffer between terminals X and Z. Closed-loop architectures are usually employed for the former, resulting in an accurate voltage gain α, wide bandwidth and low distortion, whereas a current mirror is typically employed for the current buffer since it naturally provides a wide bandwidth [30]. This, however, results in gain error on the current gain β, especially in low-voltage designs with deep submicron devices that present a low-output resistance, and in some nonlinearity in the current buffering action.



$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

Figure 1. CCII$^+$ schematic symbol and matrix representation of an ideal CCII.

To deal with this problem, we implemented the proposed CCII topology, which exploits closed-loop architectures for both the voltage buffer and the current buffer, improving gain precision even under PVT variations. Moreover, the linearizing effect of the feedback allows class-AB topologies to also be used for the current buffer, resulting in a fully class-AB CCII topology, which can be useful in low-power applications.

The proposed CCII topology is shown in Figure 2 for the case of a non-inverting CCII (CCII$^+$). The inverting topology (CCII$^-$) only requires the way in which R_{SX} is connected to the left differential difference amplifier (DDA) inputs to be inverted. We provide a detailed analysis of this topology in Section 3, while in this section, we provide insights into its operation.

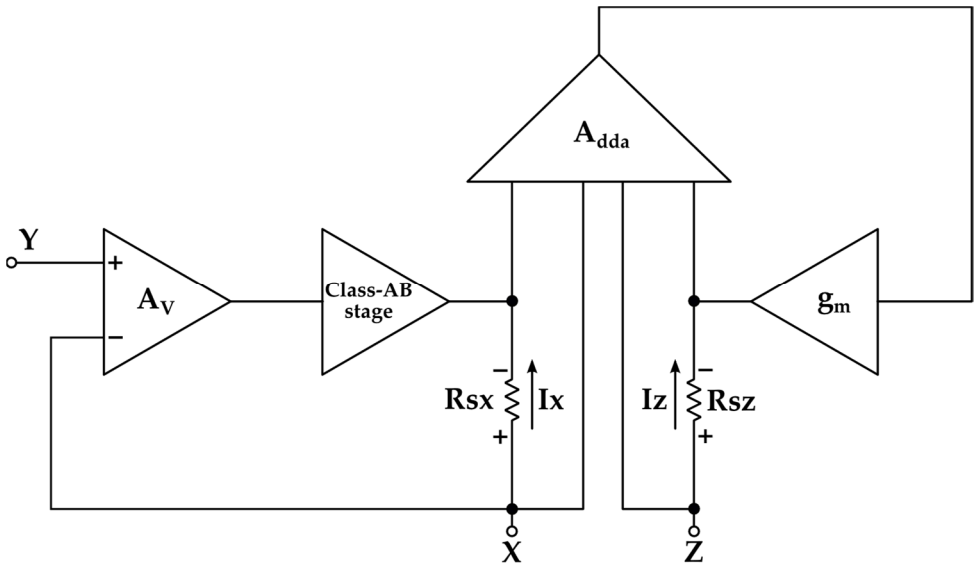


Figure 2. The proposed CCII at block scheme level for a non-inverting topology.

The voltage transfer function from node Y to node X must have an ideal unitary voltage gain, and this is ensured by voltage feedback, which also provides a high impedance at node Y and a low impedance at node X, thus amplifying the input error voltage $V_Y - V_X$ of the operational amplifier (A_V), which drives a class-AB output stage with low-output impedance. Hence, the system inherently has high-input impedance and low-output impedance, while voltage feedback additionally improves both impedances. Furthermore, the output class-AB stage allows high power efficiency by providing large output currents at node X with a limited quiescent current. Linearity in the voltage transfer function is finally improved by feedback. The open-loop gain of the stage mostly depends on the operational amplifier A_V. The input common-mode signal swing of the operational amplifier and the output signal swing of the output stage set the maximum and minimum voltages at nodes X and Y, respectively, as $V_X = V_Y$ when the system operates correctly. Hence, large voltage swing operation is possible if the output stage and operational amplifiers are suitably designed, whereas the output current is limited by the (class-AB) output stage so that low-impedance high-current loads at node X can also be efficiently driven.

The operation of the voltage transfer function is straightforward, as its topology, composed of an operational amplifier and a class-AB output stage, is conventional. The only difference is the presence of the resistor R_{SX}, which has some impact on the open-loop frequency response of the stage (as shown in Section 3). This resistor is necessary to sense the current flowing at node X and, thus, to obtain $R_{SX} = R_{SZ}$, the unity-gain current transfer function between nodes X and Z. The current transfer function is achieved by a novel class-AB architecture, which ensures high linearity and improved input and output impedances due to feedback. This is unlike conventional class-AB CCIIs, where a P-type current source, in parallel with an N-type current source, mirrors the push and pull currents at node X toward the output node Z, with an output impedance dependent on the topology of the current mirror (which is usually cascoded, if not gain-boosted, to maximize the output impedance).

The conventional approach (shown in Figure 3) to class-AB current buffering has a significant disadvantage in terms of linearity under mismatch variations. In fact, let us assume that the P-type current mirror has current gain $A_I^P \approx 1$ and that the N-type current mirror has current gain $A_I^N \approx 1$. When both gains are unitary, no problem occurs; when a current enters node X, the P-type current mirror provides less current, and the N-type provides more current. In ideal class-AB operation, the positive (inflowing) current at node X would be mirrored to node Z by the N-type mirror, and the negative (outflowing) current would be mirrored by the P-type mirror. Both the N-type and P-type mirrors would amplify the input current by $A_I^P = A_I^N = 1$ in the ideal case. However, especially under mismatch variations, both A_I^P and A_I^N will not be unitary, and, above all, they will change differently, because mismatches among P devices will be mostly uncorrelated to mismatches among N devices. Hence, linearity will be greatly reduced under mismatches, because the positive output current will be amplified by a factor other than the negative output current. In an ideal class-AB current mirror, where the positive and negative parts of the signal are separately amplified by the N-type and P-type current mirrors, we have the following: $I_Z = I_Z^P + I_Z^N = A_I^P I_X^P + A_I^N I_X^N = A_I^P \frac{(I_X + |I_X|)}{2} + A_I^N \frac{(I_X - |I_X|)}{2} = \frac{A_I^P + A_I^N}{2} I_X + \frac{A_I^P - A_I^N}{2} |I_X|$. Of course, the term $\frac{A_I^P - A_I^N}{2} |I_X|$ is heavily nonlinear and will be significant if large mismatches occur.

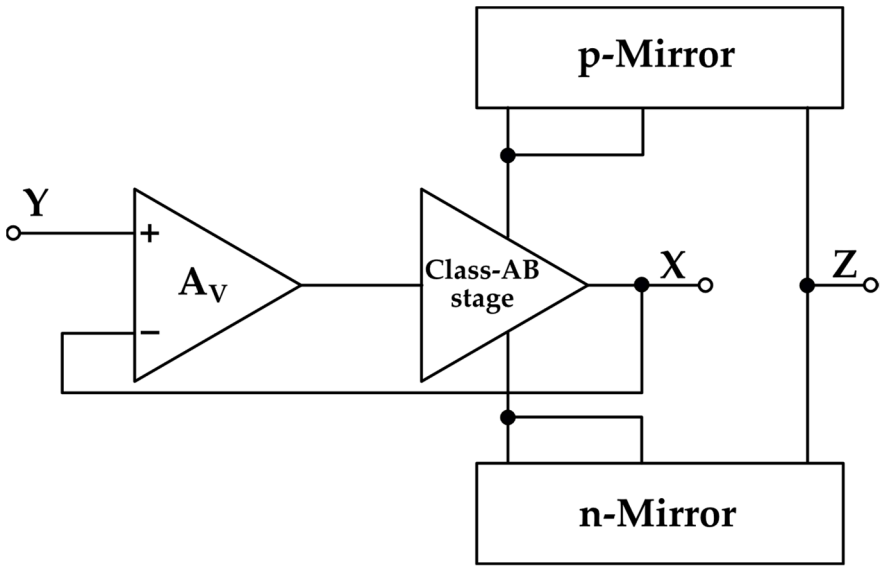


Figure 3. A block scheme showing the conventional approach for class-AB current buffering in CCII.

Because of this problem, in this work, we propose the closed-loop class-AB current mirror shown in Figure 2. The input current I_X is sensed by the resistor R_{SX}, so the left input of the DDA is fed by the input differential voltage $R_{SX} I_X$. However, the output current I_Z is sensed by the resistor R_{SZ}, so the right input of the DDA sees the differential

input voltage $R_{SZ}I_Z$. The feedback loop provided by the DDA and the class-AB output stage copies the current at node X to node Z by enforcing $R_{SZ}I_Z \approx R_{SX}I_X$. It also provides high output impedance at node Z, as the current at node Z is set by the current at node X, and, thus, node Z must have large impedance, as the current is insensitive to voltage variations. In order to prove this point, we consider Figure 4, where ideal current generators and current mirrors are assumed, so the equilibrium can only be reached when the currents of the output node are matched. Calling I_{Di}, i = 1, 2, 3, 4, the drain currents of the four NMOS devices of the differential pairs, counted from left to right, we have

$$I_{D1} = I_B + \frac{g_m R_{SX} I_X}{2},\ I_{D2} = I_B - \frac{g_m R_{SX} I_X}{2} \tag{1}$$

$$I_{D3} = I_B + \frac{g_m R_{SZ} I_Z}{2},\ \ I_{D4} = I_B - \frac{g_m R_{SZ} I_Z}{2}. \tag{2}$$

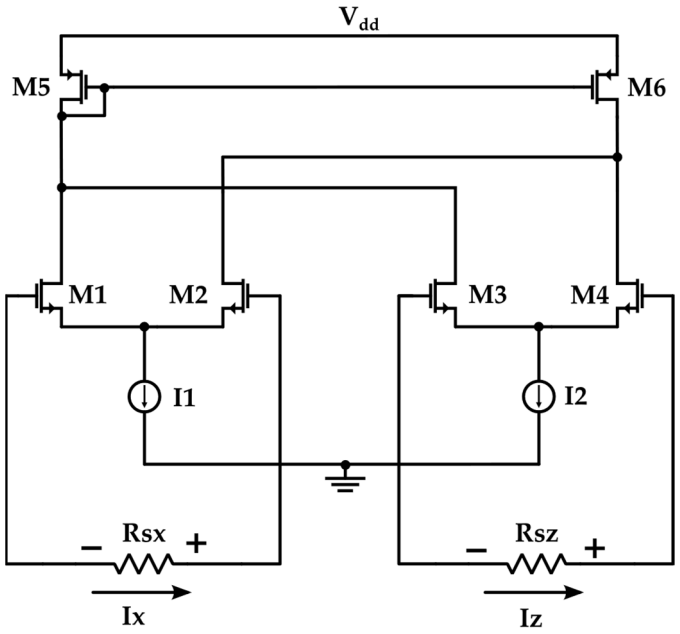


Figure 4. Simplified schematic of the DDA for current gain evaluation.

The equilibrium at the output node is given by

$$I_{D1} + I_{D3} = I_{D2} + I_{D4} \rightarrow 2I_B + \frac{g_m R_{SX} I_X + g_m R_{SZ} I_Z}{2} = 2I_B - \frac{g_m R_{SX} I_X + g_m R_{SZ} I_Z}{2} \tag{3}$$

Hence, in this ideal case,

$$g_m R_{SX} I_X + g_m R_{SZ} I_Z = 0 \rightarrow I_Z = -\frac{R_{SX}}{R_{SZ}} I_X = -I_X. \tag{4}$$

under the hypothesis of $R_{SX} = R_{SZ} = R_{sense}$.

The class-AB output stage ensures that a large output current can be provided at node Z. However, when the input current at node X is large, the input differential voltages at the two inputs of the DDA become large, as they are $R_{SX}I_X \approx R_{SZ}I_Z$, so it may happen that the DDA saturates with large input differential voltages. In order to avoid deep saturation, the maximum voltage across $R_{SX} = R_{SZ}$ must not be much larger than the linear range of the inputs of the DDA. Thus, the value of the sensing resistors must be set by taking into account the maximum currents at terminals X and Z. However, a linear voltage-to-current transfer function in the DDA is not required for linearity to the extent that the DDA ensures that $R_{SZ}I_Z$ is close to $R_{SX}I_X$; however, when close to saturation, the two differential pairs

of the DDA will show a limited gain, thus reducing the effectiveness of the feedback loop in ensuring good linearity.

The values of the sensing resistors R_{SX} and R_{SZ} have to be chosen by carefully weighing the trade-off among the maximum current, terminal impedances and noise, as shown by the simulations in Section 4.

3. Circuit Analysis

3.1. Analysis of the Proposed CCII

The proposed architecture of the current conveyor shown in Figure 2 has to be designed, at transistor level, by considering the ideal properties of a current conveyor; the negative feedback from both the Z and X outputs allows voltage gain α and current gain β to be obtained close to 1. If the same class-AB stage, showing voltage gain A_{Vbuf} and output resistance $1/g_m$, is used to design both the voltage buffer A_I and the transconductance stage G_m in Figure 2, the following expressions for α and β are found:

$$\alpha = \frac{A_V \cdot A_{Vbuf}}{1 + A_V \cdot A_{Vbuf}}, \tag{5}$$

$$\beta = \pm \frac{A_{DDA} \cdot A_{Vbuf} \cdot \frac{g_m R_{sense}}{1+g_m R_{sense}}}{1 + A_{DDA} \cdot A_{Vbuf} \cdot \frac{g_m R_{sense}}{1+g_m R_{sense}}}. \tag{6}$$

As can be seen from Equation (6), a sufficiently high value for R_{sense} has to be chosen in order not to degrade the gain of the current feedback loop too much.

At the same time, the feedback allows us to lower the impedance at the X node (R_X) and to enhance the one at the Z node (R_Z), as required, so that a very high R_Z/R_X ratio can be obtained:

$$R_X = \frac{R_{sense} + 1/g_m}{1 + A_V \cdot A_{Vbuf}}, \tag{7}$$

$$R_Z = (R_{sense} + 1/g_m) \cdot \left(1 + A_{DDA} \cdot A_{Vbuf} \cdot \frac{g_m R_{sense}}{1 + g_m R_{sense}}\right), \tag{8}$$

$$\frac{R_Z}{R_X} = \left(1 + A_V \cdot A_{Vbuf}\right) \cdot \left(1 + A_{DDA} \cdot A_{Vbuf} \cdot \frac{g_m R_{sense}}{1 + g_m R_{sense}}\right). \tag{9}$$

The presence of the R_{sense} resistor allows the open-loop impedance at node Z to be enhanced, but, unfortunately, it also increases the open-loop impedance at node X; if a given closed-loop R_X is specified, the gain of the voltage feedback loop and the value of R_{sense} have to be jointly designed in order obtain the required R_X value according to Equation (7). Then, the gain of both feedback loops (in terms of A_V, A_{DDA}, A_{Vbuf} and $1/g_m$) must be designed to be sufficiently high and, at the same time, to permit the desired R_Z/R_X ratio (>1000 in most practical cases). It has to be noted that the value of R_{sense} also affects the noise and linear range of the CCII, as shown in the simulation Section, thus making the choice of the most appropriate value even more critical.

3.2. Application as Differential Capacitive Sensor Interface

The proposed CCII can be applied in a differential capacitive sensor, whose architecture is shown in Figure 5. Two CCIIs, one inverting and the other non-inverting, were employed to sense the differential current passing through two capacitors, namely, C_0 and C_1, whose difference has to be measured. An input current generator provides a square wave with period T and amplitude I_{REF}, which is fed to the two capacitors (C_2 in Figure 6 represents parasitic capacitance at the input node). The input node voltage increases and decreases linearly with slope $I_{in}/(C_0 + C_1 + C_2)$; thus, there is a trade-off between the input current amplitude, the square wave period—related to the speed of the variation in the capacitance difference—and the average value of the capacitances C_0 and C_1 due to there being a limit on the maximum value that the input voltage can assume. The CCIIs buffer the currents

through the capacitors, and their output currents are summed on resistor R_3, providing the output voltage V_{out}. The output voltage during the positive cycle of the square wave is thus dependent on the capacitance difference $C_1 - C_0$, provided that the circuit operates in the linear region. As an alternative, current-mode processing can be adopted, with the output current read by some current input block (e.g., a current amplifier or a transimpedance amplifier); in this case, I_3 and R_3 in Figure 5 model the input of such a block. Techniques to compensate for the stray capacitance C_2 are discussed in [27] and are outside the scope of this paper.

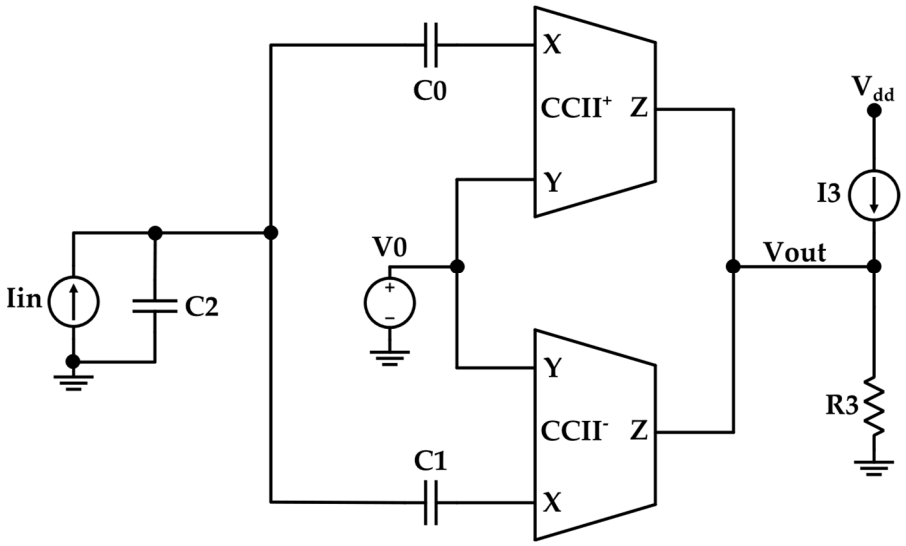


Figure 5. Block scheme and simulation setup for capacitive sensor interface.

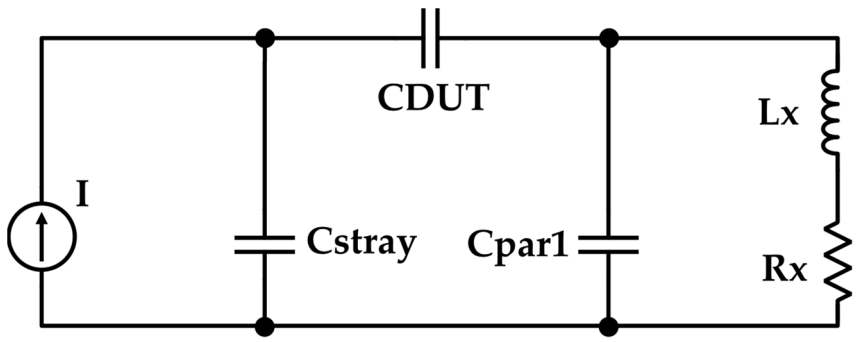


Figure 6. Input terminal model for a current-mode sensor interface based on the proposed CCII architecture.

The use of the proposed CCII scheme as a current-mode interface for capacitive sensors therefore also requires a more accurate analysis of parasitic capacitance at input node *X*. It can be seen that a parasitic capacitance C_{par1} at node *X* is found, given by the sum of the parasitic capacitance at the A_V- input and the parasitic capacitance at the negative A_{DDA} input. Moreover, a parasitic capacitance C_{par2} ($<C_{par1}$) is found at the positive A_{DDA} input. The expression for the overall input impedance at node *X*, Z_X, is the following:

$$Z_X = \frac{1}{sC_{par1}} || \, Z_X{}' \cong \frac{1}{sC_{par1}} || \, R_X, \tag{10}$$

where

$$Z_X' = R_X \cdot \left(1 + s \cdot \frac{C_{par2} R_{sense}}{1 + g_m R_{sense}}\right) = R_X + s \cdot L_X \cong R_X, \tag{11}$$

and

$$L_X = \frac{C_{par2} R_{sense} R_X}{1 + g_m R_{sense}}. \tag{12}$$

The parasitic capacitance C_{par2} creates a zero in the $Z_X{}'$ expression, and an equivalent inductance can be considered to account for its frequency behavior; particular care has to be paid during the design of the CCII, so the zero of $Z_X{}'$ is placed outside the range of the input frequencies used as a stimulus for the sensor interface. Under the previous hypothesis, the approximate expression in Equations (10) and (11) can be adopted.

In the general case, the model in Figure 6 has to be considered for the input terminal of the current-mode sensor interface. The stray capacitance C_{Stray} of the sensor (equivalent to half C_2 in Figure 5) has to be estimated in order to calibrate the measurement and improve accuracy. The following partition function α_{SENS} is found between the current stimulus I and the current I_{DUT} entering the sensor:

$$\alpha_{SENS} = \frac{C_{DUT}}{C_{DUT} + C_{Stray}} \cdot \frac{1 + s \cdot C_{par1} R_X (1 + s \cdot L_X / R_X)}{1 + s \cdot \left(C_{par1} + \frac{C_{DUT} C_{Stray}}{C_{DUT} + C_{Stray}} \right) R_X (1 + s \cdot L_X / R_X)}. \tag{13}$$

A second condition, concerning the time constant $\tau_1 = L_X / R_X$, has to be fulfilled in order to set the input bandwidth of the interface. Moreover, the time constant τ_2, given by

$$\tau_2 = R_X \cdot \left(C_{par1} + \frac{C_{DUT} C_{Stray}}{C_{DUT} + C_{Stray}} \right) \tag{14}$$

has to be suitably chosen in order to avoid limits in the input bandwidth of the sensor interface.

4. Simulation Results of a Sensor Design Case Study

Both inverting and non-inverting CCIIs based on the proposed approach were designed and simulated using the Cadence software suite, in a 130 nm CMOS technology from STMicroelectronics, in order to develop a current-based sensor interface for differential capacitance [25] based on the architecture described in Section 3.2 [28]. The two feedback loops were designed with an overall voltage gain of about 40 dB for the cascade of the block A_V (or DDA) and buffer. In Figure 7, the transistor implementation of the CCII$^+$ stage is shown. The current mirrors were designed to bias the A_V stage with a 29.9 µA tail current (M3), the DDA stage with a 14.9 µA tail current (M30, M31) and the class-AB stages with 68.8 µA (M7, M21) and 39.7 µA (M13, M26) tail currents. The overall power consumption from a 1.2 V supply voltage is about 600 µW. The transistor sizes are reported in Table 1.

Table 1. CCII$^+$ transistor dimensions.

Transistor	Dimensions (W, L)
M1, M2	43.2 µm, 3.1 µm
M3, M4	86.4 µm, 3.1 µm
M5, M6, M19, M20	14.4 µm, 3.1 µm
M7, M9, M21, M23	576 µm, 1.6 µm
M8, M22	36 µm, 0.2 µm
M10, M24	144 µm, 0.2 µm
M11, M25	144 µm, 0.3 µm
M12, M13, M26, M27	576 µm, 3.1 µm
M14, M28	576 µm, 0.3 µm
M15, M16, M17, M18	21.1 µm, 3.1 µm
M29, M30, M31	42.2 µm, 3.1 µm

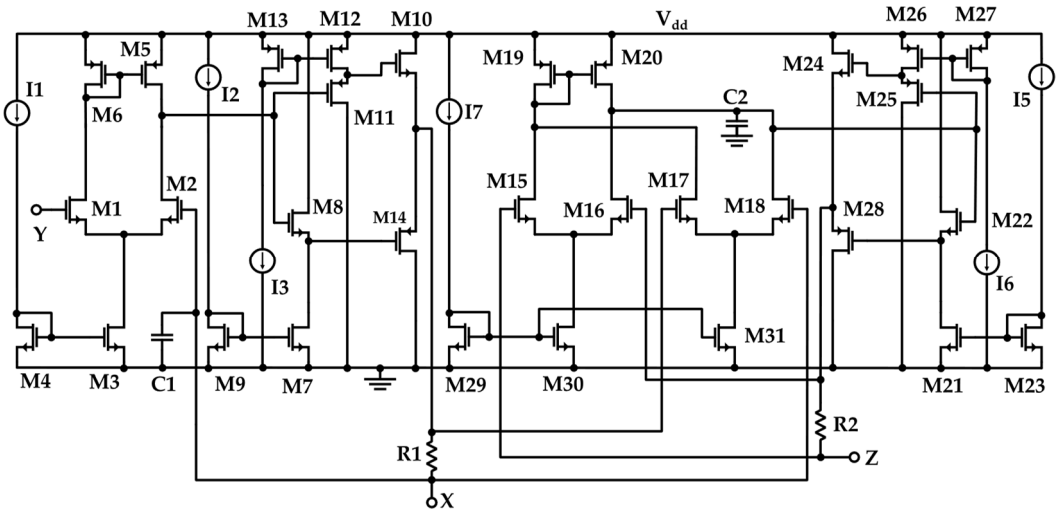
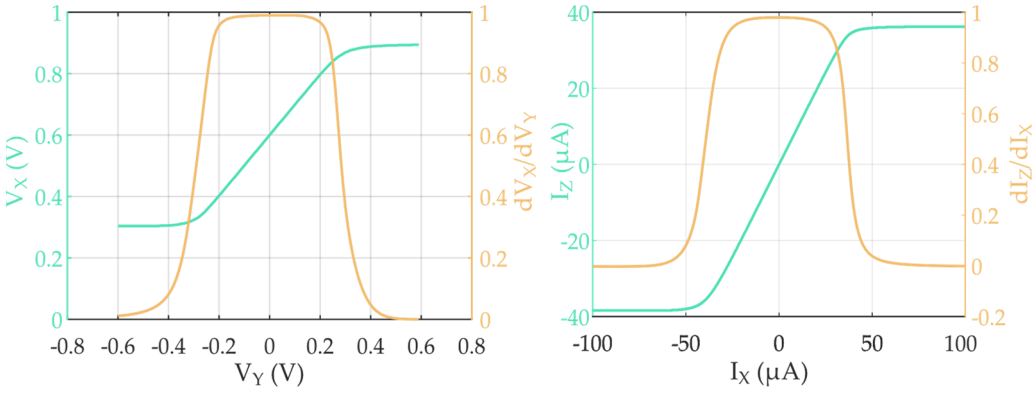


Figure 7. Transistor-level implementation of the proposed class-AB CCII$^+$.

To evaluate the effect of the sensing resistor on CCII performance, simulations for two different values of R_{sense} are reported. When R_{sense} is set to 5 kΩ, the DC transfer functions shown in Figure 8 are achieved. The input range at terminal Y is about ±250 mV, and the current range is about ±30 µA, limited by the input voltage range of the DDA. The corresponding small-signal performance is reported in Figure 9, and it shows small gain errors with bandwidths of 12 MHz and 12.8 MHz for the voltage and current buffers, respectively. In particular, the value of R_{sense} allows a loop gain of 47.5 dB to be achieved, resulting in a closed-loop current gain of about −0.2 dB. Figure 10 reports the impedances at the terminals of the CCII, highlighting a ratio of impedances at Z and X terminals larger than 1000 and up to 100 kHz.



(**a**) (**b**)

Figure 8. DC performances of the α (**a**) and the β parameters (**b**) for R_{sense} = 5 kΩ.

The modeling inductor L_X defined in Section 3.2 is equal to 99.7 µH. Capacitive behavior can be seen at high frequencies for Z_X; from the graph in Figure 10, the value C_X = 0.9 pF is evaluated. Finally, analysis of the Z_Z graph allows the definition of a modeling capacitance C_Z = 3.5 pF.

In Figure 11, the input equivalent noise current at terminal X and the noise voltage at terminal Y are reported: an input equivalent noise voltage V_{NY} = 11.5 nV/$\sqrt{\text{Hz}}$ at terminal Y and an input equivalent noise current I_{NX} = 5.3 pA/$\sqrt{\text{Hz}}$ at terminal X can be observed at 1 MHz.

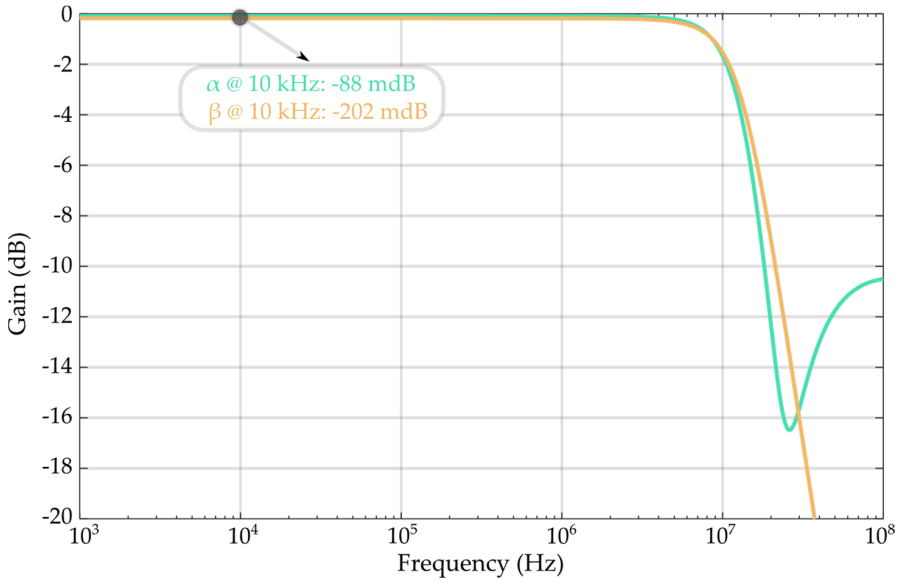


Figure 9. Simulated voltage (green curve) and current (gold curve) gain of the CCII for R_{sense} = 5 kΩ.

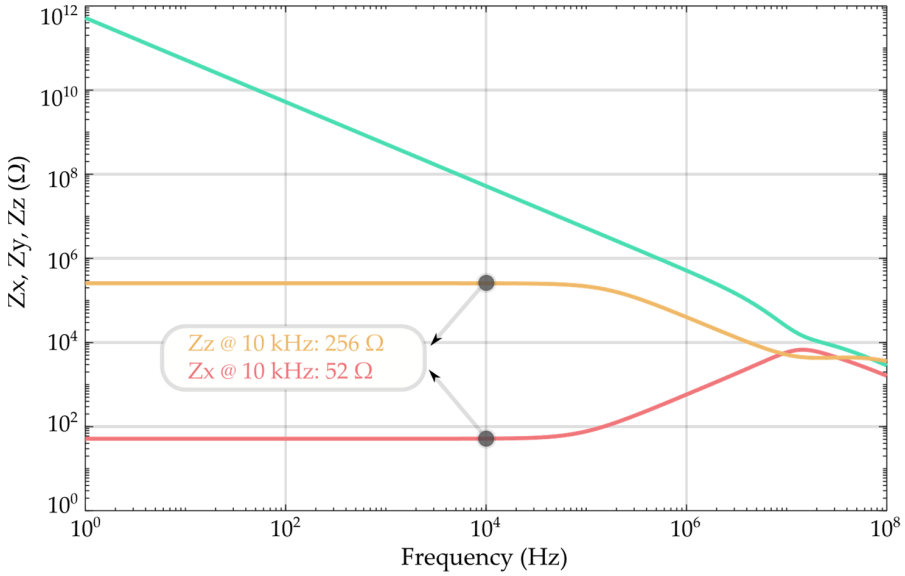
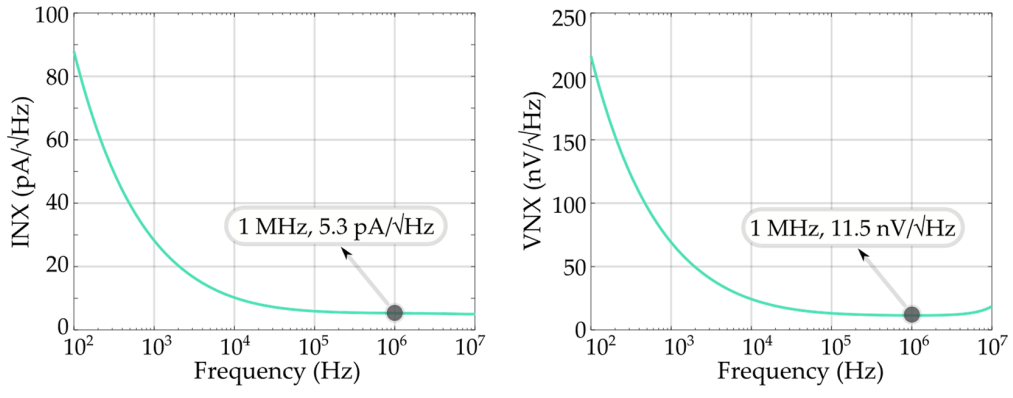


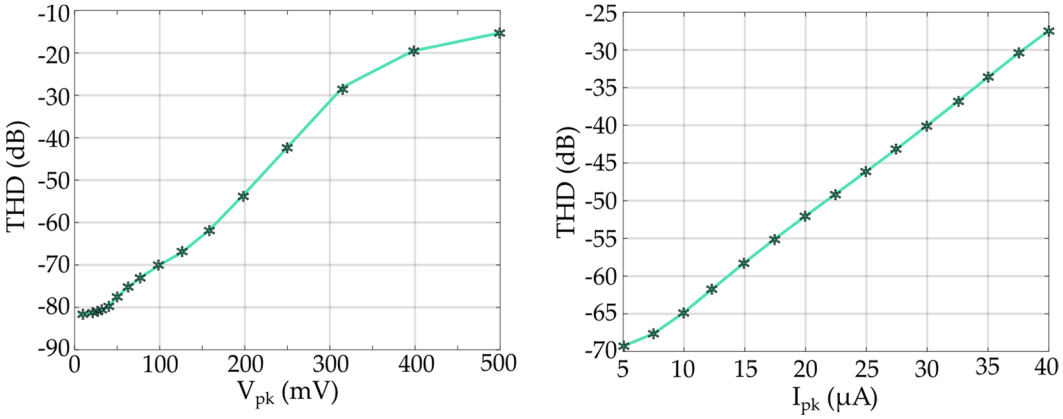
Figure 10. Impedance at terminal *X* (red curve), *Y* (green curve) and *Z* (gold curve) for R_{sense} = 5 kΩ.



(**a**) (**b**)

Figure 11. Equivalent noise current at *X* (**a**) and noise voltage at *Y* (**b**) for R_{sense} = 5 kΩ.

Linearity was evaluated by testing both the voltage buffer and the current buffer with a 100 kHz sinusoidal input, and Figure 12 reports the total harmonic distortion (THD) versus the input amplitude. The relatively large value of R_{sense} leads to significant distortions of the current buffer for currents in the range of tenths of µA, with −40 dB THD achieved at 30 µA. From this point of view, this choice of sensing resistor seems appropriate when a relatively large load resistance at the *X* terminal is used.



(**a**) (**b**)

Figure 12. Total harmonic distortion vs. input amplitude for the voltage (**a**) and current buffers (**b**) for R_{sense} = 5 kΩ.

The simulations were repeated in the case R_{sense} = 500 Ω, and the main performance parameters for both of the designs are reported in Table 2. Scaling the sense resistors obviously directly impacts the terminal impedances; in particular, a lower sense resistor results in a lower R_X, which is an advantage in many applications, but also a lower R_Z. The ratio of terminal resistances remains approximately constant. The loop gain of the feedback in the current buffer reduces to 31.5 dB, allowing a closed-loop gain β of about −0.27 dB.

Table 2. Comparison of CCII+ simulation performance to published results.

Item	This Work		[31]	[32]	[33]	[34]	[35]	[36]	[37]	[38]
	R_{sense} = 5 kΩ	R_{sense} = 0.5 Ω								
CMOS tech. (µm)	0.13		0.35	0.18	0.18	0.18	0.18	0.18	0.13	0.35
Power supply (V)	1.2		±0.75	±0.75	±1	±0.5	1.0	±0.75	1.5	±0.75
Power diss. (mW)	0.605		0.118	0.27	-	120	0.4	0.23	1.5	0.00015
Y Input range (V)	±0.250		-	±0.75	±0.4	±0.24	±1.0	±0.75	1.5	-
X Input range (µA)	±30	±225	-	±125	±350	±24	±1000	±220	±20	-
DC-α (dB)	−0.088	−0.088	0	0.009	−0.464	−0.087	0	0	−0.005	−0.04
f_{-3dB} of α (MHz)	12	18.6	10.5	1200	3340	36	25.7	3000	94	4.2
DC-β (dB)	−0.181	−0.271	0	0	0	−0.141	0	0	−0.130	−0.82
f_{-3dB} of β (MHz)	12.8	17.6	10.5	1200	4370	30.2	30	2960	99	4.4
R_X (Ω)	51	7.8	13	2.4	169	137	-	8.26	200	52
R_Z (kΩ)	256	25.8	2600	-	6.81	225	-	46.5	560	700
C_Y (pF)	0.305	0.305	0.5	0.004	0.164	3×10^{-6}	-	0.012	10	0.5
I_Z THD (dB)	−46.4 @225 mV 100 kHz	−46.4 @225 mV 100 kHz	-	-	−52.4 @300 mV 1 MHz	-	-		-	-
V_X THD (dB)	−46.1 @25 µA 1 kHz	−46.1 @200 µA 1 kHz	-	-	−47.7 @300 µA 1 MHz	-	-		−35 @10 µA 1 kHz	-

A lower series resistance results in a wider linear range for the current buffer, as shown by the DC transfer curve in Figure 13a, but also in a higher equivalent noise current at terminal *X* (about 48.4 pA/$\sqrt{}$Hz at 1 MHz). The plot of THD versus peak input current for a

100 kHz sinusoidal input is reported in Figure 13b. The voltage buffer results were practically unaffected by the value of R_{sense}, apart from the value of the resistance at node *X*.

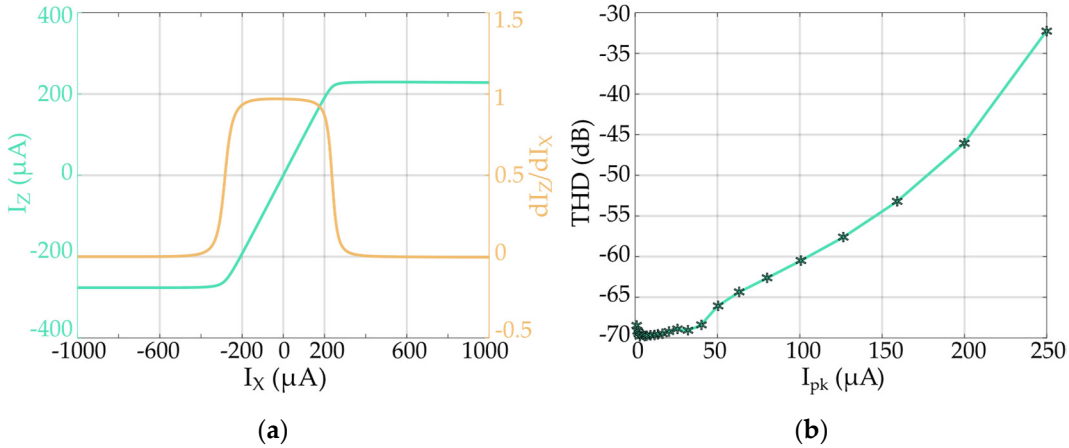


Figure 13. DC performance (**a**) and THD vs. input amplitude (**b**) of the current buffer for R_{sense} = 500 Ω.

Analysis of the CCII$^+$ performance under process, voltage supply and temperature (PVT) variations was carried out, together with a Monte Carlo analysis involving process variations and mismatches at 27 °C and nominal voltage supply. Tables 3 and 4 report the results for the case of R_{sense} = 5 kΩ (similar results were obtained at 500 Ω). Table 3 shows a very low variation in the current gain under PVT variations: this good result is due to the use of a closed-loop approach for the current buffer, where feedback is employed to desensitize the performance from variations in the open-loop gain. Analogously, the Monte Carlo results reported in Table 4 show a very good stability of the gain and distortion. This is in contrast with the results typically achieved in class-AB CCIIs with an open-loop current buffer, where distortion under mismatch is much worse than that obtained in typical conditions [39]. Histograms for the current gain and the THD of the current buffer for a peak input current of 25 μA are reported in Figure 14 to better highlight the advantage of the proposed approach.

Table 3. Analysis of CCII$^+$ performance under PVT variations.

Item	Temperature		Supply		FF	FS	SF	SS
Temperature (°C)	0	70	27	27	27	27	27	27
Power supply (V)	1.2	1.2	1.14	1.26	1.2	1.2	1.2	1.2
Power diss. (mW)	585	639	572	640	631	605	607	583
DC-α (dB)	−0.085	−0.093	−0.095	−0.082	−0.086	−0.103	−0.084	−0.090
f_{-3dB} of α (MHz)	12.7	11.1	11.9	12.1	12.5	12.1	11.9	11.5
DC-β (dB)	−0.177	−0.193	−0.191	−0.173	−0.180	−0.230	−0.171	−0.184
f_{-3dB} of β (MHz)	13.7	11.7	12.6	13	13.5	13.0	12.7	12.1
R_X (Ω)	51.4	53.9	53.3	50.2	52.3	66.2	48.3	51.4
R_Z (kΩ)	268	233	237	270	259	219	272	250
I_Z THD (dB)	−46.2	−45.7	−42.1	−53.2	−50.2	−36.9	−37.5	−42.5
V_X THD (dB)	−44.1	−47.5	−44.3	−46.9	−46.1	−38.1	−44.4	−45.2

The proposed CCII was also used to simulate the differential capacitive sensor in Figure 5. Given the 3 dB bandwidth of the CCII, we chose a frequency of 2 MHz for the input square wave current. The peak value of such a current has to be determined according to the average value C_{DUT} of the capacitances; for C_{DUT} = 4 pF, limited by stability considerations, a peak current of 20 μA was chosen. The CCII was sized with sensing resistors R_{sense} = 500 Ω as a trade-off between speed, terminal impedances and noise.

Table 4. CCII$^+$ performance under a 1000-iteration Monte Carlo analysis.

Item	Mean	Std
Power diss. (mW)	0.606	0.0018
DC-α (dB)	−0.087	0.0002
f_{-3dB} of α (MHz)	12	0.04
DC-β (dB)	−0.181	0.043
f_{-3dB} of β (MHz)	12.8	0.05
R_X (Ω)	51.6	0.12
R_Z (kΩ)	246	16.5
I_Z THD (dB)	−46.4	0.13
V_X THD (dB)	−45.1	1.3

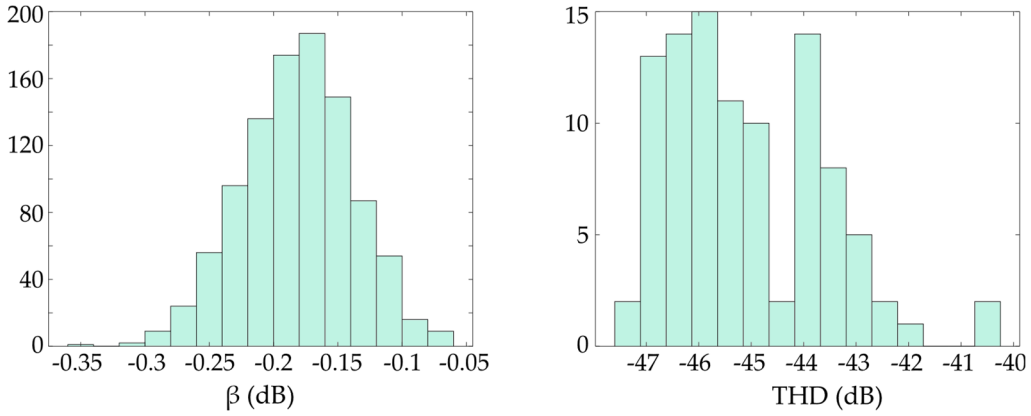


Figure 14. Histograms of the current gain β (**a**) and the THD of the current buffer for a peak input current of 25 µA (**b**) for 1000 Monte Carlo mismatch iterations (R_{sense} = 5 kΩ).

Figure 15 reports the resulting characteristic of the sensor (output current in the positive period of the square wave vs. capacitance difference), which shows very good linearity for the whole range of variations in the capacitance (C_0, $C_1 = C_{DUT} \pm \Delta C/2$, with C_{DUT} = 4 pF) and allows a sensitivity of about 2.34 nA/fF to be estimated. Transient noise simulations allow us to estimate an output noise current of 94 nA rms, corresponding to a minimum detectable ΔC of 40 fF.

Table 5 reports the main performance parameters of the sensor and compares them with similar reports in the literature. To allow an easy comparison between different implementations, the following figure of merit is defined:

$$FOM = \frac{BW}{Pd}\frac{\Delta C_{max}}{\Delta C_{min}} \tag{15}$$

where the bandwidth BW is calculated as half of the clock frequency and the minimum ΔC is obtained from noise and sensitivity values, if not explicitly declared in the papers. While the best FOM is achieved by the sensor in [27], which uses very simple circuits for the readout, the proposed sensor, which has not been optimized for noise, shows interesting results regardless, allowing a large bandwidth and a large C_{DUT} at the same time.

Table 5. Comparison to published results of capacitive sensor interfaces.

Item	This Work *	[23] *	[27]	[28]	[29] *
CMOS tech. (μm)	0.13	0.35	0.065	0.8	0.18
Sensor type	Differential	Differential	Differential	Single ended	Differential
Power supply (V)	1.2	±1.65	2.5	5	1.8
Power diss. (mW)	1.2	5.6	0.22	0.725	0.04
Bandwidth (kHz)	1000	50	500	290	50
Sensitivity	2.34 nA/fF	6.1 mV/pF	5 nA/fF	1.2 nA/fF	N.A.
Full-scale ΔC (pF)	8	20	1.8	1	0.01
Minimum ΔC (fF)	40 **	N.A.	0.8	N.A.	0.23 **
Conversion type	C-I	C-V	C-I	C-I	C-V
$\Delta C_{max}/\Delta C_{min}$	200	N.A.	2250	N.A.	43.5
FOM (MHz/mW)	167	N.A.	5134	N.A.	54

* Simulated, ** estimated from noise data.

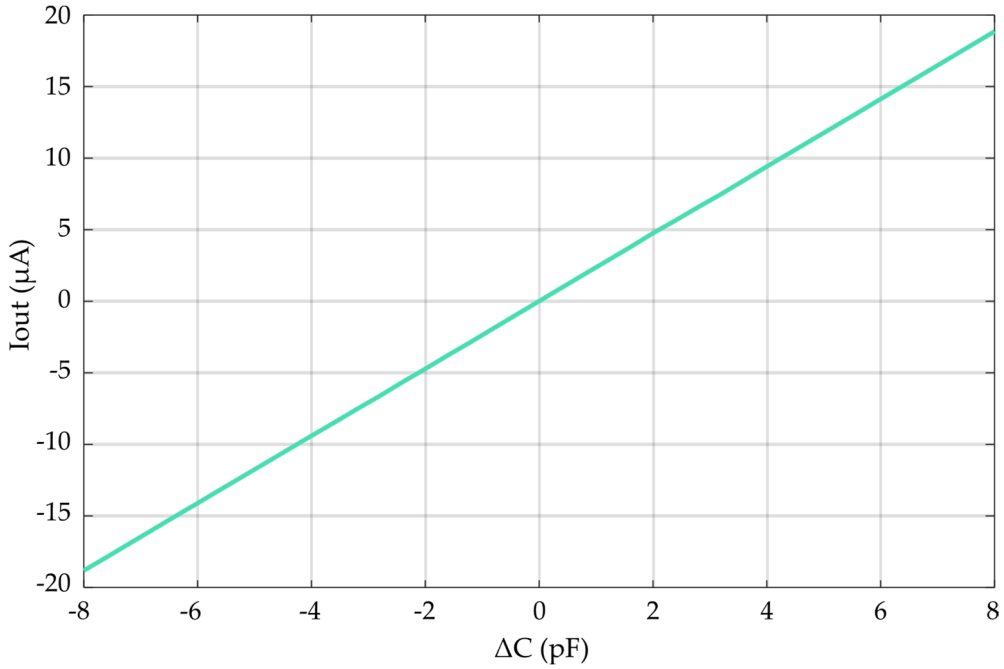


Figure 15. Characteristic of the differential capacitance sensor (C_{DUT} = 4 pF).

5. Conclusions

A novel architecture of a second-generation current conveyor, which also exploits a closed-loop feedback approach for the current buffer, was presented, thus combining the advantages of class-AB biasing with the linearizing and desensitizing effects of feedback. In addition to good linearity, very robust performance was in fact achieved under PVT variations and device mismatches due to the use of a unity-gain feedback loop for the X-Z transfer. Inverting and non-inverting CCIIs can be easily obtained by simply changing the sign of the differential voltage, thus maximizing the symmetry in applications where both conveyors are needed and have to be matched. Sensing resistors were employed to implement the current feedback loop, and their values can be optimized according to the required application by finding the desired trade-off between gain precision, bandwidth, linearity and noise.

A CCII was designed in a 130 nm CMOS technology by STMicroelectronics, and it was characterized for different values of the sensing resistors to highlight the trade-offs. PVT and Monte Carlo simulations showed very good robustness of the performance for both the voltage and current buffers. An inverting and a non-inverting CCII were employed to design and simulate a differential capacitive sensor interface that allows a high operating

frequency with large capacitive values and good linearity for a 100% variation in the capacitance.

Author Contributions: Conceptualization: P.M.; methodology: F.C., P.T., A.T.; software: P.T., G.B.; validation: F.C., P.M., G.F., V.S.; formal analysis: P.T.; investigation: F.C., P.M., P.T.; writing—original draft preparation: P.M., P.T., G.B., L.P.; writing—review and editing: F.C., G.F., L.P.; supervision: F.C., G.F., V.S. All authors have read and agreed to the published version of the manuscript.

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