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0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control

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Abstract: A two-stage CMOS transconductance amplifier based on the inverter topology, suitable for very low supply voltages and exhibiting rail-to-rail output capability is presented. The solution consists of the cascade of a noninverting and an inverting stage, both characterized by having only two complementary transistors between the supply rails. The amplifier provides class-AB operation with quiescent current control obtained through an auxiliary loop that utilizes the MOSFETs body terminals. Simulation results, referring to a commercial 28 nm bulk technology, show that the quiescent current of the amplifier can be controlled quite effectively, even adopting a supply voltage as low as 0.5 V. The designed solution consumes around 500 nA of quiescent current in typical conditions and provides a DC gain of around 51 dB, with a unity gain frequency of 1 MHz and phase margin of 70 degrees, for a parallel load of 1 pF and 1.5 MΩ. Settling time at 1% is 6.6 µs, and white noise is 125 nV/$\sqrt{Hz}$.

Keywords: feedback amplifier; analog; CMOS; bulk; class AB; low voltage

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1. Introduction

It is known that CMOS technology scaling, together with supply voltage reduction, is principally aimed at improving the performance of digital circuits and that, in this framework, the design of analog and mixed-signal blocks becomes increasingly demanding. It is indeed very difficult to obtain high linearity and high precision under near- and sub-threshold supply.

For this reason, operational transconductance amplifiers (OTAs) remain indispensable blocks for the implementation of high-accuracy closed-loop analog circuits, and several techniques have been proposed for the implementation of (ultra) low-voltage solutions. These include subthreshold-operated MOS transistors [1,2], bulk (body) driven [3,4], floating gate and quasi-floating gate MOS transistors [5,6], threshold lowering [7,8], level shifting [9], complementary pairs with body-driven gain boosting, and non-tailed pairs [10]. Additional approaches have also been proposed to replace OTAs, though not for general purpose usage, including dynamic amplifiers [11], ring amplifiers [12], and zero-crossing based circuits [13]. In addition, one interesting trend is the use of inverter-based topologies [14–28]. (A good review of the principal techniques for low-voltage OTAs can be found in the last reference.) At the basis of this approach is the single inverter (CMOS NOT gate), which is topologically simple, as it requires only two transistors between the supply rails, it provides a quite good voltage gain (though multi-stage topologies are usually required for 40 dB or more), and it exhibits class-AB and full swing operation. Therefore, it is rather effective under low supply voltages. However, the main drawback of the inverter-based solutions is related to the difficult control of the quiescent current feature that is especially required in low-power applications with a restricted current budget.

In this paper, a body-biasing technique, originally developed in [29] and utilized in [30], is applied to set the quiescent current of the generic inverter stage. Starting from this generic stage, a gate-driven, two-stage, inverter-based transconductance amplifier, suitable for switched-capacitor applications, is designed. Simulations results are also provided taking into account process and temperature variations. The proposed amplifier is designed in a 28-nm bulk process and is powered by a 0.5 V supply voltage. Typical quiescent current is 488 nA and, with a 1-pF//1.5-MΩ load, it provides 51-dB DC gain with a unity gain frequency of 1 MHz and phase margin of 70 degrees. Settling time at 1% is 6.6 µs and white noise is 125 nV/$\sqrt{Hz}$.

2. The Proposed Solution

Figure 1 shows the circuit schematic of the proposed amplifier. It consists of a first noninverting stage, made up of transistors M_1-M_6, and a second inverting stage, made up of transistors M_7-M_8. As it is seen, the second stage is a straight CMOS NOT gate while the first one is based also onto the NOT topology, but rearranged to invert the gain trough two complementary p-channel and n-channel current mirrors M_3, M_5 and M_4, M_6. In quiescent conditions, the input terminal is set to $V_{DD}/2$ and thanks to the overall negative feedback (not shown) also the output and intermediate node, *out1*, are all biased at $V_{DD}/2$.

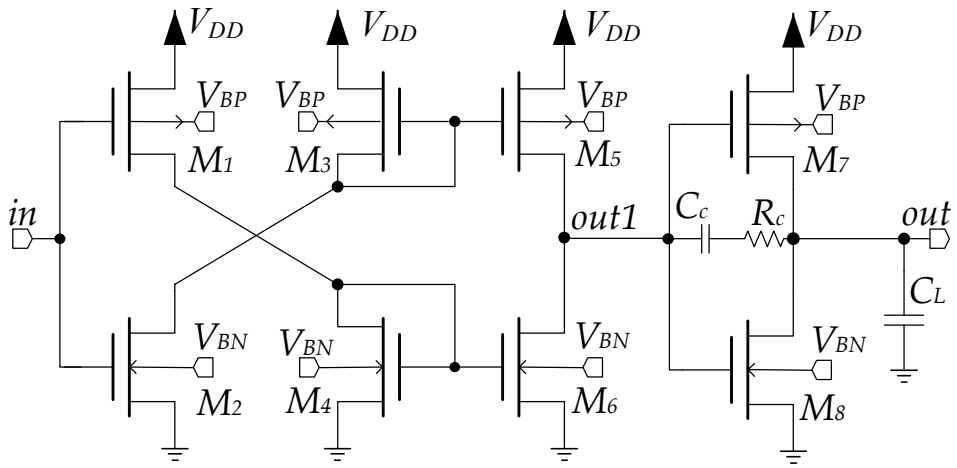

Figure 1. Simplified schematic of the proposed solution.

As far as the quiescent current control of the two stages is concerned, it is implemented through the bulk terminals via voltage V_{BP}, for p-channel transistors, and V_{BN}, for the n-channel ones. These voltages are generated by exploiting a technique proposed in [29] and utilized also in [10,30]. The basic working principle can be inferred with the aid of Figure 2, showing the simplified schematic of the amplifier's biasing section.

M_{R1} and M_{R2} are two reference transistors both with their $|V_{GS}|$ equal to $V_{DD}/2$. Their quiescent drain current is equal to I_{BIAS} thanks to the local feedback loop operated by the auxiliary amplifiers A_1 and A_2, which generate the required bulk voltages, V_{BP} and V_{BN}, under the following summarized constraints:

(a) assigned aspect ratios $(W/L)_{R1}$ and $(W/L)_{R2}$;
(b) $I_{D1,2} = kI_{BIAS}$, where k is the ratio of the transistors aspect ratio as in (1);
(c) $V_{SGR1} = V_{GSR2} = V_{DD}/2$;
(d) $V_{SDR1} = V_{DSR2} = V_{DD}/2$, assuming ideal input virtual short in A_1 and A_2.

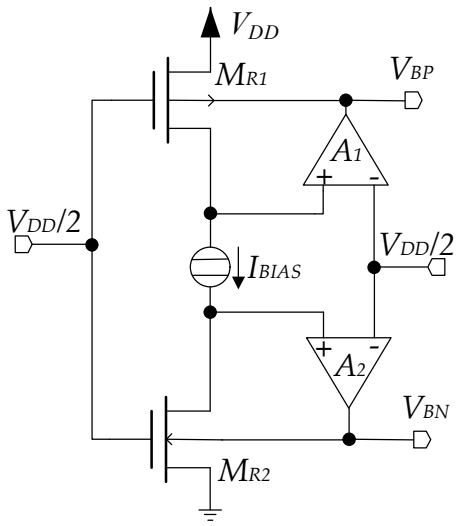

Figure 2. Simplified schematic of the biasing section generating V_{BN} and V_{BP} for the main amplifier in Figure 1.

Of course, aspect ratios of M_{R1} and M_{R2} must be set so that the required bulk voltages are within V_{DD} and ground. Moreover, the auxiliary amplifiers A_1 and A_2 should provide a maximum (rail-to-rail) output voltage range, whereas input common mode range is not a concern as input voltage is kept constant to $V_{DD}/2$. Therefore, simple two-stage OTAs biased in subthreshold can be profitably used. An example of implementation of this type of amplifier is found in [10], albeit operating with MOSFETs in saturation.

Consider now transistor M_1 of the main amplifier in Figure 1 and remember that in quiescent conditions *Vin* is equal to $V_{DD}/2$. As a consequence, M_{R1} and M_1 have respectively the same source, gate, and bulk voltage and hence the drain current of M_1 is related to that of M_{R1} in a mirror-like condition

$$I_{D1} = \frac{(W/L)_1}{(W/L)_{R1}} I_{BIAS} \tag{1}$$

where equality is accurately verified because the source-drain voltage of M_1 is also equal to $V_{DD}/2$, thanks to the diode-connected transistor M_4 in Figure 1 which absorbs I_{D1} and is designed so that

$$\frac{(W/L)_2}{(W/L)_{R2}} = \frac{(W/L)_1}{(W/L)_{R1}} \tag{2}$$

and consequently $V_{GS4} = V_{DD}/2$.

Similar considerations hold for all the transistors in the main amplifier, in practice, all p-channel and n-channel devices have their current linked to I_{BIAS} via the current-mirror-like relations

$$I_{Di\_P} = \frac{(W/L)_{i\_P}}{(W/L)_{R1}} I_{BIAS} \tag{3a}$$

$$I_{Dj\_N} = \frac{(W/L)_{j\_N}}{(W/L)_{R2}} I_{BIAS} \tag{3b}$$

where $(W/L)_{i\_P}$ (i = 1,3,5,7) and $(W/L)_{j\_N}$ (j = 2,4,6,8) are respectively the aspect ratios of the generic p-channel and n-channel MOSFET in the main amplifier.

As a concluding remark, closed loop stability is ensured thanks to the conventional frequency compensation network made up of the Miller capacitor, C_C, and nulling resistor, R_C, around the last inverting stage.

3. Validation Results

The proposed solution was designed in a 28-nm triple-well CMOS technology provided by STMicroelectronics and simulated at the schematic level. Threshold voltages of the n- and p-channel devices were 445 mV and −462 mV, respectively. Single power supply was set to 0.5 V, I_{BIAS} was 60 nA, and transistor dimensions, together with other component values, were set as summarized in Table 1. All p-channel (n-channel) MOSFETS are equal to the reference device 990/90 (210/90) nm/nm, except for the last stage transistors that have four times greater aspect ratios. This is important to increase the output current drive capability and the output transconductance to reduce the required value of the nulling resistor (to avoid introducing a positive zero), whose value is in the range of $1/g_{m2}$. Observe that the DC gain of the auxiliary amplifiers, A_1 and A_2, is around 40 dB. As a consequence of the transistor's dimension, the nominal quiescent current in each branch of the first stage is 60 nA, while it is 240 nA in the last stage, resulting in a total nominal quiescent current of 420 nA. The small-signal parameters of the amplifier stages are summarized in Table 2. Load capacitor C_L was 1 pF in parallel to a load resistor of 1.5 MΩ, and the compensation capacitor and the nulling resistor were set to 1.5 pF and 50 kΩ, respectively.

Table 1. Design parameters used in simulations.

Parameter	Value
V_{DD}	0.5 V
I_{BIAS}	60 nA
$(W/L)_{R1}$, $(W/L)_1$, $(W/L)_3$, $(W/L)_5$	990/90 nm/nm
$(W/L)_{R2}$, $(W/L)_2$, $(W/L)_4$, $(W/L)_6$	210/90 nm/nm
$(W/L)_7$	4 × (990/90) nm/nm
$(W/L)_8$	4 × (210/90) nm/nm
R_C, C_C	50 kΩ, 1.5 pF
A1, A2	40 dB
$C_L//R_L$	1 pF//1.5 MΩ
V_{DD}	0.5 V

Table 2. Small signal parameters of the amplifier.

Parameter	Value
g_{m1}	3.55 µA/V
r_{O1}	7.7 MΩ
g_{m2}	18.12 µA/V
r_{O2}	1.47 MΩ

The robustness of the quiescent conditions were validated at first. The nominal bulk voltages, V_{BP} and V_{BN}, generated by a circuit in Figure 2 were 256.4 mV and 231.9 mV, respectively. The simulated quiescent current in the main amplifier in Figure 1 was 488 nA, on average, with a standard deviation of 93.7 nA, after running 1000 Monte Carlo iterations. The difference with respect to the expected value of 420 nA is due to the low DC gains of the auxiliary amplifiers, which cause a closed-loop gain error.

Figure 3 shows the Bode plots (magnitude and phase) of the amplifier open-loop gain at the standard temperature (27 °C) and nominal component models with a 1-pF and 1.5-MΩ parallel load. DC gain is 51 dB, unity gain frequency (UGF) is 1 MHz and phase margin (PM) is 70 degrees. Note that the load resistance is almost equal to r_{o2} in Table 2, hence causing a 6-dB reduction in the maximum achievable gain.

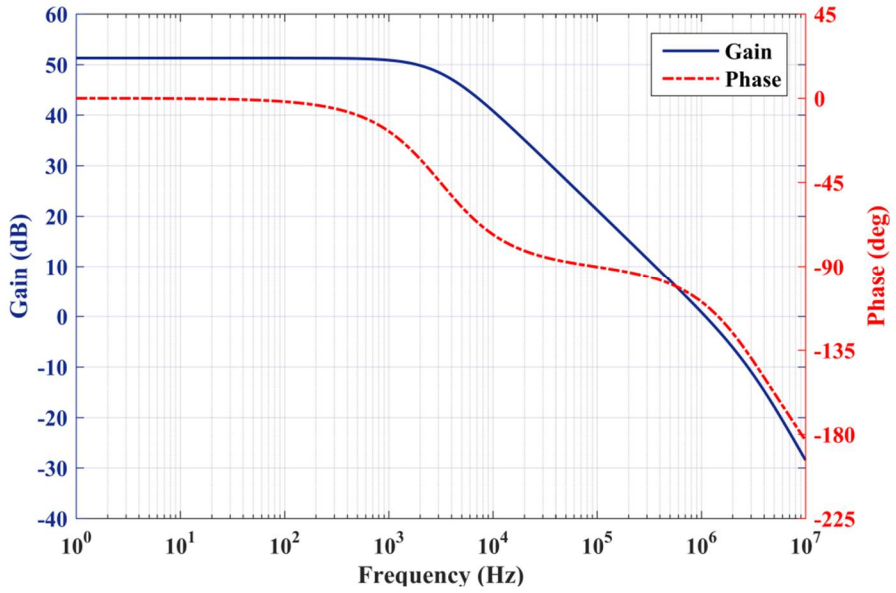

Figure 3. Bode plots (magnitude and phase versus frequency) of the amplifier open-loop gain with 1-pF and 15-MΩ parallel load.

Figure 4 shows the time transient response of the amplifier with the closed-loop gain set to −2. These plots are achieved with two feedback resistors, as in an inverting closed-loop amplifier topology, one of 1 MΩ (connected between the input and output) and the other of 0.5 MΩ (connected between the signal source and the input). The almost rail-to-rail output behavior is apparent. Positive/negative settling time at 1% of the final value is symmetrical and equal to 6.6 µs.

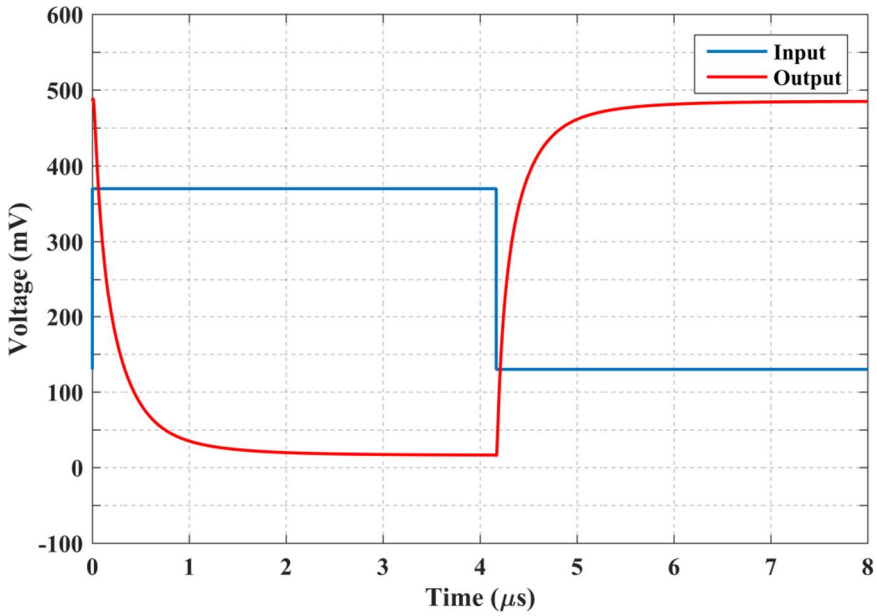

Figure 4. Time response to a 240-$mV_{p\text{-}p}$ input step (closed-loop gain is set to −2).

Power Supply Rejection Ratio was also evaluated from both supply rails. Magnitude versus frequency of PSRR is shown in Figure 5. $PSRR^+$ was 56 dB at DC, while $PSRR^-$ was 58 dB. Equivalent input noise is also simulated and depicted in Figure 6. The white component is 125 $nV/\sqrt{Hz}$ and is dominated by the voltage noise of transistors M1–M6 forming the input stage.

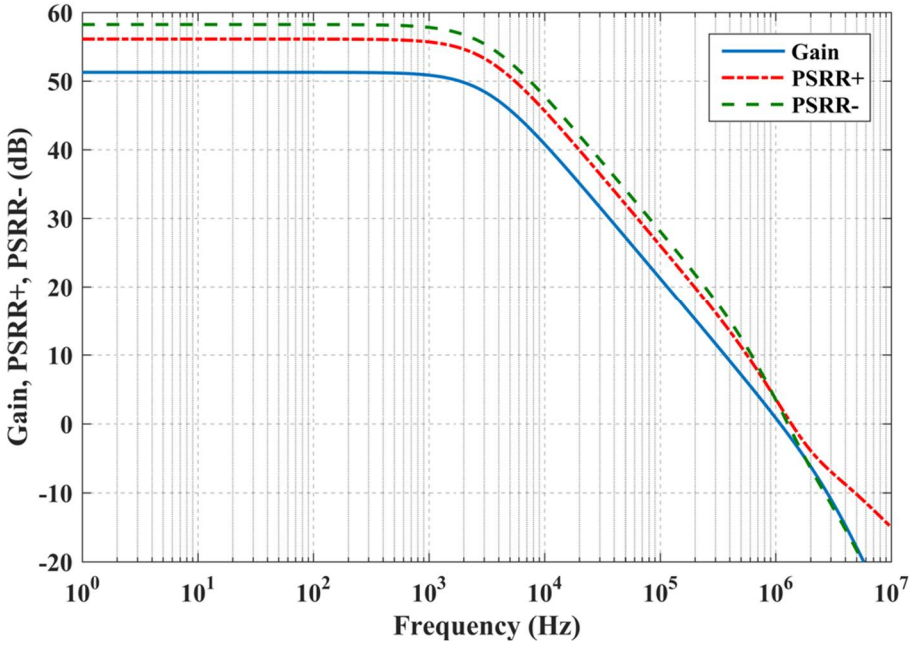

Figure 5. Magnitude versus frequency of the Power Supply Rejection Ratio (PSRR) from positive ($PSRR^+$) and negative ($PSRR^-$) supply rail. Open loop gain is also shown.

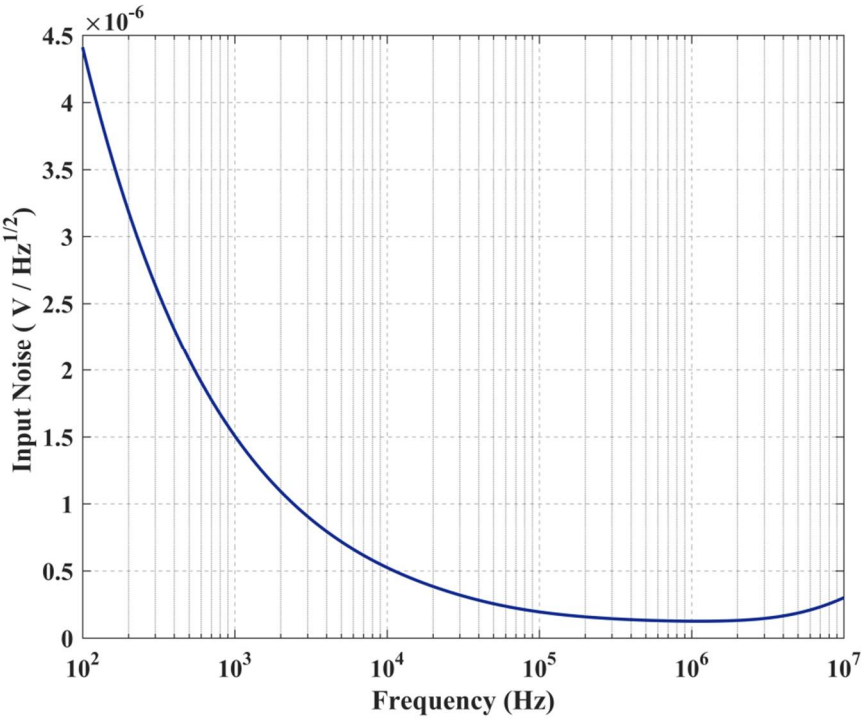

Figure 6. Equivalent input noise voltage spectral density.

The effect of mismatches was also simulated through 1000 Monte Carlo iterations. Table 3 summarizes the results. The largest variation is experienced by the unity gain frequency and settling times (more than 30%).

Table 3. Statistical analysis of main performance parameters due to mismatches (1000 Monte Carlo iterations).

Parameter	μ	σ	σ/μ
V_{out} (mV)	250.1	11.8	4.7%
I_{DD} (nA)	488.1	93.7	19.2%
DC Gain (dB)	51.3	0.56	1.1%
UGF (MHz)	1.13	0.34	30.1%
PM (degrees)	68.9	5.2	7.5%
$PSRR^+$ (dB)	56.1	0.56	1%
$PSRR^-$ (dB)	58.2	0.56	0.9%
1% Ts^+/Ts^- (ns) [1]	522/348	206/135	39.5/38.8%

[1] with 100-mV_{p-p} input and in inverting unity gain configuration.

Temperature and process variations were also evaluated via corner simulations under three different temperatures (−20 °C, +27 °C and +85 °C). Results are summarized in Table 4. It is seen that the quiescent current is sensitive to temperature and to FF and SS corners. In particular, the total amplifier nominal current (which was approximately 488 nA) decreases to 249 nA at −20 °C, SS corner, and increases to 2.4 μA at +80 °C, FF corner. DC gain, PM and PSRR exhibit only quite negligible changes, whereas UGF and settling time are affected by these standby current variations. This problem is mainly related to the large threshold voltage excursion induced by temperature variation that cannot be counteracted by the restricted range of the bulk control voltages limited to V_{DD}.

Table 4. Corner simulations (Typical, Fast-Fast, Fast-Slow, Slow-Fast, and Slow-Slow) under three different operating temperatures.

Corner T = −20 °C	**TT**	**FF**	**FS**	**SF**	**SS**
V_{out} (mV)	244.4	248.6	229.7	264.7	249.3
I_{DD} (nA)	256	475	243	227	104
DC Gain (dB)	49.8	52	50	50.4	47.4
UGF (MHz)	0.67	1.58	0.63	0.59	0.22
PM (degrees)	69.2	64.6	69	69.9	76.9
PSRR+ (dB)	54.4	56.7	54.7	55.2	52
PSRR- (dB)	56.9	58.9	57.1	57.4	54.7
1% Ts+/Ts- (ns)	685/438	272/182	566/337	854/336	2632/880
Corner T = 27 °C	**TT**	**FF**	**FS**	**SF**	**SS**
V_{out} (mV)	249.9	244.5	249.3	249.9	250
I_{DD} (nA)	488	579	505	479	485
DC Gain (dB)	51.3	51.7	52.1	50.4	51
UGF (MHz)	1.09	1.68	1.13	1.08	0.88
PM (degrees)	69.2	64.3	69.5	69	73.1
PSRR+ (dB)	56.1	56.7	56.9	55.2	55.7
PSRR- (dB)	58.2	58.5	59.8	58.9	58.3
1% Ts+/Ts- (ns)	520/319	240/207	506/322	519/321	719/490
Corner T = 80 °C	**TT**	**FF**	**FS**	**SF**	**SS**
V_{out} (mV)	255.8	249.1	233.9	277.1	259.8
I_{DD} (nA)	1177	2417	1338	1061	621
DC Gain (dB)	52.6	53	53	52.1	51.5
UGF (MHz)	2.2	5.68	2.5	1.98	0.97
PM (degrees)	74.3	77.3	75.8	73.3	73.4
PSRR+ (dB)	57.4	57.7	57.9	56.7	56.3
PSRR- (dB)	59.4	59.7	59.8	58.9	58.4
1% Ts+/Ts- (ns)	356/235	130/123	230/239	233/210	838/436

4. Conclusions

A novel inverter-based two-stage CMOS transconductance amplifier, with quiescent current control and suitable for very low supply voltages was presented. The solution consists of the cascade of a noninverting and an inverting stage both characterized by having only two complementary transistors between the supply rails, thus providing rail-to-rail and class-AB output capability. The designed solution is supplied from 0.5 V and in quiescent conditions consumes (typically) approximately 488 nA, while providing a DC gain of approximately 51 dB, with a unity gain frequency of 1 MHz and phase margin of 70 degrees, for a 1-pF//1.5-MΩ load.

The quiescent current control loop proved to be effective against mismatches and process variations. Further investigation is currently being carried out to reduce the quiescent current sensitivity to temperature. This drawback is caused by the limited variation allowed to the body biasing control voltage, which is of course restricted to V_{DD} and ground. Once V_{BP} and V_{BN} reach these limits and saturate, the control loop becomes ineffective. For this reason, making I_{BIAS} with a coefficient negative to absolute temperature (NTAT) could be a favorable solution and subject for further study.

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