Low Power Class-AB VCII With Extended Dynamic Range

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Abstract: In this paper we present a novel CMOS second generation voltage conveyor (VCII) topology featuring a wide voltage swing both at the X terminal and at the Z terminal. The VCII consists of a regulated common gate configuration at the Y current input terminal and a class-AB complementary-MOS closed loop output voltage follower that ensures the voltage buffering action between the voltage input X and the voltage output Z terminals. Spice simulation results using AMS 0.35 μm with a ±0.9 V supply voltage are provided to demonstrate the validity of the proposed topology. With a total power consumption of 28 μW, the VCII achieves a voltage swing at the X terminal of ±0.8 V, whereas a ±0.72 V is achieved on the Z terminal. Simulation results for DC and AC voltage and current gains are given, as well as harmonic distortions and noise figures. A final comparison table is also presented, where the proposed VCII is compared with other solutions presented in the literature.

Keywords: VCII, Current Mode, Voltage Conveyor Applications, Low Power Circuits, Rail-to-Rail Circuits.

1. Introduction

The second generation voltage conveyor (VCII) was introduced in 2001 [1] as the dual circuit of the second generation current conveyor CCII [2-3], in order to be used in applications requiring voltage-mode processing. Current conveyors derive intrinsic benefits from current mode signal processing: circuits employing current conveyors, in particular the CCII, exhibit better frequency performance and simpler circuitry with respect to Operational Amplifier (Op-Amp) based circuits [4-9]. However, as the CCII lacks a low impedance voltage output port, it is not suitable for applications requiring a voltage output signal: in these cases, an extra voltage buffer is required to provide a low output impedance, so leading to higher power consumption and a larger chip area.

The VCII shows low impedance at voltage output port and allows to overcome CCII limitation in voltage-mode applications: this makes it the ideal linkage between voltage mode and current mode processing chains allowing the designer to mix the two approaches and choose the best for the specific task. The ideal internal structure (a) and the symbol (b) of a second-generation voltage conveyor (VCII) are shown in Fig. 1, where a clear duality can be observed with respect to the CCII. It is composed of a current buffer between Y and X terminals and a voltage buffer between X and Z terminals.

Unlike the CCII, the Y terminal of VCII is a current input port, showing low impedance Z_Y (ideally $Z_Y = 0$), X is a high impedance current output port (ideally showing $Z_X \to \infty$), and Z is a low impedance voltage output port (ideally $Z_Z = 0$).

The relationships between port voltages and currents are expressed as follows:

$$\begin{bmatrix} i_X \\ V_Z \end{bmatrix} = \begin{bmatrix} \pm\beta & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} i_Y \\ V_X \end{bmatrix}, \tag{1}$$

where VCII+ (VCII-) is identified by a positive (negative) current gain $+\beta$ ($-\beta$), where β should be ideally equal to 1, as well as the voltage gain α. Since the Y terminal has a low input impedance, it can be considered as a virtual ground node. The main features of a VCII can be summarized by the following three key points: first, unlike other active blocks, current summing operation can be easily performed at the current input low impedance Y port; second, as VCII shows a low impedance voltage output Z port, its flawlessly use in a voltage mode workflow is allowed, giving to the designer the flexibility to easily perform current mode operations. Finally, positive and negative voltage gains are simply obtained employing VCII+ and VCII-, respectively.

VCIIs are gaining more and more attention as proved by recent literature where many applications and some topologies for the VCII block have been presented [10-15] but were based on class-A output stages and suffered from limited voltage swings. When used without external feedback, the VCII can implement all the standard building blocks such as voltage amplifiers, current amplifiers, current to voltage amplifiers, transconductance amplifiers, integrators, differentiators and so on [4]. When used with a feedback path, it can be used to implement both current-mode (CM) and voltage mode (VM) oscillators (unlike Op-Amps).

The low voltage-low power restrictions imposed by advanced integrated technologies require the design of a high performance VCII circuit which is able to operate under low supply voltages and to provide an appropriate voltage swing at the voltage output port. Moreover, class-AB behavior can often be a key feature to minimize power consumption without sacrificing performance. These features are fundamental especially for applications such as sensor interfaces where it is often challenging to achieve good sensitivity and resolution levels. In [16], some of the authors proposed an improved VCII topology based on a more efficient high drive class-AB output stage, that is able to provide a load current much larger than the bias current for large input signals. Other transistor-level implementations of class-AB VCII have been recently presented [17-18]. The topology in [17] presents a complex structure to allow a large voltage swing, resulting in an increased power consumption and the need of

several voltage references. The VCII in [18] presents a simpler structure with open-loop buffers, but this results in higher gain errors and nonideal port impedances.

In this paper, we propose a high-swing VCII topology suitable for low voltage applications, where the voltage swing has to be maximized to fully exploit the limited supply range. The topology allows an almost rail-to-rail swing both at X and Z nodes, thus overcoming the limitations of most of the previously published VCII topologies. Moreover, a class-AB output stage is exploited, in order to achieve low quiescent current and high current drive capability. This is achieved with a simpler closed-loop structure, resulting in a low quiescent power consumption.

This paper is structured as follows: in Section 2, the proposed topology is presented in terms of internal transfer functions and equivalent impedances at input and output nodes. Simulations of the topology in the AMS 0.35 μm integrated process are presented in Section 3 in order to highlight performance that can be achieved. Main results and conclusions are summarized in Section 4.

2. The Proposed Topology

The proposed VCII topology is shown in Figure 2. The current input terminal Y is implemented through a regulated common gate structure composed by the common gate transistor M1 and the feedback differential amplifier M2-M5. The low input impedance is ensured by the topology as well as by the negative feedback itself. The negative feedback is responsible also for keeping Y at virtual ground thanks to the voltage at the gate of M3, so setting the input dc current bias. The current mirror M6-M7 ensures the condition $I_X = I_Y$, together with almost rail-to-rail operation at node X, only limited by the overdrive voltages of transistors M7 and MB3.

The input impedance at node Y has been evaluated under the hypothesis that device output conductance is negligible with respect to the transconductance ($g_m >> g_{ds}$), and for $C_{GS} >> C_{GD}$, as follows:

$$Z_Y = R_{Y0}\frac{1+sC_{GS1}(R_{DS2}//R_{DS5})}{(1+s/\omega_{1Y})\cdot(1+s/\omega_{2Y})}, \tag{2}$$

being:

$$R_{Y0} \cong \frac{1}{g_{m1}[1+g_{m2}(R_{DS2}//R_{DS5})]}. \tag{3}$$

The approximated dominant pole ω_{1Y} and the second pole ω_{2Y} are expressed as:

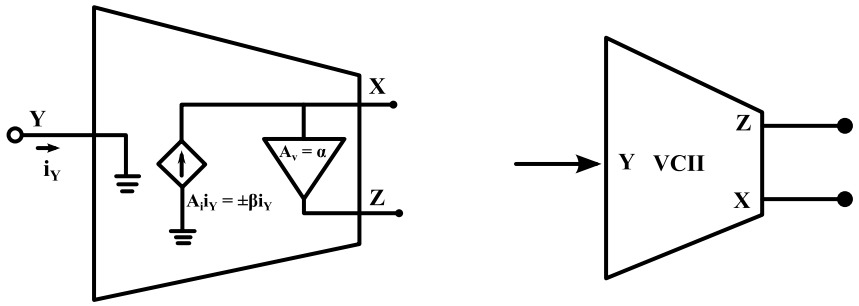
$$\omega_{1Y} \cong \frac{g_{m1}[1 + g_{m2}(R_{DS2}//R_{DS5})]}{(C_{GS1} + C_{GS2}) + (R_{DS2}//R_{DS5}) \cdot [C_{GS1}g_{ds1} + C_{GD1}g_{m1} + C_{GD2}g_{m2}]}, \tag{4}$$

$$\omega_{2Y} \cong \frac{(C_{GS1}+C_{GS2})+(R_{DS2}//R_{DS5})[C_{GS1}g_{ds1}+C_{GD1}g_{m1}+C_{GD2}g_{m2}]}{(R_{DS2}//R_{DS5})[C_{GD1}C_{GD2}+(C_{GS1}+C_{GS2})\cdot C_{GS1}]}, \tag{5}$$

The current gain β is given by:

$$\beta \cong \frac{1}{(1+s/\omega_{1Y})\cdot(1+s/\omega_{2Y})}, \tag{6}$$

From (2) and (3) we can say that the impedance Z_Y behaves like a resonant low-pass filter, showing a zero and a couple of complex conjugate poles, and can be modelled as a series-parallel resonance, according to the circuit shown in Fig. 3, where:



(a) (b)

Fig. 1. VCII internal structure a) and symbol b).

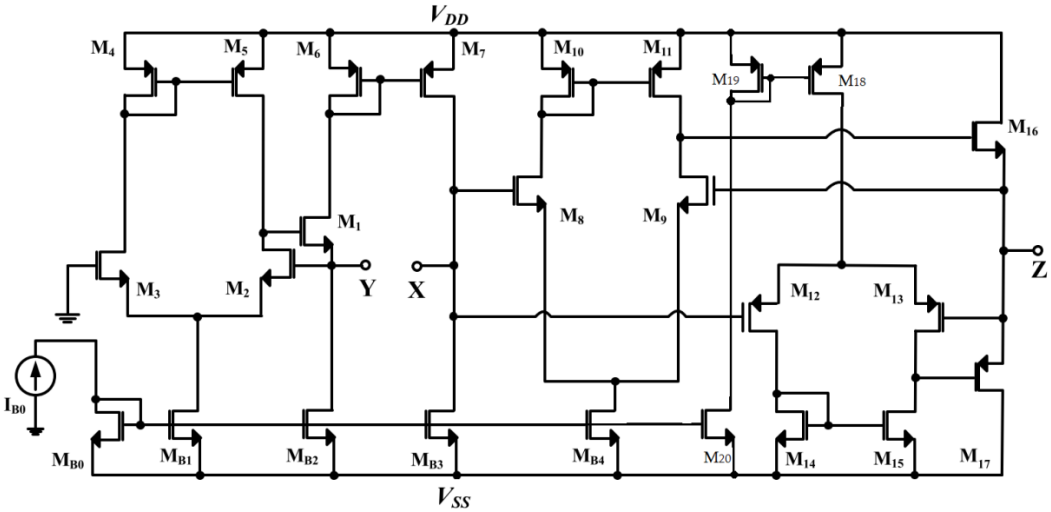


Fig. 2. The proposed high-dynamic VCII.

$$R_{eqY} = R_{Y0}, \tag{7}$$

$$L_{eqY} = \frac{C_{GS1}(R_{DS2}//R_{DS5})}{g_{m1}[1+g_{m2}(R_{DS2}//R_{DS5})]} \cong \frac{C_{GS1}}{g_{m1}g_{m2}}, \tag{8}$$

$$C_{eqY} = C_{GS1} + C_{GS2}, \tag{9}$$

In order to save the available dynamic of the current buffer, the voltage buffer is implemented as a push-pull stage with auxiliary amplifiers: the feedback network allows to obtain a unity voltage gain α, and at the same time to lower both the output impedance at the node Z and the parasitic capacitance at node X (C_X). The following expressions have been derived when the positive output voltage peak is considered, i.e., when the transistor M16 is pushing current in the load, for the output impedance Z_Z and for the voltage gain α, respectively:

$$Z_Z = R_{Z0}\frac{1+sC_{GS16}(R_{DS9}//R_{DS11})}{(1+s/\omega_{1Z})\cdot(1+s/\omega_{2Z})}, \tag{10}$$

$$\alpha = \frac{g_{m8}(R_{DS9}//R_{DS11})}{1+g_{m8}(R_{DS9}//R_{DS11})}\frac{1+sC_{GS16}/g_{m16}}{(1+s/\omega_{1Z})\cdot(1+s/\omega_{2Z})}. \tag{11}$$

being:

$$R_{Z0} = \frac{1}{g_{m16}[1+g_{m8}(R_{DS9}//R_{DS11})]}, \tag{12}$$

The approximated expressions for the dominant pole ω_{1Z} and for the second pole ω_{2Z} are:

$$\omega_{1Z} \cong \frac{g_{m8}\cdot g_{m16}}{C_{GD16}\cdot g_{m16}+C_{GS16}\cdot g_{m8}}, \tag{13}$$

$$\omega_{2Z} \cong \frac{C_{GD16}\cdot g_{m16}+C_{GS16}\cdot g_{m8}}{C_{GD16}\cdot C_{GS16}}. \tag{14}$$

Together with the approximations on g_{ds} and C_{GD}, the voltage gain $g_{m8}(R_{DS9}//R_{DS11})$ of the symmetrical (i.e., $g_{m8} = g_{m9}$) differential pair has been considered much greater than 1. Similar to Y terminal, from (10) and (12) we can say that impedance Z_Z behaves like a resonant low-pass filter, showing a zero and a couple of complex conjugate poles, and can be modelled again as a series-parallel resonance, according to the circuit shown in Fig. 3, where now:

$$R_{eqZ} = R_{Z0}, \tag{15}$$

$$L_{eqZ} = \frac{C_{GS16}(R_{DS9}//R_{DS11})^2}{[1+g_{m8}(R_{DS9}//R_{DS11})][g_{m16}(R_{DS9}//R_{DS11})-1]} \cong \frac{C_{GS16}}{g_{m8}g_{m16}}, \tag{16}$$

$$C_{eqZ} \cong \frac{C_{GD16}C_{GS16}}{C_{GD16}+C_{GS16}}[1+g_{m8}(R_{DS9}//R_{DS11})], \tag{17}$$

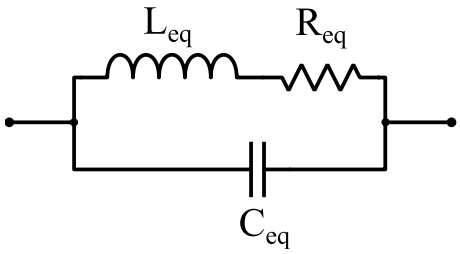


Fig. 3. Resonant model for the input and output impedances of the VCII.

Finally, the approximated expression for the impedance at node X (which can be modelled as a parallel of an equivalent resistance and a capacitance) has been determined as:

$$Z_X = \frac{R_{DSB3}//R_{DS7}}{1 + sC_X(R_{DSB3}//R_{DS7})} = \frac{R_{x0}}{1 + sC_X R_{x0}}, \tag{18}$$

being:

$$R_{x0} = R_{DSB3}//R_{DS7}, \tag{19}$$

$$C_X \cong \frac{\frac{C_{GS8}}{2} + C_{GD8}\left(1 + \frac{g_{m8}}{2g_{m10}}\right)}{1 + g_{m8}(R_{DS9}//R_{DS11})}. \tag{20}$$

The class AB output stage allows to improve the VCII overall efficiency, as the quiescent current is much lower than the current available for load driving. The output dynamic range at node Z is limited by the V_{GS} voltages of the output stage devices.

3. Simulation Results

The proposed VCII has been implemented using a 0.35 µm standard CMOS technology from AMS and simulated through the PSpice suite. Current mirrors were designed to source a 3 µA bias current (MB2, MB3) and a 1.5 µA (MB1, MB4, M20). With a supply voltage of ±0.9 V, the static power consumption stands at 28 µW. Transistor dimensions are listed in Table I.

Table I. TRANSISTOR DIMENSIONS AND PARAMETER VALUES.

Transistor	Dimensions (W, L)
M1	60.2 µm, 0.35 µm
M2, M3, M8, M9	100.1 µm, 0.35 µm
M4, M5, M10, M11	40.25 µm, 1.4 µm
M6, M7	21 µm, 0.7 µm
M19, M18	7 µm, 0.35 µm
M12, M13	120.05 µm, 0.35 µm
M12, M13	20.3 µm, 1.4 µm

MB0, MB2, MB3	10.5 µm, 0.7 µm
MB1, MB4, M20	5.25 µm, 0.7 µm
M16	20.3 µm, 0.35 µm
M17	60.9 µm, 0.35 µm

The gain of the feedback differential amplifiers M2-M5, M8, M11, M12-M15 has been tuned to about 35 dB (Fig. 4). Terminal impedances are reported in Fig. 5, showing, as expected, a high value of 1.9 MΩ at the voltage input X, whereas a low value of 160 Ω and 367 Ω is experienced at the current input Y and voltage output Z, respectively. The rail-to-rail capabilities of this circuit have been tested configuring the circuit as a transimpedance amplifier (TIA, Fig. 6), injecting a full-dynamic ±3 µA ramp current signal at the Y terminal, while connecting a variable load at the X terminal that varies from 1 kΩ to 300 kΩ. For this configuration we can in fact write:

$$V_{out} = \alpha V_x = \alpha R_g I_x = \alpha R_g \beta I_y \cong R_g I_{in} \quad (21)$$

Such a circuit allows us to evaluate both the X and Z voltage dynamic ranges with a voltage signal theoretically ranging from -0.9 V to 0.9 V according to the input current. Figures 7, 8, and 9 show the DC current transfer function between Y and X terminals, the corresponding voltage signal produced at the X terminal, and the voltage swing at the Z terminal. We can conclude that the voltage at the X terminal can range between ±0.82 V, whereas, at the Z terminal the swing is equal to ±0.72 V. Linearity error has been evaluated as well and plotted in Fig. 9. It remains always below 2% (calculated respect to the best fit straight line and referred to the full scale) for gains up to 100 kΩ, while it raises to a maximum value of 8% for the full scale gain of 300 kΩ, considering the range of input currents that does not saturate the output voltage.

The AC performances of the proposed VCII are given in Fig. 10, showing the behavior of the magnitude of α and β parameters. For this analysis a 3 pF load has been connected to the Z terminal. The former shows a -0.02 dB magnitude with a bandwidth of 3.2 MHz, while the latter shows a 0.1 dB magnitude with a bandwidth of 71 MHz. Ultimately, the AC performances are limited by the voltage buffer. Noise levels are reported in Fig. 11 where the input-referred current and voltage spectral densities are plotted, respectively, showing a value of 130 pA/√Hz and 182 nV/√Hz at 1 kHz, respectively.

Time-domain simulations were conducted using the same TIA configuration reported in Fig. 6 at different input current and gain levels (see Fig. 12). Through this analysis both large and small signal harmonic distortions were evaluated both for the current at X terminal and the

voltage at Z terminal considering a total of 10 harmonics. The former analysis was conducted injecting a full scale ±3 μA current at the Y input with a large 200 kΩ gain. Results show that the THD remains close to -30 dB up to 100 kHz. Small signal harmonic distortion has been evaluated as well and reported in the same Fig. 13.

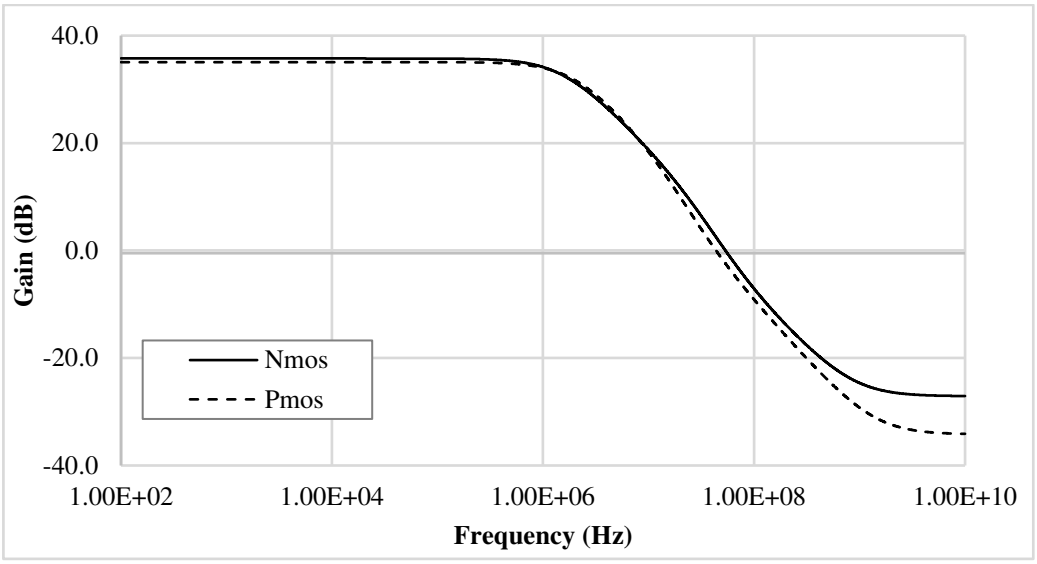


Fig. 4. Feedback amplifiers open loop gain.

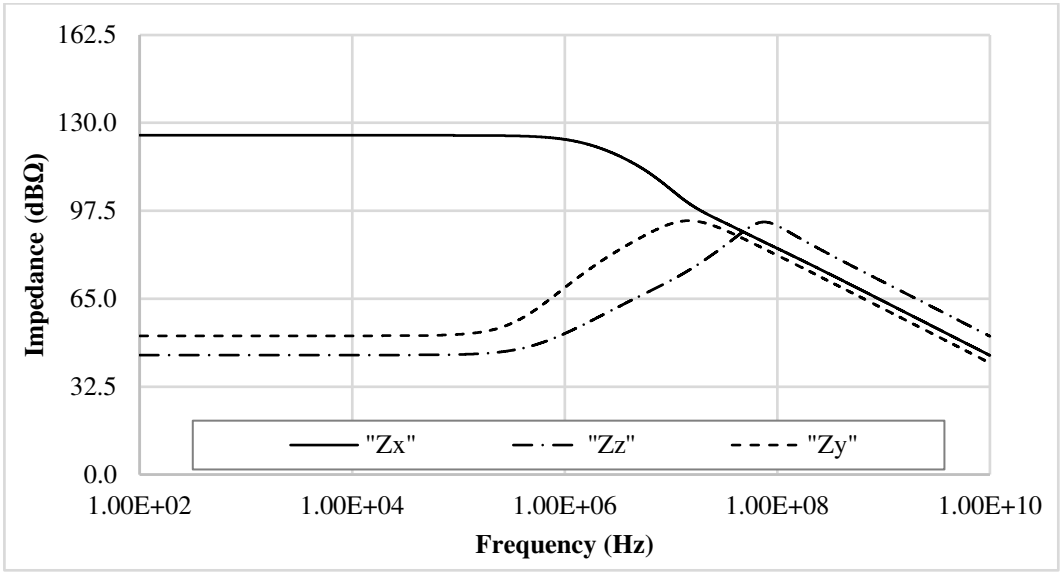


Fig. 5. VCII terminal impedances.

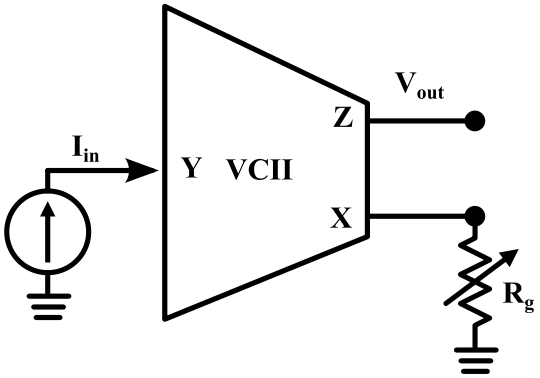


Fig. 6. VCII used as a transimpedance amplifier.

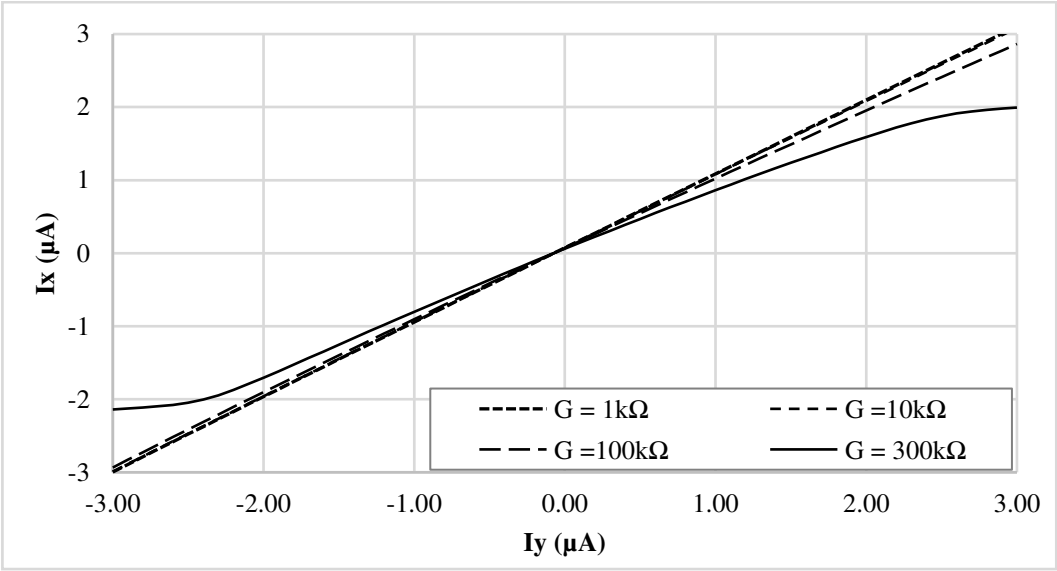


Fig. 7. DC current transfer function between Y and X terminals at different transimpedance gain (G).

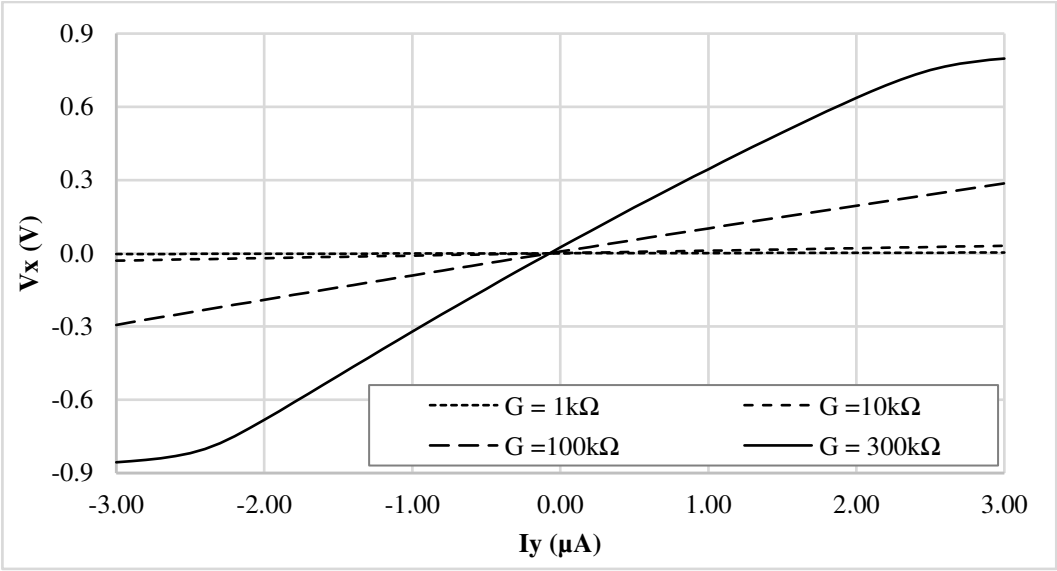


Fig. 8. Voltage swing at the X terminal.

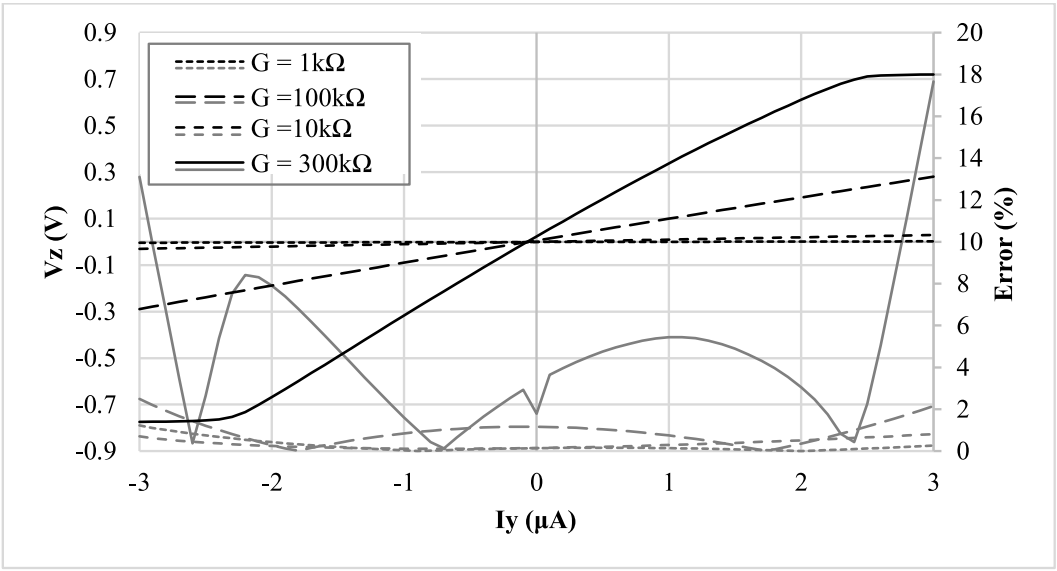


Fig. 9. Voltage swing at the Z terminal, and linearity error.

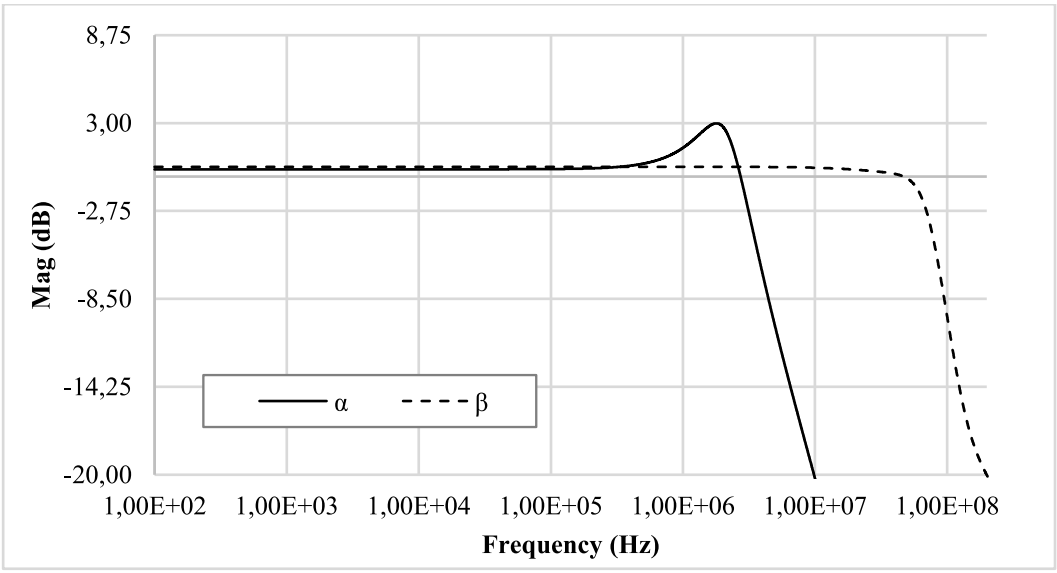


Fig. 10. AC performances of the α and β parameters.

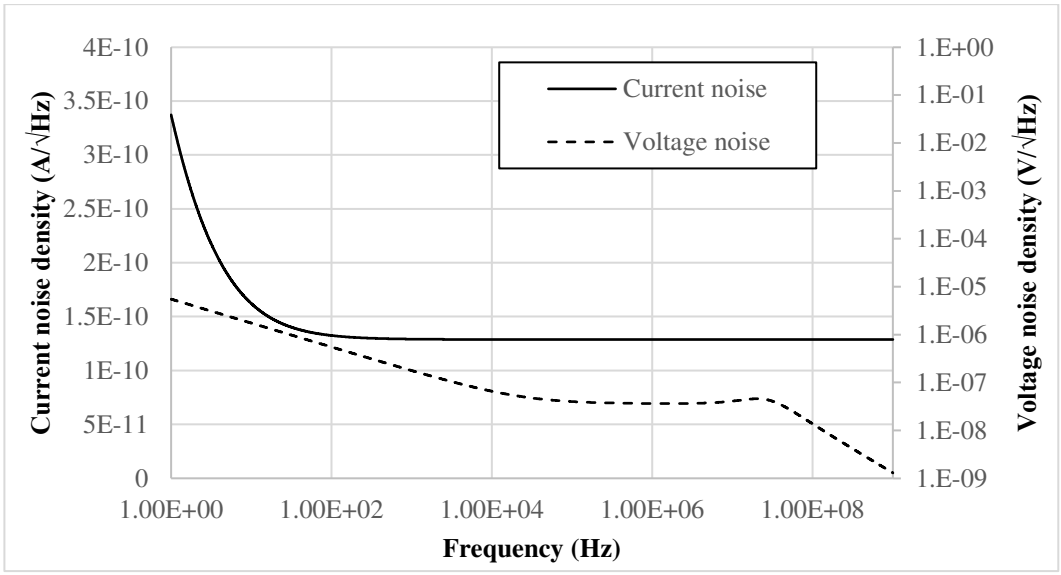


Fig. 11. Input referred current and voltage noise density at the X and Z terminal, respectively.

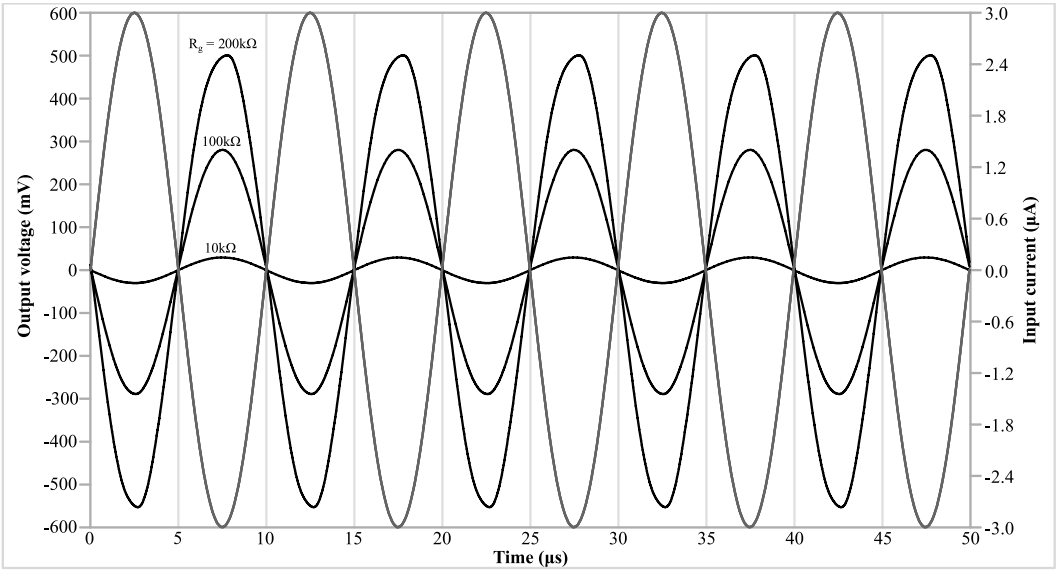


Fig. 12. Time-domain simulations with an input current of ±3µA, at 100 kHz, for different values of gain.

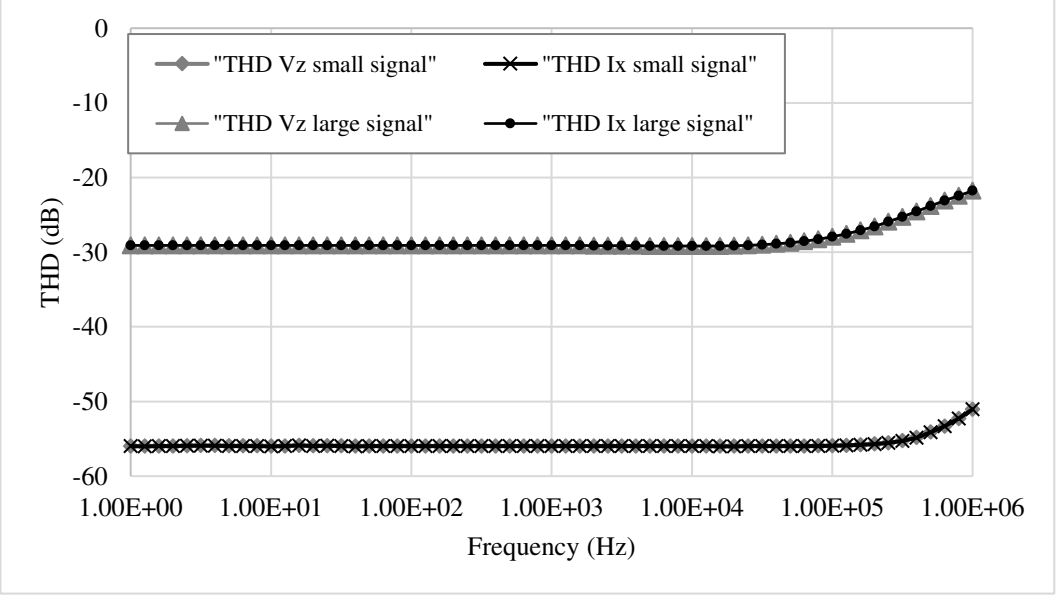


Fig. 13. THD performance of the VCII at X and Z terminals.

In this analysis, a 1 µA current has been injected into the terminal Y and a trans-impedance gain of 10 kΩ has been set, so to generate a 10 mV voltage signal at X node. As visible, THD level remains good for the entire useful bandwidth, being -51 dB at 1 MHz for both Ix and Vz. Robustness of the proposed architecture was tested as well. Table II reports statistical outputs derived from 100 Monte Carlo runs at each one of the three PVT corners. Being the main source of non idealities, α and β variations were analysed both in terms of magnitude and bandwidth. Results show a negligible impact of both PVT and random variations, except for the bandwidth of the α parameter that drops down to 1 MHz when in the slow corner.

To conclude, a comparison with other works from the literature is given in Table III. Specifically, the following figure of merit (FOM), introduced in [19], aims to quantify the dynamic range of each circuit and is evaluated as:

$$FOM = \frac{V_{DD} + |V_{SS}|}{V_{in,pp_{max}}} I[\mu A]. \tag{21}$$

where the first term represents the ratio between the total supply range and the maximum allowable amplitude that can be placed at any input terminal without distortion, and the second is the overall current that the circuit needs to operate.

From Table III results, we can say that the proposed topology shows the best value for the FOM, due to its large voltage swing and low static power consumption. The closed-loop structure allows a very low gain error on the voltage stage, while the much different loading conditions do not allow an easy comparison of bandwidth and efficiency. Moreover, a large ratio between max and min values of impedances at the VCII terminals is achieved, making it particularly versatile in any practical applications, especially those where an external feedback network is required (e.g., oscillators).

Table II. OUTPUTS OF THE PVT AND MONTE CARLO ANALYSIS.

	|α|	**|β|**	**α, BW**	**β, BW**
μ	-0.021 dB	0.13 dB	2.26 MHz	7.06 MHz
σ^2	0.013 dB	0.012 dB	567 kHz	240 kHz
Max	0.002 dB	0.15 dB	3.9 MHz	7.12 MHz
Min	-0.05dB	0.10 dB	1.01 MHz	7.00 MHz

μ: mean value*;* ***σ²:*** standard deviation

Table III. COMPARISON TABLE.

	This	**[4]**	**[17]**	**[18]**	**[20]**	**[21]-a**	**[21]-b**	**[22]**
Tech.	AMS 0.35μm	AMS 0.35μm	LFoundry 0.15μm	0.18μm	TSMC 0.35μm	TSMC 0.18μm	TSMC 0.18μm	TSMC 0.18μm
Class	AB	A	AB	AB	A	A	A	AB
Supply	±0.9V	±1.65V	±0.9V	±0.9V	±1.65V	±0.9V	±0.9V	±0.45V
Active element	VCII	VCII	VCII	VCII	UVC**	VCII	VCII	VCII
R_{x0}	1.9MΩ	1.2MΩ	522kΩ	274kΩ	240kΩ	75kΩ	75kΩ	156kΩ
R_{y0}	160Ω	6.7Ω	23Ω	1.88kΩ	650mΩ	930mΩ	930mΩ	2.7kΩ
R_{z0}	367 Ω	0.7 Ω	160 Ω	1.75kΩ	1.4 Ω	705mΩ	35mΩ	38Ω

$\|\alpha\|$	-0.02dB	–0.03dB	-0.24dB	-0.11dB	0.32dB	-0.28dB	0dB	0.972
$\|\beta\|$	0.1dB	–0.1dB	-0.03dB	0dB	N.A.	-0.1dB	-0.1dB	0.987
$\|\alpha\|$, *BW**	3.2 MHz	217 MHz	55 MHz	100 GHz	74 MHz	2.57 GHz	1.92 GHz	49.2 MHz
$\|\beta\|$, *BW*	71 MHz	200 MHz	155 MHz	170 MHz	64 Hz	794 MHz	794 MHz	225 MHz
Vz, THD	-50.8 dB	–63 dB	-32.4 dB	1%@ $1.78V_{pp}$	2.7%	N.A.	N.A.	N.A.
Ix, THD	-51 dB	–59 dB	-39 dB	1%@ $2.4mA_{pp}$	N.A.	N.A.	N.A.	N.A.
Power consumption	28 µW	330 µW	120 µW	179 µW	5 mW	664 µW	622 µW	79 µW
FOM	20	330	85	100.6	4950	618	345	196
*Data source***	S.	S.	S.	S.	M.	P.L.S.	P.L.S.	P.L.S.

|α|, BW is evaluated with a capacitive load of 3 pF at Z for the presented work, 1 pF for [10] and unloaded for the others; ** Universal voltage conveyor; * S: schematic simulations, P.L.S: post layout simulations, M: measurements.*

6. Conclusion

A novel topology of CMOS second generation voltage conveyor suitable for low-voltage, high dynamic range and high driving capability applications has been proposed and analysed. Expressions for transfer functions and Input/Output impedances have been evaluated and used to design a VCII in a standard 0.35 µm process. Simulated performance has been compared to other implementations reported in technical literature, and better dynamic range and FOM at low voltage supply has been obtained.

References

1. I. Filanovsky, "Current conveyor, voltage conveyor, gyrator," in 44th IEEE 2001 Midwest Symposium on Circuits and Systems. MWSCAS 2001, Dayton, OH, USA, USA, 2001, pp. 314-317.
2. K. Smith and A. Sedra, "The current conveyor—A new circuit building block," Proceedings of the IEEE, vol. 56, no. 8, pp. 1368-1369, 1968.
3. G. Ferri and N. Guerrini, Low voltage, low power CMOS current conveyors. New York: Springer, 2011.
4. L. Safari, G. Barile, V. Stornelli and G. Ferri, "An Overview on the Second Generation Voltage Conveyor: Feature, Design and Applications," IEEE Trans. Circuits and Systems II: Express Briefs, 2018.

5. L. Safari, G. Barile, G. Ferri, and V. Stornelli, ‘Traditional Op-Amp and new VCII: A comparison on analog circuits applications’, AEU - International Journal of Electronics and Communications, vol. 110, p. 152845, Oct. 2019.
6. A. M. Soliman, "Generation of current conveyor-based all-pass filters from op amp-based circuits," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 4, pp. 324-330, April 1997.
7. A. A. Khan, S. Bimal, K. K. Dey and S. S. Roy, "Novel RC sinusoidal oscillator using second-generation current conveyor," in IEEE Transactions on Instrumentation and Measurement, vol. 54, no. 6, pp. 2402-2406, Dec. 2005.
8. A. A. El-Adawy, A. M. Soliman and H. O. Elwan, "A novel fully differential current conveyor and applications for analog VLSI," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 4, pp. 306-313, April 2000.
9. J. A. Svoboda, L. McGory, E S. Webb, "Applications of a commercially available current conveyor", International Journal of Electronics, vol. 70, n. 1, pp. 159–164, gen. 1991.
10. P. Rani and R. Pandey, "Voltage Conveyor based Electronically Tunable Multifunction Biquadractic Filter," 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN), 2020, pp. 1110-1113.
11. L. Safari, G. Barile, G. Ferri, V. Stornelli and A. Leoni, "New Current Mode Wheatstone Bridge Topologies with Intrinsic Linearity," in 2018 14th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Prague, Czech Republic, 2018, pp. 9-12.
12. L. Safari, G. Barile, G. Ferri and V. Stornelli, "High performance voltage output filter realizations using second generation voltage conveyor," International Journal of RF and Microwave Computer-Aided Engineering, vol. 28, no. 9, p. e21534, 2018.
13. F. Centurelli, P. Monsurrò, P. Tommasino, A. Trifiletti, “On the use of voltage conveyors for the synthesis of biquad filters and arbitrary networks,” ECCTD 2017, European Conference on Circuit Theory and Design, 4-6 Sept. 2017, Catania.
14. S. D. Pathak, A. Luitel, S. Singh and R. Pandey, "Second Generation Voltage Conveyor II based Shadow Filter," 2021 2nd International Conference for Emerging Technology (INCET), 2021, pp. 1-5.
15. M. A. Al-Absi, "Realization of inverse filters using second generation voltage conveyor (VCII) ", Analog Integr Circ Sig Process, vol. 109, n. 1, pp. 29–32, Oct. 2021.
16. G. Barile, G. Ferri, L. Safari and V. Stornelli, "A New High Drive Class-AB FVF Based Second Generation Voltage Conveyor,” IEEE Trans. Circuits and Systems II: Express Briefs, Vol. 67, pp. 405-409, Mar. 2020.

17. G. Barile, V. Stornelli, G. Ferri, L. Safari and E. D'Amico, "A New Rail-to-Rail Second Generation Voltage Conveyor," Electronics 2019, Vol. 8, 1292.
18. M. Kumngern, U. Torteanchai, F. Khateb, "CMOS Class AB Second Generation Voltage Conveyor," IEEE International Circuits and Systems Symposium, Kuantan, Malaysia, 18-19 Sept. 2019.
19. S. Balasubramanian and M. Ismail, "Rail-to-rail input stages: A voltage-mode design technique and a figure-of-merit," Proceedings of the 8th IEEE International NEWCAS Conference 2010, Montreal, QC, Canada, 2010, pp. 277-280.
20. J. Koton, N. Herencsár, and K. Vrba, "KHN-equivalent voltage-mode filters using universal voltage conveyors," AEU - International Journal of Electronics and Communications, vol. 65, no. 2, pp. 154–160, Feb. 2011, doi: 10.1016/j.aeue.2010.02.005.
21. A. Yesil and S. Minaei, "New simple transistor realizations of second- generation voltage conveyor," International Journal of Circuit Theory and Applications, vol. 48, no. 11, pp. 2023–2038, 2020, doi: https://doi.org/10.1002/cta.2879.
22. A. Yesil, S. Minaei, and C. Psychalinos, "± 0.45 V CMOS Second-Generation Voltage Conveyor Based on Super Source Follower", Circuits Syst Signal Process, Oct. 2021.