A SiGe HBT 6th-order 10GHz Inductor-less Anti-aliasing Low-pass Filter for High-speed ATI Digitizers

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***Abstract*—High-speed digitizers operating at sampling rates higher than 10GS/s require low-pass anti-aliasing filters in the multi-GHz range. Asynchronous Time-Interleaved (ATI) digitizers also need low-pass filters before digitization, and additional requirements on their design are set by this specific application. In integrated solutions, inductor-less filters are important for minimizing the chip area footprint.**

In this paper, we present the design of a 6th-order inductor-less 10GHz low-pass filter implemented in the STMicroelectronics SiGe BiCMOS55 process. It can be used as anti-aliasing filter for conventional 30GS/s digitizers or at the output of a 40GS/s ATI digitizer. We exploit positive feedback to synthesize the active inductor based on a stacked topology, minimizing the number of current branches, and thus power consumption.

Analysis and design guidelines for the biquad are presented. The filter exhibits a bandwidth of 10GHz with a power consumption of 43mW, a THD of -45dB and an SNR of 43dB with an input amplitude of 710mV peak-to-peak differential. Extensive corner and Monte Carlo post-layout simulations have been carried out to highlight the robustness of the circuit to PVT and mismatch variations.

Experimental results have confirmed very good agreement between measured and simulated performance, validating the proposed design flow.

***Index Terms*—analog filters, anti-aliasing filters, inductor-less filters, low-pass filters, SiGe integrated circuits.**

I. Introduction

HIGH-speed Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are more and more required in applications such as digital communication systems [1-2], wideband spectrum monitoring [3-5] and advanced measurement instrumentation, where ADCs based on the Asynchronous Time Interleaved (ATI) architecture [6-7] can be exploited to build digital sampling oscilloscopes with very large signal bandwidth.

ADCs operating with sampling frequencies beyond 20GS/s require anti-aliasing filters with a sharp frequency response and a low-pass cut-off frequency higher than 10GHz [8-13]. Pulse-shaping filters with similar requirements are needed at the output of DACs with clock frequencies in excess of 20GHz [14-16]. Two anti-aliasing filters with a bandwidth of 10GHz are also needed to implement a 40GS/s ADC front-end based on the ATI architecture [6-7]. Anti-aliasing or pulse-shaping filters require large bandwidth, steep out-of-band attenuation, and good linearity and noise performance, not to impair system performance.

Integrated active filters without external components can reduce weight and size, and remove the need of power-hungry wideband off-chip interfaces. Modern SiGe HBT processes allow achieving tens of GHz of bandwidth, but designing passive resonators at such high frequencies typically requires the use of inductors and transmission lines, which consume large silicon area and may cause electromagnetic (EM) compatibility issues. Furthermore, computationally expensive 2.5D and 3D EM models are needed to design circuits operating up to several tens of GHz, when the dimensions are such to require a distributed approach. For a 10GHz filter, the required inductors would be in the range of a few nH and would occupy a large silicon area.

On the contrary, implementations based on active inductors result in minimal area footprint and in a more compact layout, which also implies short interconnection lines between devices. This reduction in chip area occupation is extremely advantageous in particular for highly integrated systems, such as a whole ATI ADC. Furthermore, the limited length of the interconnection lines results in lower parasitic capacitances, resistances and inductances, and allows the use of lumped models for the parasitic elements with a negligible impact on accuracy.

High-order filters are typically designed by following one of these approaches:

- the gyrator synthesis method, starting from a doubly terminated LC-ladder prototype [18-19];
- the leapfrog LC-ladder simulation technique [20];
- the cascade of biquadratic sections [21-22].

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In this paper we focus on high-order, low-pass filters which are implemented through the cascade of biquadratic sections. Gm-C [18-21], Sallen-Key [22-23], and Tow-Thomas [24] topologies have been previously used to design low-pass biquadratic filters with a cut-off frequency up to a few GHz. Implementations based on active inductors can be found in [17] and [25-27]. To the best of our knowledge, the only low-pass biquad filters suitable for operation up to 10GHz reported in the literature can be found in [17], [18] and [23].

In the following, we start from the biquad topology reported in [17], that exploits the active inductor based on positive feedback and exhibits the lowest power consumption with adequate noise and linearity performance for our application. A thorough analysis of the topology is presented to derive design guidelines. The biquad is then used to implement a 6th-order low-pass filter for a 40GS/s ATI front-end in SiGe HBT technology. A custom filter is designed to meet the requirements of the ATI application, using an optimization procedure with constraints on the quality factors of the biquads. Measured results in good agreement with the presented models are reported to demonstrate the effectiveness of the proposed design methodology.

This paper is organized as follows: Section II describes the filter specifications and system level design, Section III presents the topology of the biquad stages with a theoretical analysis of the frequency response, noise and distortions. Section IV and Section V describe the design of the test chip in the STM BiCMOS55 technology and the results of simulations, respectively. Section VI reports the measurements results, and Section VII concludes.

II. Filter Specifications and Design

The filter presented in this paper has been designed to implement an ATI digitizer front-end operating at 40 GS/s. This application poses further constraints with respect to conventional anti-aliasing filters. In this Section we briefly present the ATI digitizer architecture and the role played by the low-pass filter in it, to derive the specifications for the filter. Successively, the system-level design of the filter is described.

A. Filter Specifications

The ATI digitizer [6] is an innovative time-interleaved ADC architecture which, unlike conventional time-interleaving, relaxes not only the sampling frequency, but also the analog bandwidth requirement of the channel ADCs. This is achieved by decomposing the input signal of bandwidth B into two analog signals of bandwidth $B/2$, thanks to a nonlinear processing requiring two sub-Nyquist mixers operating at $f_S/2$ (where f_S is the overall sampling frequency) and two low-pass filters of bandwidth $f_S/4$, followed by two ADCs operating at $f_S/2$. The two ADC outputs can be interleaved to reconstruct the input signal, and linear signal processing can be used to correct for aliasing and linear errors, as in conventional time-interleaved architectures [6-7].

The architecture of the two-channel ATI-based digitizer is depicted in Fig. 1 [6]. The sampler implements the mixing function, by performing the multiplication of the input signal by a pulse train, composed of identical pulses of shape $p(t)$,

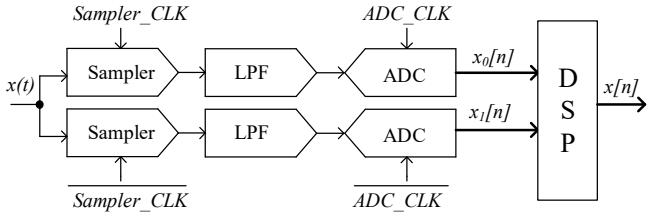

Fig. 1. Block diagram of an ATI-based architecture. The samplers and the ADCs are driven by independent clocks at *fs/2*; the blocks named LPF denote the anti-aliasing low-pass filters with bandwidth *fs/4*; digital signal processing allows reconstructing the input signal, correcting both aliasing and frequency response errors.

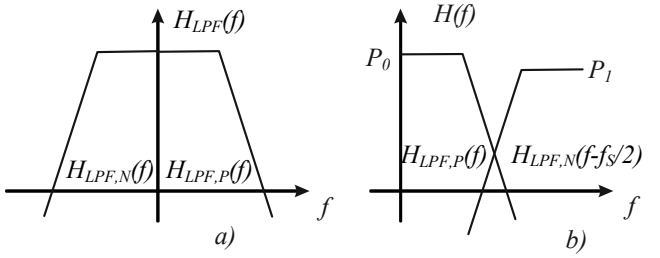

Fig. 2. Frequency response of the filter (a), and of the ATI system (b), which is the sum of the low-pass filter (a) and its scaled replica centered around f_S, $H_{LPF}(f - f_S/2)$. The resulting frequency response (b) is approximately all-pass in the Nyquist band, but the high-pass section is scaled by $P_1 \leq P_0$, which are the first two Fourier series coefficients of the pulse shape $p(t)$.

spaced by $2T_S$. The two channels operate in time-interleaved mode, implemented by using CLK and $\overline{CLK}$ on both the sampler and the ADC clock paths.

The overall frequency response *H(f)* of the ATI digitizer, in the ideal case where no mismatches are present and no signal processing is performed for equalization (no aliasing occurs in the absence of mismatches), can be found by applying multi-rate signal processing theory [6] in the discrete-time domain. The frequency response for positive frequencies (subscript P) can be written as [6]:

$$H_P(f) = P_0 H_{LPF,P}(f) + P_1 H_{LPF,N}\left(f - \frac{f_S}{2}\right), \quad (1)$$

(see Fig. 2) where $H_{LPF,P}(f)$ is the (positive) frequency response of the low-pass filter, $H_{LPF,N}\left(f - \frac{f_S}{2}\right)$ is the frequency-translated (negative) frequency response of the low-pass filter, and P_0 and P_1 are the first two coefficients of the Fourier series of the sampling pulse shape *p(t)* [6]. Therefore, the term $H_{LPF,P}(f)$ represents a low-pass filter in the band $[0, f_S/2]$ (with cut-off at $f_S/4$), whereas, since the term $H_{LPF,N}\left(f - \frac{f_S}{2}\right)$ is the frequency-translated frequency response of the low-pass filter around the pulse train frequency $f_S/2$, it acts as a high-pass filter in the second half of the Nyquist band $[f_S/4\,, f_S/2]$.

In the ideal case of Dirac pulses, $P_0 = P_1 = 1$, but in the implemented architecture the pulse train is a square wave with period $2T_S$ and 50% duty cycle, so $P_0 = 1$ and $P_1 = \operatorname{sinc} 0.5 \approx -3.9dB$.

From (1), with an ideal pulse train and brickwall low-pass filters, the frequency response would be equal to 1 across the Nyquist band, but with a rectangular pulse train there would be

an attenuation of about 3.9dB in the second half of the Nyquist band, which can be removed by equalization performed in the DSP. With real low-pass filters, the frequency response is given by (1). This poses a further constraint on the design of the filter, to achieve low ripple in the overall response, and possibly monotonic behavior throughout the Nyquist band, to simplify digital equalization. In particular, (1) poses constraints also on the phase behavior of the filter, to avoid notches in the overall frequency response.

From the system level considerations reported in [6], considering an ATI digitizer with $f_S = 40GS/s$ and a rectangular sampling pulse, and targeting an effective number of bits (ENOB) of 6, the following specifications have been derived for the two anti-aliasing low-pass filters LPF in Fig. 1, considering the overall frequency response given by (1):

- Pass-band frequency: $f_{PB} \cong 10GHz$;
- Stop-band frequency: $f_{SB} = 2f_{PB}$;
- Pass-band ripple: $A_{PB} \leq 1dB$;
- Stop-band attenuation at f_{SB}: $A_{SB} \geq 40dB$;
- Signal to noise ratio: $SNR > 40dB$;
- Spurious Free Dynamic Range: $SFDR > 40dB$ at ADC full scale amplitude;
- Dynamic Range: $DR \geq 40dB$.

In addition to these requirements, the overall transfer function of the ATI $H(f)$ should present low ripple, and possibly be monotonic. This constraint cannot be easily mapped on the specifications of the low-pass filter, hence the filter's frequency response has been synthetized to fulfill these requirements, as will be shown in the next subsection.

A filter fulfilling these requirements is also suitable as anti-aliasing filter in a conventional ADC with a sampling frequency[1] $f_S = 30GS/s$ and 6 bits of ENOB. In fact, such ADC would digitize a signal at 10GHz (within the pass-band of the filter) and suffer aliasing at the same frequency for input signals at 20GHz (within the stop-band of the filter).

B. Filter Design

The above specifications in terms of frequency response could be satisfied by using a 6th-order Butterworth or a 5th-order Chebyshev Type-I (all-poles) prototype filter. As a preliminary design step, we have synthesized a 6th-order Butterworth filter with a 10GHz cut-off frequency and a 5th-order Chebyshev filter with pass-band frequency $f_{PB} = 10GHz$ and pass-band ripple $A_{PB} \leq 1dB$. The resonance frequencies f_{0i} and the quality factors Q_i ($i = 1,2,3$) of the biquad sections needed to implement these filters are reported in Table I (for the 5th-order Chebyshev filter, f_{01} and Q_1 denote a single real pole).

TABLE I
RESONANT FREQUENCIES AND QUALITY FACTORS FOR DIFFERENT FILTERS

Filter type	f_{01} (GHz)	Q_1	f_{02} (GHz)	Q_2	f_{03} (GHz)	Q_3
Butterworth 6th-order	10	0.52	10	0.7	10	1.93
Chebyshev 5th-order	2.89	0.5	6.55	1.4	9.94	5.55
Custom 6th-order	7.8	0.6	10.5	1.0	14.8	1.7

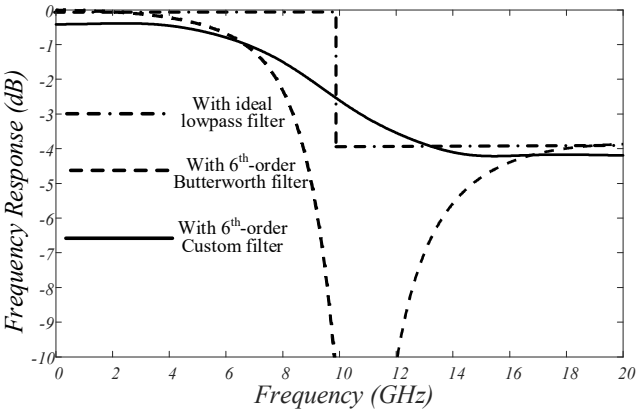

Fig. 3. Frequency response of a $40GS/s$ ATI digitizer with LPF filters implemented as an ideal low-pass filter, a Butterworth filter, and the optimized custom 6th-order filter.

From the results in Table I, we see that the implementation of the 5th-order Chebyshev filter requires a biquad section with $Q_3 = 5.55$: such a high Q value results in a strong sensitivity to process, supply voltage and temperature (PVT) variations, as well as to layout parasitics and mismatches. For this reason, we have discarded the Chebyshev filter[2]. The maximum Q required by the 6th-order Butterworth filter is 1.931, resulting in a much lower sensitivity than the Chebyshev one.

We can use (1) (and the corresponding equation for negative frequencies) together with the transfer functions of these filters to verify if a satisfactory frequency response for the overall front-end is obtained [6]. Fig. 3 shows the frequency response $H(f)$ of the ATI digitizer channel when the 6th-order Butterworth filter with 10GHz cut-off frequency is used to implement the LPF block (dashed line). The $H(f)$ when an ideal (brickwall) low-pass filter is adopted (dashed-dotted line) is also reported. It is apparent that, using a Butterworth filter, $H(f)$ shows a 35dB drop in gain around $f_S/4$. This is due to the fact that the real and imaginary parts of $P_0 H_{LPF,P}(f)$ and $P_1 H_{LPF,N}\left(f - \frac{f_S}{2}\right)$ sum almost to zero at about 10.76GHz. Similar results (not shown) have been obtained using 6th-order Butterworth filters with cut-off frequencies ranging from 8 to 12GHz: no Butterworth filter provided a monotonic frequency response from 0 to -3.9dB in the Nyquist band.

From the above considerations, none of the considered conventional filters is adequate to implement the LPF block in the ATI digitizer. To improve the frequency response $H(f)$ of the ATI digitizer, we have chosen a filter architecture based on the cascade of three biquadratic sections with resonance frequencies f_{0i} and quality factors Q_i, $i = 1,2,3$. We have then implemented an optimization procedure in Matlab™ similar to the one reported in [28] to synthesize a custom 6th-order filter. The resonance frequencies f_{0i} and quality factors Q_i of the three

[1] A 10GHz LPF would be ideally adequate for a 20GS/s system; a higher sampling frequency however has to be considered in the practical case due to the width of the transition band.

[2] A 6th order Chebyshev filter would require biquad stages with even higher Q factors.

biquad sections have been optimized with the goal of obtaining a flat and monotonic frequency response $H(f)$, close to the one obtained with an ideal low-pass filter as LPF block (dashed-dotted line in Fig. 3). This goal allowed to define the cost function of the optimization routine, in which the constraint on the maximum value ($Q_i \leq 2, i = 1,2,3$) of the biquads' quality factors has been included. We used a Monte Carlo optimization algorithm, randomly choosing the quality factors and resonance frequencies for the three biquad stages in order to minimize the above cost function. After a suitable solution was found, the Monte Carlo search was narrowed to find a better optimum around the previous one. Too narrow search areas are not necessary, due to process and mismatch variations affecting the filters' frequency responses. The resonance frequencies f_{0i} and quality factors Q_i of the custom filter resulting from this optimization are reported in the last row of Table I, and Fig. 3 shows the resulting frequency response $H(f)$ (solid line), which now presents a monotonic behavior with a smooth transition between low and high frequencies.

III. Biquad Stage Analysis

The schematic of the biquad stage adopted for the implementation of the anti-aliasing low-pass filter is reported in Fig. 4 [17]. The differential pair $Q_{F1L,R}$, with degeneration resistors $R_{EL,R}$, acts as the main transconductor loaded by an equivalent RLC load to implement the biquadratic transfer function. The RLC load is made up of the capacitor C_1, and of active inductors (in the dashed box) implemented through the cross-coupled devices $Q_{F2L,R}$, the capacitor C_2, and the resistors $R_{DL,R}$ and $R_{CL,R}$ which are needed both for biasing purposes and to set the value of the quality factor Q of the biquad stage, as shown in the following.

A. Active Inductor Model

In order to develop a simplified model for the frequency response of the biquad filter suitable for pencil and paper calculations, we have considered the small signal differential half-circuit reported in Fig. 5, where R_C, R_D and R_E denote the resistance values of the resistors $R_{CL,R}$, $R_{DL,R}$ and $R_{EL,R}$, respectively, and G_M is the equivalent transconductance of the differential pair $Q_{F1L,R}$, with degeneration resistors $R_{EL,R}$.

Referring to Fig. 5, the capacitances C_B and C_T can be expressed as:

$$\begin{cases} C_B = 2C_1 + C_{PB} \\ C_T = 2C_2 + C_{PT} \end{cases}, \tag{2}$$

where C_{PB} and C_{PT} account for the parasitic capacitances to ground at the nodes v_c and v_o respectively.

Then, neglecting the r_b, r_0 and r_π parasitic resistances in the model of the bipolar transistors in Fig. 5, the equivalent impedance Z_{IND} at the emitter of Q_{F2} can be computed as:

$$Z_{IND} = \frac{1 - g_{m2}R_C + sR_C(C_T + C_\pi + 4C_\mu)}{g_{m2} + \left[g_{m2}R_C(C_T + 4C_\mu) + C_\pi\right]s + \left[R_C(C_TC_\pi + 4C_TC_\mu)\right]s^2} \tag{3}$$

where g_{m2}, C_π, and C_μ are the transconductance and the parasitic capacitances of transistors $Q_{F2L,R}$.

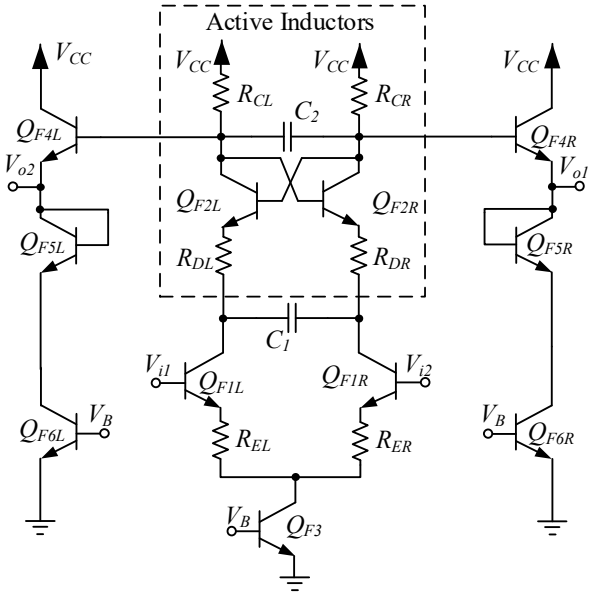

Fig. 4. Biquad stage topology. The three biquad stages are identical, with the same device sizing and layout, but for capacitors C_2 and C_1, which allow setting the quality factor and resonance frequency of the stages.

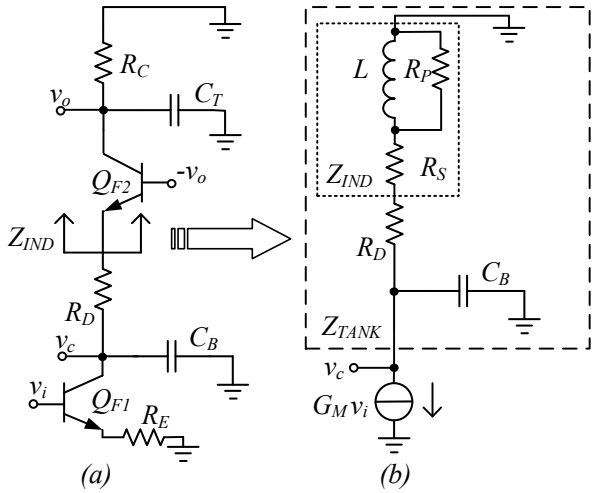

Fig. 5. Biquad small signal differential half-circuit (a) and active inductor equivalent circuit (b).

Equation (3) can be rewritten as:

$$Z_{IND} = Z_0 \frac{1 + s\tau_z}{(1 + s\tau_{p1})(1 + s\tau_{p2})}, \tag{4}$$

where:

$$Z_0 = \frac{1}{g_{m2}} - R_C \tag{5a}$$

is the dc value (i.e., setting *s=0*) of Z_{IND},

$$\tau_z = \frac{R_C(C_T + C_\pi + 4C_\mu)}{1 - g_{m2}R_C}, \tag{5b}$$

$$\tau_{p1} = R_C\left(C_T + 4C_\mu\right), \tag{5c}$$

$$\tau_{p2} = \frac{C_\pi}{g_{m2}}. \tag{5d}$$

From (4), neglecting the high frequency pole τ_{p2}, the equivalent inductance and the parallel and series parasitic

resistances of the equivalent circuit in Fig. 5b can be derived as follows:

$$L = R_C^2\left(C_T + 4C_\mu\right) + \frac{R_C C_\pi}{g_m} \approx R_C^2\left(C_T + 4C_\mu\right), \quad (6)$$

$$R_S = Z_0, \quad (7)$$

$$R_P = R_C + \frac{C_\pi}{g_m\left(C_T+4C_\mu\right)} \approx R_C. \quad (8)$$

Simulations show an accuracy better than 8% for the estimate of the inductance value, and 5% for the resistances.

B. Biquad Frequency Response

To evaluate the resonance frequency and the quality factor of the biquad filter, we compute the impedance Z_{TANK} of the RLC load of the main transconductor which, multiplied by the equivalent transconductance G_M of the differential pair $Q_{F1L,R}$ with degeneration resistors $R_{EL,R}$, results in the expression of the voltage gain $\frac{v_c}{v_i}$.

Referring to Fig. 5b, the impedance Z_{TANK} can be derived as:

$$Z_{TANK} = \frac{(R_D+Z_0)+s\left(R_D\tau_{p1}+Z_0\tau_z\right)}{1+s\left[\tau_{p1}+C_B(R_D+Z_0)\right]+s^2C_B\left(R_D\tau_{p1}+Z_0\tau_z\right)} \quad (9)$$

and the equivalent transconductance G_M can be easily computed as:

$$G_M = \frac{g_{m1}}{1+g_{m1}R_E}. \quad (10)$$

Referring to the circuit in Fig. 5a, and using the above assumptions, the expression of the voltage gain $\frac{v_o}{v_i}$ can be derived as:

$$\frac{v_o}{v_i} \cong -\frac{G_M\cdot R_C}{1+s\left[\tau_{p1}+C_B(R_D+Z_0)\right]+s^2C_B\left(R_D\tau_{p1}+Z_0\tau_z\right)}. \quad (11)$$

The resonance frequency, the quality factor and gain of the biquad can then be evaluated from the denominator of both (9) and (11) as follows:

$$\omega_0 \cong \frac{1}{\sqrt{C_BR_C\left[\left(C_T+4C_\mu\right)\left(R_D+\frac{1}{g_{m2}}\right)+\frac{C_\pi}{g_{m2}}\right]}}, \quad (12a)$$

$$Q \cong \frac{1}{\omega_0\left[R_C\left(C_T+4C_\mu\right)+C_B\left(R_D+\frac{1}{g_{m2}}-R_C\right)\right]}, \quad (12b)$$

$$A_{dc} \cong G_M \cdot R_C. \quad (12c)$$

For what concerns the stability analysis, we can focus on the denominator of the frequency response (11). The first- and second-degree terms are $\tau_{p1} + C_B(R_D + Z_0)$ and $C_B\left(R_D\tau_{p1} + Z_0\tau_z\right)$. The former term can be negative since from (5a) $Z_0 = -R_C + 1/g_m$, but R_D sums up a positive contribution, and τ_{p1} (5c) is positive. The latter term is the sum of two positive terms, because both Z_0 and τ_z (5b) are negative, whereas τ_{p1} is positive. Hence, a sufficient, though not necessary, condition for the positiveness of the first-degree term (and hence the stability of the filter) is $C_T > C_B$.

Due to additional high frequency zeroes and poles which have been neglected in the above analysis, Q and ω_0 estimated by (12) exhibit a mean percentage error of about 10% (with a maximum percentage error lower than 15%). A more accurate model for the frequency response of the circuit in Fig. 4 can be found in [17], but it is of limited usefulness at the design stage, owing to its complexity.

It has to be noted that the biquad described in this Section is not suited to achieve high Q factors, because excessive use of positive feedback would cause stability and sensitivity issues against PVT variations and mismatches. With the adopted BiCMOS process we have successfully designed biquad filters with Q values in the range of 3.5, but we have also seen that the higher the Q factor, the higher the sensitivity to process parameter variations. However, the limited achievable Q factor is not an issue for the use of this biquad in high-order filters. In fact, as discussed in section II, the proposed filter design approach is based on the inclusion of a constraint on the maximum value of the biquads' quality factors Q_i, to minimize the sensitivity to PVT variations.

C. Noise Analysis

In this Subsection we compute the equivalent input noise of the biquad filter in Fig. 4. For this purpose, we consider the equivalent noise circuit in Fig. 6a in order to find an expression for the equivalent noise current generator i_{on} at the collector node of Q_{F1}. By applying the principle of superposition of effects, i_{on} can be computed as the sum of two contributions: the short circuit noise current i_{Tn} at the output of the main transconductor and the equivalent short circuit noise current i_{Ln} of the active load made up of R_D, Q_{F2} and R_C. For the computation of i_{Tn} we consider the base resistance r_{b1}, (and the corresponding noise generator v_{rb1n}), together with the conventional base and collector noise generators i_{b1n} and i_{c1n} of transistor Q_{F1}, and the degeneration resistor's noise generator i_{REn} as the main noise contributions. For the computation of i_{Ln} we refer to the circuit in Fig. 6b and consider the base resistance r_{b2}, (and the corresponding noise generator v_{rb2n}), together with the conventional base and collector noise generators i_{b2n} and i_{c2n} of transistor Q_{F2}, and the collector resistor noise generator i_{RCn} (we assume R_D<<R_C) as the main noise contributions.

The noise model in Fig. 6 is derived for low frequencies, and the parasitic resistance $r_{01,2}$ of transistors Q_{F1} and Q_{F2} are neglected in these computations for simplicity.

The equivalent output noise current of the main transconductor can be expressed as:

$$i_{Tn} \cong \frac{i_{c1n}+(g_{m1}r_{b1}+g_{m1}R_E)i_{b1n}+g_{m1}R_Ei_{REn}+g_{m1}v_{rb1n}}{g_{m1}R_E+1}, \quad (13a)$$

Assuming a large value of the transistors current gain β, the equivalent noise current i_{Ln} of the active load can be written as:

$$i_{Ln} \cong \frac{-i_{b2n}(2R_C+r_{b2})+(i_{RCn}R_C+v_{rb2n})}{R_C}. \quad (13b)$$

Denoting with $S_{i_{REn}}$ and $S_{i_{RCn}}$ the power density spectra of the equivalent current noise generators in parallel to the degeneration resistor R_E and the collector resistor R_C respectively, we can write:

$$S_{i_{REn}} = \frac{4K_BT}{R_E} = \frac{4qV_T}{R_E}, \quad (14a)$$

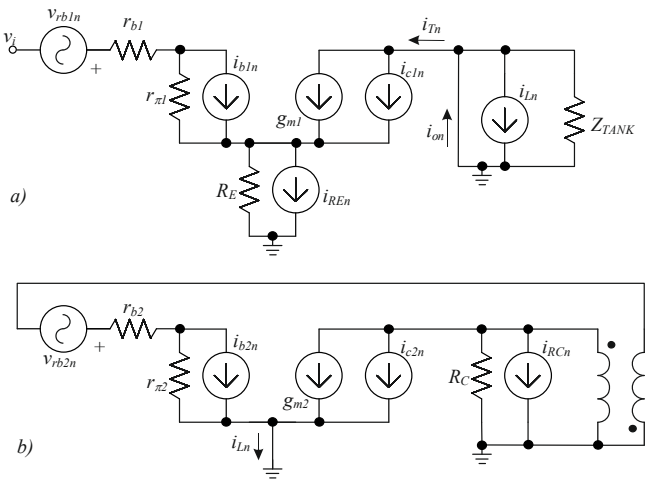

Fig. 6. Equivalent circuits for noise analysis: a) overall noise of the biquad; b) noise due to the active inductor load.

$$S_{i_{RCn}} = \frac{4K_BT}{R_C} = \frac{4qV_T}{R_C}. \quad (14b)$$

Then, starting from (13a), using (14a) and assuming $\beta \gg 1$, the power density spectrum of i_{Tn} can be written as:

$$S_{i_{Tn}} \cong 2qV_T g_{m1} \frac{1+2A_E+2A_B}{(A_E+1)^2} \quad (15a)$$

where, $A_E = g_{m1}R_E$ and $A_B = g_{m1}r_{b1}$.

Starting from (13b), using (14b), the power density spectrum of i_{Ln} can be written as:

$$S_{i_{Ln}} \cong \frac{4qV_T}{R_C}\left(1+\frac{r_{b2}}{R_C}\right) + \frac{2qg_{m2}V_T}{\beta}\left(2+\frac{r_{b2}}{R_C}\right)^2. \quad (15b)$$

Equation (15b) can be further simplified by using (12c) and (10) to express R_C as a function of A_{dc}, g_{m1}, and R_E, and assuming $g_{m2} \cong g_{m1}$, and $r_{b2} \cong r_{b1}$:

$$S_{i_{Ln}} \cong \frac{4qV_T g_{m1}}{A_{dc}(A_E+1)}\left[1+\frac{A_B}{A_{dc}(A_E+1)}\right]. \quad (15c)$$

The power density spectrum $S_{i_{on}}$ of the equivalent noise current generator i_{on} at the collector node of Q_{F1} can then be computed by summing the expressions in (15a) and (15c) as follows:

$$S_{i_{on}} \cong \frac{2qV_T g_{m1}}{(A_E+1)^2} \cdot K_{noise}, \quad (16)$$

$$K_{noise} = \left[3 + 4A_E + 2A_B\left(1+\frac{1}{A_{dc}}\right)\right]. \quad (17)$$

Because $A_E \gg 1$, the noise contribution of the transconductor and the active inductor are almost equivalent, so that total noise (17) is about twice that of the transconductor alone, when $A_{dc} = 1$.

Finally, the power density spectrum of the equivalent input noise is found to be:

$$S_{v_{in}} = \frac{S_{i_{on}}}{G_M{}^2} \cong \frac{2qV_T^2}{I_{C1}} K_{noise}. \quad (18)$$

Eq. (18) shows that increasing the bias current reduces the noise, and that increasing the value of the degeneration resistor R_E increases the noise, due both to the additional noise source and to the reduced transconductance gain of the stage.

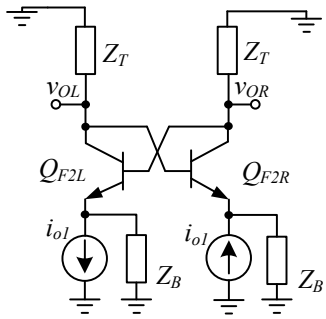

Fig. 7. Equivalent circuit for the evaluation of the distortions due to the active inductor.

The circuit in Fig. 4 could be modified by splitting the bias current source Q_{F3} into two bias current sources $Q_{F3L,R}$ to allow the use of a floating degeneration resistor $2R_E$ connected between the emitters of Q_{F1L} and Q_{F1R}. This configuration allows a lower minimum supply voltage because it eliminates the voltage drop across R_{EL} and R_{ER}, but strongly increases the equivalent input noise of the circuit, since, for such a modified circuit, $S_{i_{Tn}}$ in (15a) has to account also for the noise contributions of the current source transistors $Q_{F3L,R}$.

D. Distortion Analysis

In order to analyze the distortion performance of the biquad cell in Fig. 4, we start focusing on the transconductor made up of the differential pair $Q_{F1L,R}$ with degeneration resistors $R_{EL,R}$. We assume the conventional exponential model for the collector currents i_{C1L} and i_{C1R} of bipolar transistors $Q_{F1L,R}$ and utilize the usual Taylor approximation as follows:

$$i_{C1L,R}\left(v_{be1L,R}\right) = I_{C1L,R}e^{\frac{v_{beL,R}}{V_T}} \approx I_{C1} + g_m v_{be1L,R} + \alpha_2 g_{m1} v_{be1L,R}^2 + \alpha_3 g_{m1} v_{be1L,R}^3, \quad (19)$$

where $\alpha_2 = 1/2V_T$ and $\alpha_3 = 1/6V_T^2$. Then the emitter voltages v_{e1L} and v_{e1R} of $Q_{F1L,R}$ can be expressed as a function of the input voltage v_i as follows:

$$v_{e1L} = p_1 v_i + q_1 v_i^2 + r_1 v_i^3 \quad (20a)$$

$$v_{e1R} = -p_1 v_i + q_1 v_i^2 - r_1 v_i^3 \quad (20b)$$

Since the collector currents $i_{C1L,R}\left(v_{be1L,R}\right)$ of $Q_{F1L,R}$ in (19) are related to the currents flowing in the degeneration resistors $R_{EL,R}$, we can solve for p_1, q_1 and r_1, find $v_{e1L,R}$, and then compute the differential output current $i_{o1} = i_{C1L}(v_i) - i_{C1R}(v_i)$ of the differential pair $Q_{F1L,R}$ as:

$$i_{o1} = \frac{g_{m1}}{1+A_E} v_i - \frac{2\alpha_3 g_{m1}}{(1+A_E)^4} v_i^3. \quad (21)$$

To find the output voltage $v_{od} = v_{oL} - v_{oR}$ of the biquad cell, we now consider the equivalent circuit reported Fig. 7, where i_{o1} is given by (21), Z_B denotes the Norton equivalent impedance in parallel to the current sources at the output of $Q_{F1L,R}$, and Z_T denotes the equivalent impedance of the output nodes $v_{oL,R}$ to ground. Note that Z_B and Z_T also include the effect of the capacitors C_B and C_T and that we are assuming $R_D \ll R_C$. Referring to the circuit in Fig. 7, we can express the base-emitter voltages of transistors $Q_{F2L,R}$ as follows:

$$v_{be2L,R} = v_{OR,L} - v_{e2L,R} = -Z_T i_{C2R,L} - v_{e2L,R} =$$

$$= -Z_T\left(\frac{v_{e2R,L}}{Z_B} \mp i_{o1}\right) - v_{e2L,R}. \quad (22)$$

We exploit again (19) for the collector current $i_{C2R,L}$ and the 3rd-order Taylor approximation for $v_{e2L,R}$; by imposing *KCL* at the emitter nodes, after simple calculations we can derive the differential output voltage as follows:

$$v_{oD} = -g_{m2}Z_T G_M h_1[v_i + (\lambda + \rho G_M^2)v_i^3], \quad (23)$$

where:

$$h_1 = \frac{Z_B}{1-g_{m2}(Z_T-Z_B)} \quad (24a)$$

$$\lambda = \frac{2\alpha_3}{(1+A_E)^3} \quad (24b)$$

$$\rho = \frac{Z_B^2}{6V_T^2}\frac{1-2g_{m2}(Z_T+Z_B)}{[1-g_{m2}(Z_T-Z_B)]^3[1+g_{m2}(Z_T+Z_B)]}. \quad (24c)$$

Eq. (23) shows the well-known result that a higher degeneration resistance R_E provides a lower transconductance G_M, hence lower distortions. The resulting trade-off with noise behavior will be discussed in the next Subsection.

We would like to point out that, if very high-speed bipolar devices and fairly linear passive components are used for the implementation, the above "low frequency" analysis results reasonably accurate up to 10GHz. In fact, in our implementation we have exploited the bipolar devices available in the BiCMOS55 process, which exhibit an f_T in excess of 300GHz. Such transistors operate at fairly low frequency even at 10GHz, and distortions are still dominated by transconductances. For what concerns the passive components utilized in the filter, capacitors have been implemented as multi-layer MIM (metal-insulator-metal) capacitors and can be considered as almost ideal. Resistors have been implemented as polysilicon strips and exhibit a fairly linear behavior.

E. Dynamic Range Optimization

As shown in Appendix, the optimal input power $P_{I,opt}$ (optimal input amplitude $\hat{V}_{I,opt}$), which maximizes the signal-to-noise-and-distortion ratio (*SNDR*) and provides the optimal dynamic range (*DR*), is found by equating the signal-to-distortion ratio (*SDR*) to two times the signal-to-noise ratio (*SNR*). At this purpose, given an input signal $v_i = \hat{V}_I \cos\omega t$, the *SNR* over a bandwidth B can be derived from (18) as follows:

$$SNR = \frac{\hat{V}_I^2 \cdot I_C}{4qV_T^2 B \cdot K_{noise}} \quad (25)$$

To find an expression of the *SDR*, due to the fully differential architecture of the circuit, we consider only the third-order term. Then, starting from (23) and remembering that $v_i^3 = \frac{3}{4}\hat{V}_I^3\cos\omega t + \frac{1}{4}\hat{V}_I^3\cos 3\omega t$, and substituting α_3, we find, after straightforward manipulation:

$$SDR = \left[\frac{4}{(\lambda+\rho G_M^2)\cdot\hat{V}_I^2}\right]^2 = \left[\frac{4}{\hat{V}_I^2}\cdot\frac{3V_T^2(1+A_E)^3}{K_{disto}}\right]^2, \quad (26)$$

where,

$$K_{disto} = \frac{(\lambda+\rho G_M^2)}{3V_T^2(1+A_E)^3} \quad (27)$$

Equating the SNR in (25) to two times the SDR in (26), the optimal input signal level which maximizes the DR of the biquad section can be easily found to be:

$$\hat{V}_{I,opt} = 2V_T(1+A_E)\left[\frac{9qB}{2I_C}\left(\frac{K_{noise}}{K_{disto}^2}\right)\right]^{1/6}. \quad (28a)$$

For this input signal level $\hat{V}_{I,opt}$, the dynamic range is finally computed as:

$$DR_{opt} = \frac{2}{3}\left(\frac{9}{2}\right)^{1/3}(1+A_E)^2\left[\frac{I_C}{qBK_{noise}K_{disto}}\right]^{2/3}. \quad (28b)$$

This result can be extended to the case of M identical cascaded biquad stages. In fact, remembering that noise contributions of the biquads sum in power, whereas distortion contributions sum in amplitude, the condition for optimal input power becomes in this case:

$$SDR(P_{I,opt}) = 2\cdot M\cdot SNR(P_{I,opt}), \quad (29)$$

thus yielding:

$$\hat{V}_{I,opt,N} = 2V_T(1+A_E)\left[\frac{9qB}{2MI_C}\left(\frac{K_{noise}}{K_{disto}^2}\right)\right]^{1/6}. \quad (30a)$$

$$DR_{opt,N} = \frac{2M}{2M+1}\left(\frac{9}{2M}\right)^{1/3}(1+A_E)^2\left[\frac{I_C}{qBK_{noise}K_{disto}}\right]^{2/3} \quad (30b)$$

From (28b) and (30b) it is evident that the dynamic range increases with A_E. Therefore, it is always convenient to increase the degeneration resistance, because noise increases slower than distortions improve. Since DR increases in power with $\sqrt[3]{I_C^2}$ (keeping A_E constant), it is also always convenient to increase the bias current I_C if power dissipation is not a concern. There are of course limitations, and too large R_E values would limit the bandwidth of the degeneration feedback ($R_E C_\pi$ would be too large). Hence, R_E increases the dynamic range monotonically, up until the C_π of the input differential pair starts to be relevant owing to the large degeneration of the input stage.

F. Design Flow

Starting from the analysis reported in the previous Subsections, we derive useful design equations and present a simple design flow, which allows sizing the main circuit parameters starting from specifications in terms of frequency response, noise and distortions.

For the frequency response, we specify the dc gain A_{dc}, the resonance frequency ω_0 and the quality factor Q of the biquad stages. For what concerns noise and distortions, we work under the condition of optimal Dynamic Range in (30b) and specify the desired dynamic range DR and the maximum input amplitude V_{FS} of the filter.

From the specified values of DR and V_{FS} we can solve equations (30) to find A_E, I_C, and thus R_E as follows:

$$A_E = \left[\frac{2M+1}{9}DR\cdot K_{disto}^2\cdot\left(\frac{V_{FS}}{2V_T}\right)^4\right]^{1/6} - 1 \quad (31a)$$

$$I_C = \frac{3+4A_E}{\left(\frac{V_{FS}}{2V_T}\right)^2\cdot\frac{2M}{2M+1}\frac{1}{qBDR} - 2\left(1+\frac{1}{A_{dc}}\right)\frac{r_{b2}}{V_T}} \quad (31b)$$

$$R_E = \frac{A_E V_T}{I_C} \quad (32)$$

For the computation of K_{disto} in (31a), we assume, in this preliminary design step, $C_B = C_T$, which results in $Z_B \cong Z_T$.

From the specified dc gain A_{dc} we can calculate R_C starting from (12c), and using (10):

$$R_C = \frac{A_{dc}(1+A_E)V_T}{I_C} \quad (33)$$

If we now look at (12), we see that there are still three parameters (i.e., C_T, C_B, and R_D) to choose to set ω_0 and Q. In the proposed design flow, we start by setting C_T arbitrarily in its allowed range. The allowed range for C_T can be determined by setting appropriate conditions on τ_{p1} in (5c). In fact, in order to guarantee $R_D > 0$ and $R_D < |Z_0|$, τ_{p1} has to fulfill the following inequalities:

$$\frac{1}{\omega_0 Q} < \left[\tau_{p1} = R_C\left(C_T + 4C_\mu\right)\right] < \frac{1}{\omega_0 Q}\cdot\left(1 + \frac{g_{m2}|Z_0|Q}{\frac{1}{Q}+\omega_0 C_\pi R_C}\right) \quad (34)$$

Under these conditions, C_B and R_D can be derived from ω_0, Q and C_T by solving (12), thus obtaining the following design equations:

$$C_B = \frac{\frac{1}{\omega_0^2} - \tau_{p1}\left(\frac{1}{\omega_0 Q} - \tau_{p1}\right)}{|Z_o|\tau_{p1} + \frac{C_T R_C + (C_\pi + 4C_\mu)R_C}{g_{m2}}} \quad (35)$$

$$R_D = \frac{\left(\frac{1}{\omega_0 Q} - \tau_{p1}\right)}{C_B} + |Z_o| = \frac{\frac{|Z_o|}{\omega_0^2} + \left(\frac{1}{\omega_0 Q} - \tau_{p1}\right)\frac{C_T R_C + (C_\pi + 4C_\mu)R_C}{g_{m2}}}{\frac{1}{\omega_0^2} - \tau_{p1}\left(\frac{1}{\omega_0 Q} - \tau_{p1}\right)} \quad (36)$$

IV. Test Chip Design

The 6th-order filter presented in this paper has been designed in the commercial STMicroelectronics BiCMOS55 technology [29]. This technology offers SiGe HBT devices with f_T/f_{max} up to 320/370 GHz (HS devices), slower HBT devices with a higher breakdown voltage (HV devices), and 55nm CMOS devices, together with passives (including inductors and transmission lines) and 9 levels of metals of different thickness.

Three biquad stages with the topology in Fig. 4 have been designed according to the resonance frequencies and quality factors reported in the last row of Table I (Custom 6th-order filter). According to the design flow outlined in Section *III.F,* the collector current I_C of transistors $Q_{F1,2L,R}$, the degeneration resistance R_E, and the collector resistance R_C have been set to $1.1mA$, 410Ω, and 450Ω respectively resulting in $A_E \cong 18$, $A_{dc} \cong 1$, $\hat{V}_{I,opt,N} \cong 0.23V$ and $DR_{opt,N} \cong 45dB$, obtained from (31)-(33) with $M = 3$[3]. Then the parameters of the third biquad (i.e. the one with the highest resonance frequency $f_{03} = 14.7GHz$ and the highest quality factor $Q_3 = 1.7$) have been set according to the proposed design flow. In particular, the total equivalent capacitance of the third stage, denoted as $C_{T,3}$ has been arbitrarily set to $65fF$, and (35) and (36) have been used to find $C_{B,3} = 64fF$ and $R_{D,3} = 27\Omega$.

The parameters of the first and second biquad have been then set to allow an easy tuning of capacitors C_1 and C_2 (see Fig. 4) after post-layout simulations. In order to reuse the layout macros, whose parasitic capacitances affect the effective value of C_1 and C_2, as shown in (2), for the first two biquads $R_{D,1}$ and $R_{D,2}$ have been chosen equal to $R_{D,3}$. The capacitors have then been sized to implement the different f_{0i} and Q_i, exploiting equation (12) to derive the values of the overall capacitances C_T and C_B for a given R_D.

Table II shows the sizing of the devices for the three biquads. The explicit floating capacitances of the three stages are denoted as $C_{1,i}$ and $C_{2,i}$, whereas the total equivalent capacitances defined in (2) are $C_{B,i}$ and $C_{T,i}$. Parasitic capacitances $C_{PB,i}$ and $C_{PT,i}$ were about *30-40fF*. The voltage V_B in Fig. 4 is generated through the input branch of a conventional current mirror to set the tail current (Q_{F3}) to 2.2mA and the emitter follower currents ($Q_{F6L,R}$) to 1.2mA.

The test chip includes input and output buffers, to allow testing the anti-aliasing filter with input and output 100Ω differential terminations over a wide frequency range.

Fig. 8 shows the topology of the input buffer (only left side is shown). Input wideband 50Ω matching is implemented by means of resistors $R_{i4L,R}$, whereas the input common mode voltage is set through the same resistors and the current source transistors $Q_{i5L,R}$.

This solution allows the use of an ac coupled source without the need of an external biasing circuit. The common drain transistors $Q_{i4L,R}$ are biased through the current source devices $Q_{i3L,R}$ with a current of about 2.2mA to provide an output resistance of about 18Ω driving the filter block.

The schematic of the output buffer is reported in Fig. 9. This output stage has been implemented as a cascode differential pair made up of transistors $Q_{o7L,R}$ and $Q_{o8L,R}$ with 50Ω loads.

The degeneration resistors $R_{o4L,R}$ have been sized to provide about 0 dB gain when loaded by a differential 100Ω load (decoupling capacitors are external to the test chip).

TABLE II
DEVICE SIZING FOR THE BIQUADRATIC SECTIONS OF THE FILTER

Device			
	Emitter Area		
$Q_{F1,2}$	$0.3\mu m^2$		
Q_{F3}	$1.68\mu m^2$		
$Q_{F4,5,6}$	$0.84\mu m^2$		
	Transistor capacitances		
$C_{\pi 1,2,3}$	*14.7fF*		
$C_{\mu 1,2,3}$	*1.3fF*		
	Component value		
R_E	*410Ω*		
$R_{D1,2,3}$	*27Ω*		
R_C	*450Ω*		
Total Equivalent Capacitance		***Explicit Floating Capacitance***	
$C_{B,1}$	*103fF*	$C_{1,1}$	*33fF*
$C_{T,1}$	*160fF*	$C_{2,1}$	*56fF*
$C_{B,2}$	*86fF*	$C_{1,2}$	*21fF*
$C_{T,2}$	*104fF*	$C_{2,2}$	*35fF*
$C_{B,3}$	*64fF*	$C_{1,3}$	*16fF*
$C_{T,3}$	*66fF*	$C_{2,3}$	*18fF*

[3] Referring to the 6th-order custom filter whose parameters are reported in Table I, the first and the second biquad stages exhibit a Q lower than 1 and the third biquad has a Q of 1.7. With these low Q values the assumption of 3 identical cascaded stages is reasonable.

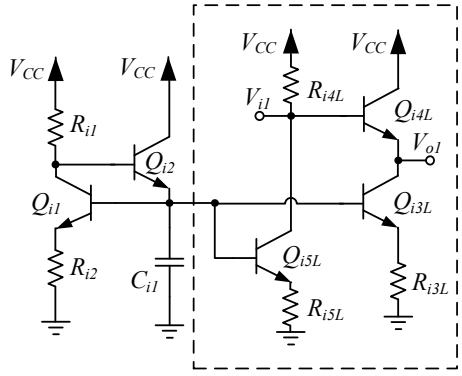

Fig. 8. Input buffer schematic. The other differential path has input V_{i2} and output V_{o2}, and the corresponding devices within the box are called "R" (right) instead of "L" (left). R_{i4} performs input matching at 50Ω.

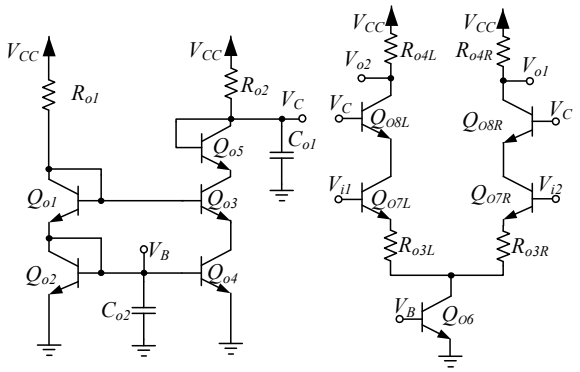

Fig. 9. Output buffer schematic. $R_{o4L,R}$ performs output matching at 50Ω.

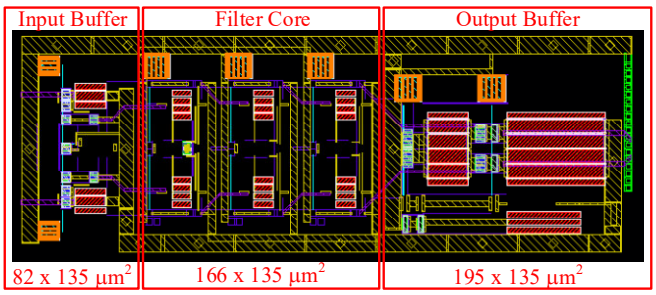

Fig. 10. Layout of the filter, including the I/O buffers.

The layout of the overall filter, including the input and output buffers, is shown in Fig. 10: the core filter requires an area of 166 x 135 μm², thus resulting extremely compact.

V. Simulation Results

This Section reports simulation results for the filter core with and without the I/O buffers. Post-layout simulations are reported in typical 27°C conditions, and then parametric simulations are shown to determine the sensitivity of the filter to supply voltage and temperature variations. These simulations include layout parasitics extracted with the Cadence QRC tool. The I/O pads and the transmission lines at the input and output of the test chip have been modeled by using the Keysight Momentum 2.5D EM simulator.

Monte Carlo simulations (with 200 iterations) are reported, which include process variations and mismatches, and are used to determine offset voltages, even-order distortions due to mismatches, and sensitivity to process and mismatch variations.

TABLE III
TYPICAL FILTER CORE SIMULATION RESULTS

Parameter	Symbol	Value	Unit
Supply voltage	V_{CC}	3.0	V
DC gain	A_{dc}	-0.1	dB
Gain ripple	ΔA	0.5	dB
3db cutoff frequency	f_{3dB}	10.3	GHz
Attenuation at 20GHz	A_{20GHz}	-42.9	dB
Output voltage swing (diff.)*	$V_{out,PP}$	783	mV
2nd order distortion*	HD_2	-75.3	dB
3rd order distortion*	HD_3	-44.5	dB
5th order distortion*	HD_5	-59.2	dB
Total Harmonic Distortion*	THD	-44.3	dB
Output noise (integrated up to 10GHz)	V_{noise}^{10GHz}	1.68	mVrms
Output noise (integrated up to 20GHz)	V_{noise}^{20GHz}	2.4	mVrms
SNR (considering V_{noise}^{10GHz})*	SNR_{10GHz}	44.3	dB
Optimum Dynamic Range *	DR	39.6	dB
Current consumption	I_{tot}	14.3	mA
Overall current consumption including I/O buffers	I_{filt}	65	mA

* Input power: -1dBm

A. Typical Post-Layout Simulations

As discussed before, layout parasitics affect the value of f_0 and Q of the biquad, thus post-layout simulations have been exploited to optimize the values of C_1 and C_2 of the three biquad stages, to match the desired filter frequency response. The optimized values are reported in Table II. Table III reports the main performance of the filter obtained from post-layout simulations after optimization of the capacitances showing how the obtained performance exceeds the main specifications discussed in Section II.

The results in Tab. III show a good agreement with the performance estimated by the proposed model, that predicts a 46-dB SNR and a -48-dB HD3, resulting in a dynamic range of 45 dB.

B. Supply Voltage and Temperature Variations

To evaluate the robustness of the filter against supply voltage and temperature variations, parametric simulations in which the supply voltage has been varied from 2.8 to 3.2V and the temperature from -30 to 120°C have been carried out.

Table IV shows the results of supply voltage variations, showing limited variations of filter performances which are

TABLE IV
EFFECT OF SUPPLY VOLTAGE VARIATIONS

Name	Value	Value	Value	Value	Value	Unit
V_{CC}	2.8	3.0	3.2	3.0	3.0	V
T	27	27	27	-30	120	°C
A_{dC}	-0.4	-0.1	-0.0	0.1	-1.0	dB
ΔA	0.5	0.5	0.6	0.3	0.9	dB
f_{3dB}	10.2	10.3	10.5	9.9	10.3	GHz
A_{20GHz}	-44.6	-42.9	-41.5	-39	-47	dB
$V_{out,PP}$	755	783	804	773	730	mV
HD_2	-75.5	-75.3	-74.2	-65.5	-85	dB
HD_3	-43.4	-44.5	-44.8	-38.9	-45.8	dB
HD_5	-58.7	-59.2	-57.8	-50	-55	dB
THD	-43.3	-44.4	-44.7	-38.8	-45.7	dB
V_{noise}^{10GHz}	1.57	1.68	1.79	1.48	1.88	mVrms
V_{noise}^{20GHz}	2.2	2.4	2.5	2.2	2.4	mVrms
SNR_{10GHz}	44.3	44.3	44.2	45.3	42.3	dB

TABLE V
MONTE CARLO SIMULATION RESULTS

Name	Min	Max	Mean	Std Dev	Unit
A_{dc}	-0.5	0.4	-0.1	0.3	dB
ΔA	0.5	1.5	0.6	0.3	dB
f_{3dB}	8.3	12.9	10.3	1.15	GHz
A_{20GHz}	-34.9	-49.8	-42.9	3	dB
$V_{out,PP}$	741.2	825	783	12.9	mV
HD_2	-112.3	-63.3	-75.3	8	dB
HD_3	-46.4	-41.6	-44.5	0.8	dB
HD_5	-63.3	-53.4	-59.2	1.5	dB
THD	-46.2	-41.2	-44.3	0.9	dB
V_{noise}^{10GHz}	1.55	1.9	1.7	0.07	mVrms
V_{noise}^{20GHz}	2.51	3.4	2.88	0.17	mVrms
SNR_{10GHz}	43.5	45	44.3	0.3	dB

mainly due to variations in the bias current of the biquad cells.

The results of temperature variations are also reported in Table IV. When the temperature is varied from -30 to 120°C, the filter bandwidth changes from 9.9 to 10.3GHz, and gain ripple approaches 1dB. However, these variations can be easily counteracted by using a proportional to absolute temperature (PTAT) bias current in the biquad cells.

C. Process Variations and Mismatches

In order to verify the robustness of the circuit against process variations and mismatches, 200 Monte Carlo iterations have been carried out.

For these Monte Carlo simulations, accurate statistical models provided by the IC manufacturer have been exploited to model both process and mismatch variations for all the active and passive devices. Table V shows the results of the Monte Carlo simulations in which nominal supply voltage ($V_{CC} = 3V$) and nominal temperature $T = 27°C$ have been considered. Results confirm the robustness of the circuit.

VI. MEASUREMENT RESULTS

The test chip (see Fig. 11) including the filter described in Section IV has been mounted chip-on-board on a suitable substrate for testing, and in this Section we report the results of the measurements, including both the S-parameters and the response to single-tone and two-tone excitations.

A. Description of the Testbed

A test board has been designed and fabricated on a 10mil low-loss Rogers 4350B substrate. It includes lines for supply and dc bias, with filtering capacitors and potentiometers to set the currents, and connections to SMPM connectors, provided by 50Ω grounded coplanar lines designed by 3D EM simulations up to 50GHz. A discontinuity on the central strip of the coplanar line has been added to solder series decoupling microwave capacitors. Width and spacing of such lines are much larger than pad dimensions and pitch on the chip, thus requiring very long bonding wires: to improve the interface with the chip, allowing bonding with low losses, a 10mil interposer alumina board has also been designed.

The die is bonded to the alumina board, allowing thinner lines with small pitch to be designed, and low-loss short metal strips have been used to connect the lines on the alumina to the coplanar lines on the Rogers board. The back sides of both the alumina substrate and the Rogers board are metalized and grounded to a metal block, used also for mechanical support.

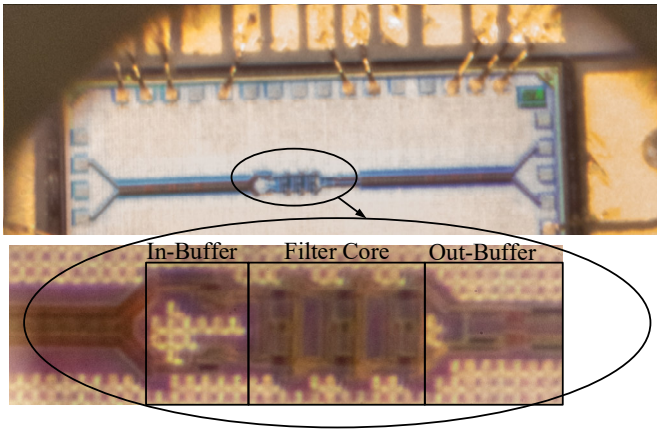

Fig. 11. Test-chip microphotograph.

S-parameters have been measured through an Anritsu 37397A vector network analyzer, using a dc-67GHz balun at the input and a dc-50GHz balun at the output of the filter.

In the test setup for linearity and noise measurements, a HP83650B signal generator with a dc-50GHz balun is used as signal source, and the output of the filter is sent to an Anritsu MS2668C spectrum analyzer, through a dc-20GHz balun, or to a Tektronix DSA8300 digital sampling oscilloscope.

For two-tone tests, a Rohde & Schwarz SMF100A signal generator and a dc-18GHz power combiner are used before the balun. The bandwidth of the measurement setup is therefore well beyond the 10GHz nominal bandwidth of the filter for all the considered tests. The circuit absorbs about 65mA from the 3V voltage supply, as expected from simulations.

B. VNA Test Results

The S-parameters of the filter have been measured by using the setup described above: the cut-off frequency of the filter is 10.3GHz and the low-frequency gain is about -0.6dB, mostly due to the output buffer (we have estimated and de-embedded about 7dB of setup losses). The attenuation at 20GHz is 43.5dB, and gain rises at higher frequencies up to an attenuation of 35dB. Measurements of S_{21} and S_{12} exhibit two resonances at 21 and 30GHz which are due to the test board.

The S_{21} is consistent with that of a 6th-order filter in the transition band from 10 to 20GHz, as the roll-off is 36dB per octave. Fig. 12 shows the measured S_{21} (setup losses have been de-embedded), and it includes also the frequency response of the custom filter reported in the last row of Table I from ideal Matlab™ simulations, to show the good agreement between the actual and the desired filter frequency response.

Fig. 13 reports the frequency response of the whole ATI digitizer (as in Fig. 3) with LPF filters implemented as an ideal low-pass filter, the optimized custom 6th-order filter (ideal response) and the optimized custom 6th-order filter (measured response) showing how the measured filter response results in a response of the ATI system very close to the ideal one.

Fig. 14 shows the S_{12} and the S_{11} and S_{22} of the filter from 0 to 50GHz. Input and output matching remain below -15dB in the filter band from 0 to 10GHz, and rise to -10 and -8dB,

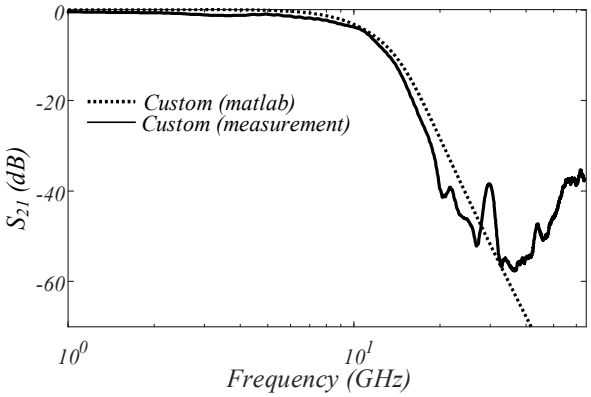

Fig. 12. Measured S_{21} of the filter, (about 7.5dB losses of the measurement setup due to cables and baluns have been de-embedded).

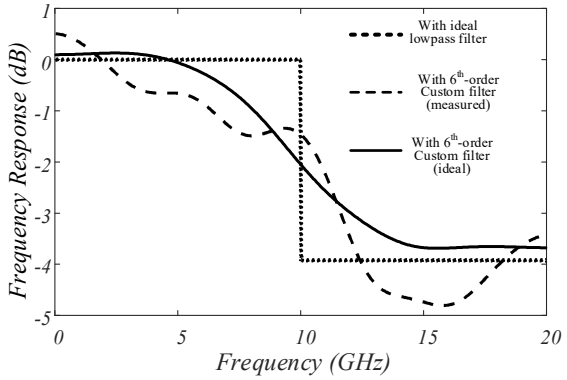

Fig. 13: Frequency response of a $40GS/s$ ATI digitizer with LPF filters implemented as an ideal low-pass filter, the optimized custom 6th-order filter (ideal response) and the optimized custom 6th-order filter (measured response).

respectively, at 20GHz. This is probably due to passive coupling effects, as similar effects are present in the S_{21} and S_{12} plots, and may not be due to the IC but to the board (either the internal one in Alumina or the external one in Rogers).

C. Distortions and Noise

Fig. 15 shows the large signal S_{21} of the test chip vs. input power at 1GHz and 9GHz (normalized with respect to the value at $P_{IN} = -13dBm$). The input 1dB compression point is about 6.3dBm at 1GHz and 1dB lower at 9GHz. Fig. 16 reports the THD with an input tone at 2GHz. The filter shows about -45dB of THD with about -2dBm input power.

A two-tone test with input frequencies at 1.9 and 2GHz has been performed for several input power levels. Results of a typical 3rd-order intercept point (IP3) linearity test are reported in Fig. 17. The output IP3 (OIP3), measured with two tones at 1.9 and 2GHz, is about 16.75dBm, that is in good agreement with the simulated value of 17dBm.

The total measured output noise has a rms value of $1.6mV_{rms}$, which is in reasonable agreement with the simulations of V_{noise}^{10GHz} reported in Table III. Fig. 18 shows the simulated output noise spectrum with superimposed measured results in the 6-13 GHz bandwidth.

Fig 19 shows the plots of SDR, SNR and $2SNR$ versus the input power: the SDR and the $2SNR$ plots cross each other around -2.4dBm input power, which corresponds to about

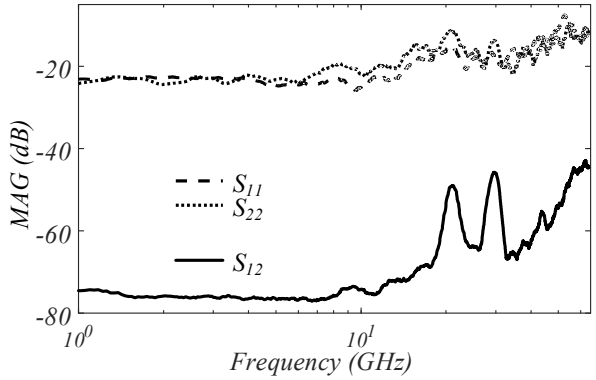

Fig. 14. Measured S_{12}, S_{11} and S_{22} of the filter, (about 7.5dB losses of the measurement setup due to cables and baluns have been de-embedded).

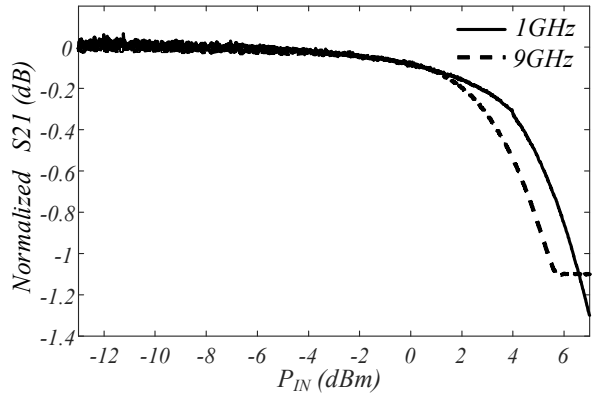

Fig. 15. Large signal S_{21} at 1GHz and 9GHz vs. input power.

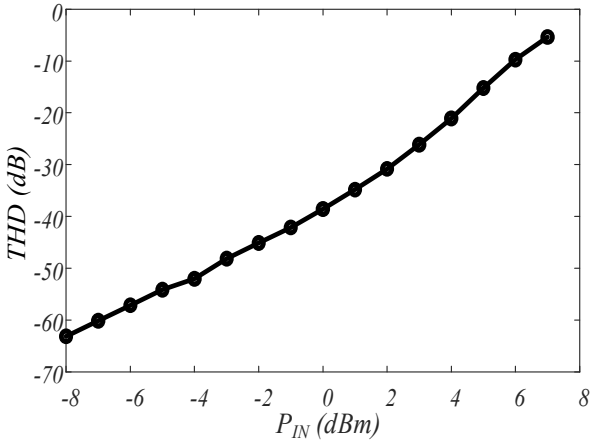

Fig. 16. THD vs. input power at 2GHz.

170mV peak single ended input signal, and the corresponding optimum Dynamic Range (DR) is 41.6dB. Measured output noise is lower than simulated, and this justifies a higher DR with a lower optimum input power.

D. Comparison against the State-of-the-Art

A comparison against the state-of-the-art of multi-GHz low-pass filters is reported in Table VI, where the following figures of merit (FOM) are reported for the different implementations:

$$FOM_1 = \frac{P_{diss}}{N_{pole}}, \quad (37a)$$

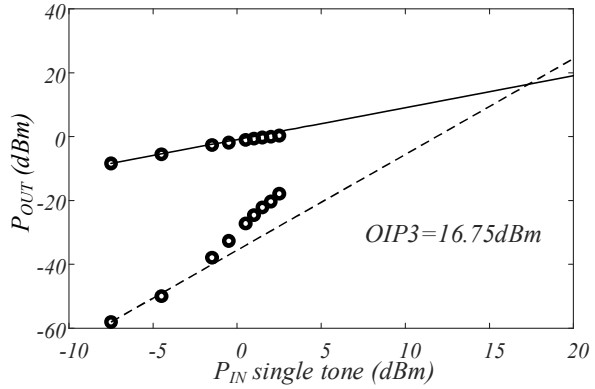

Fig. 17. IP3 plot at 2GHz.

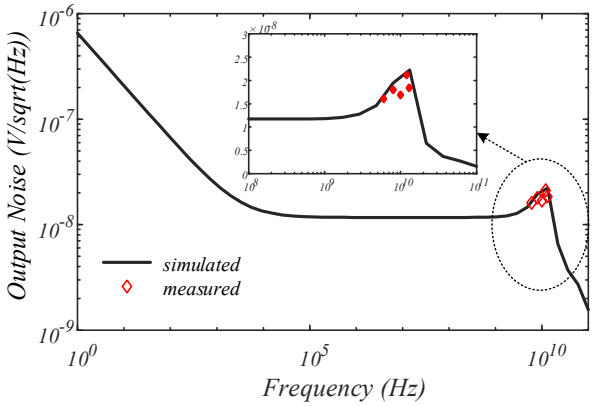

Fig. 18. Simulated and measured output noise spectrum.

$$FOM_2 = \frac{P_{diss}}{N_{pole} f_{3dB}}, \quad (37b)$$

$$FOM_3 = \frac{P_{diss}}{N_{pole} f_{3dB} 10^{DR/10}}, \quad (37c)$$

where P_{diss} and N_{pole} are the power dissipation and the number of poles of the filter respectively.

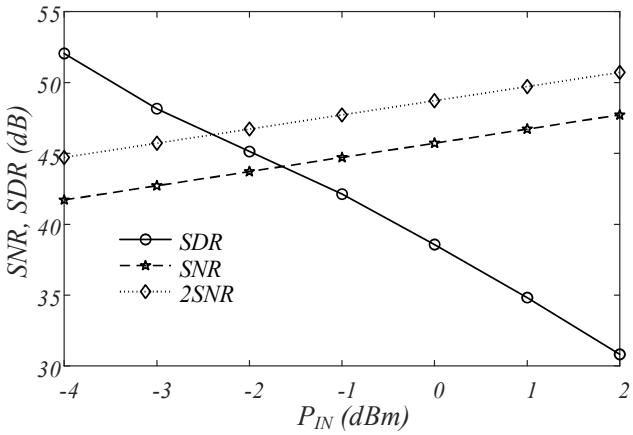

Fig. 19. Linearity and noise vs input signal power.

From Table VI it is evident that only references [18] and [23] achieve a cut-off frequency around *10GHz* and that this work outperforms [18] and [23] in terms of FOM_1 and FOM_2. The filter in reference [23] has a better FOM_3 than the one reported in this work and this is mainly due to the higher *DR* obtained thanks to the closed-loop implementation; however [23] refers to a single biquad stage and no measured results are reported.

The CMOS implementations in Table VI exhibit lower power consumption, but their cut-off frequency is below 5GHz.

For what concerns the area footprint, the proposed filter has the lowest area per pole among the high-order (5th or 6th) filters.

VII. Conclusion

In this paper, we have presented the design of a 6th-order low-pass filter with 10GHz cut-off frequency implemented in a SiGe 55nm BiCMOS technology from STMicroelectronics.

Starting from a theoretical analysis of the frequency response, noise and distortions of the basic biquadratic cell, we

TABLE VI
COMPARISON WITH THE LITERATURE

	This Work	[18]	[19]	[20]	[21]	[23]	[26]	Unit
Technology	BiCMOS 55nm	CMOS 65nm	BiCMOS 250nm	CMOS 28nm	BiCMOS 180nm	BiCMOS 55nm	CMOS 180nm	-
Number of poles N_{pole}	6	3	5	5	6	2	5	-
Measurements available	Y	Y	Y	Y	Y	N	N	-
Supply voltage	3	1.4	3.5	1.1	3.3	3	1.8	V
Power dissipation P_{diss}	43	140	100	30	300	18	1.6	mW
Cut-off frequency f_{3dB}	10.3	10	4.1	3.3	3.2	9.5	4.6	GHz
DC gain A_{dc}	-0.2	1.3	-6.8	-1	11.1	-0.5	5.2	dB
Input power level P_{in}^{Q}	-1	-10.6	-18	-17	-11.1	-1	-19	dBm
Input noise power P_n	-45.9	-56	-40.1	-56	-	-46.8	-44.8	dBm
Signal to noise ratio SNR at P_{in}^{Q}	44.7	45.4	22.1	39	-	45.8	25.7	dB
Total Harmonic Distortion THD at P_{in}^{Q}	-42.6	-45	-25	-40	-40	-64	-56.9	dB
Output 3rd-order intercept point $OIP3$	16.7	6.3	-12.3	-2	13.1	30.5	14.7	dBm
Maximum Dynamic Range DR	41.6	42.5	20.3	36.6		49.1	30.7	dB
Total filter area	0.02	0.01	-	0.09	0.17	0.0027	-	mm^2
Area per pole	0.003	0.003	-	0.018	0.028	0.0014	-	mm^2
FOM_1	7.2	47	20	6	50	9	0.32	mW
FOM_2	0.69	4.7	4.9	1.8	15.6	0.95	0.07	$\frac{pW}{Hz}$
FOM_3	48.14	262.43	45524	401.46		11.66	58.83	$\frac{aW}{Hz}$

have derived useful design equations and a simple design flow which allows sizing all the circuit parameters according to the specified DR and V_{FS} of the whole filter and the A_{dc}, ω_o and Q of the biquad stages.

Parametric and Monte Carlo post-layout simulations have been carried out to assess the robustness of the implemented filter to PVT variations and mismatches. Measurements on the test chip manufactured in the STM BiCMOS55 technology have resulted in a very good agreement between measured and simulated performance, confirming the effectiveness of the proposed design flow.

Power consumption is less than 43mW, THD and SNR are about -43dB and 45dB, respectively, with an input signal amplitude of about 800mV peak-to-peak differential, and the maximum dynamic range of 41.6dB is achieved for -2.4dBm input power.

Based on the comparison against the state of the art reported in Table VI, the proposed architecture, which exploits positive feedback to synthesize an active inductor and resistive degeneration of the differential pair to improve linearity, shows very low power consumption, exhibiting the best FOM1 and FOM2 with respect to all the filters approaching 10GHz bandwidth. Moreover, the use of an active inductor has resulted in a very low silicon area footprint, further simplifying integration in complex systems.

APPENDIX

In this Appendix we compute the optimal input power $P_{I,opt}$ (optimal input amplitude $\hat{V}_{I,opt}$) which maximizes the signal-to-noise-and-distortion ratio ($SNDR$) resulting in optimal dynamic range (DR). Denoting with P_I, N, G and $\delta G P_I^3$ the input power, the equivalent input noise power, the power gain and the third harmonic component of the output power, respectively, the signal-to-noise ratio (SNR), the signal-to-distortion ratio (SDR), and $SNDR$ can be written as follows:

$$SNR = \frac{P_I}{\mathrm{N}}, \tag{A1}$$

$$SDR = \frac{GP_I}{\delta G P_I^3} = \frac{1}{\delta P_I^2}, \tag{A2}$$

$$SNDR = \frac{P_I}{N+\delta P_I^3}. \tag{A3}$$

Then, to find $P_{I,opt}$ we compute the derivative of $SNDR$ in (A3) with respect to P_I and equate it to zero, obtaining:

$$P_{I,opt} = \left(\frac{N}{2\delta}\right)^{1/3}. \tag{A4}$$

Finally, substituting (A4) in (A1) and (A2) we find:

$$SNDR\left(P_{I,opt}\right) = \frac{1}{3} SDR\left(P_{I,opt}\right) = \frac{2}{3}\, SNR\left(P_{I,opt}\right) \tag{A5}$$

$$SDR\left(P_{I,opt}\right) = 2\, SNR\left(P_{I,opt}\right). \tag{A6}$$

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