IEEE Open Journal of
Circuits and Systems

Received 26 April 2021; revised 30 June 2021; accepted 14 July 2021. Date of publication 27 July 2021; date of current version 2 August 2021.

Digital Object Identifier 10.1109/OJCAS.2021.3098055

A Detailed Model of the Switched-Resistor Technique

FRANCESCO CENTURELLI (Member, IEEE), ALESSANDRO FAVA,

GIUSEPPE SCOTTI (Senior Member, IEEE), AND ALESSANDRO TRIFILETTI

Department of Information Engineering, Electronics, and Telecommunication, University of Rome La Sapienza, 00184 Rome, Italy

This article was recommended by Associate Editor Y. Dong.

CORRESPONDING AUTHOR: G. SCOTTI (e-mail: giuseppe.scotti@uniroma1.it)

ABSTRACT The Switched-Resistor (S-R) approach is gaining popularity among integrated circuits designers because it allows to implement very high equivalent resistances, and thus very large time constants, in CMOS circuits. In this paper, we present an in-depth analysis of the S-R technique and propose a novel detailed model which allows to accurately predict the value of the equivalent resistance even for values of the duty cycle as low as 0.0001% which result in a huge resistance multiplication factor. We show that the conventional model of the S-R technique provides a reasonable accuracy for duty cycle values down to 1%, but its accuracy becomes unacceptable for smaller values of the duty cycle. In the proposed detailed model of the S-R we take into account also the parasitic capacitances of the integrated poly resistors and the non-ideal resistance of the CMOS switches. The modeling strategy is based on the solution of the differential equations for the different switches settings and exploits the Y-matrix to represents the floating S-R. The proposed model has been validated against periodic steady state (PSS) and periodic AC (PAC) simulations referring to a 130nm CMOS technology. Results have shown an average and maximum error lower than 0.53% and 5.15% respectively. As a further validation, a first-order active low-pass filter has been implemented with the same technology with a cutoff frequency tunable from 1.68Hz to 1.46kHz. The average and maximum errors in the estimation of the cutoff frequency have resulted lower than 3.6% and 7% respectively.

INDEX TERMS Biomedical applications, large time constants, integrated circuits, switched-resistor, S-R modeling.

I. INTRODUCTION

INTEGRATED filters and front-end amplifiers for audio, IoT and biomedical applications require high resistance values to implement the required very large time constants. Referring to biomedical applications, front-end amplifiers for neural recording systems often rely on AC coupling with very low cut off frequencies (below 1Hz) in order to remove the DC offset of the electrodes and to properly process the neural signals [1]–[2]. Such systems are typically designed to cover different bandwidths in the range from 1Hz to 10kHz. For example, in the case of epileptic seizure detection, band-pass filters with a bandwidth from 250Hz to 500Hz and a sharp frequency response are required to extract the signals of interest [3]–[4].

Designers of CMOS integrated circuits typically rely on the Switched-Capacitor [5] or the pseudo-resistor [6]–[8] approaches to implement large resistance values. However, it has to be noted that, in switched-capacitor implementations, the resistance value is tuned by varying the clock frequency thus changing also the sample rate of the system, and this can be a disadvantage in many applications. On the other hand, pseudo-resistors are typically tuned over a wide range by changing the gate-source voltage. When using this technique, the value of the equivalent resistance is very sensitive to the common mode voltage and to PVT variations and a limited linearity performance has to be expected [9].

The Switched-Resistor (S-R) approach is becoming more and more popular within the community of integrated circuits designers, because it allows implementing very high resistances whose value can be tuned over several decades by adjusting the duty cycle of the clock signal without modifying the sample rate of the system. These characteristics are very attractive to implement large time constants in integrated circuits for IoT [10]–[11] and biomedical applications [1]–[8] and for a wide set of very low power integrated circuits such as for example analog to digital converters [12]. The Switched-Resistor approach has been

exploited in [13]–[16] to implement tunable filters and analog front-ends for biomedical integrated circuits. The value of the duty cycle adopted in [13] and [14] is in the range of 10% to 75% whereas a much lower value is used in [15]–[17].

In this paper we demonstrate that the conventional model adopted for the S-R is inaccurate for values of duty cycle below 1% and propose a new analytic model of S-R which is able to describe, in an accurate way, all the main parasitic effects due to the involved devices (e.g., MOS switches and polysilicon resistors). The proposed model is very accurate even for duty cycle values as low as 0.0001% and allows to properly model both grounded and floating resistors implemented by using very small duty cycles resulting in a huge resistance multiplication factor.

The paper is structured as follows. Section II reviews the basic principle of S-R approach and the conventional model. The proposed detailed model is introduced and explained in Section III referring firstly to a grounded S-R and then to a floating S-R. The implementation of a first-order active low-pass filter with a cutoff frequency tunable from 1.68Hz to 1.46kHz is presented in Section IV and used to perform a further validation of the proposed detailed model. Conclusions are finally drawn in Section V.

II. REVIEW OF THE SWITCHED-RESISTOR TECHNIQUE

The scheme of the well-known S-R architecture is depicted in Fig. 1. The conventional S-R model [13]–[17] is based on a MOSFET switch, characterized by its on resistance R_{on}, in series with an ideal poly resistor R_p. (The off-state resistance of the switch R_{off} is assumed to be infinite).

A duty cycle controlled clock is applied to the MOSFET gate to set the *average* current that flows in the series. The assumptions of this model lead to neglect the current in the off-state of the switch and therefore the average current depends only on the current that flows during the on-state of the switch:

$$I_{avg} = \frac{1}{T_s}\int_0^{\delta Ts} \frac{V1 - V2}{R_p + R_{on}}\, dt = \delta \frac{V1 - V2}{R_p + R_{on}} \tag{1}$$

where δ is the duty cycle and V_1 and V_2 the voltages on the terminals of the S-R, as shown in Fig. 1. The equivalent resistance is then obtained as:

$$R_{eq} = \frac{R_p + R_{on}}{\delta} \tag{2}$$

It is evident from the above equations that the conventional model completely neglects the parasitic current flowing through the TG switch in the off-state, the currents flowing through the parasitic capacitances and the current flowing in the bulk terminals of the devices implementing the TG switch. Furthermore, this model assumes that in the on-state all the current flows through the switch and the resistor, so that the current entering at node 1 is equal to the current exiting from node 2 and therefore it can be enough accurate only when the average current flowing through the resistor is much larger than the sum of all the parasitic currents.

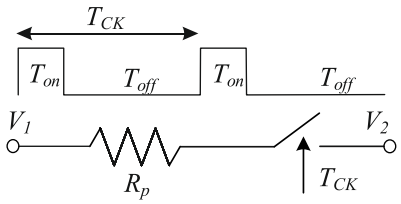


FIGURE 1. Switched-Resistor ideal circuit.

In order to quantitatively test the accuracy of the conventional S-R model, we have implemented a switched-resistor referring to a commercial 130nm CMOS technology. In particular we have implemented a 500kΩ, high resistivity poly (hipo) resistor, taken from the technology library, followed by a transmission gate (*TG*) acting as switch (Wn/Ln = 150nm/130nm and Wp/Lp = 150nm/130nm) implemented with the low leakage PMOS and NMOS devices.

Periodic steady state (*PSS*) and periodic AC (*PAC*) simulations within the Cadence Virtuoso™ environment have been exploited to estimate the equivalent resistance (and therefore the equivalent conductance) as a function of the duty cycle δ.

In order to estimate the rise and fall times (T_{rise} and T_{fall} respectively) of realistic clock waveforms, we have carried out some simulations in which the CMOS NOT gates taken from the digital library of the 130nm technology have been used to drive the clock inputs of the TG switches adopted in our S-R implementations. The rise and fall times have been found lower than 30ps, and according to this result we have chosen a clock frequency of 10kHz and pushed the duty cycle down to 0.0001% in order to have a $T_{on} = \delta * T_{ck} = 100\text{ps} > (T_{rise} + T_{fall})$.

The simulation setup and the tolerance settings of PSS and PAC simulations have been carefully analyzed and verified against several examples with fully known behavior. We have found that a simulation setting parameter which is very important for the simulation accuracy is the number of harmonics in the PSS simulation. In fact, since the clock of the S-R is a square wave with steep edges, a very high number of harmonics of the clock fundamental frequency is required to fully describe the commutations of the TG switch. Extensive simulation analysis allowed us to set the number of harmonics to 60000 which resulted in sufficient simulation accuracy for all the considered duty cycle values.

The equivalent conductance of the S-R predicted by the conventional model in equation (2) and by means of the *PSS+PAC* simulations are reported in Fig. 2a, whereas the relative error of the model with respect to simulations is shown in Fig. 2b. By looking at Fig. 2, it is evident that the accuracy of the model in (2) starts to decrease when the duty cycle is reduced below 1%. This fact demonstrates that the conventional model is not adequate to represent the behaviour of the S-R for low duty cycles.

This strongly limits the usability of the conventional model for high resistance multiplication factors which are very important for most applications. As it will be better shown

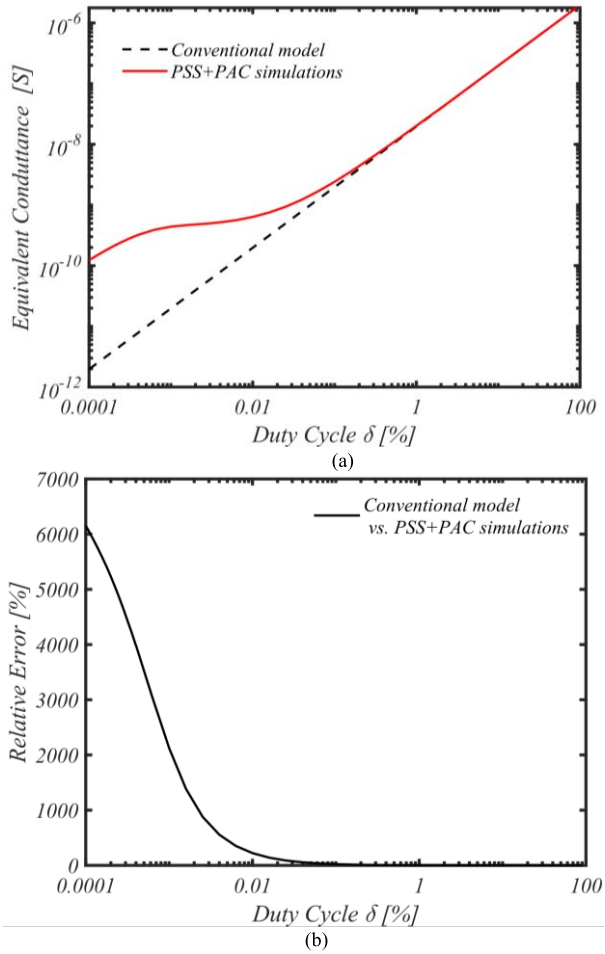


FIGURE 2. Switched-Resistor conventional model: (a) comparison with the experimental Switched-Resistor; (b) relative error of the conventional model with respect to the simulated Switched-Resistor.

in the following, the large relative error obtained in Fig. 2b for low duty cycles can be explained by two main parasitic effects which are not taken into account:

1) the parasitic current loss in the parasitic capacitances of both the poly resistor and the MOS switches;
2) the current flowing in the off-state, due to the finite value of the off-state resistance R_{off} of the MOS switches.

III. PROPOSED DETAILED MODEL OF THE SWITCHED-RESISTOR

A more detailed and accurate model of the S-R can be obtained by accounting also for parasitic capacitances and off-state resistances as shown in Fig. 3. In Fig. 3, the polysilicon resistor is represented by its resistance R_p and two parasitic capacitances $C_{p1,2}$ whose value is dependent on R_p [18]. The *TG* MOS switch is characterized by the parasitic resistances R_{on}/R_{off} which denote its *on/off*-state equivalent resistances and by two parasitic capacitances $C_{TG1,2}$.

We have computed the values of the parameters of the model in Fig. 3 for the S-R implemented in the 130nm

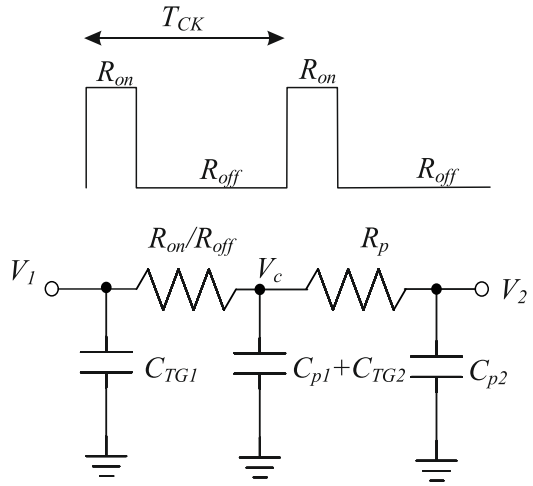


FIGURE 3. Proposed detailed model of the Switched-Resistor.

CMOS technology and adopted in Section II to quantify the accuracy of the conventional model.

From the simulations we have seen that the *TG* switch provides parasitic capacitances $C_{TG1,2}$ in the range of 0.1fF, whereas the $500k\Omega$, hipo resistor exhibits parasitic capacitance $C_{p1,2}$ of about 45.1fF. Finally, the parasitic resistances R_{on}/R_{off} of the *TG* switches have been computed as $7.34k\Omega/166G\Omega$ respectively.

It is evident from Fig. 3 that the current flowing into the terminal V_1 of the S-R will be different from the current flowing out of the terminal V_2. In the general case, the S-R has thus to be modeled not as a bipole but as a 2-port network. We will initially consider the case of a grounded resistor (i.e., $V_2 = 0$) to illustrate the development of the model, and will then develop the complete model of the floating resistor.

A. MODELING A GROUNDED SWITCHED-RESISTOR

In this subsection we start with the model of a grounded S-R, where V_2 is grounded and V_1 is given by the signal voltage V_{sig}. In the following analysis, we assume a constant V_{sig} and therefore we neglect the capacitor C_{TG1}, in parallel to V_1. However the effect of C_{TG1} can be always added in parallel to the S-R model that we are going to derive.

Being the S-R a switched system, the average current is determined considering the two equivalent circuits corresponding to the *on*- and *off*-state of the switch as shown in Fig. 3. In our approach we determine for each state the voltage V_c in the "s" domain as follows:

$$V_{c_{on}} = V_{sig}(s)\frac{R_p}{R_p + R_{on}} * \frac{1}{1 + s\tau_{on}} \tag{3}$$

where $\tau_{on} = (C_{p1} + C_{TG2})(R_{on}//R_p)$

$$V_{c_{off}} = V_{sig}(s)\frac{R_p}{R_p + R_{off}} * \frac{1}{1+s\tau_{off}} \tag{4}$$

where $\tau_{off} = (C_{p1} + C_{TG2})(R_{off}//R_p)$

Since we are assuming a constant signal $V_{sig} = V_s$ and an ideal clock, we can exploit the Laplace inverse transform to obtain the time domain expressions:

$$V_{c_{on}}(t) = V_s\ \alpha_{on}\ \left(1 - e^{-\ \frac{t}{\tau_{on}}}\right) + \mathrm{V_c(0)e^{-\frac{t}{\tau_{on}}}} \tag{5}$$

$$V_{c_{off}}(t) = V_s\ \alpha_{off}\left(1 - e^{-\ \frac{t}{\tau_{off}}}\right) + \mathrm{V_c(\delta T_{ck})e^{-\frac{t}{\tau_{off}}}} \tag{6}$$

where $\alpha_{on} = \frac{R_p}{R_p+R_{on}}$; $\alpha_{off} = \frac{R_p}{R_p+R_{off}}$.

Furthermore, since the initial voltage on the parasitic capacitances is unknown, the initial conditions are necessary to describe the phenomena that depend on the previous cycle states. At this purpose we set the following conditions:

$$\begin{cases} V_{c_{on}}(0) = V_{c_{off}}(T_{ck}) \\ V_{c_{on}}(\delta T_{ck}) = V_{c_{off}}(\delta T_{ck}) \end{cases} \tag{7}$$

After solving the system in (7) we can derive the initial conditions as follows:

$$V_c(0) = V_s\left[\frac{\alpha_{off}\left(1-e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)+\alpha_{on}\left(1-e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}}{\left(1-e^{-\frac{\delta T_{ck}}{\tau_{on}}} * e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)}\right] \tag{8}$$

$$V_c(\delta T_{ck}) = V_s\left[\alpha_{on}\left(1 - e^{-\ \frac{\delta T_{ck}}{\tau_{on}}}\right) + \frac{\alpha_{off}\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right) + \alpha_{on}\left(1 - e^{-\ \frac{\delta T_{ck}}{\tau_{on}}}\right)e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}}{\left(1 - e^{-\ \frac{\delta T_{ck}}{\tau_{on}}} * e^{-\ \frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)} * \mathrm{e^{-\frac{\delta T_{ck}}{\tau_{on}}}}\right] \tag{9}$$

Then we can determine the expression of the equivalent resistor (R_{S-R}) by computing the average current that flows in R_p and $C_p = \left(C_{p1} + C_{TG2}\right)$ in a clock period:

$$I_{avg} = \frac{1}{T_{ck}}\left[\int_0^{\delta Tck}\left(C_p\frac{dV_{c_{on}}(t)}{dt} + \frac{V_{c_{on}}(t)}{R_p}\right)dt + \int_{\delta T_{ck}}^{T_{ck}}\left(C_p\frac{dV_{c_{off}}(t)}{dt} + \frac{V_{c_{off}}(t)}{R_p}\right)dt\right] \tag{10}$$

Since the average current in (10) is the sum of two contributions (the first referred to the *on* state and the second to the *off*-state), the equivalent resistance can be calculated as two resistances in parallel, the first ($R_{S-R_{on}}$) is related to the current flowing when the switch is close, whereas the second $R_{S-R_{off}}$ is related to the small current flowing when the switch is open:

$$R_{S-R} = \frac{V_s}{I_{avg}} = R_{SR_{on}} // R_{SR_{off}} \tag{11}$$

$$R_{S-R_{on}} = \frac{R_p}{\delta\ \alpha_{on} + F_{ck}\left[\left(\tau_{on} - C_pR_p\right)\left(V_{anc}(0) - \alpha_{on}\right)\right]\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)} \tag{12}$$

$$R_{S-R_{off}} = \frac{R_p}{(1-\delta)\ \alpha_{off} + F_{ck}\left[\left(\tau_{off} - C_pR_p\right)\left(V_{anc}(\delta T_{ck}) - \alpha_{off}\right)\right]\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)}, \tag{13}$$

where $V_{anc}(0) = \frac{V_c(0)}{V_s}$ and $V_{anc}(\delta T_{ck}) = \frac{V_c(\delta T_{ck})}{V_s}$.

In order to quantitatively test the accuracy of the proposed detailed S-R model we have considered the same S-R used to test the validity of the standard model (thus the simulated curve in Fig. 4a is the same than in Fig. 2a) and we have compared the results of PSS+PAC simulations with respect to the conductance $(R_{S-R})^{-1}$, computed from (11). The simulation parameters are the same adopted in Section II. The results of this comparison are reported in Fig. 4a to show how the detailed model fits very well with the behavior of the simulated Switched-Resistor. Fig. 4b reports the relative error of the detailed model which results lower than 2% even for duty cycle values as low as 0.0001%.

A comparison of the proposed model against the conventional one shows how it is able to reproduce the simulated curve even when it starts differing from the linear behaviour.

In particular, by looking at the detailed model in Fig. 3 it can be understood that, due to the parasitic capacitance C_{p1}, a part of the current flowing through the *TG* is steered toward ground so that the current flowing through the resistor R_p is scaled by a factor $(1 - e^{-\ \frac{\delta T_{ck}}{\tau_{on}}})$.

This effect becomes dominant when the duty cycle decreases and explains the behaviour of the conductance curve in Fig. 2a.

B. FLOATING SWITCHED-RESISTOR

In this subsection we consider the model of the generic floating S-R. As stated in the previous subsection, in the general case, the S-R has to be modeled as a 2-port network to take into account the difference of the currents at the two terminals.

The 2-port network can be described by means of different kinds of parameters and we adopt the Y parameters to develop our model. The choice of the Y-matrix allows to easily include the capacitances in parallel to port 1 and port 2 of the network (e.g., C_{TG1} and C_{p2} in Fig. 3) after having developed the model of the internal part of the circuit (see Fig. 5).

The parameters of the Y-matrix can be written as follows:

$$Y11 = \left.\frac{I_1}{V_1}\right|_{V_2=0} = Y11_{on} + Y11_{off} \tag{14}$$

$$Y21 = \left.\frac{I_2}{V_1}\right|_{V_2=0} = Y21_{on} + Y21_{off} \tag{15}$$

$$Y12 = \left.\frac{I_1}{V_2}\right|_{V_1=0} = Y21_{on} + Y21_{off} \tag{16}$$

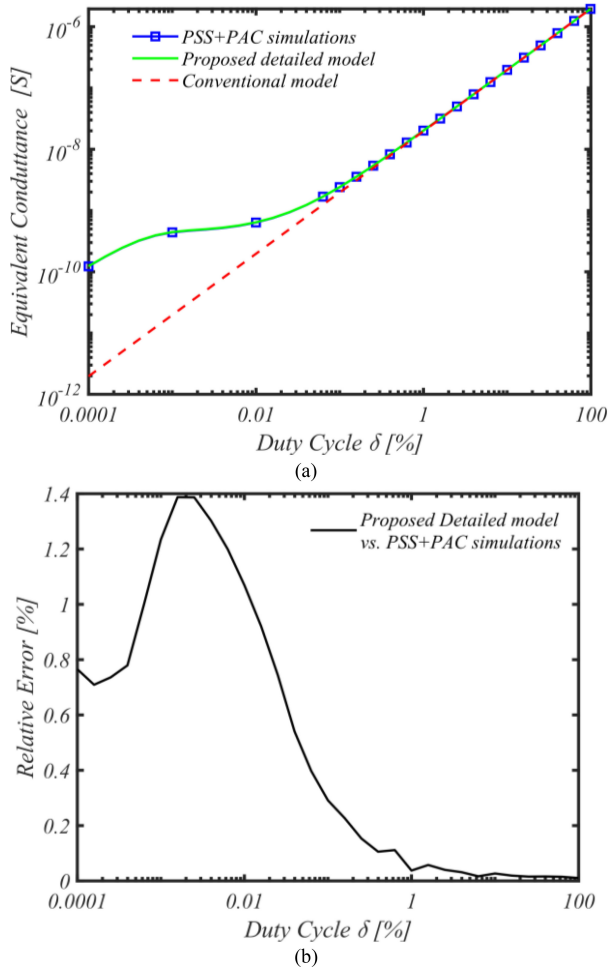


FIGURE 4. Proposed Switched-Resistor detailed model: (a) comparison between PSS+PAC simulations and conventional model; (b) relative error of the proposed detailed model against PSS+PAC simulations.

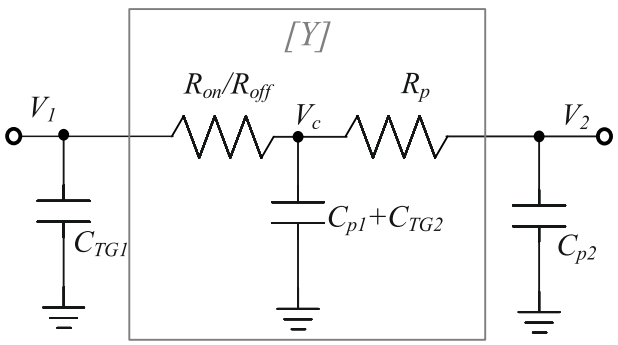


FIGURE 5. Y-parameters model of the floating Switched-Resistor.

$$Y22 = \left.\frac{I_2}{V_2}\right|_{V_1=0} = Y22_{on} + Y22_{off} \tag{17}$$

The Y11 parameter has been already calculated in the previous subsection (Grounded S-R model) and is equal to $1/R_{S-R}$, whereas the other parameters can be computed in a similar manner, according to their definition, as shown below:

$$Y21_{on} = -\frac{\delta\,\alpha_{on} + [F_{ck}\tau_{on}(V_{anc}(0) - \alpha_{on})]\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)}{R_p} \tag{18}$$

$$Y21_{off} = -\frac{(1-\delta)\alpha_{off} + [F_{ck}\tau_{off}(V_{nc}(\delta T_{ck}) - \alpha_{off})]\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)}{R_p} \tag{19}$$

$$Y22_{on} = \frac{\delta\beta_{on} + F_{ck}[(\tau_{on} - C_pR_{on})(V_{bnc}(0) - \beta_{on})]\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)}{R_{on}} \tag{20}$$

$$Y22_{off} = \frac{(1-\delta)\beta_{off} + F_{ck}[(\tau_{off} - C_pR_{off})(V_{bnc}(\delta T_{ck}) - \beta_{off})]\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)}{R_{off}} \tag{21}$$

$$Y12_{on} = -\frac{\delta\beta_{on} + [F_{ck}\tau_{on}(V_{bnc}(0) - \beta_{on})]\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)}{R_{on}} \tag{22}$$

$$Y12_{off} = -\frac{(1-\delta)\beta_{off} + [F_{ck}\tau_{off}(V_{bnc}(\delta T_{ck}) - \beta_{off})]\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)}{R_{off}} \tag{23}$$

where we define $V_{bnc}(0)$, $V_{bnc}(\delta T_{ck})$, β_{on}, β_{off} as follows:

$$V_{bnc}(0) = \left[\frac{\beta_{off}\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right) + \beta_{on}\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}}{\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}} * e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)}\right] \tag{24}$$

$$V_{bnc}(\delta T_{ck}) = \left[\beta_{on}\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right) + \frac{\beta_{off}\left(1 - e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right) + \beta_{on}\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right)e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}}{\left(1 - e^{-\frac{\delta T_{ck}}{\tau_{on}}} * e^{-\frac{(1-\delta)T_{ck}}{\tau_{off}}}\right)} e^{-\frac{\delta T_{ck}}{\tau_{on}}}\right] \tag{25}$$

$$\beta_{on} = \frac{R_{on}}{R_p + R_{on}};\ \beta_{off} = \frac{R_{off}}{R_p + R_{off}} \tag{26}$$

An interesting consideration that can be done looking at the equations derived above is related to the maximum equivalent resistance that can be realized by a S-R in the limit case of zero duty cycle. In fact, if we consider $\delta \to 0$, then $Y_{ij_{off}} > Y_{ij_{on}}$ and the value of the equivalent resistance is set by the off-state resistance of the switch R_{off}. In other words, the average current in off-state is much larger than the average current in the on-state.

The Y-parameters curves obtained for the proposed model are compared with the simulated S-R in Fig. 6. The simulation parameters are the same used in Section II. All the Y-parameters of the model fit the simulated curves with a maximum error lower than 5.15% and an average error lower than 0.53%.

It has to be noted that further parasitic effects are present in a real S-R implementation: in particular we can mention the channel charge injection and clock feedthrough effects associated with the switch [19]–[21].

The channel charge injection is associated to the switch changing from the on- to off-state and vice versa: charge is absorbed by the switch to form the conducting channel and released when the devices enter the cutoff region,

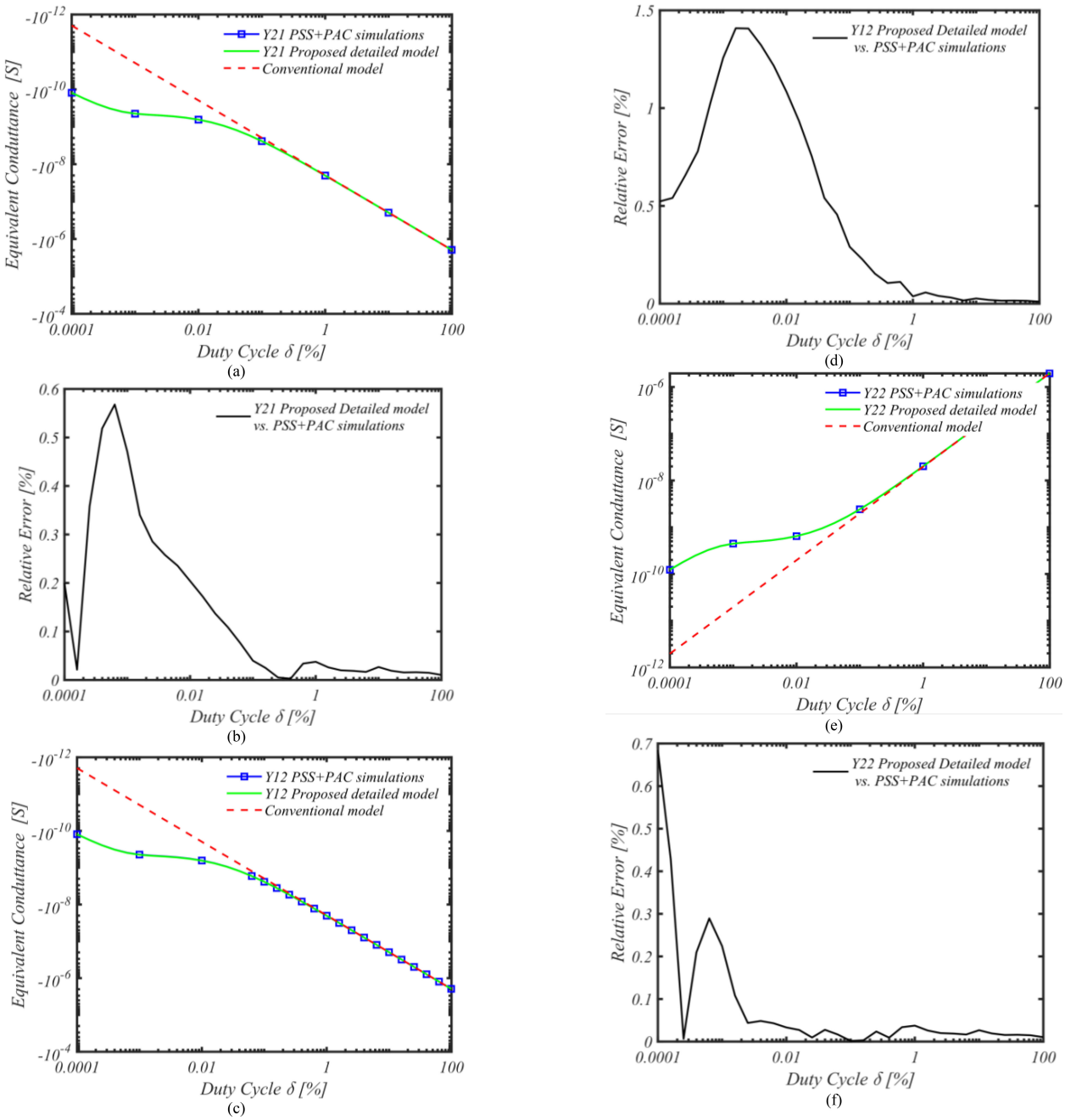


FIGURE 6. Y-parameters validation: (a-c-e) Comparison Y-parameters with Switched-Resistor simulations and conventional model; (b-d-f) relative error of model for each Y-parameter.

thus altering the voltage on the parasitic capacitances C_{TG1} and C_{TG2}. The clock feedthrough is related to the edges of the clock signal that affect such parasitic capacitances through the internal capacitances of the MOS devices. Both these effects can be modeled by a voltage ΔV to be added to the initial conditions (8) and (9); however for practical implementations of the S-R their effect is negligible, resulting in an average current in the order of fA, as also shown by the good fitting of the proposed model.

As a further validation, post-layout simulations of the switched-resistor have been carried out. The two CMOS inverters driving the TG switch have been included in the layout to account for realistic clock waveforms. Post-layout simulations results show very limited variations of the Y parameters with respect to pre-layout ones, which are mainly due to the CMOS inverters and to additional parasitic capacitance of the layout. The error of the proposed accurate model with respect to post-layout simulations has been found to be below 1.5%.

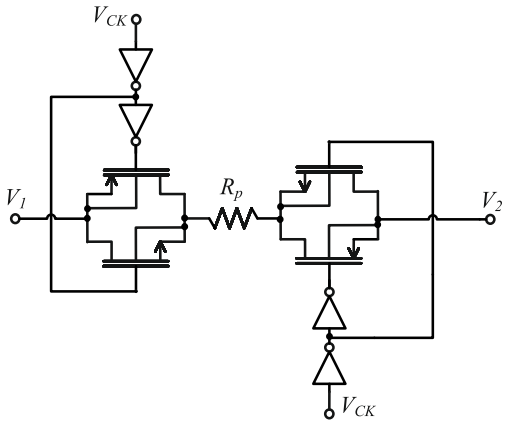


FIGURE 7. Proposed symmetrical S-R topology.

C. SYMMETRICAL SWITCHED-RESISTOR

The S-R Y-model derived above does not take into account the parasitic capacitances C_{p2} and C_{TG1} shown in Fig. 5. Since these capacitances are in parallel with the Y11 and Y22 parameters, the Y-matrix including the parasitic capacitances can be easily derived as follows:

$$Y_{S-R} = \begin{bmatrix} Y11 + sC_{TG1} & Y12 \\ Y21 & Y22 + sC_{p2} \end{bmatrix} \quad (27)$$

It has to be noted that the Y-matrix of an ideal floating resistor is symmetrical with diagonal elements equal to each other (i.e., $Y11 = Y22$ and $Y12 = Y21$) and therefore these properties of the Y-matrix of a S-R are fundamental to achieve an accurate emulation of the floating resistor behavior.

By inspecting the Y_{S-R} matrix in (27) it is evident that $Y11_{S-R}$ and $Y22_{S-R}$ are not equal to each other end therefore the Y_{S-R} matrix does not represent an ideal floating resistor.

Starting from this observation we propose a simple modification to the basic S-R topology in order to design a fully symmetric S-R. The proposed S-R topology is reported in Fig. 7, showing how an additional *TG* can be exploited to improve the floating resistor symmetry and performance.

The model of the circuit in Fig. 7 can be easily derived by using the Bartlett's theorem on the symmetrical structures after splitting R_p into two series resistors each equal to $R_p/2$. In fact, starting from the basic model reported in Fig. 5, we can obtain the model of the symmetrical S-R as shown in Fig. 8 in which the parasitic capacitance relative to R_p is denoted as C_p. The Y-parameters of symmetrical model have been computed referring to the equivalent circuit in Fig. 8 as shown below:

$$Y11_{SYM} = Y_{11A} - \frac{Y_{21A} * Y_{12A}}{Y_{22B} + Y_{22A}} \quad (28)$$

$$Y12_{SYM} = -\frac{Y_{21B} * Y_{12A}}{Y_{22B} + Y_{22A}} \quad (29)$$

$$Y21_{SYM} = -\frac{Y_{21A} * Y_{12B}}{Y_{22B} + Y_{22A}} \quad (30)$$

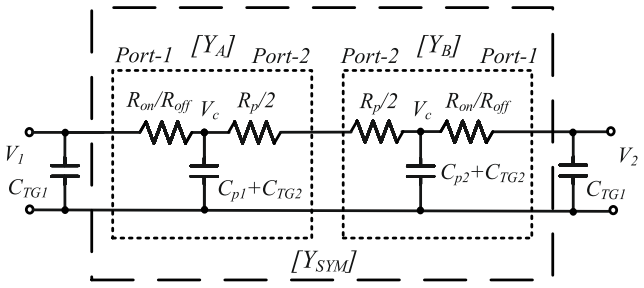


FIGURE 8. Model of the proposed symmetrical S-R.

$$Y22_{SYM} = Y_{11B} - \frac{Y_{21B} * Y_{12B}}{Y_{22B} + Y_{22A}} \quad (31)$$

It has be noted that, according to Fig. 8, the *Yij* parameters in (28)-(31) can be expressed as (14)-(17) by using $R_p/2$ in place of R_p.

If the two *TG* switches are equally sized, then $Y_{ijA} = Y_{ijB}$ and the Y_{SYM} matrix results symmetric with diagonal elements equal to each other. Starting from Y_{SYM}, the complete $Y_{SYM,FULL}$ matrix including the parasitic capacitances of the *TG* switches can be easily computed and results symmetric too:

$$Y_{SYM,FULL} = \begin{bmatrix} Y11_{SYM} + sC_{TG1} & Y12_{SYM} \\ Y21_{SYM} & Y22_{SYM} + sC_{TG1} \end{bmatrix}. \quad (32)$$

IV. LOW-PASS FILTER IMPLEMENTATION AND MODEL VALIDATION

To provide further validation of the S-R technique and of the proposed modeling approach, we designed a first-order low-pass filter (LPF) with tunable cutoff frequency and variable gain exploiting the tuning capability of Switched-Resistors.

The schematic of the designed first order active filter is shown in Fig. 9. The filter has been designed referring to the same 130nm CMOS process used in the previous sections: a MIM capacitor C of 1pF and two polysilicon resistors $R_1 = 100k\Omega$ and $R_2 = 500k\Omega$ have been taken from the technology library.

Minimum size n-MOS and p-MOS transistors have been used to implement the two TG switches in Fig. 9 (Wn/Ln = 150nm/130nm and Wp/Lp = 150nm/130nm), resulting in R_{on}/R_{off} equal to $7.34k\Omega/166G\Omega$ respectively and $C_{TG1,2}$ about equal to 0.1fF.

The parasitic capacitances relative to R_1 and R_2 have been estimated as $C_{1p1,2} = 9.21fF$ and $C_{2p1,2} = 45.1fF$ respectively: $C_{TG1,2}$ are therefore negligible because they are three orders of magnitude smaller than $C_{1p1,2}$ and $C_{2p1,2}$.

The clock frequency for the switched-resistors R_1 and R_2 has been set to $F_{ck} = 10kHz$.

The schematic of the Operational Transconductance Amplifier (OTA) used in the filter is shown in Fig. 10. The first stage of the OTA is a telescopic cascode differential pair, whereas the second stage is a conventional common source stage with Miller compensation. The bias current I_{ref} has been set to $2\mu A$ and the adopted supply voltage is 1V. Transistors dimensions and bias settings of the OTA are

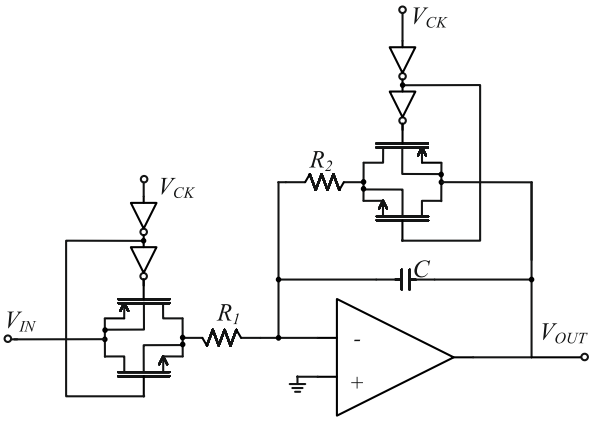


FIGURE 9. First-order LPF-SR topology.

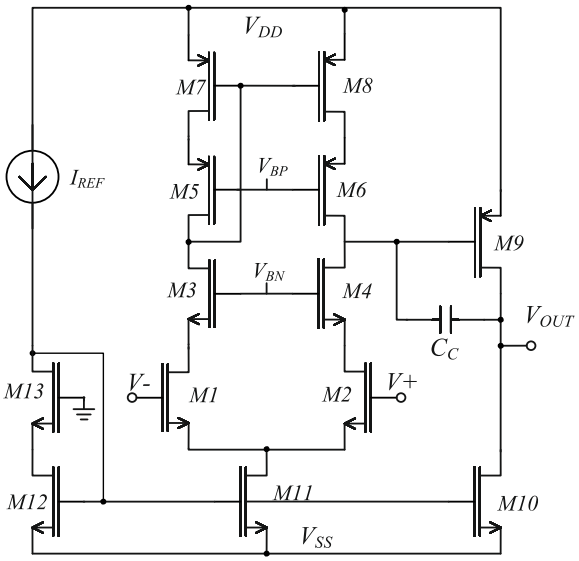


FIGURE 10. Single-ended OTA topology.

reported in Table 1. The designed OTA exhibits a dc-gain of about 75dB and a unity gain frequency in the order of a few MHz.

According to the conventional model of the S-R, the dc-gain $Gain_{dc}$ and the cutoff frequency f_{cutoff}, of the active filter in Fig. 9 can be derived as:

$$|Gain_{dc}(\delta)| = \frac{\frac{R_2+Ron}{\delta}}{\frac{R_1+Ron}{\delta}} = \frac{R_2+Ron}{R_1+Ron} \tag{33a}$$

$$f_{cutoff}(\delta) = \frac{\delta}{2\pi\cdot(R_2+Ron)\cdot C} \tag{33b}$$

From (33a) it is evident that the conventional model predicts a constant dc-gain independent on the duty cycle δ, whereas, according to (33b), the cutoff frequency should be linearly dependent on δ. Both these predictions are not in agreement with simulations for low values of δ (see Fig. 14a), showing again the limitation of the conventional model applied to this case study.

TABLE 1. Transistor dimensions and bias settings for the OTA.

Devices	*W/L [μm]*	*Number of Fingers*
M1,M2,M3,M4	2.53/0.39	5
M5,M6	0.79/0.39	5
M7,M8	3.13/0.39	1
M9	30.89/0.39	1
M10	100/0.13	25
M11,M12,M13	22.23/0.13	25
C_C	500fF	-
Bias Settings		
I_{REF}=2μA	V_{BN} =660mV	V_{BP} =340mV

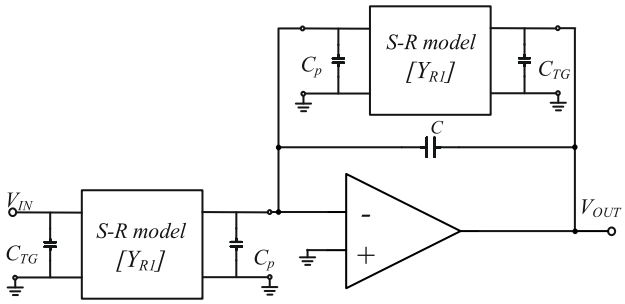


FIGURE 11. First-order LPF-SR model based on Y-matrix theory.

Starting from the S-R model developed in the previous sections, we have developed the model of the full first order active filter reported in Fig. 9 referring to the equivalent circuit reported in Fig. 11. Since the focus of this paper is on the S-R model, we have used a very simple model for the OTA which is considered ideal, but with a finite open-loop gain K.

With these assumptions, the frequency response of the active filter has been computed as:

$$\frac{V_o}{Vin}(\delta, s) = \frac{-KY_{21A}}{Y_{12B}K - Y_{11B} - Y_{22A} - sC(1+K) - s(C_{2A}+C_{2B})}. \tag{34}$$

From equation (34) the dc-gain and cutoff frequency can be easily derived as:

$$|Gain_{dc}(\delta)| = \frac{KY_{21A}}{KY_{12B} - Y_{11B} - Y_{22A}} \tag{35a}$$

$$f_{cutoff}(\delta) = \frac{1}{2\pi}\frac{(Y_{12B}K - Y_{11B} - Y_{22A})}{(C(1+K) + C_{2A} + C_{2B})} \tag{35b}$$

The simulated frequency response of the active filter for δ = 10% and δ = 0.0001% is reported in Fig. 12, showing the extreme tuning range achieved thanks to the S-R approach (cutoff frequency ranging from 1.68Hz to 1.46kHz).

It is evident from Fig. 12 that the dc-gain drops from the ideal value of 13.5dB for δ = 10% to the much lower value of about -5dB for δ = 0.0001% due to the effect of parasitic capacitances which become dominant for δ = 0.0001%. In fact, the 500$k\Omega$ poly resistor R_2 exhibits a much higher parasitic capacitances than the 100$k\Omega$ poly resistor R_1 so

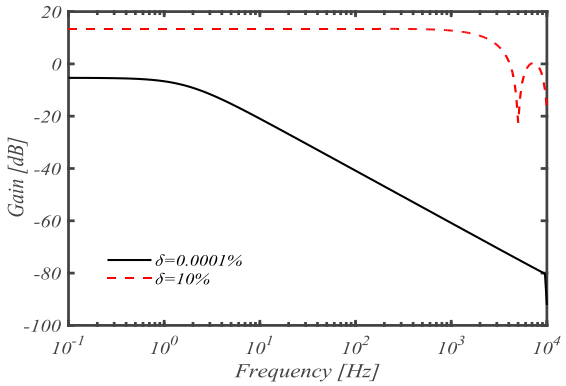


FIGURE 12. Simulated frequency response with for δ = 10% and δ = 0.0001%.

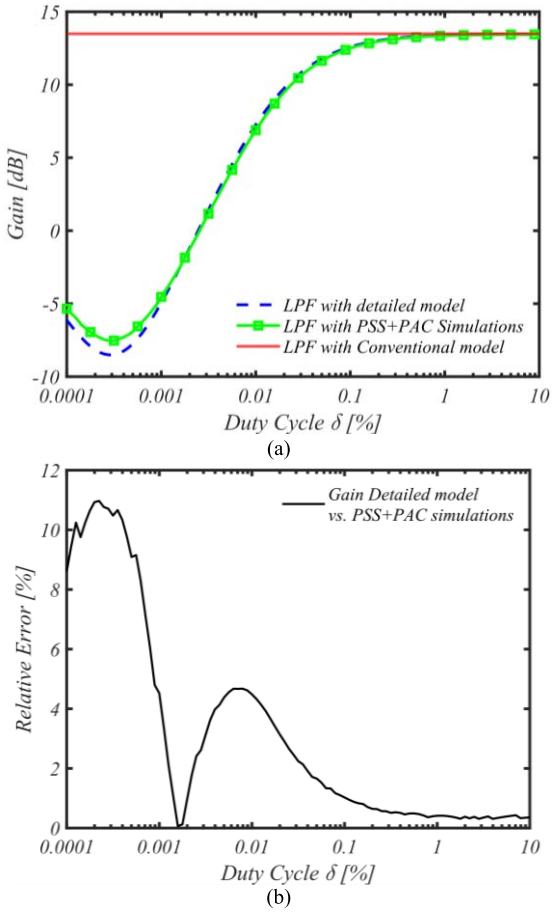


FIGURE 13. DC Gain of the active LPF: (a) comparison between the simulated gain and the proposed gain model; (b) relative error of the proposed gain model.

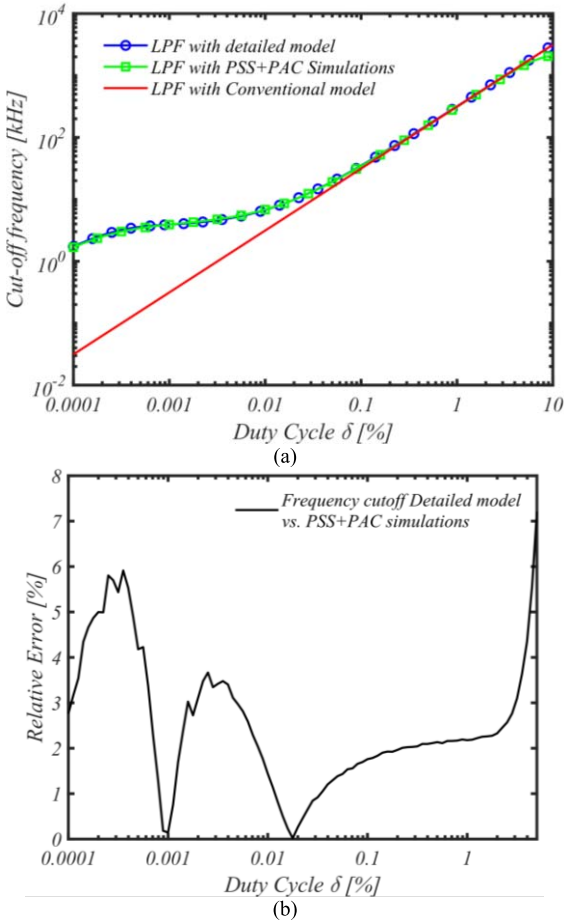


FIGURE 14. Gain LPF- (a) Comparison of the simulated cutoff frequency with the detailed model and the conventional model; (b) relative error of the proposed cutoff frequency model.

that the ratio between the equivalent impedance of the S-R R_2 and of the S-R R_1 is lower than 1 when parasitic effects are dominant.

Fig. 13a reports the comparison between the dc gain of the active LPF obtained from *PSS+PAC* simulations and from the proposed gain model in (35a). The relative error of the model is shown in Fig. 13b.

By inspection of Fig. 13, it is evident that the conventional model in (33a) is not adequate to describe the gain of the LPF which exhibits more than 15dB of variation across the considered duty cycle range instead of being constant as predicted by (33a). On the other hand, the proposed gain model in (35a) is able to fit well the simulated gain curve with an average relative error of 3.17% and a maximum relative error of about 12% (despite the very simple model assumed for the OTA).

Fig. 14a reports the comparison between the cutoff frequency of the active LPF obtained from *PSS+PAC* simulations and from the proposed cutoff frequency model in (35b). The relative error of the model is shown in Fig. 14b.

By inspection of Fig. 14, it is evident that also in this case the conventional model is not able to predict the real dependence of f_{cutoff} on δ, across the whole tuning range. The proposed model in (35b) is instead able to fit well the simulated cutoff frequency curve with an average error of 3.6% and a maximum error of 7%.

V. CONCLUSION

We have presented a detailed analysis of the Switched-Resistor technique, showing how the conventional model is not adequate to describe the equivalent resistance for very small values of the duty cycle. We have then proposed

a novel, detailed model including the main parasitic effects, which is able to guarantee a very good accuracy even for duty cycle values as low as 0.0001%. The proposed modeling approach is useful to understand the real limitations of the S-R approach and to gain insight into the real behavior of switched-resistors. Furthermore, since the model is able to accurately predict the equivalent resistance as a function of the duty cycle, it allows to easily design the digital controller which sets the duty cycle in order to maximize the tuning range of cutoff frequency in active filters based on switched-resistors or to compensate PVT variations. To validate this last claim, an active, first order LPF has been implemented referring to a commercial 130nm CMOS technology showing a tuning range of the cutoff frequency about three decades (from 1.68Hz to 1.46kHz). Since the average error in the estimation of the cutoff frequency has resulted lower than 3.6% the relationship between the desired cutoff frequency and the duty cycle to set can be accurately predicted during the design phase.

REFERENCES

[1] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[2] M. Avoli, F. Centurelli, P. Monsurrò, G. Scotti, and A. Trifiletti, "Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS," *AEU Int. J. Electron. Commun.*, vol. 92, pp. 30–35, Aug. 2018.

[3] C. Qian, J. Parramon, and E. Sanchez-Sinencio, "A micropower low-noise neural recording front-end circuit for epileptic seizure detection," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1392–1405, Jun. 2011.

[4] F. Centurelli, A. Fava, P. Monsurrò, G. Scotti, P. Tommasino, and A. Trifiletti, "Low power switched-resistor band-pass filter for neural recording channels in 130 nm CMOS," *Heliyon*, vol. 6, no. 8, 2020, Art. no. e04723.

[5] J. Lee, M. Johnson, and D. Kipke, "A tunable biquad switched-capacitor amplifier-filter for neural recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 5, pp. 295–300, Oct. 2010.

[6] T.-Y. Wang, L.-H. Liu, and S.-Y. Peng, "A power-efficient highly linear reconfigurable biopotential sensing amplifier using gate-balanced pseudoresistors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 2, pp. 199–203, Feb. 2015.

[7] M.-T. Shiue, K.-W. Yao, and C.-S. A. Gong, "Tunable high resistance voltage-controlled pseudo-resistor with wide input voltage swing capability," *Electron. Lett.*, vol. 47, no. 6, pp. 377–378, Mar. 2011.

[8] D. Djekic, G. Fantner, K. Lips, M. Ortmanns, and J. Anders, "A 0.1% THD, 1-MΩ to 1-GΩ tunable, temperature-compensated transimpedance amplifier using a multi-element pseudo-resistor," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1913–1923, Jul. 2018.

[9] H. Hu, T. Islam, A. Kostyukova, S. Ha, and S. Gupta, "From battery enabled to natural harvesting: Enzymatic biofuel cell assisted integrated analog front-end in 130 nm CMOS for long-term monitoring," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 534–545, Feb. 2019.

[10] M. Alioto and M. Shahghasemi, "The Internet of Things on its edge: Trends toward its tipping point," *IEEE Consum. Electron. Mag.*, vol. 7, no. 1, pp. 77–87, Jan. 2018.

[11] M. Alioto, *Enabling the Internet of Things*. Cham, Switzerland: Springer, 2017.

[12] B. Sedighi and M. S. Bakhtiar, "An 8-bit switched-resistor pipeline ADC," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCS)*, New Orleans, LA, USA, 2007, pp. 1963–1966.

[13] A. Jiraseree-Amornkun, A. Worapishet, E. A. M. Klumperink, B. Nauta, and W. Surakampontorn, "Theoretical analysis of highly linear tunable filters using switched-resistor techniques," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3641–3654, Dec. 2008.

[14] Y.-P. Hsu, Z. Liu, and M. M. Hella, "A –68 dB THD, 0.6 mm^2 active area biosignal acquisition system with a 40–320 Hz duty cycle controlled filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 1, pp. 48–59, Jan. 2020.

[15] L.-C. Zhou, Z.-C. Li, J. Li, and Q. Xiong, "Design of low noise and low power chopper stabilized amplifier for neural recording applications," in *Proc. IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Qingdao, China, 2018, pp. 1–3.

[16] H. Chandrakumar and D. Marković, "A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, Mar. 2017.

[17] H. Chandrakumar and D. Marković, "An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017.

[18] M. Alioto and G. Palumbo, "Feature—Power-aware design techniques for nanometer MOS current-mode logic gates: A design framework," *IEEE Circuits Syst. Mag.*, vol. 6, no. 4, pp. 42–61, 4th Quart., 2006.

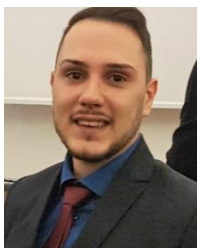
[19] W. B. Wilson, H. Z. Massoud, E. J. Swanson, R. T. George, and R. B. Fair, "Measurement and modeling of charge feedthrough in n-channel MOS analog switches," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1206–1213, Dec. 1985.

[20] C. Eichenberger and W. Guggenbuehl, "Charge injection of analogue CMOS switches," *IEE Proc. Circuits Devices Syst.*, vol. 138, no. 2, pp. 155–159, Apr. 1991.

[21] W. Xu and E. G. Friedman, "Clock feedthrough in CMOS analog transmission gate switches," in *Proc. 15th Annu. IEEE Int. Conf. ASIC/SOC*, Rochester, NY, USA, 2002, pp. 181–185.

FRANCESCO CENTURELLI (Member, IEEE) was born in Rome, in 1971. He received the Laurea degree (*cum laude*) and the Ph.D. degree in electronic engineering from the University of Roma "La Sapienza," Rome, Italy, in 1995 and 2000, respectively.

In 2006, he became an Assistant Professor with the DIET Department, University of Roma La Sapienza. He has published more than 100 papers on international journals and refereed conferences, and has been also involved in R&D activities held in collaboration between Università "La Sapienza" and some industrial partners. His research interests were initially focused on system-level analysis and design of clock recovery circuits and high-speed analog integrated circuits, and now concern the design of analog-to-digital converters and very low-voltage circuits for analog and RF applications.



ALESSANDRO FAVA was born in Rome, in 1994. He received the B.Sc. and M.Sc. degrees (*cum laude*) in electronics engineering from Sapienza University of Rome, Italy, in December 2017 and October 2020, respectively, where he is currently pursuing the Ph.D. degree in information and communication technology with the Department of Information Engineering, Electronics and Telecommunications.

His research activity is focused on integrated circuits design for brain-implanted biomedical devices.

GIUSEPPE SCOTTI (Senior Member, IEEE) was born in Cagliari, Italy, in 1975. He received the M.S. and Ph.D. degrees in electronic engineering from the University of Rome "La Sapienza," Rome, Italy, in 1999 and 2003, respectively. In 2010, he became a Researcher (Assistant Professor) with the DIET Department, University of Rome "La Sapienza," where he was appointed as an Associate Professor in 2015. He teaches undergraduate and graduate courses on basic electronics and microelectronics. In the context of analog design his research activity was concerned with circuit topologies for the realization of low-voltage analog building blocks using ultra-short channel CMOS technology, whereas in the context of cryptographic hardware his focus has been on novel PAAs methodologies and countermeasures. He has been also involved in R&D activities held in collaboration between "La Sapienza" University and some industrial partners, which led, from 2000 to 2015, to the implementation of 13 ASICs. He has coauthored more than 45 publications in international journals, about 70 contributions in conference proceedings and is the co-inventor of two international patents. His research activity was mainly concerned with integrated circuits design and focused on design methodologies able to guarantee robustness with respect to parameter variations in both analog circuits and digital VLSI circuits.

ALESSANDRO TRIFILETTI was born in Rome, Italy, in October 4, 1959. In 1991, he joined the Electronic Engineering Department, "La Sapienza" University, Rome, as a Research Assistant, where he was involved in research activities dealing with analogue, RF and microwave IC's design. In 2001, he became as an Assistant Professor and he got the position of an Associate Professor in 2005, and the position of Full Professor with the Engineering Faculty of "La Sapienza" University in 2019. He has worked in the field of microelectronics, both from the point of view of design methodologies and circuit topologies. On these subjects, he has (co)authored over 210 publications, of which about 80 published on international journals, the others published on the proceedings of major international Conferences (a large part of these sponsored by the IEEE). In last 20 years, he has been engaged in the coordination of research teams from DIET (previously DIE) in the framework of national and international programs, involving both industrial and academic partners. From an industrial perspective, he expertise covers topics about analogue and RF microelectronics, radar and ESM systems, high-speed communication systems, security issues in cryptographic algorithms implementation, and embedded system design. He is currently a Reviewer for some IEE and IEEE reviews, among them: IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS, *IEE Proceedings on Circuits, Devices and Systems*, *IEE Electronic Letters*.