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Abstract. A 2-channel digitizer based on a mixing-filtering-processing (MFP) strategy capable of granting ultra-high bandwidth and sampling rate is presented. The digitizer requires suitable digital signal processing resources, which consist of several dedicated integrated circuits (ICs), to produce a digital representation of the input signal. Processing is also in charge of streamline calibration, that involves eliminating the artefacts due to mismatches between individual channels and equalizing the frequency response of the system. The design issues related to the implementation of calibration and signal reconstruction are presented. Tests needed to assess the system configuration at the manufacturing stage are also discussed.

1. Introduction

Real-time digitizers can appropriately measure signals characterized by limited bandwidth, provided that they support the whole bandwidth of the signal and offer a sampling rate twice greater than it. For challenging applications, requiring sampling rates higher than those offered by monolithic fast analog-to-digital converters (ADCs), digitizers use time-interleaved ADCs. A digitizer made of N time-interleaved ADCs, in fact, provides a sampling rate N times greater than that of the individual ADCs.

Time-interleaving (TI) is implemented by means of multi-channel architectures, where a multi-way track-and-hold amplifier at the front-end feeds multiple channels, assuring a high input bandwidth. Identical ADCs are deployed on the individual channels; time-interleaving then grants high sampling rates. Unfortunately, as the number of channels increases, these architectures show mounting size and complexity, longer on-chip communication paths, higher parasitic capacitances, and, ultimately, higher noise. In fact, to assure sufficient rise-time, each converter cascaded to the track-and-hold amplifier requires an analog bandwidth larger than half its maximum sampling rate. Widening the bandwidth of the individual ADCs allows more input noise into the system, thus degrading the overall performance.

Performance loss can be avoided by exploiting new technologies such as digital bandwidth interleaving (DBI) or asynchronous bandwidth interleaving (ATI). These technologies improve both sampling rate and bandwidth without widening the bandwidth requirements of the individual ADCs. They perform mixing and filtering operations before digitization, and exploit digital signal processing to obtain a digital representation of the input signal. They are therefore different realizations of a general strategy based on modulation, filtering and processing operation, identified by means of the acronym MFP in the following.

In detail, DBI divides the input bandwidth into adjacent sub-bands by filtering. The higher sub-bands are down-converted to baseband by mixing, and acquired by ADCs clocked at a lower sampling rate. After digitization, the sub-bands are digitally up-converted to their original frequency ranges, and combined into a representation of the input signal. The real advantage of DBI solutions is bandwidth improvement rather than noise performance, since they suffer from the superposition of quantization noises coming from the individual channels.

On the other hand, ATI exploits a multi-channel architecture that use harmonic mixing to attain downconversion, and time interleaving to lower the sampling rate requirement of the individual channels. ATI solutions are the most recent and promising ones in terms of noise performance. They are characterized by more flexible requirements in terms of synchronicity between channels, and

allow noise reduction by means of inherent averaging operations, which are necessary to gain a digital representation of the input signal.

Hereinafter a 2-channel digitizer based on an MFP strategy is presented. It shares with the solutions addressing ultra-high bandwidth and sampling rate extensive and massive use of digital signal processing resources. These resources consist in several dedicated integrated circuits (ICs) deployed throughout the system. They are necessary to perform streamline calibration that allows eliminating the artefacts due to mismatches between individual channels, equalizing the frequency response of the system, and finally attaining a digital representation of the input signal. The main attention is paid to the test methods needed to assess the system configuration at the manufacturing stage, and the design of the algorithms to be implemented by the internal ICs.

2. MFP digitizer operation principle

As shown in Fig. 1, the input signal is intermittently routed on 2 separate channels, by means of a fast switching system that splits the propagation path. The switching system grounds the input of a channel to zero when connecting the other channel, thus performing ON/OFF modulation. The signals on the channels can be thought as a couple of complementary signals, obtained by modulating with complementary rectangular pulse trains, characterized by 50% duty cycle and pulse repetition rate f_p (pulse train period T_p) equal to the bandwidth pursued by design. The pulse train on one channel is 180 degrees out of phase with respect to that of the other channel, so that when a pulse is ON the other is OFF. The signals at the output of the modulators are burst-wise signals windowing the input signal in time-slots of duration $T_p/2$. The time slots in which the signal is grounded on a channel correspond to the time slots in which bursts are present on the other channel.

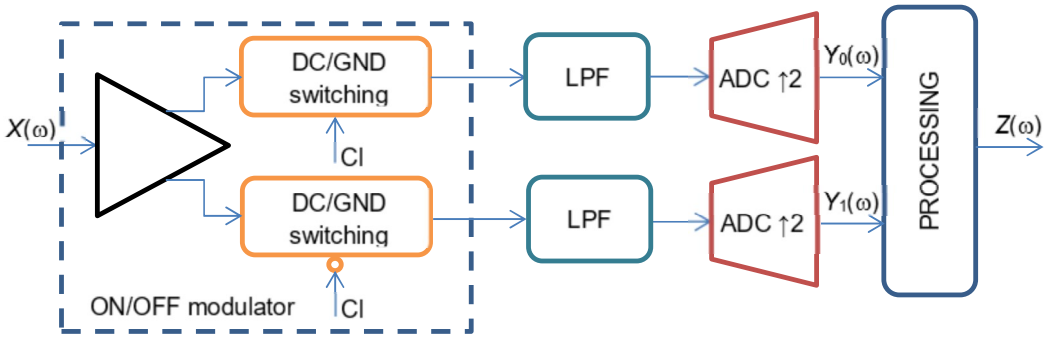

Figure 1. Block Diagram of the considered MFP digitizer.

In order to understand the operation principle, first notice that the Fourier series of the pulse train, describing the front-end modulation, enlists, among the others, a DC term and a fundamental harmonic at frequency f_p; the nearest non-zero harmonic is the third one, which is already far outside the bandwidth of the system. The spectra of the modulated signals include the spectral contributions of the original signal and, additional ones due to mixing with the fundamental harmonic at frequency f_p; further contributions related to higher harmonics are cancelled by the limited bandwidth of the channel, and by the subsequent low-pass filter (LPF).

The modulated signals are filtered by means of a low-pass filter with flat frequency response up to $f_p/2$, and sharp cut-off. The low-pass filtered signals are then acquired by the individual ADCs, at a sampling rate $f_s \geq f_p$. The system is equipped with an internal counter to accurately determine the ratio between f_p and f_s, whose knowledge is needed to perform synchronization. Digital signal processing allows combining the acquired signals and obtaining a representation of the input signal over the whole bandwidth pursued by design; the sampling rate characterizing the output signal is $2f_s$. Digital processing also allows implementing further processing to flatten the bandwidth of the system.

3. Proposed calibration and reconstruction method

3.1. Problem statement

The MFP digitizer given in Fig. 1 can be described by means of an equivalent discrete-time system operating at sampling rate $2f_s$. In the following the description is presented assuming that the sampling process of the individual ADCs is synchronous to the DC/GND switching units which is deployed on the same channel, so that $f_s = f_p$. Moreover, since the digital data acquired by the individual ADCs are characterized by a sampling rate f_p, they need to be up-sampled to $2f_p$. This operation is performed by

interleaving each data stream with a zero sequence, and produces replication of the spectrum at a pace f_s. The signals provided as input to the final processing unit can be represented in the frequency domain as functions of the dimensionless angular frequency ω ranging in the limited interval $(0, 2\pi)$, by:

$$Y_0(\omega) = \frac{1}{4}\big((L_0(\omega)P_{00} + L_0(\omega-\pi)P_{10})F_0(\omega)X(\omega) + (L_0(\omega)P_{10} + L_0(\omega-\pi)P_{00})F_0(\omega-\pi)X(\omega-\pi)\big) \quad (1.a)$$

$$Y_1(\omega) = \frac{1}{4}\big((L_1(\omega)P_{01} + L_1(\omega-\pi)P_{11})F_1(\omega)X(\omega) - (L_1(\omega)P_{11} + L_1(\omega-\pi)P_{01})F_1(\omega-\pi)X(\omega-\pi)\big) \quad (1.b)$$

where $X(\omega)$ is the input and signal, $Y_0(\omega)$ and $Y_1(\omega)$ are the signals available to the final processing unit, $F_0(\omega)$ and $F_1(\omega)$ are linear filters that account for the gain and delay of the individual channels of the ON/OFF modulator, P_{ij} is the magnitude of the j-th coefficient of the Fourier series describing the ON/OFF modulation effect on the i-th channel, and $L_0(\omega)$ and $L_1(\omega)$ are linear filters that account for the analog low-pass filter, the frequency response of the ADCs front-ends and their relative timing skew. Equations (1.a) and (1.b) can be expressed in a more compact form as:

$$Y_0(\omega) = \frac{1}{4}\big(A_{00}(\omega)X(\omega) + A_{01}(\omega)X(\omega-\pi)\big) \quad (2.a)$$

$$Y_1(\omega) = \frac{1}{4}\big(A_{10}(\omega)X(\omega) - A_{11}(\omega)X(\omega-\pi)\big) \quad (2.b)$$

where

$$A_{00}(\omega) = (L_0(\omega)P_{00} + L_0(\omega-\pi)P_{10})F_0(\omega) \quad (3.a)$$

$$A_{01}(\omega) = (L_0(\omega)P_{10} + L_0(\omega-\pi)P_{00})F_0(\omega-\pi) \quad (3.b)$$

$$A_{10}(\omega) = (L_1(\omega)P_{01} + L_1(\omega-\pi)P_{11})F_1(\omega) \quad (3.c)$$

$$A_{11}(\omega) = (L_1(\omega)P_{11} + L_1(\omega-\pi)P_{01})F_1(\omega-\pi) \quad (3.d)$$

The calibration and reconstruction problem consists in the definition of suitable digital filters $H_0(\omega)$ and $H_1(\omega)$ to obtain:

$$Z(\omega) = H_0(\omega)Y_0(\omega) + H_1(\omega)Y_1(\omega) \equiv X(\omega) \quad (4)$$

where $Z(\omega)$ is the reconstructed output signal, which should be identical to the input. Forcing $Z(\omega) = X(\omega)$ provides the following linear system:

$$\begin{cases} \frac{1}{4}H_0(\omega)A_{00}(\omega) + \frac{1}{4}H_1(\omega)A_{10}(\omega) = 1 \\ \frac{1}{4}H_0(\omega)A_{01}(\omega) - \frac{1}{4}H_1(\omega)A_{11}(\omega) = 0 \end{cases} \quad (5)$$

3.2. Calibration and reconstruction

3.2.1. *Method based on sine-waves tests.* The digital filters $H_0(\omega)$ and $H_1(\omega)$ can be identified by means of sine-wave tests. In particular, according to equations (2.a) and (2.b), applying to the digitizer a cosine waveform characterized by digital frequency ω_1, magnitude M_1, and initial phase φ_1, produces a dual tone cosine output with frequencies ω_1 and $\omega_2 = \pi - \omega_1$ on each channel, hereinafter referred to as complementary frequencies. The magnitude and phase parameters of the dual tone signal measured on the j-th channel, with $j = \{0, 1\}$, are determined by the values $A_{0j}(\omega_1)|_{\omega_1}$ and $A_{1j}(\omega_2)|_{\omega_1}$ (the subscript refers to the frequency of the applied signal), which is quantified through the test. A complementary test that consists in applying a cosine waveform characterized by the digital frequency ω_2, magnitude M_2, and initial phase φ_2, allows to quantify the values $A_{0j}(\omega_2)|_{\omega_2}$ and $A_{1j}(\omega_1)|_{\omega_2}$, with $j = \{0, 1\}$. This couple of tests provides the coefficients of two mutually coupled algebraic linear systems. These systems form together a unique system made of 4 linear equations in 4 unknowns, namely:

$$\begin{cases} H_0(\omega_1)A_{00}(\omega_1)|_{\omega_1} + H_1(\omega_1)A_{10}(\omega_1)|_{\omega_1} = 4 \\ H_0(\omega_2)A_{01}(\omega_2)|_{\omega_1} - H_1(\omega_2)A_{11}(\omega_2)|_{\omega_1} = 0 \\ H_0(\omega_1)A_{00}(\omega_1)|_{\omega_2} + H_1(\omega_1)A_{10}(\omega_1)|_{\omega_2} = 0 \\ H_0(\omega_2)A_{01}(\omega_2)|_{\omega_2} - H_1(\omega_2)A_{11}(\omega_2)|_{\omega_2} = 4 \end{cases} \quad (6)$$

where the amplitude and phase of the digitized cosine waveform are made congruent to the applied one, whereas the alias term is zeroed Notice that equations in system (6) can be regrouped by

separating the first and third equations form the second and fourth ones. It is thus obtained a couple of independent systems, each one made of 2 equations with 2 unknowns, whose solutions provide the values of the frequency response of the filters $H_0(\omega)$ and $H_1(\omega)$ for ω_1 and ω_2. Repeating the procedure at different couples of complementary frequencies allows determining the frequency response of the calibration and reconstruction filters across a selected grid on the whole bandwidth of the system.

3.2.2. *Method based on step-response tests.* Actually, calibration and reconstruction issues can be approached separately, choosing one of the two digital filters quite arbitrarily, and defining additional filtering operations to assure a desired response. For instance, if $H_0(\omega)$ is chosen as an all-pass filter with constant gain G, and it is chosen as correction filter $H_1(\omega) = G\frac{A_{01}(\omega)}{A_{11}(\omega)}$, the second equation of system (5), which assures the cancellation of aliasing effects, is still satisfied. It is worth noticing that to specify $H_1(\omega)$ it is not necessary to know the magnitude and phase parameters of the input sine-wave, because it is defined in terms of a ratio. The reconstructed signal, however, has to undergo further filtering aimed at gain equalization and removal of the residual linear errors. Specifically, the considered digitizer would return:

$$Z(\omega) = G\left(Y_0(\omega) + \frac{\mathrm{A}_{01}(\omega)}{\mathrm{A}_{11}(\omega)}Y_1(\omega)\right) = U(\omega)X(\omega) \tag{7}$$

where $U(\omega)$ is the actual frequency response of the digitizer after the removal of aliasing effects, namely:

$$U(\omega) = \frac{G}{4}\left(A_{00}(\omega) + \frac{\mathrm{A}_{01}(\omega)}{\mathrm{A}_{11}(\omega)}A_{10}(\omega)\right) \tag{8}$$

At calibration, $U(\omega)$ can be identified by measuring the impulse response of the digitizer and applying Fourier transformation. The impulse response is effectively measured as derivative of the step-response. The latter can be measured with a time resolution superior to the smallest sampling period in systems equipped with high-sensitivity trigger circuits that support random interleaved sampling modes.

3.3. Digital filters synthesis

The synthesis of the required digital filters from a specified frequency response can be straightforwardly obtained if the frequencies selected during the calibration tests form a complete orthogonal basis. In this case it is sufficient to perform the inverse discrete Fourier transformation of the measured data. Otherwise, if the frequency response is specified on a set of arbitrarily selected frequencies, least square methods can be considered. In this case it is advisable that the number of available data is greater than the length of the desired filter.

4. Simulation results

The proposed 2-channel MFP digitizer has been simulated considering several issues that could affect real architectures, such as gain imbalance and skew between both ON/OFF modulator channels and ADCs, differences in the burst duration of the signals at the output of the modulator, non-ideal low-pass filters simulated by means of maximally flat 8th-order filters. The described calibration and signal reconstruction approach has been implemented and the results compared. The main attention has been paid to noise and linearity performance, expressed in terms of SINAD and THD, respectively.

Finally, a thorough analysis of the computational costs, that determine the requirements of the ICs in charge of the real-time processing operations, has been carried out for a digitizer with a sampling rate up to 100 GSa/s.

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