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A 0.3 V Rail-to-Rail Ultra-Low-Power OTA with Improved Bandwidth and Slew Rate

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Abstract: In this paper, we present a novel operational transconductance amplifier (OTA) topology based on a dual-path body-driven input stage that exploits a body-driven current mirror-active load and targets ultra-low-power (ULP) and ultra-low-voltage (ULV) applications, such as IoT or biomedical devices. The proposed OTA exhibits only one high-impedance node, and can therefore be compensated at the output stage, thus not requiring Miller compensation. The input stage ensures rail-to-rail input common-mode range, whereas the gate-driven output stage ensures both a high open-loop gain and an enhanced slew rate. The proposed amplifier was designed in an STMicroelectronics 130 nm CMOS process with a nominal supply voltage of only 0.3 V, and it achieved very good values for both the small-signal and large-signal Figures of Merit. Extensive PVT (process, supply voltage, and temperature) and mismatch simulations are reported to prove the robustness of the proposed amplifier.

Keywords: body-driven; ultra-low-voltage; ultra-low-power; operational transconductance amplifier; non-tailed differential pair; IoT

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1. Introduction

The development of ultra-low-power (ULP) and ultra-low-voltage (ULV) integrated circuits is driven by applications such as the Internet of Things (IoT) [1–4] and implanted biomedical devices [5–8]. The number of IoT devices connected to the internet for gathering and processing information is increasing at a faster and faster rate. The enormous number of connected devices and the fact that they are often battery powered or must scavenging energy from the environment make low power consumption a key feature in IoT devices [1]. Therefore, the design of integrated circuits (ICs) for IoT applications is becoming more and more difficult due to the stringent constraints in terms of power dissipation, minimum supply voltage, and area footprint [1,2]. Due to the above constraints and the low intrinsic gain of nanometer MOS transistors, analog interfaces are, in many cases, the most challenging building blocks of ICs for IoT applications [2,3].

In the context of implanted biomedical applications, front-end amplifiers for neural recording systems often rely on AC coupling with cutoff frequencies below 1 Hz to eliminate the DC offset of the electrodes and to properly process the neural signals [5,6]. Such devices are usually designed for different frequency slots in the range from 1 Hz to 10 kHz. For example, in the case of epileptic seizure detection, band-pass filters in the range of 250 to 500 Hz are required to extract the signals of interest. Low-voltage operation, low power consumption, and a small silicon area are the main requirements of ICs for these systems [7,8].

ULP and ULV operational transconductance amplifiers (OTAs) are key components for both the IoT and implanted biomedical devices, and a huge number of OTAs have been presented in recent years [9]. In [10], Stockstad et al. presented a 0.9 V operational amplifier

that, for the first time, exploited the bulk-driven technique to attain rail-to-rail input–output swing. Over the years, the research community has increasingly focused on reducing the supply voltage and power consumption at the expense of common-mode rejection ratio (CMRR) performance [11–14]. Several common-mode feedback (CMFB) approaches, which exploit triode-biased devices or current cancellation, have been proposed with the aim of minimizing the common-mode gain in fully differential OTAs, thus improving their CMRR performance [15–19].

Multi-stage OTAs based on folded cascode or gain-boosting topologies and with supply voltages in the range from 0.6 to 0.9 V have been presented in the literature [20–24]. However, when targeting supply voltages lower than 0.4 V, the adoption of the topologies and design strategies reported above is no longer possible, and pseudo-differential or inverter-based architectures are often used [25–32]. In fact, at these supply voltages, gate-driven amplifiers are not adequate for ensuring a rail-to-rail input common-mode range (ICMR). However, due to the lack of tail current generators, pseudo-differential and inverter-based circuits typically exhibit a not-well-defined bias point and a poor CMRR, and body bias strategies are less effective due to the limited available voltage swing on body terminals.

ULV circuits can employ floating gate devices [33] or body-driven stages [34,35] to increase the input common-mode swing. Body-driven input stages are inherently rail-to-rail in ULV applications, and forward biasing of the NP junctions is not a concern when supply voltages are lower than about 0.6 V. Unlike gate-driven stages, however, they tend to have higher noise, lower bandwidth, and resistive input impedance. Despite these shortcomings, there is no alternative at supply voltages around 0.3 V if a large common-mode input signal swing is desired. Furthermore, the gate terminals of the input devices can be used for biasing, the biasing current of the amplifiers can be accurately set, and pseudo-differential architectures can even be exploited.

Additional interesting OTA architectures based on fully digital operation were recently proposed in [36,37], which showed the feasibility of full standard-cell-based analog amplifiers.

In addition to gain and robustness considerations, ULP and ULV topologies may have low bandwidth (because of sub-threshold biasing) and poor slew-rate performance (because of low biasing currents). Hence, it is important to assess the OTA performance in terms of bandwidth and slew rate for a given current or power consumption and capacitive load, which refer to the popular large-signal and small-signal Figures of Merit (FOMs).

In this paper, we present a novel OTA topology based on a body-driven input stage with a dual path to improve CMRR that exploits body-driven current mirror load for differential-to-single-ended conversion at the output. The proposed OTA has only one high-impedance node, and can therefore be compensated at the output stage, thus avoiding Miller compensation. The body-driven input stage ensures the rail-to-rail input common-mode range, whereas the coupling between the first and second stages and the gate-driven output stage ensure high open-loop gain and good slew-rate performance.

The paper is organized as follows: Section 2 describes the proposed topology; Section 3 analyzes the small-signal and large-signal circuit responses, including the CMRR; Section 4 reports the design and simulation results, with emphasis on the process, supply voltage, and temperature (PVT) variations, as well as on stochastic mismatch variations; a comparison with the related literature to highlight the advantages of the proposed topology in terms of the FOMs is also presented in Section 4. Finally, the conclusions are reported in Section 5.

2. Proposed Topology

The block scheme of the proposed OTA is reported in Figure 1, showing the usage of two matched transconductors G_{M_A} and G_{M_B}, whose output currents are sent to a transimpedance stage T_Z, in which the common-mode currents are ideally cancelled, and the differential currents are summed to double the transconductance gain. Figure 2 shows

the detailed schematic of the OTA. Transistors M_{1A}, M_{2A}, M_{3A} and M_{1B}, M_{2B}, M_{3B} form the two input transconductance stages, which are shown in Figure 1 as G_{M_A} and G_{M_B}. The second stage of the OTA is made up of transistors $M_{4A}, M_{4B}, M_5, M_6, M_7, M_8$, which implement the transimpedance stage T_Z shown in Figure 1.

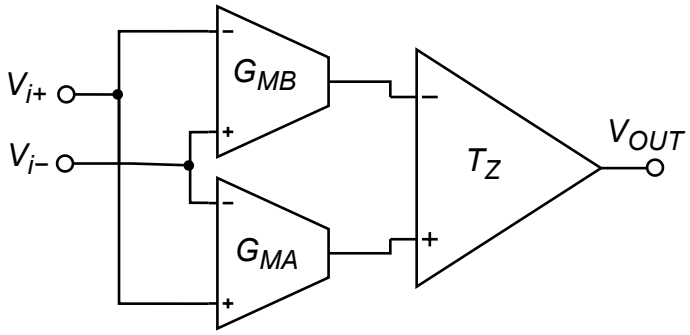

Figure 1. Block scheme of the proposed OTA.

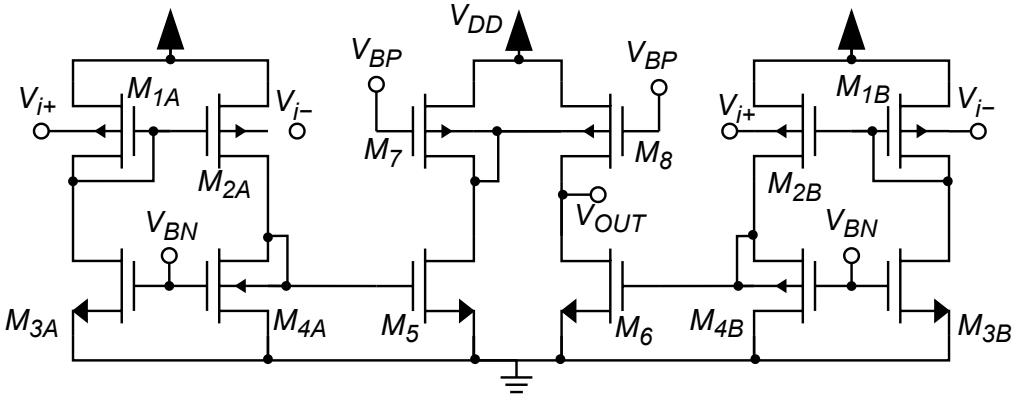

Figure 2. Detailed schematic of the proposed OTA.

To allow rail-to-rail input swing, a body-driven first stage is used. Due to the ULV supply, particular care was taken to identify a biasing strategy that was able to guarantee robustness with respect to the PVT and mismatch variations. In fact, since each transistor requires a minimum V_{ds} to properly operate, tail current generators are not an option, and the lack of tail current generators reduces common-mode rejection. Hence, the dual transconductance path in the input stage was exploited to guarantee high CMRR under the hypothesis of well-matched transconductances. Furthermore, since $M_{1A,B}$ and $M_{2A,B}$ comprise a current mirror and $M_{3A,B}$ acts as a current source, a well-defined bias current is obtained. It has to be noted that the two transconductors G_{M_A} and G_{M_B} have to be designed symmetrically and must be well matched with each other in order to optimize common-mode cancellation. The second stage of the OTA exploits two body-diode NMOSs, so the input impedance is equal to $1/g_{mb}$. Transistors M_{4A}, M_5 and M_{4B}, M_6 act as current amplifiers. The gates of transistors M_7 and M_8 determine the biasing current of the second stage. The body-driven current mirror M_7 and M_8 provides differential-to-single-ended conversion and allows further rejection of the common-mode current component, since the common-mode current in M_6 and M_8 is the same. The output conductance $g_{ds_8} + g_{ds_6}$ of the stage provides voltage gain to the amplifier.

It has to be noted that the differential input stage is very similar to the one used in [35,38,39]. However, in these works, the transconductors G_{M_A} and G_{M_B} are loaded by a conventional gate-driven current mirror, which performs the differential-to-single-ended conversion in the first stage. The first stage is then followed by one or two stages with Miller or Nested Miller compensation. In the proposed circuit, instead, the transconductors G_{M_A} and G_{M_B} are loaded by a differential body-diode load, and therefore, the input stage can

be considered as a fully differential amplifier. The second stage of the proposed topology can be seen as a pseudo-differential pair loaded with a body-driven current mirror that performs the differential-to-single-ended conversion at the output, thus further increasing the CMRR and avoiding Miller compensation. The relatively high CMRR is obtained as a combination of two kinds of effects: the intrinsic CMRR of the simple differential pairs M1A-M3A and M1B-M3B, as explained in [38], and trough symmetry and cancellation of currents due to the body-driven current mirror in the output stage.

3. Circuit Analysis

In this section, we present a small-signal and large-signal analysis of the proposed amplifier, including the frequency response, the CMRR, and the slew-rate performance.

3.1. Differential Gain Frequency Response

Referring to the block scheme in Figure 1, the differential gain of the proposed OTA can be easily computed as:

$$A_{V_D} = 2 \cdot G_{M_{A(B)}} \cdot T_Z \tag{1}$$

where $G_{M_{A(B)}}$ is the transconductance gain of the first stage and T_Z is the transimpedance gain of the second stage. To calculate the gains, we refer to the detailed schematic in Figure 2 and denote with subscript p_1 the small-signal parameters of M_{1_A} M_{1_B} M_{2_A} M_{1_B}, with subscript n_1 the small-signal parameters of M_{3_A} M_{3_B} M_{4_A} M_{4_B}, with subscript n_2 the parameters of M_5 and M_6, and with subscript p_2 those of M_7 and M_8. Note that we have exploited both the symmetry of the matched devices and the identity of their bias point due to the appropriate sizing of the devices.

Therefore:

$$g_{m_{1_{A(B)}}} = g_{m_{2_{A(B)}}} = g_{m_{p_1}}; \quad g_{mb_{1_{A(B)}}} = g_{mb_{2_{A(B)}}} = g_{mb_{p_1}}; \tag{2}$$

$$g_{mb_{4_{A(B)}}} = g_{mb_{n_1}}; \quad g_{mb_{7(8)}} = g_{mb_{p_2}}; \tag{3}$$

$$g_{m_{5(6)}} = g_{m_{n_2}}; \tag{4}$$

$$C_{gs_{1_{A(B)}}} = C_{gs_{2_{A(B)}}} = C_{gs_{p_1}}; \quad C_{gs_{5(6)}} = C_{gs_{n_2}}; \tag{5}$$

and under the hypotheses that

$$g_{ds_{1A(B)}} + g_{ds_{2A(B)}} << g_{m_{1_{A(B)}}} \tag{6}$$

$$C_{gd_{2_{A(B)}}} << C_{gs_{1_{A(B)}}} + C_{gs_{2_{A(B)}}} \tag{7}$$

$G_{M_{A(B)}}$ can be calculated as:

$$G_{M_{A(B)}} = g_{mb_{p_1}} \cdot \frac{1 + s\frac{C_{gs_{p_1}}}{g_{m_{p_1}}}}{1 + s\frac{2C_{gs_{p_1}}}{g_{m_{p_1}}}} \tag{8}$$

Since the ratio between the pole and the zero in the above equation is 2 and because they are at a high frequency, the effect of the pole–zero doublet can usually be neglected.

Now, focusing on the second stage, the transimpedance gain T_z can be expressed as:

$$T_z = \frac{g_{m_{n_2}}}{g_{mb_{n_1}}\left(g_{ds_{n_2}} + g_{ds_{p_2}}\right)} \cdot \frac{1 - s\frac{C_{gd_{n_2}}}{g_{m_{n_2}}}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{9}$$

where p_1 and p_2 are respectively equal to:

$$p_1 = \frac{g_{ds_{n_2}} + g_{ds_{p_2}}}{C_L} \tag{10}$$

$$p_2 = \frac{g_{mb_{n_1}}}{C_{gs_{n_2}}} \tag{11}$$

In Equation (9), we neglect the effect of the pole–zero doublet of the current mirror M_7–M_8, analogously to the one in Equation (8), and that of the mirror M_{4_A}–M_5 (M_{4_B}–M_6), since they have a negligible impact on the frequency response. In addition, the additional pole–zero doublets were neglected due to transistors $M_{4_{A(B)}}$ and $M_{5(6)}$, thus introducing a limited error in the frequency response derivation.

Now, we focus on the DC differential gain, which can be expressed as:

$$A_{V_D} = 2 \cdot \frac{g_{mb_{p_1}}}{g_{mb_{n_1}}} \cdot \frac{g_{m_{n_2}}}{g_{ds_{n_2}} + g_{ds_{p_2}}} \tag{12}$$

Considering Equations (8) and (9), it is clear that the dominant pole is given by the output impedance $g_{ds_8} + g_{ds_6}$, whereas the poles and zeros proportional to g_{mb_i} or g_{m_i} are positioned at a higher frequency. Therefore, the GBW can be easily derived as:

$$GBW = A_{V_D} \cdot \frac{p_1}{2\pi} = \frac{1}{\pi} \frac{g_{mb_{p_1}}}{g_{mb_{n_1}}} \cdot \frac{g_{m_{n_2}}}{C_L} \tag{13}$$

3.2. Common-Mode Gain

The common-mode gain was estimated under the hypothesis of there being no mismatch between the two input transconductors (i.e., $G_{M_A} = G_{M_B}$).

According to these approximations and to Equation (3), the common-mode gain can be written as:

$$A_{V_C} = g_{m_{n_2}} \frac{\alpha}{1+\alpha} \cdot \frac{g_{mb_{p_1}}}{g_{mb_{n_1}}} \cdot \frac{\beta}{1+\beta} \cdot \frac{\gamma}{1+\gamma} \cdot \frac{1}{g_{ds_{n_2}} + g_{ds_{p_2}}} \tag{14}$$

where α depends on the M_1–M_2 current mirror:

$$\alpha = \frac{g_{ds_{n_1}} + g_{ds_{p_1}}}{g_{m_{n_1}}} \tag{15}$$

β is defined as:

$$\beta = \frac{g_{ds_{n_1}} + g_{ds_{p_1}}}{g_{mb_{p_1}}} \tag{16}$$

and the third term γ depends on the M_7–M_8 mirror:

$$\gamma = 2 \cdot \frac{g_{ds_{p_2}}}{g_{mb_{p_2}}} \tag{17}$$

The factors in Equations (15)–(17) are inversely proportional to g_m/g_{ds} (the intrinsic gain of the device) or g_{m_b}/g_{ds} (the intrinsic gain when driven by the body terminal). Equation (14) thus shows that, for the ideal case of infinite output resistance (infinite intrinsic gain), the common-mode gain would be zero. This is, however, not the case for deep submicron devices, which present a limited intrinsic gain; thus, the gain in Equation (15) is not negligible. Equations (13)–(15) allow the calculation of the CMRR as:

$$CMRR = 2\left(1 + \frac{1}{\alpha}\right)\left(1 + \frac{1}{\beta}\right)\left(1 + \frac{1}{\gamma}\right) \tag{18}$$

3.3. Noise Analysis

The noise analysis of the amplifier can be performed by considering a current noise generator between the drain and source terminals for each device. The generator includes both thermal channel noise and flicker noise; thus, its power spectral density can be expressed with Equation (19):

$$I_{n(p)_d} = I_{n(p)_w} + I_{n(p)_f} \tag{19}$$

where:

$$\overline{i^2_{n(p)_w}} = 4kTn_{n(p)}\gamma g_{m_i} \approx 2qI_d \tag{20}$$

$$\overline{i^2_{n(p)_f}} = \frac{K_{n(p)}}{fC_{ox}}\frac{g^2_m}{WL} \tag{21}$$

The equivalent input noise voltage can be derived by calculating the output voltage due to the noise sources and dividing it by the differential gain in Equation (12).

$$\overline{v^2_{eq}} = \frac{\overline{i^2_{n_1}} + \overline{i^2_{p_1}}}{g^2_{m_{b_{p_1}}}} + \frac{g^2_{m_{b_{n_1}}}}{2g^2_{m_{b_{p_1}}}g^2_{m_{n_2}}}\left(\overline{i^2_{n_2}} + \overline{i^2_{p_2}}\right) \tag{22}$$

The resulting power spectral density can be expressed as Equation (22), where the noise spectra $\overline{i^2_{n(p)_i}}$ (i = 1, 2) represent the noise spectra of i-th NMOS or PMOS stage.

Therefore, Equation (22) shows that the main noise contributions are due to the input stages of N(P)MOS, as can be expected. However the body-driven stage rejects the noise contributions less efficiently than the gate-driven ones. Thus, a larger device size must be chosen to achieve the same noise performance.

3.4. Large-Signal Analysis

The amplifier was optimized for large-signal performance by exploiting class AB behavior. Indeed, the first-stage output current is not limited by the $M_{3(A,B)}$ bias current I_{bias}, but by the voltage swing on the input body terminals. The output terminal of the first stage can thus practically reach the supply voltage V_{DD}. Therefore, the current in the output stage is also not limited by the bias current, but by the maximum V_{gs} of M_5 and M_6. To be more precise, the negative slew rate is limited by the gate voltage of M_6 reaching the supply voltage. On the other hand, the maximum current of M_8 is limited by the available voltage swing of the body terminal of M_7 and M_8, thus resulting in a slightly asymmetrical slew rate. The positive and negative slew rates are respectively equal to:

$$SR_+ = \frac{I_{d_0}}{C_L} \cdot \frac{W_8}{L_8} \cdot \exp\left(\frac{\alpha V_{DD} - V_{th_{p_0}} - V_{gs_{q8}}}{nU_T}\right) \tag{23}$$

and

$$SR_- = \frac{I_{d_0}}{C_L} \cdot \frac{W_6}{L_6} \cdot \exp\left(\frac{V_{DD} - V_{th_n}}{nU_T}\right) \tag{24}$$

where $V_{th_{p_0}}$ represents the absolute value of the threshold voltage when V_{sb} is equal to 0. On the other hand, in Equation (24), the V_{th_n} represents the NMOS threshold voltage at the selected V_{bs_n}.

4. Amplifier Design and Simulation Results

The proposed amplifier was designed with the 130 nm STMicroelectronics CMOS technology and simulated within the Cadence Virtuoso environment.

4.1. Sizing

To achieve the minimum power consumption with a supply voltage V_{dd}-V_{ss} of only 0.3 V and $|V_{th}| \approx 0.35$ V, all devices were biased in the sub-threshold region, and $|V_{ds}|$ and $|V_{gs}|$ were equal to 150 mV. A load capacitance C_L of 40 pF was assumed in reference to a typical IoT sensor interface application [16,40–43].

Large transistor widths and lengths were used to reduce the contributions of thermal and flicker noise, which represent a crucial issue in body-driven amplifiers [21,39,44]. In fact, larger devices have lower narrow- and short-channel effects, lower flicker noise, and larger body transconductance, which are useful for ULV and ULP applications. The bias current of the two symmetrical stages G_{M_A} and G_{M_B} was set to 13.1 nA as a tradeoff between noise and power consumption. The bias current of the second stage was set to about 95 nA as a tradeoff between slew rate, GBW, and phase margin for the assigned load capacitance. The sizing of the MOS transistors and their small-signal parameters are reported in Table 1.

Table 1. Transistor sizing and small-signal parameters of the proposed OTA.

	W[µm]	**L [µm]**	I_D **[nA]**	g_m **[nS]**	g_{mb} **[nS]**	g_{ds} **[nS]**
$M_{1,2A(B)}$	15	2	13	396.3	65.38	2.13
$M_{3,4A(B)}$	1.5	9.3	13	335.4	58.61	4.13
$M_{5,6}$	12	9.3	95	2462	430.3	25.90
$M_{7,8}$	120	2	95	2903	35.29	15.67

4.2. Circuit Simulations

The results of the open-loop AC simulations of the proposed OTA are reported in Figures 3 and 4. In particular, Figure 3 shows that the amplifier attains an overall DC gain and GBW of about 40 dB and 18.65 kHz, respectively, as expected from the model in Equations (12) and (13). Furthermore, as previously mentioned, the pole–zero doublets have a marginal effect on the amplifier frequency response. The positive zero $g_{mn_2}/C_{gd_{n_2}}$ is at a much greater frequency than the poles p_1 and p_2, and is therefore negligible. The phase margin (mφ) of the amplifier is set with the position of pole p_2 with respect to the unity gain frequency: the transistor sizing reported in Table 1 results in mφ = 52°. Figure 4 shows the CMRR of the amplifier, which resulted in about 67 dB.

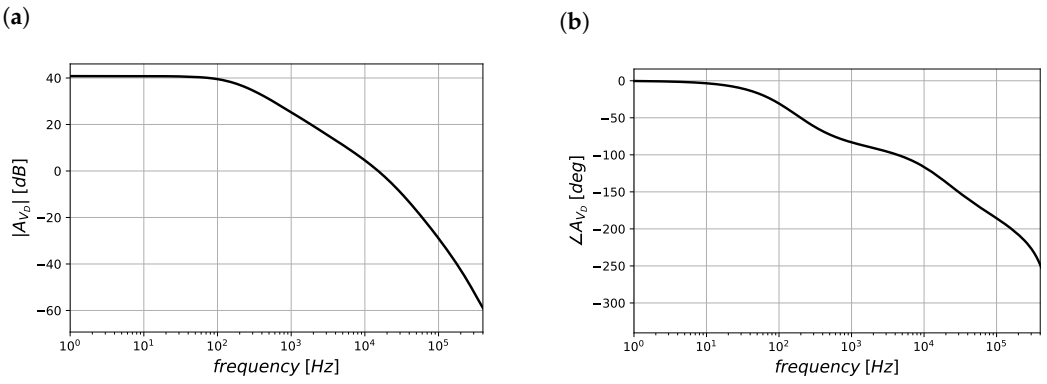

Figure 3. Differential gain of the proposed OTA: magnitude (**a**) and phase (**b**).

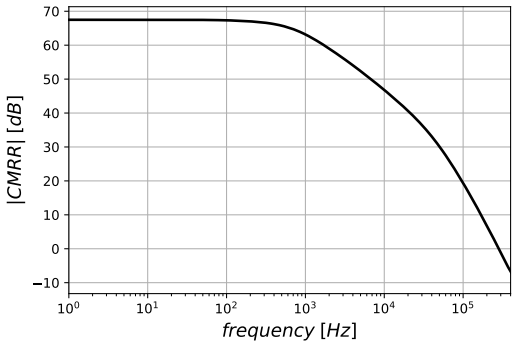

Figure 4. CMRR of the proposed OTA.

The amplifier was then simulated in a non-inverting buffer configuration, as shown in Figure 5a. The closed-loop frequency response of the OTA is depicted in Figure 5b, whereas the DC transfer characteristics are shown in Figure 6a, which highlights a rail-to-rail behavior. Figure 6b shows the dependence of the first-stage bias current when the amplifier is excited with a rail-to-rail signal. The positive and negative slew rates of the proposed amplifier were simulated with a full-swing input square wave. Figure 7a shows the time-domain response of the non-inverting buffer in the slew-rate test. The positive and negative slew rates are SR_+ = 10.83 V/ms and SR_- = 32.37 V/ms, respectively, and are thus in good agreement with Equations (23) and (24). The simulation results validate the preliminary analysis. The total harmonic distortion (THD) was simulated for different values of the peak-to-peak amplitude of a sinusoidal wave as the input, and is plotted in Figure 7b, which shows a THD lower than 1% for peak-to-peak amplitudes lower than about 230 mV. The plot of the power supply rejection ratio (PSRR) as a function of frequency is reported in Figure 8a, which shows a PSRR of about 45 dB at low frequencies.

(**a**) (**b**)

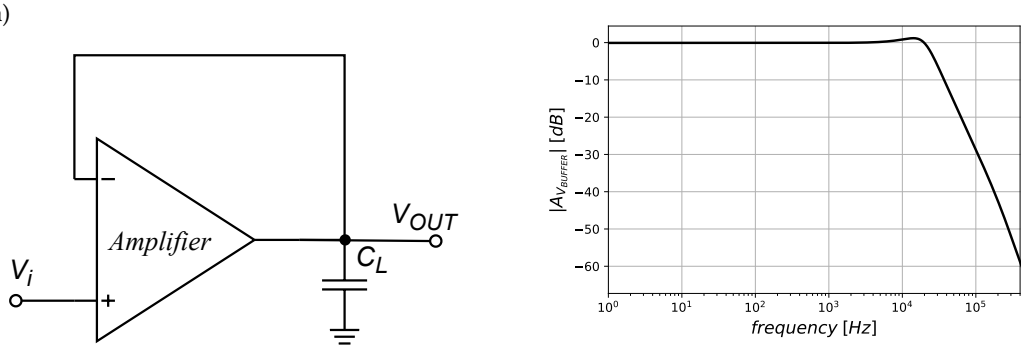

Figure 5. Schematic of the unity gain non-inverting buffer (**a**) and closed-loop frequency response (**b**).

(**a**) (**b**)

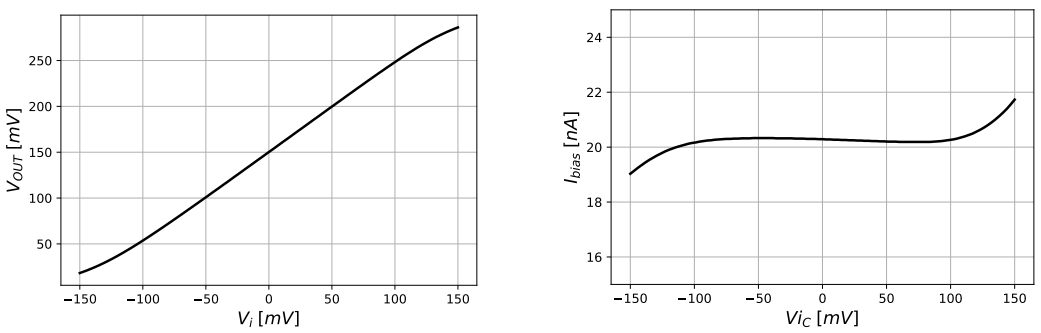

Figure 6. DC input–output transfer characteristics of the buffer (**a**) and quiescent current of the input stage as a function of the input common-mode voltage (**b**).

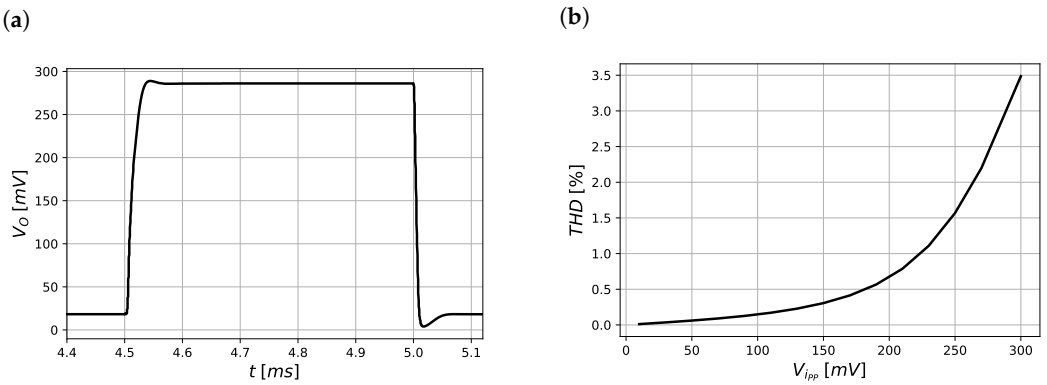

Figure 7. Transient response to a full-swing square-wave input. (**a**) and the THD as a function of the peak-to-peak amplitude of the input voltage (**b**).

Figure 8b reports the input-referred noise plot of the proposed OTA, which shows a noise corner frequency of about 1 kHz and an input-referred noise at f_{nc} of about 2.1 $\mu V/\sqrt{Hz}$.

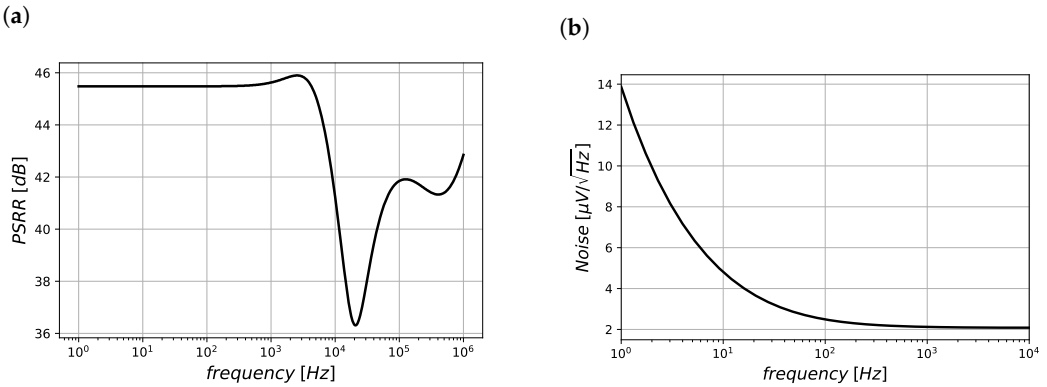

Figure 8. PSRR (**a**) and input-referred noise (**b**) of the proposed OTA.

4.3. Robustness to Mismatch and PVT Variations

The robustness of the amplifier to device mismatches was validated through Monte Carlo simulations, whose results are summarized in Table 2. The results are consistent with those of typical simulations. However, mismatches negatively affect the CMRR of the amplifier, as it strongly depends on the matching between two symmetrical paths. The Monte Carlo simulations still show a CMRR of about 52 dB, which is a good result considering the low supply voltage and the lack of tail generators. The amplifier area amounts to about 0.0036 μm^2, and it was estimated with the aid of Cadence Layout XL. Additionally, the amplifier performances were also validated using PVT variations. The amplifier shows a good stability with $\pm$10% supply voltage variations, as shown in Table 3.

It has to be pointed out that the proposed topology can work at higher supply voltages provided that the circuit is properly resized according to the main guidelines reported at the beginning of this section (e.g., $|V_{ds}|$ and $|V_{gs}|$ are equal to half of $|V_{dd}$-$V_{ss}|$). As a confirmation, we successfully resized the circuit to operate at 0.4 V, thus obtaining an improvement of about 12 dB in the DC gain. If a supply voltage in the range of 0.6 V is available, the topology can still work, but in this case, it would be preferable to add cascode MOS devices in order to keep the devices in the sub-threshold and to achieve a much larger DC gain.

Table 4 reports the performance of the OTA as a function of the operating temperature, showing that the amplifier is robust in a range of $[-10, 80]$ °C, whereas at higher temperatures, the performances exhibit larger variations. However, if needed, the effects of

temperature variations could be mitigated by exploiting PTAT (proportional to absolute temperature) current sources.

Table 2. Results of mismatched Monte Carlo simulations.

Output	Offset [mV]	Pd [nW]	SR_p [V/ms]	SR_m [V/ms]	SR_{AVG} [V/ms]	Gain (1 Hz) [dB]	mφ [deg]	GBW [kHz]	CMRR [dB]
Mean	0.072	73.3	10.82	32.32	21.57	42.93	52.12	18.6	51.77
Std Dev	4.614	7.16	1	0.189	0.488	3.597	3.156	2.187	5.64

Table 3. Amplifier performance vs. power supply voltage variations [±10%].

V_{dd}-V_{ss} [mV]	270.0	276.0	282.0	288.0	294.0	300.0	306.0	312.0	318.0	324.0	330.0
Pd [nW]	49.41	53.40	57.77	62.50	67.60	73.09	79.00	85.32	92.04	99.11	106.4
SR_- $[\frac{V}{ms}]$	19.10	21.44	23.90	26.54	29.37	32.37	35.48	38.69	41.92	45.17	48.28
SR_+ $[\frac{V}{ms}]$	9.404	10.13	10.73	11.11	11.16	10.83	10.21	9.472	8.727	8.031	7.411
mφ [deg]	71.30	65.64	61.04	57.57	54.63	51.93	49.38	46.99	44.80	43.86	42.32
DC Gain (dB)	40.32	39.82	39.61	39.85	40.29	40.80	41.36	41.97	42.71	43.68	45.14
GBW [kHz]	8.908	10.73	12.96	15.02	16.87	18.65	20.41	22.16	23.82	25.27	26.29
CMRR (dB)	47.75	51.10	57.58	65.01	68.67	67.49	64.54	61.42	58.46	55.76	53.62
Offset [mV]	3.834	2.049	1.090	0.62	0.36	0.17	0.006	−0.17	−0.38	−0.67	−1.094
Noise $[\mu V/\sqrt{Hz}]$	2.310	2.184	2.130	2.120	2.120	2.123	2.128	2.133	2.140	2.151	2.172

Table 4. Amplifier performance vs. temperature variations: [−10, 110] °C.

Temperature [°C]	−10.00	0.000	10.00	20.00	30.00	40.00	50.00	60.00	70.00	80.00	90.00	100.0	110.0
Offset [mV]	10.67	4.459	1.314	0.45	0.057	−0.472	−1.896	−5.711	−12.00	−19.81	−28.76	−38.95	−50.75
Pd [nW]	36.98	43.88	53.05	64.17	77.19	91.88	106.7	117.7	123.8	127.3	130.0	132.6	136.2
DC Gain [dB]	41.03	43.13	41.71	40.97	40.76	40.97	43.14	57.92	43.00	35.33	30.75	27.28	24.68
GBW [kHz]	6.640	8.192	12.04	16.17	19.65	22.46	22.76	20.62	18.93	17.56	16.22	14.83	13.39
mφ	81.84	74.83	63.13	55.88	50.38	46.00	43.98	45.80	48.02	49.34	50.51	51.98	54.16
CMRR [dB]	51.68	51.08	58.23	70.93	64.75	55.80	49.28	58.52	40.79	31.49	25.99	22.21	19.99
SR_p [V/ms]	10.50	11.78	12.27	11.78	10.32	8.551	6.996	5.802	5.001	4.525	4.211	3.960	3.735
SR_m [V/ms]	22.62	26.41	29.03	31.08	32.90	34.27	35.11	35.55	35.64	35.50	35.10	34.46	33.54
SR_{AVG} [V/ms]	16.56	19.10	20.65	21.43	21.61	21.41	21.05	20.68	20.32	20.01	19.66	19.21	18.64
Noise [μ V/$\sqrt{Hz}$]	2.367	2.197	2.042	2.079	2.143	2.214	2.348	2.717	3.095	3.362	3.563	3.726	3.860

4.4. Results and Comparison with the Literature

In Table 5, the proposed amplifier is compared to other ULV–ULP topologies from the literature. To fairly compare the performance of different designs, we considered the following well-known small-signal and large-signal FOMs:

$$IFOM_S = \frac{GBW \cdot C_L}{I_{TOT}} \tag{25}$$

$$IFOM_L = \frac{SR_{AVG} \cdot C_L}{I_{TOT}} \tag{26}$$

$$FOM_S = \frac{GBW \cdot C_L}{P_{DISS}} \tag{27}$$

$$FOM_L = \frac{SR_{AVG} \cdot C_L}{P_{DISS}} \tag{28}$$

The small-signal FOMs (25) and (27) measure the efficiency of the OTA in providing high-frequency performance, since they measure the gain–bandwidth product, which is normalized to the load capacitance, for a given power consumption. In particular, both the total DC current and power consumption are taken into account. This also allows the comparison of the effects of different supply voltages. Analogously, the FOMs (26) and (28) measure the efficiency for large-signal behavior, since they measure the slew rate, which is normalized to the load capacitance, for a given power or current consumption. This is particularly significant for class AB amplifiers, where the large-signal performance is often the most significant one. As in the literature, the average slew rate is considered; however, for practical applications, the parameter of interest is the worst-case slew rate; thus, the FOMs (29) and (30) were also considered:

$$IFOM_{L_{WC}} = \frac{SR_{WC} \cdot C_L}{I_{TOT}} \tag{29}$$

$$FOM_{L_{WC}} = \frac{SR_{WC} \cdot C_L}{P_{DISS}} \tag{30}$$

In the cases where the OTA presents an asymmetric slew rate, both kinds of large-signal FOMs could be of interest.

The comparison in Table 5 shows that the proposed amplifier provides a trade-off between small-signal and large-signal FOMs in the state of the art. The OTAs in [28,36,44] present higher values for the small-signal FOMs; however, their large-signal performance is not optimized. The authors of [44] also used a higher supply voltage; nevertheless, their FOM_S in Equation (27) was lower than the OTA in this work. The topology in [28] is made up of an Arbel-like body-driven pseudo-differential input stage followed by a dual-path differential-to-single-ended converter with gain, and the resulting OTA is compensated by a Miller capacitance. The OTA presented in this paper has a common-mode cancelling body-driven input stage with a body-diode load, which produces a high-frequency pole, followed by a differential-to-single-ended converter, without the need for Miller compensation, as the OTA is output-compensated. The proposed design exhibits a much better slew rate and, consequently, large-signal FOM performance than those in [28]. The amplifier in [35] presents a higher value for the large-signal FOMs due to its class-AB approach, even if the worst-case SR is much lower than the average value. On the other hand, the amplifier in [38] presents good values for this latter FOM. Both of these amplifiers are, however, optimized for the large-signal behavior, providing lower values than the proposed ones for the small-signal FOMs.

Table 5. Comparison with the state of the art.

	This Work [a]	[28] [a]	[39] [b]	[29] [a]	[36] [b]	[35] [b]	[44] [a]	[31] [b]	[30] [a]	[38] [b]	[45] [b]	[32] [b]	[46] [b]	[34] [b]
Year	2021	2021	2020	2020	2020	2020	2020	2019	2018	2018	2015	2014	2014	2014
Technology [µm]	0.13	0.13	0.18	180	0.18	0.18	0.18	0.13	0.065	0.18	0.065	0.13	0.18	0.13
V_{DD} $[V]$	0.3	0.3	0.3	0.3	0.3	0.3	0.5	0.3	0.3	0.3	0.35	0.25	0.5	0.25
V_{DD}/V_{TH} $[V]$	0.86	0.86	0.6	0.6	0.6	0.6	1.19	0.86	-	0.6	1.16	1.16	1.29	1.16
DC_{gain} [dB]	40.80	64.6	64.7	39	30	98.1	69.5	49.8	60	65.8	43	-	70	60
C_L $[pF]$	40	50	30	10	150	30	15	2	5	20	3	20	30	15
GBW [kHz]	18.65	3.58	2.96	0.9	0.25	3.1	36	9100	70	2.78	3600	-	18	1.88
$m\varphi$ $[deg]$	51.93	53.76	52	90	90	54	65	76	53	61	56	-	55	52.5
SR_+ $[\frac{V}{ms}]$	10.83	1.7	1.9	-	0.068	14	9.7	-	25	6.44	5600	-	3	0.64
SR_- $[\frac{V}{ms}]$	32.37	0.15	6.4	-	0.101	4.2	9.7	-	25	7.8	5600	-	3	0.77
SR_{avg} $[\frac{V}{ms}]$	21.60	0.93	4.15	-	0.085	9.1	9.7	3.8	25	7.12	5600	94.60	3	0.71
THD [%]	1.4	0.84	1	1	2	0.49	0.27	-	-	1	-	0.53	-	0.2
% of input swing	80	100	85	23	90	83.33	80	-	-	93.33	-	40	-	60
CMRR [dB]	67.49	61	110	30	41	60	90	-	126	72	46	-	-	-
PSRR [dB] [c]	45	26/28	56	33	30	61	81/99	-	90/91	62	35	-	-	-
$spot-noise$ $[\frac{\mu V}{\sqrt{Hz}}]$	2.12	2.69	1.6	0.81	-	1.8	0.91	0.035	2.82	1.85	0.93	7.07	0.31	3.3
@freq	1000	100	-	1000	-	-	1000	100,000	1000	36	-	200	1000	100
Power [nW]	73	11.4	12.6	0.6	2.4	13	60	1800	51	15.4	17,000	10	75	18
Mode	BD	BD	BD	GD	DIGITAL	BD	BD	GD	BD	BD	BD	BD	GD	BD
$IFOM_S$ $[\frac{MHz \cdot pF}{mA}]$	3061	4711	2114	4500	4680	2148	4500	3033	2058	1083	223	-	3600	392
$IFOM_L$ $[\frac{V \cdot pF}{\mu s \cdot mA}]$	3057	1224	2964	-	1590	6300	1213	1400	735	2790	346	-	680	146
FOM_S $[\frac{MHz \cdot pF}{mW}]$	10,200	15,702	7047	15,000	15,600	7154	9000	10,111	6862	3610	635	-	7200	1568
FOM_L $[\frac{V \cdot pF}{\mu s \cdot mW}]$	11,820	4079	9880	-	5300	21,000	2425	4666	2450	9247	988	-	1200	587
$IFOM_{L_{WC}}$ $[\frac{V \cdot pF}{\mu s \cdot mA}]$	1589	197	1357	-	1275	1890	1212	-	735	2509	345.8	-	600	146
$FOM_{L_{WC}}$ $[\frac{V \cdot pF}{\mu s \cdot mW}]$	5926	658	4524	-	4250	6300	2425	-	2450	8364	988	-	1200	583
Area [mm^2]	0.0036	0.0064	0.0085	0.00047	0.000982	0.0098	0.0034	-	0.003	0.0082	0.0050	0.053	0.057	0.083

[a] Simulated. [b] Measured. [c] $PSRR_+/PSRR_-$ [dB].

5. Conclusions

In this paper, we proposed an ultra-low-voltage amplifier that operates at a supply voltage of 0.3 V and attains good Figures of Merit for both small-signal and large-signal behaviors. The amplifier exploits a pseudo-differential body-driven fully differential input stage and a gate-driven second stage, which performs differential-to-single-ended conversion. This provides a rail-to-rail input common-mode signal swing, large DC gain and CMRR, and good frequency performance. In particular, the amplifier does not present high-impedance internal nodes thanks to the body-diode active loads; thus, it does not require Miller compensation. The gate terminals are used for biasing, thus achieving robustness against PVT variations.

The comparison against the state of the art of ULV OTAs has shown how the proposed topology optimizes the trade-off between small-signal and large-signal performance, and achieves very good values for all of the considered FOMs.

On the other hand, the proposed architecture presents limitations in terms of noise performance, exhibits an input impedance that is not purely capacitive, and shows a CMRR that is strongly dependent on mismatch variations. Another limitation is due to the body-driven current mirror load of the second stage, which causes an asymmetric slew rate. Nevertheless, these drawbacks are common to many ULV and ULP OTAs, in which a trade-off between many requirements has to be pursued.

It also has to be pointed out that, even if we presented results referring to a 130 nm CMOS process, the proposed topology can be implemented in even more advanced CMOS technology nodes, provided that the design guidelines outlined in the manuscript are properly followed. In particular, if a fully depleted silicon-on-insulator (FDSOI) CMOS process is available, the implementation of the proposed OTA (as well as of all body-driven OTAs) results in an input impedance similar to those of gate-driven circuits, and this is an interesting advantage over implementations based on conventional bulk CMOS processes, especially if switched applications are targeted.

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Abbreviations

The following abbreviations are used in this manuscript:

BD	Body-Driven
CMFB	Common-Mode Feedback
CMRR	Common-Mode Rejection Ratio
GD	Gate-Driven
FOM	Figure of Merit
ICMR	Input Common-Mode Range
IoT	Internet of Things
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
PVT	Process, Supply Voltage, and Temperature
THD	Total Harmonic Distortion
ULV	Ultra-Low Voltage
ULP	Ultra-Low Power

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