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# A Power Efficient Frequency Divider With 55 GHz Self-Oscillating Frequency in SiGe BiCMOS

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**Abstract:** A power efficient static frequency divider in commercial 55 nm SiGe BiCMOS technology is reported. A standard Current Mode Logic (CML)-based architecture is adopted, and optimization of layout, biasing and transistor sizes allows achieving a maximum input frequency of 63 GHz and a self-oscillating frequency of 55 GHz, while consuming 23.7 mW from a 3 V supply. This results in high efficiency with respect to other static frequency dividers in BiCMOS technology presented in the literature. The divider topology does not use inductors, thus optimizing the area footprint: the divider core occupies  $60 \times 65 \mu\text{m}^2$  on silicon.

**Keywords:** frequency divider; Current Mode Logic; low power; SiGe HBT design

## 1. Introduction

Frequency dividers are a fundamental building block in many RF and mixed-signal high-speed systems, such as frequency synthesizers, I/Q signal generators, carrier recovery systems, SerDes systems, and time-interleaved data converters [1–6]. The evolution of technology enables faster and faster systems to be designed, with an increasing demand on higher frequency performance for all the blocks, however, on the other hand, there is a growing impulse to minimize the power consumption for these high frequency systems, to allow higher integration and to simplify packaging. The performance of SiGe BiCMOS technologies over the last 20 years has been strongly improved, with  $f_T/f_{\text{max}}$  that have increased from 60/30 GHz [7] to reach record values of 500/700 GHz [8]. Therefore, SiGe BiCMOS is often used in very high frequency applications, allowing the design of RF systems in D-band [9] and wireline transceivers at 100 Gbaud and beyond [10].

Frequency dividers for high frequency systems in the literature are typically based on four architectures: static, dynamic, regenerative, and injection-locked dividers. Static frequency dividers (SFDs) are based on a D-type flip-flop closed in feedback [11] and provide the widest frequency range, ideally from dc to their maximum operating frequency. Dynamic frequency dividers (DFD) achieve higher frequencies but with a smaller operating range and higher sensitivity to process variations [12]. Regenerative frequency dividers (RFD) show the disadvantages of a higher jitter and limited frequency range [13]. Injection-locked frequency dividers (ILFD) can operate in higher frequency bands with low power consumption, but their frequency range is extremely limited [14], because they are intrinsically tuned circuits. Excluding the latter category, frequency dividers in the literature are reported with maximum input frequencies up to 166 GHz in SiGe BiCMOS [15]; higher frequencies can be achieved if III-V technologies are used [12].

Determination of maximum operating frequency can be limited by the test setup, therefore a figure of merit often used for the dividers is the self-oscillating frequency (SOF), which is (twice)

the oscillation frequency of the divider that acts as a ring oscillator, when no clock signal is applied. For input frequencies near the SOF, the input power needed to operate the divider presents a minimum.

In this paper, we present the design and measurements of a static frequency divider in commercial 55 nm SiGe BiCMOS technology, that has been optimized for low power consumption and low area footprint. The divider has been designed as part of an integrated system for high-speed analog-to-digital conversion working at least at 40 GS/s, and SiGe BiCMOS technology has been used, driven by overall system specifications and taking into account trade-offs among speed, power consumption, and requirements on supply voltage. In Section 2 we present the design of the frequency divider core; in Section 3 the design of the test chip with input and output buffers. Measurement results are presented in Section 4, and Section 5 compares the results with the literature and concludes.

## 2. Frequency Divider Design

The Current Mode Logic (CML) style is based on the exclusive-OR (XOR) gate as the fundamental building block, and is often adopted for the design of SFDs operating at high frequencies. The divide-by-2 SFD is usually implemented by a CML D-type flip-flop (DFF) closed in negative feedback ( $D = \overline{Q}$ ). The CML DFF is based on a master–slave architecture in which two D-latches, driven by opposite clock signals, are cascaded, as shown in Figure 1.

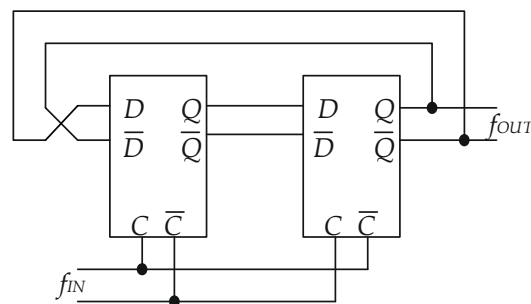


Figure 1. Block scheme of a Current Mode Logic (CML) static frequency divider.

Figure 2 shows the topology of a CML D-latch which is easily derived from the CML XOR gate. Inductive peaking, implemented by adding an inductor in series to the load resistors  $R_C$ , is sometimes adopted to enhance the performance of the divider, and achieve higher maximum operating frequencies. However, inductors require a large silicon footprint area. This large area is not a concern for RF applications, where a sparse layout style with transmission line interconnections are used, and inductors are exploited in the different blocks for tuning and impedance matching. In mixed-signal applications, a higher integration level is usually pursued, and the minimization of silicon area occupation with a denser lumped-style layout is extremely important.

The SFD presented in this work was designed in the framework of an integrated analog front-end for 40 GS/s analog-to-digital conversion, based on the Asynchronous Time Interleaving (ATI) principle [16]. In such applications, area and power minimization are very important issues in view of a high level of integration of the whole system. To minimize the footprint area of the divider, inductive peaking was not exploited: this also allowed minimization of the length of the feedback interconnection lines (see Figure 1), which can therefore be adequately described in a lumped component approach by the RLC equivalent parasitic model.

Without inductive peaking, the speed of the divider, both in terms of SOF and of maximum frequency, which is related to the clock-to-output propagation delay [17], is mostly limited by the output time constant of the DFF. The value of this time constant is set by the value of the load resistor  $R_C$  and of the capacitances at the output node, which depend both on the sizing of the transistors of the D-latch and on the length of layout interconnections.

The divider was designed to guarantee worst-case operation at 40 GHz, and to allow some margin for testing the overall system at higher bitrates. Starting point of the design procedure was choosing the required voltage drop on the load resistor of the latch,  $\Delta V = R_c I_{TAIL}$ , which we set to 150 mV in order to fully steer the tail current in the differential pairs, with some margin to cope with voltage fluctuations due to clock feedthrough, and with process, supply voltage and temperature (PVT) variations. Clock feedthrough is a critical issue in the design of CML static frequency dividers: with reference to Figure 2, let us consider the rising edge of the clock signal C. Transistor  $Q_1$  showed an increased base current, because carriers entered the base region when the transistor exited from interdiction [18]. Moreover, the source node voltage of the pair  $Q_1$ – $Q_2$  dropped when the pair was balanced, somehow reducing the tail current. All this reflects in a negative spike in the collector current, and thus in the output voltage of the D-latch, as shown in Figure 3. A too-deep spike of the output voltage could affect the behavior of the DFF and of the following blocks, in particular, when the divided output has to be used as clock signal in digital and mixed-signal applications.

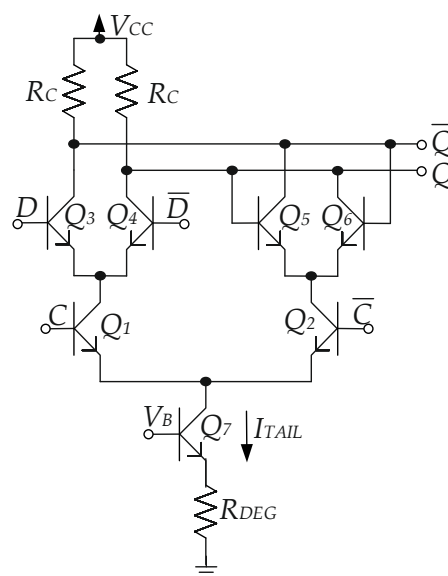


Figure 2. CML D-latch schematic.

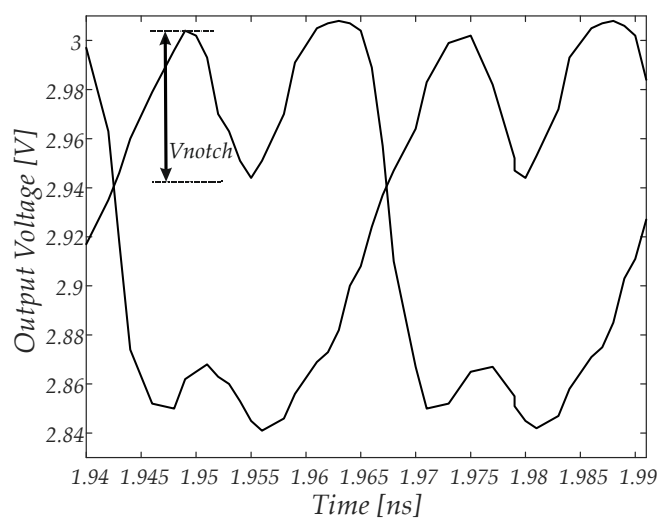


Figure 3. Output waveforms of the divider.

Once the voltage swing was set, a careful optimization of the latch design was carried out to achieve good and robust performance at 40 GHz. The available degrees of freedom were the tail current

$I_{TAIL}$  and size and layout of the transistors (total emitter area, and number of separate emitter areas); lower ( $Q_1$ – $Q_2$ ) and upper ( $Q_3$ – $Q_6$ ) levels of the D-latch were considered separately. The goals of the optimization were reliable operation of (at least) 40 GHz with sharp edges, limited clock feedthrough, low power consumption and robustness to PVT variations. An extensive set of simulations were carried out to characterize the effects of the design parameters on the output waveform of the divider, loaded by an emitter follower and a differential pair stage. The parasitic capacitive effect of interconnections, estimated in 5 fF, was also considered.

Figures 4 and 5 show the dependence of the 10–90% rise time and of the voltage drop  $V_{notch}$  due to the clock feedthrough (see Figure 3) on the design parameters  $I_{TAIL}$ ,  $L_{dn}$  and  $L_{up}$ , where the latter are the emitter lengths of the devices in the lower and upper differential pairs, respectively (emitter width is 0.2  $\mu\text{m}$ ). An  $I_{TAIL}$  of at least 2.5 mA was needed to produce an output waveform with sharp edges, but Figure 4 also shows some dependence of the clock feedthrough on the bias current. Total emitter area determines the current density, thus the  $f_T$  of the devices, but also affects the clock feedthrough [18]; these effects were particularly relevant for the lower differential pair, as shown by Figure 5a. In particular, a small emitter area minimized the notch on the output voltage, whereas sharper edges were obtained when the emitter area was increased. For the upper differential pair (Figure 5b), a minimum emitter length to current ratio of 0.5  $\mu\text{m}/\text{mA}$  was required to achieve full current switching; the emitter area had little effect on the notch, but affected the rise time, because larger transistors increased the parasitic output capacitance.

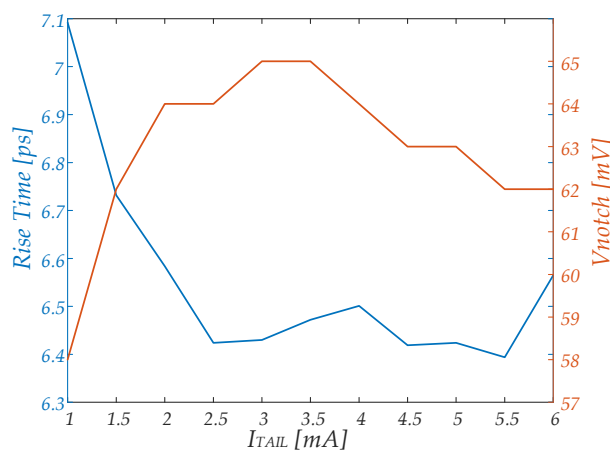


Figure 4. Dependence of rise time and notch voltage on the tail current of the latch.

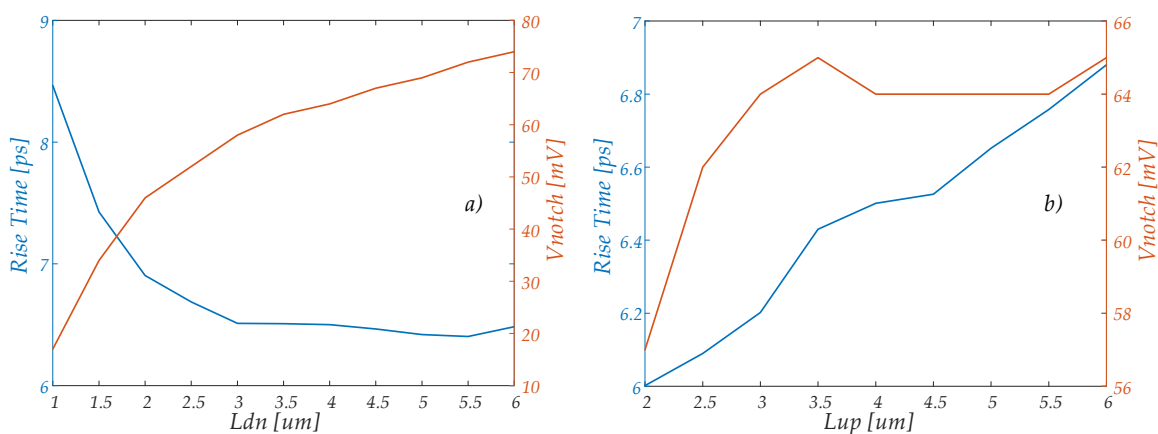
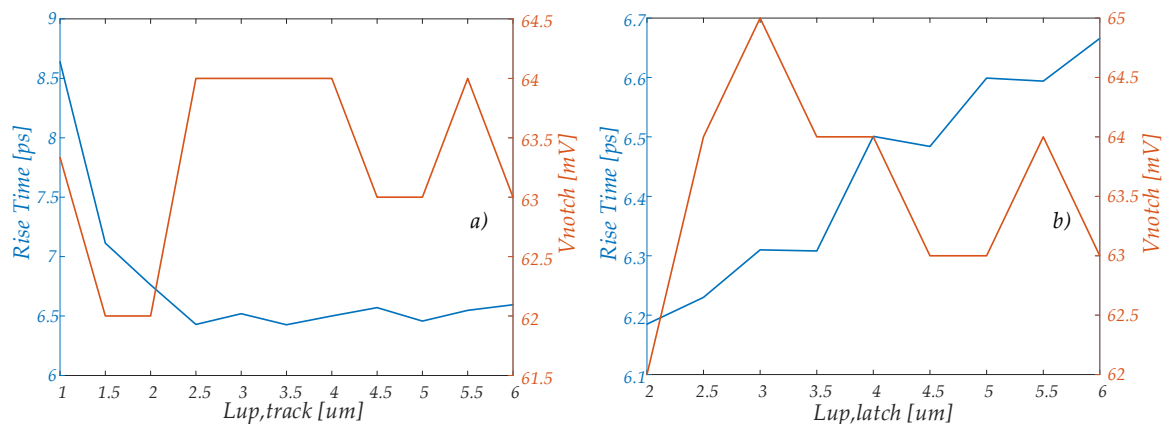


Figure 5. Dependence of rise time and notch voltage on the emitter length of (a) devices of the lower differential pair; and (b) devices of the upper differential pair.  $I_{TAIL}$  was 4 mA and the emitter length for the other devices was 4  $\mu\text{m}$ .

We also separately considered the effect of the emitter length of devices in the track ( $L_{up,track}$ ) and latch ( $L_{up,latch}$ ) differential pairs,  $Q_3$ – $Q_4$  and  $Q_5$ – $Q_6$ , respectively, in Figure 2. Figure 6 reports the dependence of the rise time and the notch voltage on these parameters, when  $I_{TAIL}$  was 4 mA and all the other emitter lengths were kept constant at 4  $\mu\text{m}$ . An increase in the area of the track devices improved the rise time without affecting the notch voltage, whereas increasing the latch devices slightly increased the rise time; the effect on the notch voltage was limited. Please note that the divider was not able to operate if an excessive current density was used in the latch devices (emitter length below 2  $\mu\text{m}$ ).



**Figure 6.** Dependence of rise time and notch voltage on the emitter length of the upper devices, considering separately (a) the track differential pair; and (b) the latch differential pair.  $I_{TAIL}$  was 4 mA and the emitter length for the other devices was 4  $\mu\text{m}$ .

We chose to keep the emitter area low for both upper and lower devices, setting the bias current to 4 mA as a trade-off between low power consumption and a limited notch in the output waveform.  $L_{dn}$  was chosen to be equal to 4  $\mu\text{m}$ , as a trade-off between sharp edges and a low notch, and the same value was also used for  $L_{up}$  to limit the current density, which would affect the full switching of the differential pairs, keeping some margin for PVT variations. Concerning the transistor layout, the output waveform was optimized when using a single emitter and single collector layout. This is justified by the fact that the capacitances both at the output nodes and at the sources of the upper level differential pair have a greater effect on the propagation delay than the parasitic base resistance, which is minimized when multiple emitter (and base) areas are used.

Degeneration resistors were added to the current mirror implementing the current source  $I_{TAIL}$  to maximize current matching and robustness. This also increased the output resistance, minimizing variations of the current  $I_{TAIL}$  and thus clock feedthrough.

The divider was designed and fabricated as 55 nm SiGe BiCMOS technology by STMicroelectronics [19], which offered both high speed HBT (heterojunction bipolar transistor) devices with  $f_T/f_{MAX}$  up to 320/370 GHz (high-speed devices, HS) and 1.5 V breakdown voltage and slower HBT transistors with a higher breakdown voltage (high-voltage devices, HV), together with passives (including inductors and transmission lines) and 9 levels of metals of different thickness. Table 1 synthesizes the sizing of the D-latch in Figure 2; a 3 V supply voltage was used.

The layout of the divider core (see Figure 7) was optimized to maximize the symmetry and minimize the length of the interconnection lines driven by the collectors of transistors in the latches, whose parasitic capacitance affects the output time constant and thus the divider speed. Figure 8 shows two alternative floorplans for the divider. In the floorplan of Figure 8a, the two D-latches are laid out side by side, and mirrored with respect to the vertical axis. The lines at the output of the D-latches, connecting the collectors of one D-latch, the bases of the latch pair of the same D-latch, and the bases of the track pair of the other D-latch, were fully symmetrical, their length was minimized, and any crossing with the input clock lines was avoided. The floorplan in Figure 8b, with the D-latches laid out

symmetrically with respect to the horizontal axis, minimizes the length of the high frequency clock lines, but at the cost of longer output lines which cross the clock lines, thus facilitating coupling and feedthrough. Due to the compact size of the layout of each D-latch ( $30 \times 65 \mu\text{m}^2$ ), the longer clock lines can still be efficiently driven by the input buffer, and we have preferred the floorplan of Figure 8a to optimize the output time constant of the D-latches and minimize clock feedthrough.

Table 1. Dimensions of transistors of the D-latch.

Transistor	Total Emitter Area ( $\mu\text{m}^2$ )	HBT Type and Number of Emitters
$Q_1, Q_2$	0.8	HS, 1 emitter
$Q_3, Q_4, Q_5, Q_6$	0.8	HS, 1 emitter
$Q_7$	3.2	HS, 2 emitters
Resistor	Value	-
$R_C$	$37.5 \Omega$	-
$R_{deg}$	$50 \Omega$	-

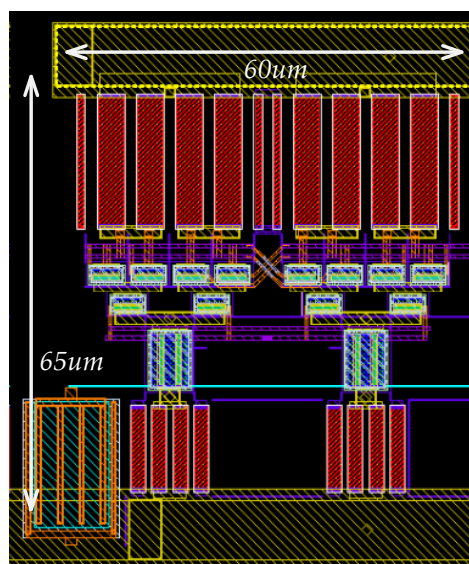


Figure 7. Layout of the divider core.

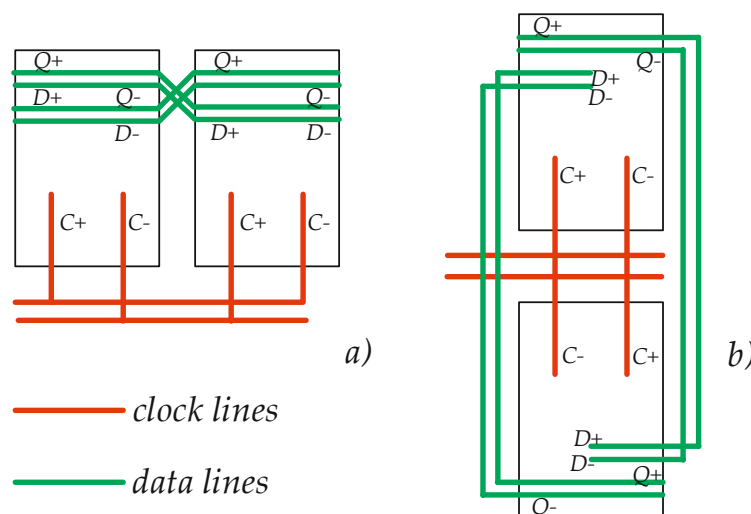


Figure 8. Floorplan of the D-type flip-flop (DFF): (a) D-latches flipped around the vertical axis; (b) D-latches flipped around the horizontal axis.

### 3. Design of the Divider Test Chip

The test chip included input and output buffers, to allow testing of the frequency divider block; wideband  $100\ \Omega$  differential buffers were used, to allow testing of the function over a wide frequency range.

Simple emitter followers were used for the input buffer, and their bias current was optimized to drive the D-latches with the connecting lines shown in Figure 7. Between the input lines and the supply voltage,  $50\ \Omega$  resistors were used for matching and biasing, as shown in Figure 9, thus allowing the use of an ac-coupled source without the need of an external biasing circuit. The common collector transistors are biased at about  $2.2\ \text{mA}$ , to provide an output resistance of about  $18\ \Omega$ .

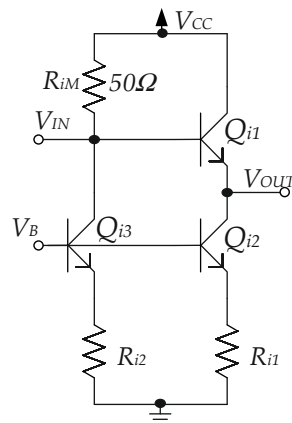


Figure 9. Schematic of the input buffer.

On the output side (Figure 10), the divider was followed by a limiting amplifier stage ( $Q_{05}$ – $Q_{08}$ ), to achieve sharper edges and limit the effect of clock feedthrough. The limiting amplifier was driven by an emitter follower (EF) ( $Q_{01}$ – $Q_{02}$ ) to minimize the loading effect and provide an adequate dc input level, and was followed by another emitter follower ( $Q_{010}$ – $Q_{011}$ ) to drive the output buffer. This was designed as a degenerated cascode differential pair ( $Q_{014}$ – $Q_{017}$ ), loaded by  $50\ \Omega$  resistors; the degeneration resistors are sized to provide about  $0\ \text{dB}$  gain when the buffer is loaded by an (ac-coupled)  $100\ \Omega$  differential load. To provide an adequate signal swing, a large dc current of more than  $26\ \text{mA}$  was used for the output buffer, thus requiring a careful design of the previous stages not to limit the bandwidth. Figure 11 shows the simulated frequency behavior of the output stage, highlighting a  $3\ \text{dB}$  bandwidth of  $64\ \text{GHz}$ .

Tables 2 and 3 report the sizing of the transistors in the input (Figure 9) and output (Figure 10) stages, respectively. It has to be noted that the test chip was designed with separate bias references for the different blocks, to maximize testing flexibility, through the use of external potentiometers to adjust the bias currents. Figure 12 shows the layout of the frequency divider including input and output stages. The different blocks are highlighted; the divider core occupies  $60 \times 65\ \mu\text{m}^2$ , whereas the total area of divider and buffers is  $190 \times 400\ \mu\text{m}^2$ . The divider is part of a larger test chip, whose dimension are pad-limited, and differential transmission lines have been added at the input and at the output to connect the pads.



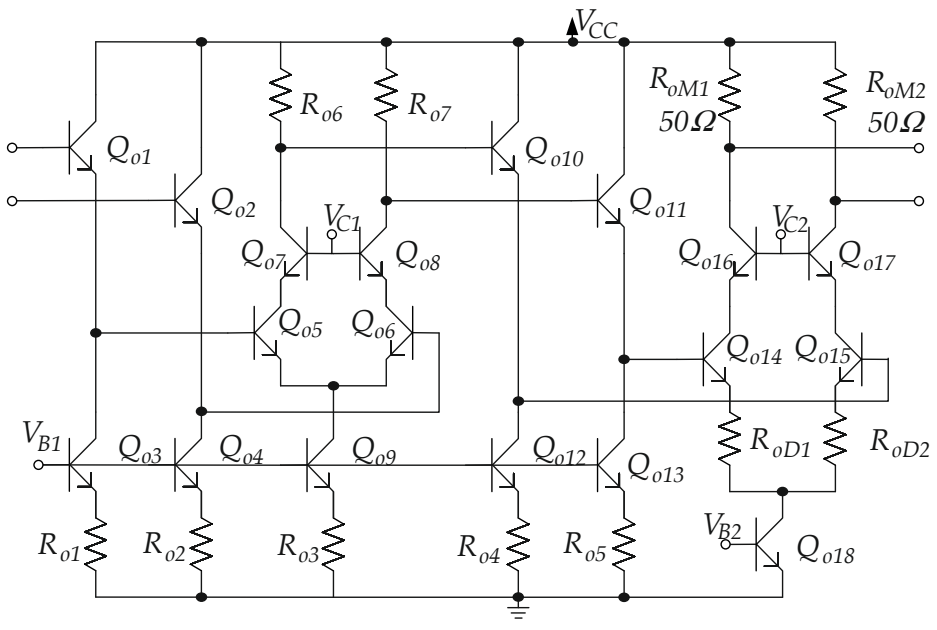


Figure 10. Schematic of the output buffer.

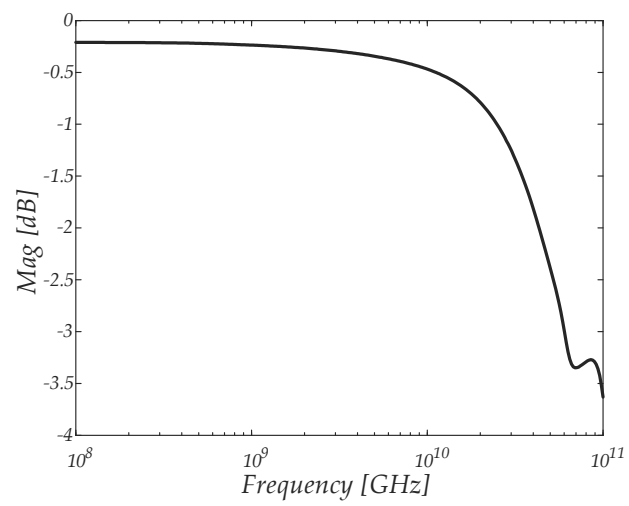


Figure 11. Simulated transfer function of the output stage.

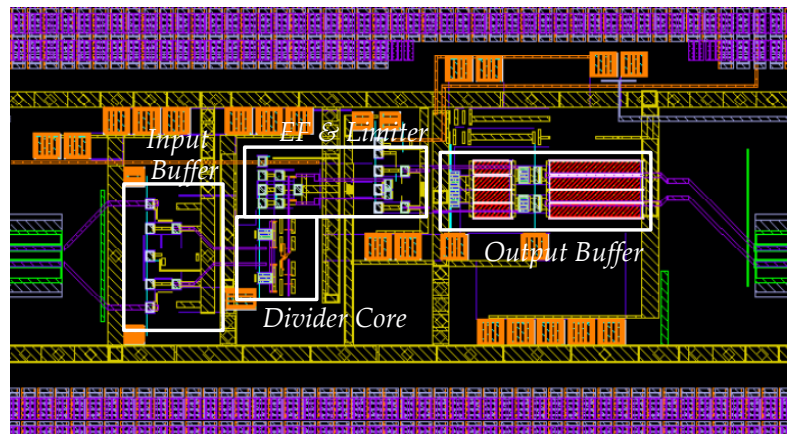


Figure 12. Layout of the full divider with input and output stages.



**Table 2.** Dimensions of transistors of the input stage.

Transistor	Total Emitter Area ( $\mu\text{m}^2$ )	HBT Type and Number of Emitters
$Q_{i1}$	1.6	HS, 2 emitters
$Q_{i2}, Q_{i3}$	1.6	HV, 2 emitters
<b>Resistor</b>	<b>Value</b>	-
$R_{iM}$	50 $\Omega$	-
$R_{i1}, R_{i2}$	100 $\Omega$	-

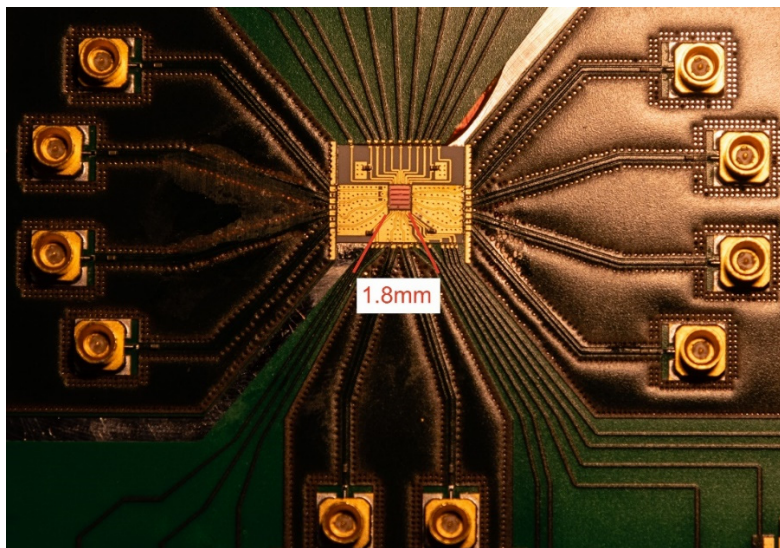
**Table 3.** Dimensions of transistors of the output stage.

Transistor	Total Emitter Area ( $\mu\text{m}^2$ )	HBT Type and Number of Emitters
$Q_{o1}, Q_{o2}$	0.4	HS, 1 emitter
$Q_{o3}, Q_{o4}$	1.6	HS, 2 emitters
$Q_{o5}, Q_{o6}$	1.2	HS, 2 emitters
$Q_{o7}, Q_{o8}$	0,6	HS, 1 emitter
$Q_{o9}$	1.6	HS, 2 emitters
$Q_{o10}, Q_{o11}$	1.6	HS, 2 emitters
$Q_{o12}, Q_{o13}$	1.6	HS, 2 emitters
$Q_{o14}, Q_{o15}$	4	HS, 4 emitters
$Q_{o16}, Q_{o17}$	2	HS, 4 emitters
$Q_{o18}$	8.4	HS, 8 emitters
<b>Resistor</b>	<b>Value</b>	-
$R_{o1}, R_{o2}, R_{o3}$	100 $\Omega$	-
$R_{o6}, R_{o7}$	100 $\Omega$	-
$R_{o4}, R_{o5}$	100 $\Omega$	-
$R_{oM1}, R_{oM2}$	50 $\Omega$	-
$R_{oD1}, R_{oD2}$	21.5 $\Omega$	-

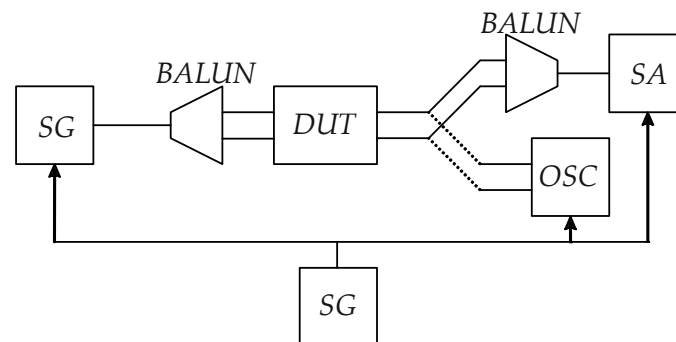
#### 4. Measurement Results

The test chip including the frequency divider was mounted bare die on a suitable board for testing. Figure 13 shows a photograph of the test board, fabricated on a 10 mil low-loss Rogers 4350B substrate, that includes SMPM connectors, and the biasing circuitry with filtering capacitors. Grounded coplanar lines with a resistance of 50  $\Omega$ , designed by 3D EM simulations, were used for the signals, and a discontinuity in the central strip was added to solder series decoupling microwave capacitors. An alumina interposer board, which allowed thinner lines with a small pitch to be designed, was used to allow short bonding wires to connect the IC; small metal strips were used to connect the lines on the alumina and on the Rogers board. The back sides of both the alumina substrate and of the board were metalized and grounded through a metal block, used also for mechanical support.

Figure 14 schematically shows the test setup: an HP83650B signal generator with a dc-50-GHz balun or an Anritsu 69397B generator with a dc-67-GHz balun were used to generate the input signal, and the output of the divider was sent to an Anritsu MS2668C spectrum analyzer through a dc-20-GHz balun, or to a Tektronix DSA8300 digital sampling oscilloscope. The circuit drew about 75 mA from the 3 V voltage supply, which was in line with the simulations. Most of this power consumption was due to the output buffer and to the current flowing in the input 50  $\Omega$  resistors to set the input dc bias: Table 4 reports the simulated power consumption of the different blocks of the circuit, showing that the divider core dissipated about 23.7 mW.



**Figure 13.** Photograph of the test board. The size of the test chip was  $1.8 \times 1.98 \text{ mm}^2$ .



**Figure 14.** Block scheme of the test setup.

**Table 4.** Break-down of power consumption of the frequency divider.

Block	Power Consumption
Input Buffer	26.8 mW
Divider Core	23.7 mW
Limiter with EFs	28.9 mW
Output Buffer	78.6 mW
Biasing	51.9 mW

Input and output return losses of the board were tested using an Anritsu 37397A vector network analyzer (the setup included the baluns) and are reported in Figure 15: good matching up to at least 40 GHz was achieved.

Figure 16 shows the output spectrum for a 50 GHz input signal, and Figure 17 shows the corresponding differential output waveform; the output buffer (and the output balun, when used) filtered out the output harmonics, providing a nearly sinusoidal waveform. Figure 18 shows the differential output waveform for a 20 GHz input signal, highlighting a nearly 50% duty cycle and steep edges.

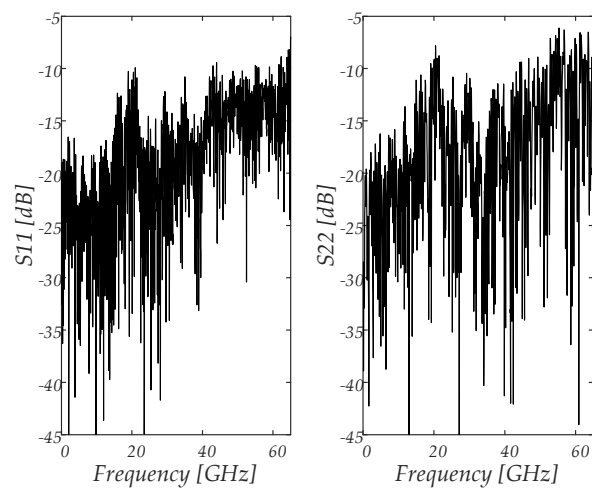


Figure 15. Measured input and output return losses.

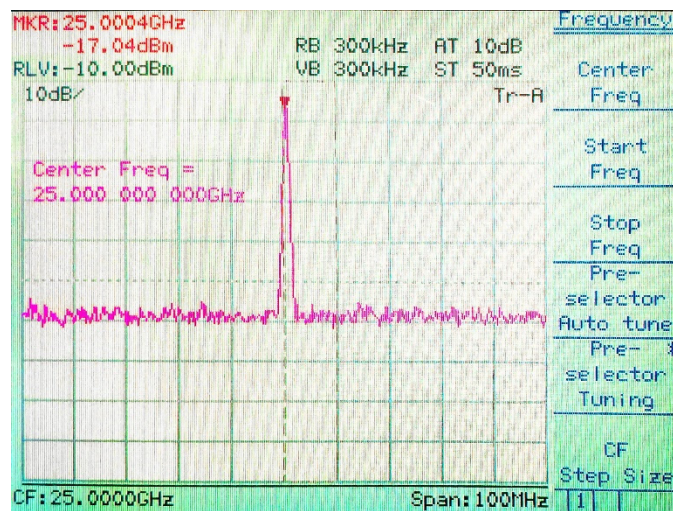


Figure 16. Output spectrum for a 50 GHz input.

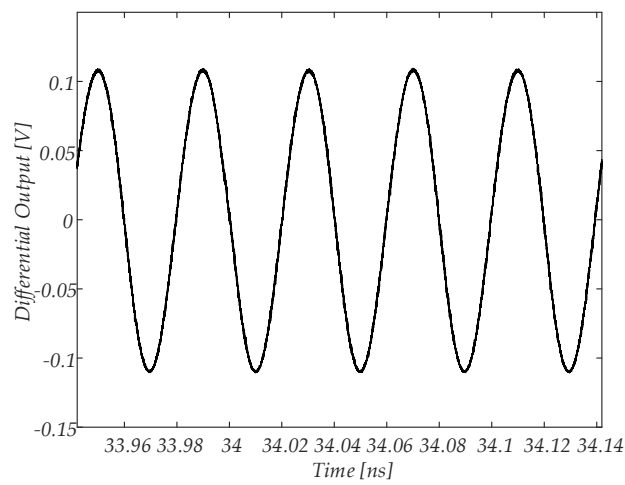
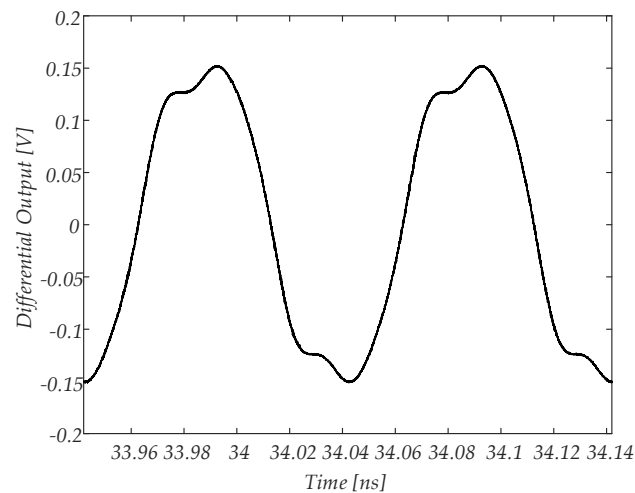
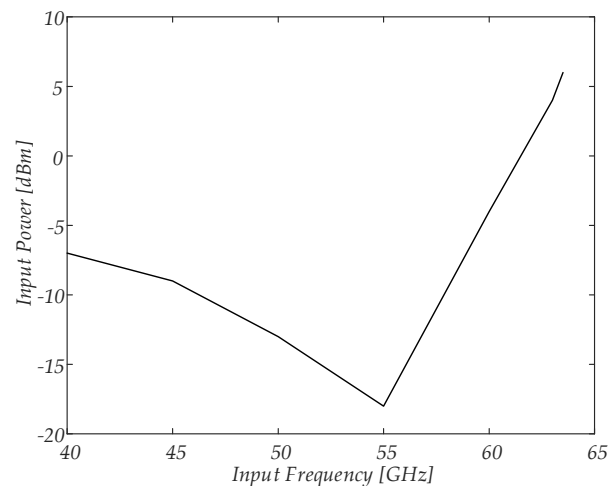


Figure 17. Differential output waveform for a 50 GHz input.



**Figure 18.** Differential output waveform for a 20 GHz input.

The measured sensitivity curve of the divider is reported in Figure 19, and shows a maximum input frequency of 63.5 GHz and a self-oscillating frequency (SOF) of about 55 GHz, in very good agreement with post layout simulations, that provided a value of about 53.2 GHz.



**Figure 19.** Measured sensitivity curve of the frequency divider.

Measured phase noise of  $-73$  dBc/Hz at 1 kHz (for a 40 GHz input) appears to have been limited by the measurement setup.

## 5. Conclusions

The frequency divider presented in this paper was designed for a 40 GS/s application, with the goal of optimizing power and area consumption. A standard CML topology was used, without inductive peaking to avoid a large area consumption, and optimization involved mostly device sizing and biasing, and layout floor planning. Table 5 compares the results with data reported in the literature for very high frequency static frequency dividers. The ratio between the self-oscillating frequency and the power consumption of the divider core  $P_{\text{core}}$  is used as a figure of merit (FOM) to evaluate the efficiency of the dividers:

$$\text{FOM} = \text{SOF}/P_{\text{core}},$$

Table 5 also specifies whether inductive peaking is used to improve frequency behavior at the cost of a larger footprint area.

**Table 5.** Comparison with the literature.

Reference	Technology ( $f_T$ )	Inductor	SOF	$f_{max}$	$P_{core}$	FOM
[20]	SiGe (230)	Y	77	100	122	0.63
[21]	CMOS 65 nm	Y	79.2	90	19.2	4.12
[21]	SiGe (150)	Y	92	104	56	1.64
[22]	SiGe (200)	N	104	113	115	0.90
[23]	InP (530)	Y	173	200	228	0.76
[24]	SiGe (230)	N	56	87	14	4.00
[24]	SiGe (230)	N	96	133	210	0.46
[5]	SiGe (240)	N	70.3	100	141	0.50
[25]	SiGe (300)	No	111.6	128.7	196	0.57
[2]	SiGe (240)	Y	52	60	115	0.45
[26]	SiGe (250)	N	77	80	80	0.96
[27]	CMOS 45 nm	Y	60	60	9.6	6.25
[28]	SiGe (200)	Y	75.1	90	61.6	1.22
This Work	SiGe (320)	N	55	63.5	23.7	2.32
-	(GHz)	-	GHz	GHz	mW	GHz/mW

The comparison shows that the proposed frequency divider provides a high efficiency, as measured by the FOM. Higher values are achieved by [24] and by dividers in CMOS technology that also exploit inductive peaking. This result shows that the proposed divider is a suitable building block to implement highly integrated, high-speed, mixed-signal systems, where minimization of footprint area and power consumption of the different building blocks is an important issue to be considered to achieve the desired level of integration.

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