Research article

Low power switched-resistor band-pass filter for neural recording channels in 130nm CMOS

Francesco Centurelli, Alessandro Fava, Pietro Monsurrò [*], Giuseppe Scotti, Pasquale Tommasino, Alessandro Trifiletti

DIET (Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni), University of Rome "La Sapienza", Italy

ABSTRACT

In this work, we present a low-power 2nd order band-pass filter for neural recording applications. The central frequency of the passband is set to 375Hz and the quality factor to 5 to properly process the neural signals related to the onset of epileptic seizure, and to strongly attenuate all the out of band biological signals and electrical disturbances. The biquad filter is based on a fully differential Tow Thomas architecture in which high-valued resistors are implemented through switched high-resistivity polysilicon resistors. A supply voltage as low as 0.8V and MOS transistors operating in the sub-threshold region are exploited to achieve a power consumption as low as 170nW, when driving a 1pF load capacitance. The filter exhibits a tuning range of the resonance frequency from 200Hz to 400Hz, and an area footprint of only 0.021 mm². Very low power consumption and area occupation are key specifications for integrated, multiple-sensors, neural recording systems.

1. Introduction

In the last fifteen years there has been a strong increase in the research interest for neural recording systems [1] and brain-computer interfaces (BCI) [2]. In both cases, implanted micro-electrode arrays (MEA) and suitable integrated circuits are used to provide connectivity between the brain of a subject and an electronic device. The block scheme of the single channel of a typical neural recording system is shown in Figure 1 [2]. It is composed of a low-noise front-end amplifier, a band-pass filter and an analog-to-digital converter (ADC). In order to record simultaneously the signals coming from a number (100–1000) of neurons, the single processing channel is instantiated multiple times to efficiently detect neural spikes associated with epileptic seizures or Parkinson disease [3, 4, 5, 6, 7]. Digitized samples are multiplexed and sent to a digital processor, that can be integrated on the same chip or external; in the latter case, an RF (radio-frequency) transmitter can be exploited to send the samples to an external processing unit. In closed loop architectures, the processed signals are used to drive on-chip stimulation channels.

The electrode array and the associated integrated circuit (IC) are implanted into the brain of the subject, and this poses stringent requirements on the mechanical and electrical characteristics of the IC: it must be small and dissipate as little power as possible, to minimize heating and to allow powering by energy harvesting. This implies that a low-voltage low-power design approach is necessary for the receiver channel, together with silicon area minimization. Low power consumption avoids damage to the surrounding tissue and makes it easier to power the system with sources of limited power, and increases the maximum number of systems that can be integrated on the same chip, thus maximizing the number of neurons that can be monitored. Area occupation also improves the sensors' density.

Different signals in the band 1Hz-10kHz can be of interest for a BCI, with typical amplitude from tens to hundreds of μV.

This paper focuses on the design of the band-pass filter placed after the the front-end amplifier in the recording channel for the detection of fast ripples (FR) due to epileptic seizures. FR lie in the band 200–500Hz, whereas their amplitude ranges from a few μV to up 1mV. This block is of fundamental importance because it acts as anti-aliasing filter for the subsequent analog-to-digital converter, hence reducing the amount of undesired noise entering system. A 2nd order tunable band-pass filter based on a fully differential Tow Thomas architecture has been chosen as anti-aliasing filter to ensure sufficient attenuation outside the band of
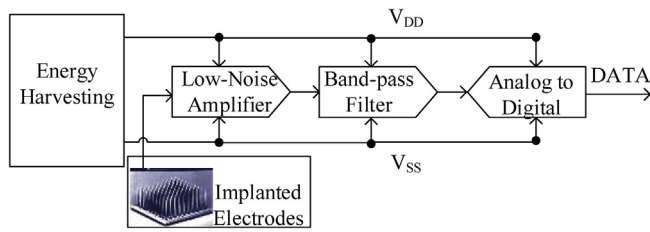
Figure 1. Block scheme of a typical neural recording system.

interest with limited distortions. MOS (Metal Oxide Semiconductor) devices biased in the sub-threshold region are exploited to maximize power efficiency and achieve very low power consumption, and a switched-resistor approach is used to keep the Silicon area low. Because the bandwidth of the filter is inversely proportional to the product of a resistance and a capacitance, implementing very-high resistances with the switched-resistor technique allows reducing the capacitance values, and hence their area occupation.

This paper is organized as follows: Section 2 introduces the architecture of the biquad filter and its switched resistor implementation, Section 3 deals with circuit level design, Section 4 presents the simulation results, and finally, Section 5 presents conclusions and a comparison against the state of the art.

2. Biquad filter topology

2.1. Biquad filter architecture

The architecture of the biquadratic filter is shown in Figure 2.

Referring to the circuit in Figure 2, the transfer function between the output of the band-pass filter V_{BP} and the input signal V_{IN} can be easily derived when assuming ideal fully differential amplifiers:

$$\frac{V_{BP}}{V_{IN}} = \frac{sK\omega_0}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{1}$$

where $R_k = \frac{R}{K}$, $R_Q = R \cdot Q$ and

$$\omega_0 = \frac{1}{RC} \tag{2}$$

The band-pass transfer function has a peak gain of $Q \cdot K$ at ω_0 and both Q (the quality factor) and K are set by the ratio between two resistors, so that they are stable under process, temperature and supply voltage (PVT) variations, except for eventual high-order parasitic effects not accounted for in (1). K is the DC gain of the lowpass output V_{LP}, and the peak gain of V_{LP} tends to $Q \cdot K$ for $Q \gg 1$.
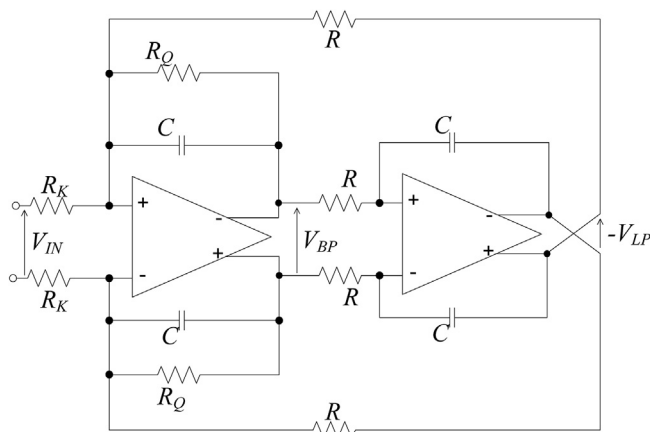

Figure 2. Fully differential Tow Thomas biquad architecture.

Hence, the maximum output swing will occur at V_{BP} at ω_0, and this will set a limit to linearity performance at high input signal swing. Another limitation to linearity is due to the maximum slew-rate and output current of the OTAs (Operational Transconductance Amplifier): the first OTA in Figure 1 drives $G + G_Q + sC + Y_L^{BP}$ (where Y_L^{BP} is the load admittance on the band-pass output), and the second one drives $G + sC + Y_L^{LP}$ (where Y_L^{LP} is the load admittance on the lowpass output). The OTAs will need to be designed with sufficient voltage output swing, peak output current, and slew-rate.

The resonance frequency of the stage is ω_0 in (2), and it varies inversely to the product of a (switched) resistor and a capacitor. Hence, the resonance frequency will change with PVT variations, and these variations will need to be counteracted by an adequate tuning system.

In conclusion, except for mismatches and higher-order parasitic effects, the filter in Figure 2 should have constant gain and quality factor, and varying (but tunable and thus controllable) resonance frequency.

2.2. Switched resistors implementation

Given the extremely low resonance frequencies of the biquadratic filter, very large capacitors and/or very high resistances are required, as demonstrated by Eq. (2): both solutions require extremely large silicon area to be implemented. To minimize area consumption, we propose using small MIM (metal-insulator-metal) capacitors and achieving large resistance values using the switched-resistor (SR) approach [8, 9].

In the SR approach, an equivalent high-value resistance is obtained by the series connection of a physical resistor and a MOS switch, as shown in Figure 3. The latter is driven by a clock signal with a frequency f_{CK} and a duty cycle δ: by changing the duty cycle, the average current flowing into the resistor R is

$$I_{avg} = \delta \frac{V_1 - V_2}{R} \tag{3}$$

where V_1 and V_2 are the voltages at the resistor terminals, thus the equivalent resistance is given by

$$R_{eq} = R/\delta \tag{4}$$

With respect to the switched-capacitor (SC) approach, the SR approach provides higher linearity and less noise, but requires OTAs with larger bandwidth and higher slew rate, to cope with the fast clock transients. The equivalent resistance can be ideally tuned from R to infinite by changing the duty cycle of the clock, but the switch series resistance r_{on} and practical limits to the minimum value of δ have to be considered.

A high resistivity polysilicon (hipo) resistor can be used to implement a large physical resistor in a limited area. Then, adopting the SR approach with a very small duty cycle, a very large equivalent resistance can be obtained. When using this approach, the MOS switch has to be sized as a tradeoff between low area consumption and parasitic capacitance versus a low value of the on resistance r_{on}, of the switch. In fact, since r_{on} is nonlinear, its value has to be negligible with respect to the value of the physical resistor in order to not affect the overall linearity.
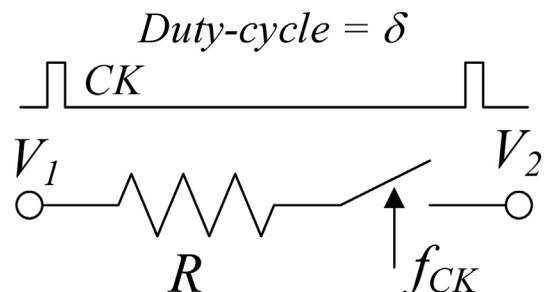

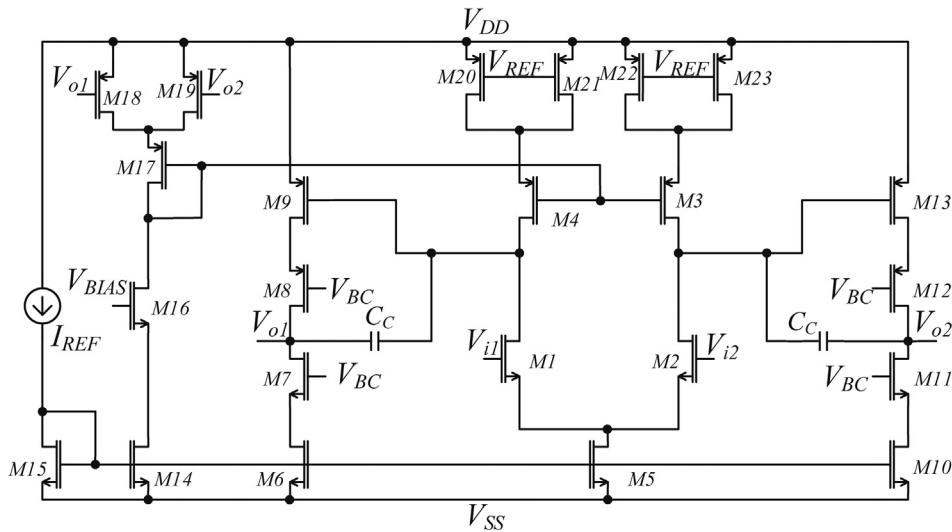**Figure 3.** Switched-resistor principle.

Figure 4. Schematic of the OTAs adopted to implement the biquad filter.

The clock frequency f_{CK} has to be much larger than the maximum signal frequency, to avoid aliasing, as in all switched systems.

3. Circuit design

The 2nd order switched-resistor band-pass filter has been designed referring to a commercial 130nm CMOS (Complementary MOS) technology, to achieve a resonant frequency of 375Hz with a quality factor $Q = 5$ in nominal conditions.

Table 1. Device sizing for circuit in Figure 4

MOS devices	W/L [μm]	Number of Fingers
M1, M2	0.15/0.78	1
M3, M4	6/0.78	8
M5	0.65/0.78	2
M6, M10	2/0.78	6
M7, M11	0.8/0.78	4
M8, M12	3/0.78	8
M9, M13	7/0.78	8
M14	0.9/0.78	1
M15	0.57/0.78	2
M16	0.3/0.78	2
M17	6.1/0.78	8
M18, M19, M20, M21, M22, M23	0.15/0.9	1

Figure 5. Implementation of SR by using two Transmission Gates (TG) switches.

With reference to Figure 2, MIM capacitors C of 5 pF have been used: the required resistances are thus, assuming $K = 1$, $R = R_K = 84.88 M\Omega$ and $R_Q = Q \cdot R = 424.4 M\Omega$.

To minimize the silicon area, these huge resistances have been implemented by the SR approach, starting from 200kΩ hipo resistors and using a 100kHz clock signal. We get from (4) that the required duty cycle is $\delta_1 = 0.236\%$ for resistor R and $\delta_{1Q} = 0.047\%$ for resistor R_Q. With these settings the clock pulses driving the switch last 23.56 ns and 4.71 ns respectively. From (2)(2) and (4)(4) we get that the resonance frequency depends on the values of the capacitor, the value of the hipo resistor and the duty cycle of the clock: this approach is thus sensitive to process variations that affect the physical components, but can be calibrated by an automatic tuning system that sets the correct value of the duty cycle.

A fine control on the duty cycle is required and can be achieved by a digital servo loop or an automatic digital tuning loop [10, 11, 12]. Such control schemes allow also keeping the quality factor of the biquad under control.

The OTAs utilized in the biquad architecture of Figure 2 have been designed to provide a high gain of at least 100dB and a unity-gain frequency in excess of 159kHz, to be able to process the current spikes due to the fast clock pulses applied to the switches. These specifications have led to the use of the fully-differential 2-stage OTA topology with cascode output stages shown in Figure 4, that is able to provide a dc gain of the order of A_0^3, where A_0 is the intrinsic gain of the MOS devices.

A triode-based common-mode feedback (CMFB) solution has been adopted to avoid additional current branches.

Table 1 reports device sizing for the OTAs: a 10nA tail current is used for the input differential pair and 40nA for each one of the output branches, with all the transistors biased in sub-threshold region. The Miller compensation capacitors have been set to 150fF.

To improve the performance of switched resistors, the switch shown in Figure 3 has been implemented by means of a transmission gate (TG_1). Furthermore, in all the switched resistors driving an input of the OTAs (e. g. R and R_K) an additional transmission gate switch (TG_2) providing a path to ground and driven by a clock signal with the same frequency, but different duty cycle with respect to TG_1 has been added as shown in

Table 2. Nominal values for the SR duty cycles.

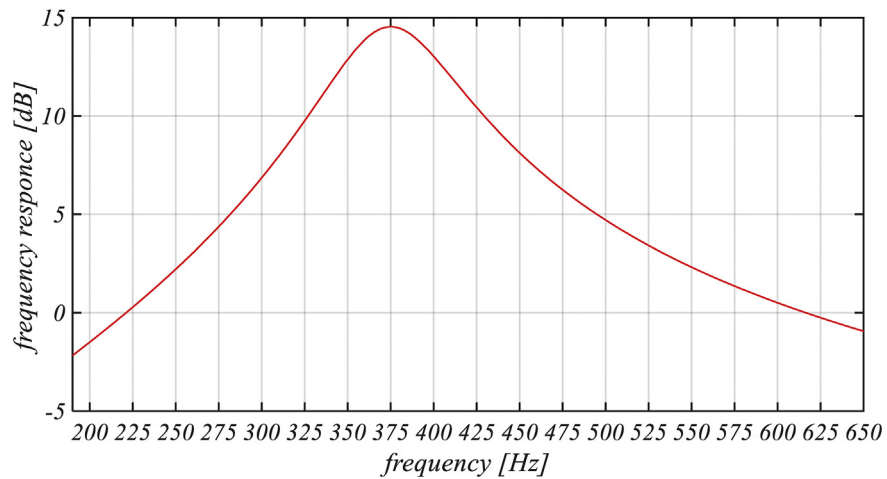| Duty Cycles	δ_1	δ_{1Q}	δ_2
	3.251%	0.575%	1.570%

Figure 6. Frequency response of the filter for the nominal duty cycle setting.

Figure 5. In fact, as mentioned above, the SR driving the OTAs inputs require a good virtual ground to accurately process the current spikes due to the fast clock pulses applied to the switches. The additional path to ground provided by TG_2 driven with a different duty cycle allowed to strongly relax the bandwidth requirement for the OTAs and therefore to strongly reduce the power consumption of whole filter.

The nominal duty cycles adopted in this work to achieve a resonant frequency of 375Hz with a quality factor $Q = 5$ are reported in Table 2.
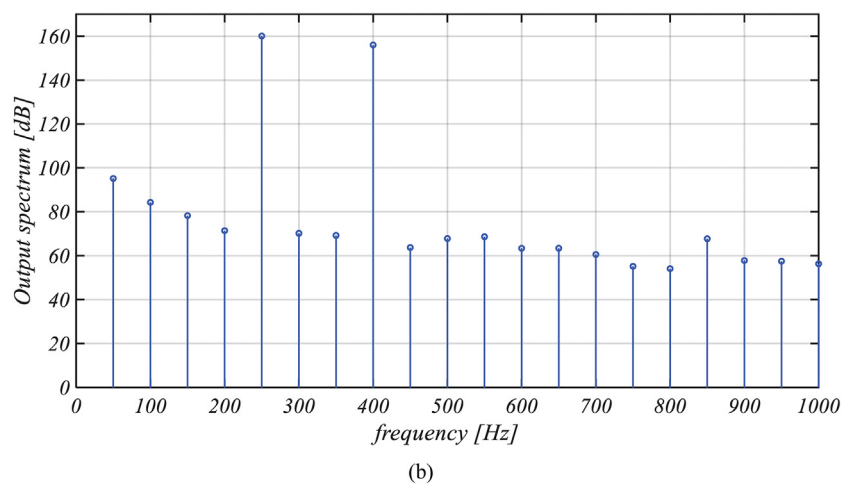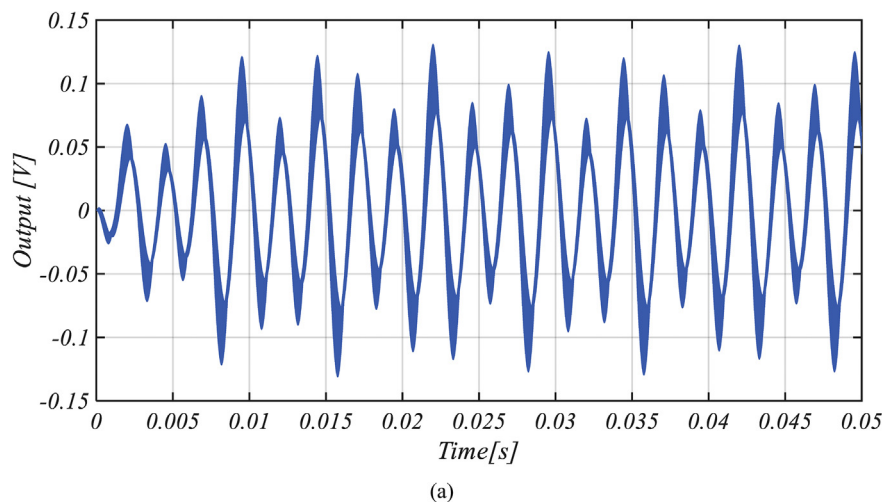

(a)

(b)

Figure 7. Two-tone response of the filter in time (a) and frequency (b).
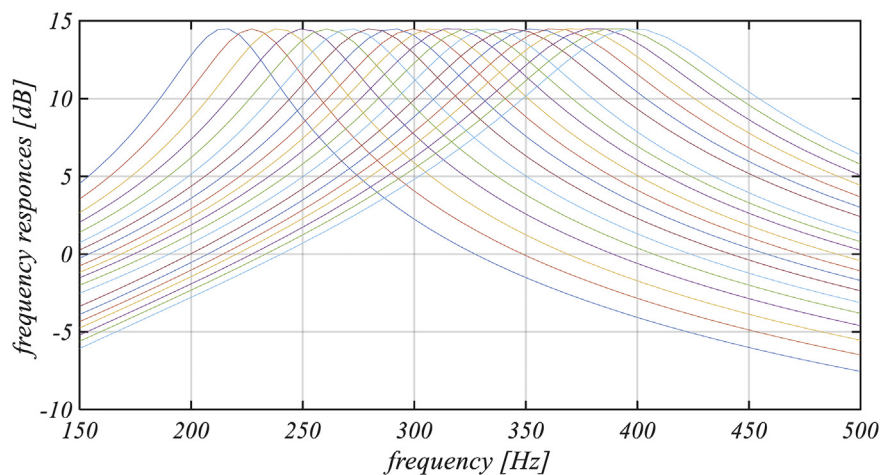
Figure 8. Frequency response for different duty cycle settings to show the tuning capability of the filter.

Table 3. Comparison with state of the art front-ends for neural recording applications.

	This work	[6]	[14]	[15]	[16]
CMOS node (nm)	130	600	180	180	500
Order of the Filter	2	6	2	2	2
Supply Voltage (V)	0.8	2.8	1	3.3	1.8
Power (µW)	1.17	4.5	3.5	51.4	9.8
Gain (dB)	54	28.5	53	60	45
Bandwidth (Hz)	75	250–486	100	3–400	75
Gain Ripple (dB)	-	0.5	-	-	-
Die area (mm^2)	0.075	0.45	0.3	0.14	0.03
FOM (µW/pole)	0.58	0.75	1.75	20.7	4.9

4. Simulation results

Simulation results of the AC frequency response of the filter are reported in Figure 6 showing a 375Hz resonance frequency and a quality factor Q of about 5. The biquad filter exhibits a total power consumption of only 170nW from a supply voltage of 0.8V, providing a figure of merit (FOM) of 80nW/pole.

Figure 7 shows the time domain response to an input two-tone wave with the tones at 350Hz and 400Hz (a), and its spectrum (b), highlighting a SFDR (Spurious Free Dynamic Range) in excess of 60dB.

Figure 8 reports the frequency response of the filter when the duty cycle of switched resistors is properly adjusted showing a tuning range of the resonance frequency of the biquad filter from about 200Hz to about 400Hz. This tuning capability can be used to compensate the effects of process, temperature and supply voltage variations.

5. Conclusions and comparisons

In this paper, we show the results for a second-order biquadratic filter based on a switched-resistor technique. The filter requires low area occupation and low power consumption because of its use in neural recording systems: hundreds of receivers, including the filter, can be integrated on the same chip to monitor individual neurons, and need to generate as little heat as possible not to damage the biological tissues. The SR technique allows achieving a low power consumption of 170nW for a band-pass filter with a bandwidth of 75Hz around 375Hz (Q = 5). The filter's frequency response is tunable by changing the duty cycle of the clock controlling the SR devices. The filter's area occupation is low, owing to the large value of the SR resistors, allowing the use of smaller capacitors.

In order to compare the proposed biquadratic filter with other state of the art front-ends for neural recording applications, we have estimated the performance of a front-end made up of the filter presented in this paper and the front-end that we proposed in [13], which has been redesigned in the same 130nm CMOS technology adopted for the filter. The redesigned front-end exhibits a power consumption of about 1µW with performances in good agreement with the original design. The input capacitors of the front-end have been reduced from 10pF to 0.5pF, resulting in a low cutoff frequency increase and in an area reduction. Table 3 shows a comparison with the literature highlighting how the proposed circuits outperform previous designs in terms of supply voltage, power consumption and FOM. Our system requires the lowest supply voltage (0.8V) among those we found in the literature, and has the lower power consumption and power consumption per number of poles (FOM). It has also the lowest area occupation. All in all, the SR technique appears to be promising for designing integrated circuits for neural recording applications.

Declarations

Author contribution statement

Francesco Centurelli & Giuseppe Scotti: Conceived and designed the experiments; Analyzed and interpreted the data; Wrote the paper.

Alessandro Fava: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Wrote the paper.

Pietro Monsurrò, Pasquale Tommasino & Alessandro Trifiletti: Analyzed and interpreted the data; Wrote the paper.

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Competing interest statement

The authors declare no conflict of interest.

Additional information

No additional information is available for this paper.

References

[1] R.R. Harrison, The design of integrated circuits to observe brain activity, Proc. IEEE 96 (7) (July 2008) 1203–1216.

[2] M.A. Lebedev, M.A.L. Nicolelis, Brain–machine interfaces: past, present and future", Trends Neurosci. 29 (9) (2006) 536–546.

[3] B. Gosselin, Recent advances in neural recording microsystems, Sensors 11 (5) (2011) 4572–4597.

[4] C. Qian, J. Parramon, E. Sanchez-Sinencio, A micropower low-noise neural recording front-end circuit for epileptic seizure detection, IEEE J. Solid State Circ. 46 (6) (June 2011) 1392–1405.

[5] V. Chaturvedi, B. Amrutur, An area-efficient noise-adaptive neural amplifier in 130 nm CMOS technology, IEEE J. Emerg. Selected Topics Circuits Sys. 1 (4) (Dec. 2011) 536–545.

[6] F. Shahrokhi, K. Abdelhalim, D. Serletis, P.L. Carlen, R. Genov, The 128-channel fully differential digital integrated neural recording and stimulation interface, IEEE Transactions Biomed. Circuits Sys. 4 (3) (June 2010) 149–161.

[7] X. Zou, et al., A 100-channel 1-mW implantable neural recording IC, IEEE Transactions on Circuits and Systems I: Regular Papers 60 (10) (Oct. 2013) 2584–2596.

[8] A. Jiraseree-amornkun, A. Worapishet, E.A.M. Klumperink, B. Nauta, W. Surakampontorn, Theoretical analysis of highly linear tunable filters using switched-resistor techniques, in: IEEE Transactions on Circuits and Systems I: Regular Papers, 55, Dec. 2008, pp. 3641–3654, 11.

[9] H. Chandrakumar, D. Marković, A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation, IEEE J. Solid State Circ. 52 (3) (March 2017) 645–656.

[10] T. Laxminidhi, V. Prasadu, S. Pavan, Widely programmable high-frequency active RC filters in CMOS technology, in: IEEE Transactions on Circuits and Systems I: Regular Papers, 56, Feb. 2009, pp. 327–336, 2.

[11] T. Oshima, K. Maio, W. Hioe, Y. Shibahara, Novel automatic tuning method of RC filters using a digital-DLL technique, IEEE J. Solid State Circ. 39 (11) (Nov. 2004) 2052–2054.

[12] T. Sumesaglam, A.I. Karsilayan, A digital approach for automatic tuning of continuous-time high-Q filters, in: IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 50, Oct. 2003, pp. 755–761, 10.

[13] M. Avoli, F. Centurelli, P. Monsurrò, G. Scotti, A. Trifiletti "Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS, Int. J. Electron. Commun. 92 (2018) 30–35.

[14] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, A.P. Chandrakasan, A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system, IEEE J. Solid State Circ. 45 (4) (April 2010) 804–816.

[15] U. Bihr, M. Ortmanns, A front-end circuit with active spike and LFP separation via a switched capacitor filter structure for neural recording applications, in: 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, 2012, pp. 2231–2234.

[16] S.U. Rehman, A.M. Kamboh, Y. Yang, A 79μW 0.24mm2 8-channel neural signal recording front-end integrated circuit, in: 2017 International Conference on Applied Electronics (AE), Pilsen, 2017, pp. 1–4.