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10-GHz Fully Differential Sallen–Key Lowpass Biquad Filters in 55nm SiGe BiCMOS Technology

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Abstract: Multi-GHz lowpass filters are key components for many RF applications and are required for the implementation of integrated high-speed analog-to-digital and digital-to-analog converters and optical communication systems. In the last two decades, integrated filters in the Multi-GHz range have been implemented using III-V or SiGe technologies. In all cases in which the size of passive components is a concern, inductorless designs are preferred. Furthermore, due to the recent development of high-speed and high-resolution data converters, highly linear multi-GHz filters are required more and more. Classical open loop topologies are not able to achieve high linearity, and closed loop filters are preferred in all applications where linearity is a key requirement. In this work, we present a fully differential BiCMOS implementation of the classical Sallen Key filter, which is able to operate up to about 10 GHz by exploiting both the bipolar and MOS transistors of a commercial 55-nm BiCMOS technology. The layout of the biquad filter has been implemented, and the results of post-layout simulations are reported. The biquad stage exhibits excellent SFDR (64 dB) and dynamic range (about 50 dB) due to the closed loop operation, and good power efficiency (0.94 pW/Hz/pole) with respect to comparable active inductorless lowpass filters reported in the literature. Moreover, unlike other filters, it exploits the different active devices offered by commercial SiGe BiCMOS technologies. Parametric and Monte Carlo simulations are also included to assess the robustness of the proposed biquad filter against PVT and mismatch variations.

Keywords: active filters; anti-aliasing filters; HBT; inductorless; low-pass filters; SiGe

1. Introduction

Integrated multi-GHz-band lowpass filters are required as antialiasing filters for very high-speed analog-to-digital (ADC) and digital-to-analog (DAC) converters [1] in applications such as wideband spectrum monitoring, high bit-rate optical communications [2,3] and wideband measurement systems [4,5]. They have to be designed in silicon technology to be integrated on the same chip with the converter blocks, thus minimizing off-chip interfaces, and should possibly avoid the use of spiral inductors, to minimize chip area. The main performance requirements are related to off-band suppression, that forces the use of high order filters, and linearity, that should be better than that of the ADC/DAC, not to limit the overall system performance. A fully differential approach is typically required, to desensitize from common-mode disturbances, reduce even-order harmonics and improve the signal-to-noise ratio (SNR).

Inductorless GHz-band lowpass filters in the literature are often based on RLC reference structures, with the use of active inductance circuits to substitute the physical inductors. However, implementations based on the Gm-C [6] approach are quite common, and filters based on the closed loop Sallen–Key [7]

and Tow–Thomas [8] topologies have also been reported in the low-GHz range. Closed loop filter architectures based on non-conventional active building blocks—such as second-generation current conveyors [9] or second-generation voltage conveyors [10]—have been also exploited at lower frequencies. However, very few lowpass filter implementations above 4 GHz are reported in the literature, and none of them are based on closed-loop architectures. In [11], a tunable 5th order elliptic Gm-C lowpass filter in 170 GHz-f_T SiGe BiCMOS with a maximum bandwidth of 4.1 GHz was reported, and in [12] a 3rd order Gm-C filter with a maximum bandwidth of 10 GHz, in 65-nm CMOS was reported. Filters based on the active inductance approach have been presented in [13], that reports a 5th order 4.57-GHz lowpass filter in 180-nm CMOS, and [14] that describes a 10.5-GHz biquad in SiGe HBT technology.

On the other hand, the ever-increasing frequency performance of advanced bipolar technologies and deep submicron CMOS allows achieving huge gain-bandwidth products, thus making it possible to adopt a closed-loop approach for the design of multi-GHz filters. This allows using filter design techniques that are typically adopted at lower frequencies, both for the topology of the basic filter stage, the biquad, and for the system design of higher order filters under technology constraints (e.g., limits on the maximum quality factor that can be achieved) [15,16]. The closed-loop approach offers the advantages of increased linearity and low sensitivity to active devices variations, thanks to feedback; the filter characteristics are related to the values of passive components and/or to their ratios, and could be easily tuned, e.g., by using varactors.

In this paper, we demonstrate a 10 GHz, fully differential, biquadratic filter exploiting Sallen–Key architecture and based on a differential difference amplifier (DDA). The proposed DDA design makes use of both the bipolar and MOS transistors available in the adopted commercial 55-nm SiGe BiCMOS technology. It must be noted that this is the first work in which a closed-loop approach is used to design filters at such high frequencies, resulting in an improved linearity with a power consumption comparable to alternative approaches.

In the following sections, Section 2 describes the proposed biquad architecture and design equations, Section 3 presents the detailed design of the DDA amplifier, Section 4 deals with filter design referring to the adopted 55-nm BiCMOS process, Section 5 summarizes the results of the simulations, and, finally, Section 6 concludes this work.

2. Proposed Biquad Architecture

Figure 1 shows the proposed fully differential topology of the Sallen–Key (*SK*) lowpass biquad stage based on a differential difference amplifier (DDA). The DDA can be considered a fully differential amplifier with two differential input pairs. *SK* filters have two feedback loops: negative feedback is used to determine the low-frequency gain, and positive feedback allows us to determine the frequency response, thanks to the feedback network formed by capacitors C_1 and C_2 and the two resistors R_1 and R_2.

The transfer function of the circuit in Figure 1, assuming an ideal DDA, can be easily computed as:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G}{C_1C_2R_1R_2}}{s^2 + \left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-G}{R_2C_2}\right)s + \frac{1}{C_1C_2R_1R_2}} \tag{1a}$$

$$G = 1 + \frac{R_B}{R_A} \tag{1b}$$

Hence, the quality factor and resonance frequency of the lowpass filter are:

$$\begin{cases} f_0 = \frac{1}{2\pi\sqrt{C_1C_2R_1R_2}} \\ Q = \frac{\sqrt{C_1C_2R_1R_2}}{R_2C_2 + R_1C_2 + R_1C_1(1-G)} \end{cases} \tag{2}$$

From (2), it can be seen that the value of pole Q is dependent on the value of the gain G and typically the amplifier in the *SK* stage is configured to have a DC gain G larger than 1 to relax the ratio of passive components when high Q is needed. If unity gain of the filter is a requirement, then resistance R_1 can be split into two resistances forming a voltage divider (with gain $1/G$ <1), thus reducing the gain from $G > 1$ to $G = 1$. However, the drawback of such a design choice is that the larger closed-loop gain limits the bandwidth of the amplifier. Therefore, the main reason to choose $G = 1$ is to maximize the closed-loop bandwidth of the DDA, which is necessary to obtain an accurate frequency response for the *SK* filter up to very high frequencies. Even if unity-gain feedback limits the maximum quality factor that can be achieved for a given ratio of passive components, a low-Q filter synthesis approach [15,16] can be used to synthesize high order filters with limited values for the Q of the biquad stages (typically in the range of 2 to 3). This results in an accurate frequency response and has the additional advantage of reducing the sensitivity and allowing a more robust design under PVT and mismatch variations.

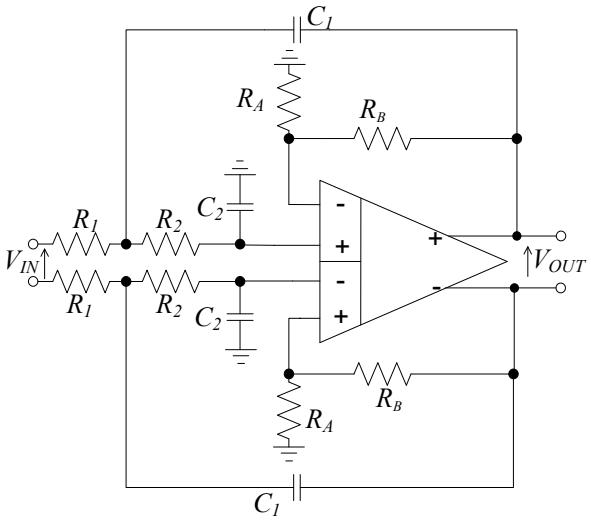

Figure 1. Architecture of the proposed lowpass biquadratic filter.

The filter architecture for $G = 1$ is reported in Figure 2, where the DDA amplifier has been configured as a fully differential closed loop voltage follower.

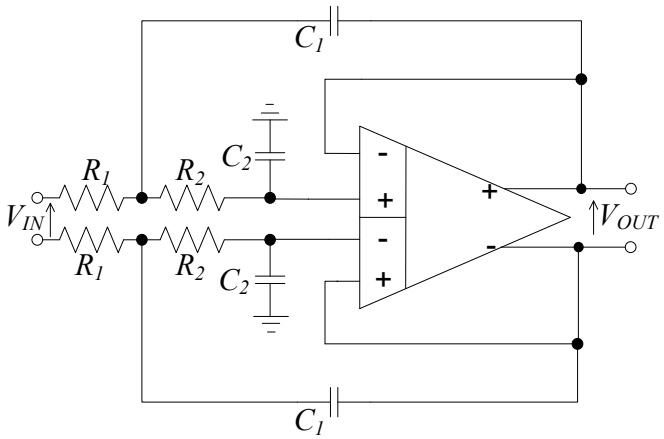

Figure 2. Architecture of the proposed lowpass filter with DDA configured as voltage follower.

The ideal frequency response of the SK stage in Figure 2 is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{C_1 C_2 R_1 R_2}}{s^2 + \left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1}\right)s + \frac{1}{C_1 C_2 R_1 R_2}} \tag{3}$$

The resonance frequency and quality factor of the biquad stage can be expressed as:

$$\begin{cases} f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \\ Q = \sqrt{\frac{C_1}{C_2}}\frac{\sqrt{R_1 R_2}}{R_1 + R_2} \end{cases} \tag{4}$$

The maximum Q value is achieved for $R_2 = R_1 = R$, hence this choice is optimal for achieving maximum $Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}}$.

It is important to point out that the closed loop architecture of the SK filter results in a resonance frequency and a quality factor which are ideally independent on the parameters of the active devices and depend only on the value of the passive components.

The quality factor is, under ideal conditions, stable under process and temperature variations, because it is given by the ratio between two capacitors. The resonance frequency, instead, varies with process and temperature conditions, as it is inversely proportional to variations in resistor and capacitor values. In particular, it can be easily shown that the sensitivity of the cut-off frequency of the *SK* biquad to each one of the parameters R_1, R_2, C_1 and C_2 is equal to −1/2, and therefore the variations of the value of integrated passive components results in a corresponding variation of the resonance frequency. However, it has to be noted that the resonance frequency can be easily tuned implementing capacitances C_1 and C_2 with varactor-diodes or tunable MOS capacitors, and the tuning voltage of variable capacitors can be used in a servo-loop or in an automating tuning loop to accurately set the value of the cut-off frequency.

$$\begin{cases} f_0 = \frac{1}{2\pi R\sqrt{C_1 C_2}} \\ Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}} \end{cases} \tag{5}$$

3. Proposed Topology for the DDA amplifier

In a single-ended implementation, the use of an opamp in non-inverting configuration allows applying both negative feedback to set the DC gain, and positive feedback to determine the frequency response. Mapping this approach to a fully differential implementation requires the use of a DDA, to make both the inverting and non-inverting differential input terminals available, whereas a standard fully differential opamp only allows the inverting configuration to be used.

Figure 3 shows the topology of the DDA used in the proposed SK biquad stage, where the different devices available in the technology have been exploited to maximize the performance: a single-stage DDA amplifier topology with output buffers (implemented as common collector stages) has been adopted to maximize the bandwidth, so to avoid the use of compensation capacitors; a common-mode feedback (CMFB) is also required, to set the output DC voltage and maximize the common-mode rejection ratio (CMRR).

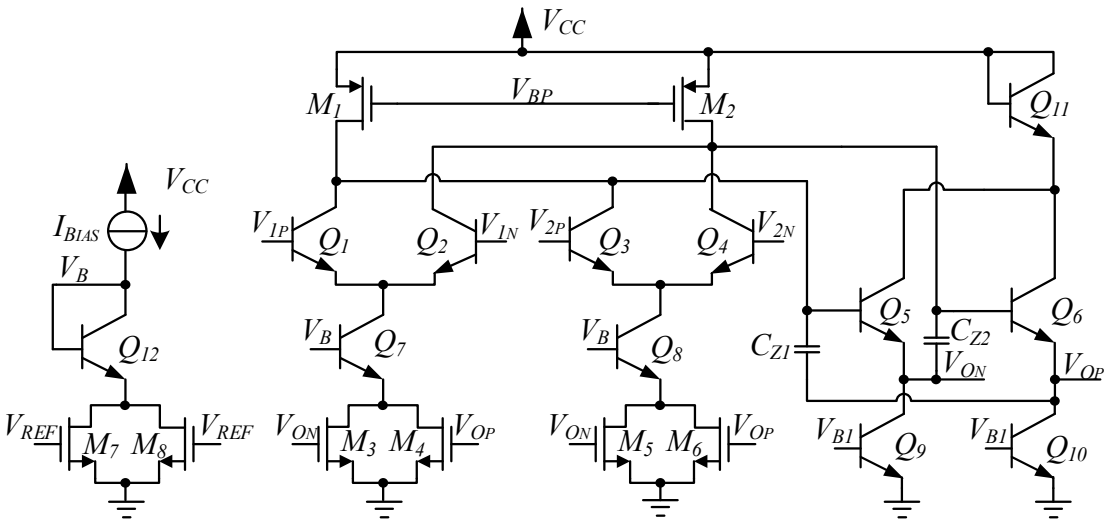

Figure 3. Proposed topology for the DDA amplifier with fully differential output.

3.1. DDA Amplifier

Referring to Figure 3, the single-stage DDA amplifier with active loads which has been used to implement the proposed biquad filter can be described as follows: high-speed npn HBT devices have been adopted for the input differential pairs (Q_1-Q_4), in order to exploit their high transconductance for a given current and outstanding frequency performance. RF PMOS transistors have been exploited as active loads to boost the DC gain without a significant frequency penalty. In the preliminary design phase, both resistive and active PMOS loads have been considered: however, when adopting a resistive load, the maximum allowed load resistance value is limited by the maximum allowable voltage drop across the resistors, and for the target supply voltage $V_{CC} = 3\ V$ the gain would have been too low to guarantee enough loop gain with a single amplifier stage. Furthermore, the good frequency performance of 55-nm PMOS devices results in a limited bandwidth penalty of the active load with respect to the resistive case, guaranteeing a very large gain-bandwidth product for the DDA. The output DC voltage and swing of the stage allows keeping the source-drain voltage of transistors M_1 and M_2, whose biasing voltage V_{BP} is generated by a conventional current mirror (not shown in Figure 3), below the safe limits imposed by the technology. This, however, requires a level shift to have an output DC voltage of the opamp compatible with the input DC common-mode range of the DDA.

The output stage is needed both as level shifter and to provide a very low output resistance: this is a critical issue in the design of *SK* filter stages, since the finite output resistance of the main active element of the filter reduces the maximum available quality factor. From this point of view, the implementation of the main active element of the *SK* filter as a closed loop voltage follower is advantageous, since it allows reducing the already low output resistance of the common collector stages.

In fact, remembering that the maximum Q is achieved for $R_2 = R_1 = R$ as discussed in Section 2, considering an output resistance of the closed loop DDA amplifier $R_o = \epsilon R$, and assuming a capacitance ratio $\alpha \equiv C_2/C_1$, the maximum achievable quality factor for the Sallen–Key stage can be rewritten as:

$$Q \leq Q^{MAX} = \frac{\sqrt{1+\epsilon}}{\sqrt{8\epsilon}} \approx \frac{1}{\sqrt{8\epsilon}} \tag{6}$$

Hence, even the value $Q = 2$ is difficult to obtain, because it would require $R_o < R/32$.

In order to reduce R_o, high-speed HBT devices Q_5 and Q_6 have been used as common collector output buffers due to the large transconductance of bipolar devices. Q_5 and Q_6 are biased by current sources implemented with high-voltage HBT devices (Q_9 and Q_{10}) – the reference branch of the conventional current mirror that sets the bias voltage V_{B1} is not shown in Figure 3. To keep the collector-emitter voltage of the high-speed HBTs below the safe limits, a common-mode level shifter,

implemented through the diode-connected transistor Q_{11}, has been exploited to reduce the collector voltage of Q_5 and Q_6. The use of a common-collector output stage is fundamental both to set the correct DC levels and to reduce the output resistance; however, the base-emitter C_π capacitance introduces a zero in the transfer function that impacts on the out-of-band behavior of the lowpass filter. To compensate this effect, cross-coupled capacitors C_{Z1} and C_{Z2} have been added, exploiting the fully differential nature of the stage to cancel out the effect of the C_π by means of positive feedback.

Neglecting r_0, C_μ, r_π in the device model and assuming a capacitive load C_L, the transfer function of the emitter follower with the cross-coupled capacitances is:

$$\frac{v_o}{v_i} = \frac{1 + s\frac{C_\pi - C_{Z1,2}}{g_m}}{1 + s\frac{C_L + C_\pi + C_{Z1,2}}{g_m}} \tag{7}$$

Hence, for $C_\pi = C_{Z1,2}$, the zero disappears, and the common collector stage only adds a pole to the transfer function, that in the limit of a large load capacitance ($C_L >> C_\pi$) results practically unaffected by the compensation capacitor.

3.2. Common Mode Feedback Loop

A fully differential amplifier requires a common-mode feedback (CMFB) loop to set the output DC voltage and improve the common-mode rejection ratio (CMRR). In this case, a standard triode-based CMFB has been adopted: triode degeneration has been added to the current mirror that sets the current of the DDA, formed by Q_7, Q_8 and Q_{12}. The triode devices on the reference branch (M_7 and M_8) are controlled by the reference voltage (in this case, $V_{REF} = V_{CC}/2$), and the devices under the differential pairs (M_3-M_6) are controlled by the output voltages. These devices act as voltage-controlled resistors, thus adjusting the tail current of the differential pairs to match the current of the PMOS loads while setting the required output common mode voltage. Thick oxide MOS devices have been used to withstand the full swing of the output DC voltage, and their size has been optimized as a trade-off between output loading and functionality of the CMFB under PVT variations.

4. Filter Design

Unity-gain feedback and finite output conductance in the DDA, besides other non-ideal effects, limit the maximum achievable quality factor of the *SK* biquad stages. This is an important issue to cope with when adopting conventional filter synthesis techniques, because the maximum quality factor increases with the order of the filter, even in relatively low-Q designs such as Butterworth filters. Hence, non-conventional design approaches are required. In these approaches, a maximum Q value is chosen, and a filter mask is synthetized subject to this constraint. Unlike in conventional approaches, a larger number of biquad stages may be required for the same stopband attenuation. When adopting these methodologies, the maximum Q allowed for the biquad stages is typically in the range from 2 to 3 [15,16]: these values of Q are compatible with the biquad design proposed in this work.

The reduced Q value also reduces sensitivity to process and mismatch variations and to parasitic effects, as they increase for large quality factors: with lower quality factors, the frequency response is less dependent on variations in Q and f_0, resulting in a more robust design with respect to process, temperature, and mismatch variations.

The proposed filter has been designed in the SiGe BiCMOS055 technology from STMicroelectronics [17], which provides high speed, heterojunction bipolar npn transistors with values of f_T in excess of 300 GHz and an f_{MAX} in excess of 350 GHz, and RF NMOS and PMOS devices with values of f_T of about 190 GHz and 95 GHz, respectively. High voltage bipolar and MOS transistors with reduced frequency performance are also available to implement current sources and biasing circuits.

The biquadratic filter has been designed for a resonance frequency $f_0 = 6.4$ GHz and a quality factor $Q = 2$, as the basic building block of a low-Q higher order filter for anti-aliasing applications in

high-speed digitizers [4,5]. A resonant frequency of 6.4 GHz is ideally equivalent to a 3-dB bandwidth (f_{3dB}) of 10 *GHz* for $Q = 2$.

Table 1 shows the device sizing and bias current of all the bipolar and MOS transistors of the circuit in Figure 3, whereas the values of filter components (referring to Figure 2) have been set as follows: $R_1 = R_2 = 100\ \Omega$, $C_1 = 380$ fF, $C_2 = 40$ fF, $C_{Z1} = C_{Z2} = 50$ fF. R_1 and R_2 have been implemented as poly-silicon resistors, and capacitances have been implemented as MIM (metal-insulator-metal) capacitors available in the RF library of the adopted technology.

Table 1. Device sizing.

Device	Size	Bias Current
Q_1, Q_2, Q_3, Q_4	L_e/W_e[1] = 1/0.2 µm	IC = 1 mA
Q_5, Q_6	L_e/W_e = 4/0.2 µm	IC = 1 mA
Q_7, Q_8,Q_{12}	L_e/W_e = 5/0.2 µm	IC = 1 mA
Q_9, Q_{10}	L_e/W_e = 5/0.2 µm	IC = 1 mA
Q_{11}	$L_e/W_e = 2 \times 4/0.2$ µm	IC = 1 mA
M_1, M_2	W/L = 6/0.06 µm	ID = 1 mA
M_3,M_4,M_5,M_6	W/L = 20/0.25 µm	ID = 1 mA

[1] L_e/W_e = Emitter Length/Emitter Width

The layout of the filter is reported in Figure 4: the filter occupies an area of only 65×42 µm^2.

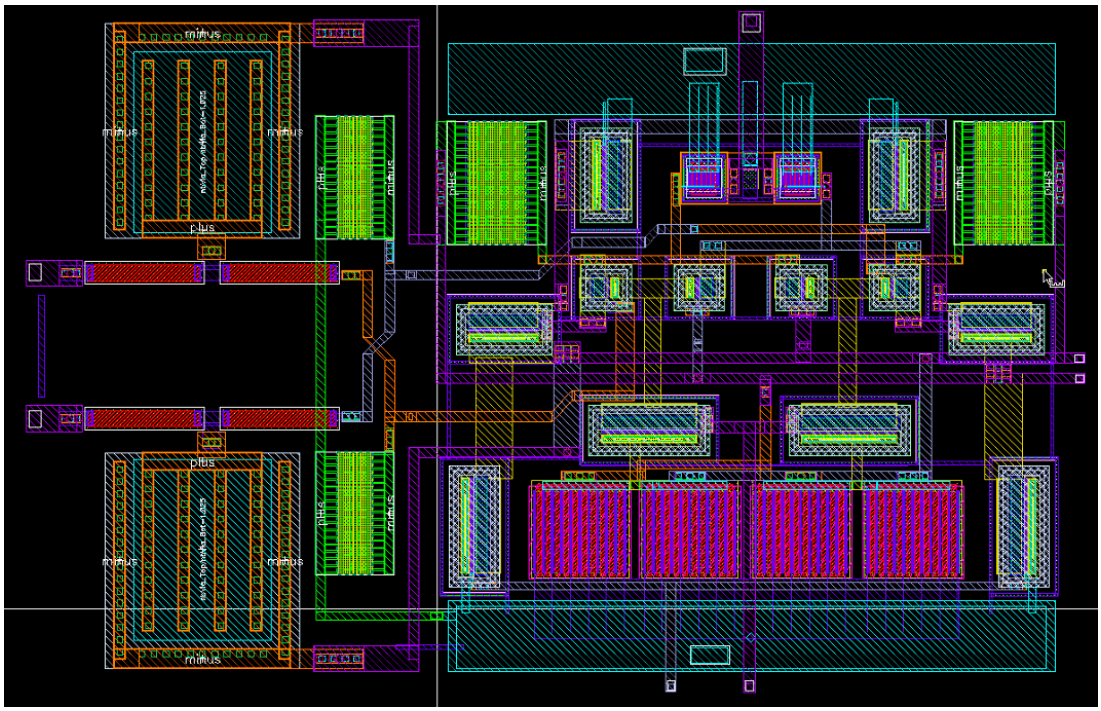

Figure 4. Layout of the proposed Biquad Filter.

5. Simulation Results

Table 2 shows simulation results for the typical process corner and temperature (T = 27 °C). The three FOMs reported in Table 2 are defined as follows:

$$FOM_1 = \frac{P_{diss}}{N_{pole}} \tag{8a}$$

$$FOM_2 = \frac{P_{diss}}{N_{pole} f_{3dB}} \tag{8b}$$

$$FOM_3 = \frac{P_{diss}}{N_{pole} f_{3dB} D_R} \tag{8c}$$

where N_{pole}, and D_R denote the number of poles (e.g., the order) and the dynamic range (computed as in [14]) of the filter respectively.

Table 2. Typical 27 °C simulations.

Name	Value	Unit	Notes
P_{diss}	18	mW	Power Dissipation
V_{cc}	3	V	Supply Voltage
f_0	6.45	GHz	Resonant Frequency
f_{3dB}	9.55	GHz	3 dB Bandwidth
A_{DC}	−0.5	dB	DC-Gain
A_{PK}	5.8	dB	Peak Gain
Q	2.06	-	Quality Factor
SFDR	64	dB	@0.8Vpp differential,1 GHz
v_{onoise}	1.36	mVrms	Output Noise integrated between 1 Hz and 10 GHz
SNR	46.4	[dB]	@0.8Vpp differential
D_R [1]	49.3	dB	Dynamic Range
FOM1	9	mW	
FOM2	0.94	pW/Hz	
FOM3	0.0032	mW/GHz	

[1] D_R has been computed as in [14].

Figure 5 shows the frequency response of the filter. The Discrete Fourier Transform (DFT) of the differential output voltage with an input tone at 1 GHz, 0.8Vpp differential is reported in Figure 6.

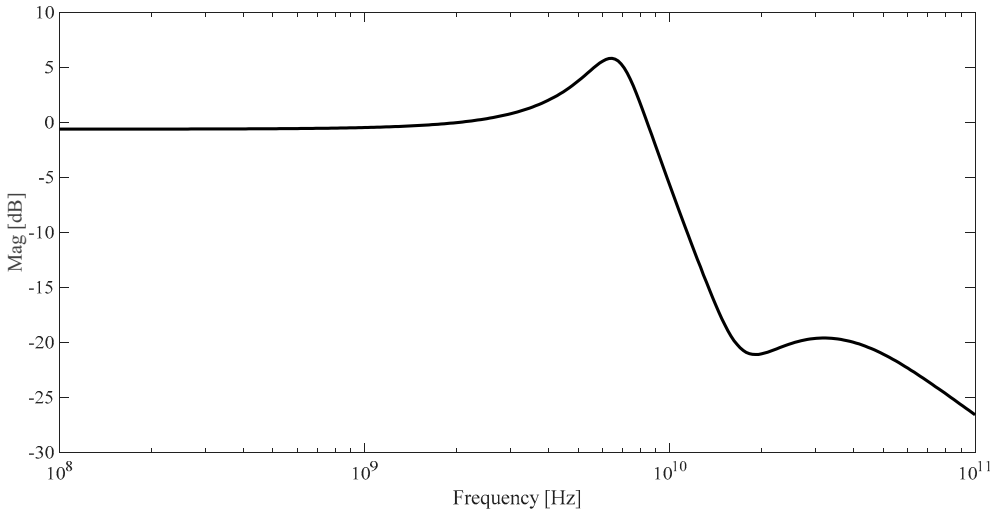

Figure 5. Frequency Response of the proposed Biquadratic Filter.

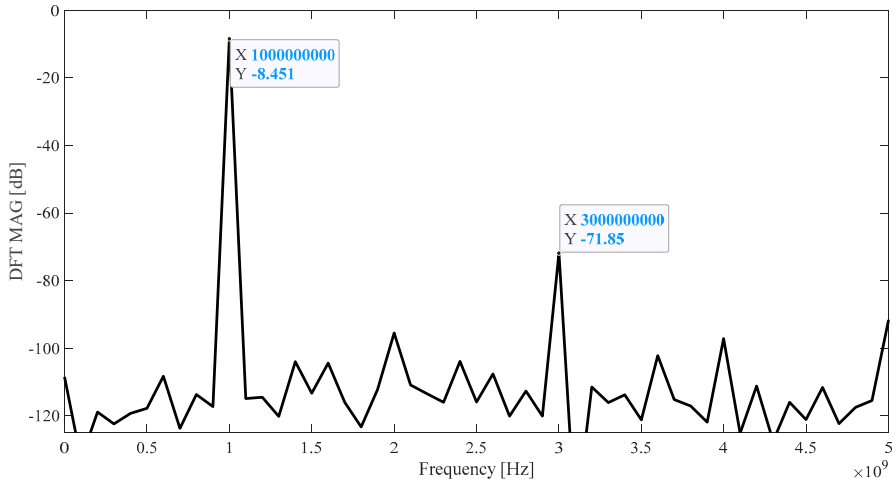

Figure 6. Discrete Fourier Transform (DFT) of the differential output voltage with an input tone at 1GHz, 0.8Vpp differential.

The DFT result reported in Figure 6 demonstrates that linearity is very good, with 64 dB SFDR in the relatively large input signal condition of 800 mVpp. The dynamic range is dominated by noise, as SFDR is much better than SNR (see Table 2).

Table 3 shows the results of the simulations accounting for temperature variations, and Table 4 shows those accounting for supply voltage variations. These results confirm the robustness of the filter to both temperature and supply voltage variations.

Table 3. Simulations vs. temperature.

Name	Minimum	Maximum	Unit
T	−30	120	°C
P_{diss}	18.4	19.56	mW
f_0	6.91	5.65	GHz
f_{3dB}	10.2	8.2	GHz
A_{pk}	5.51	5.3	dB
A_{dc}	−0.53	−0.58	dB
Q	2	1.9	-
SFDR	61	73	dB
v_{onoise}	1.12	1.51	mV
D_R [1]	49.4	51.6	dB

[1] D_R has been computed as in [14].

Table 4. Simulations vs. supply voltage.

Name	Value	Value	Unit
V_{cc}	2.85	3.15	V
P_{diss}	17.1	19.9	mW
f_0	6.1	6.4	GHz
f_{3dB}	8.9	9.6	GHz
A_{pk}	4.89	5.72	dB
A_{dc}	−0.7	−0.56	dB
Q	1.9	2	-
SFDR	48	56	dB
v_{onoise}	1.26	1.26	mV
D_R [1]	44.3	47	dB

[1] D_R has been computed as in [14].

Monte Carlo simulations, using the accurate statistical models for HBT, MOS and passive devices available in the design kit of the BiCMOS055 technology, have been carried out in the Cadence Virtuoso ADE XL environment. Figure 7 shows the frequency response of the biquad filter for 100 Monte Carlo iterations, whereas Figures 8–11 show the histograms of DC gain, quality factor, resonant frequency and 3 dB bandwidth of the filter respectively. A summary of the mean values (μ) and standard deviations (σ) for these quantities is reported in Table 5.

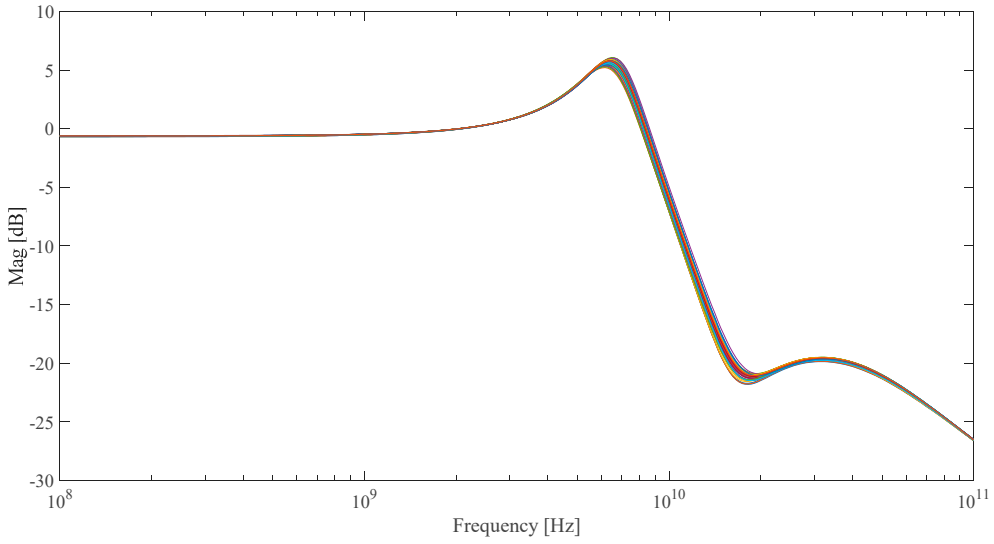

Figure 7. Frequency Response for 100 Monte Carlo iterations.

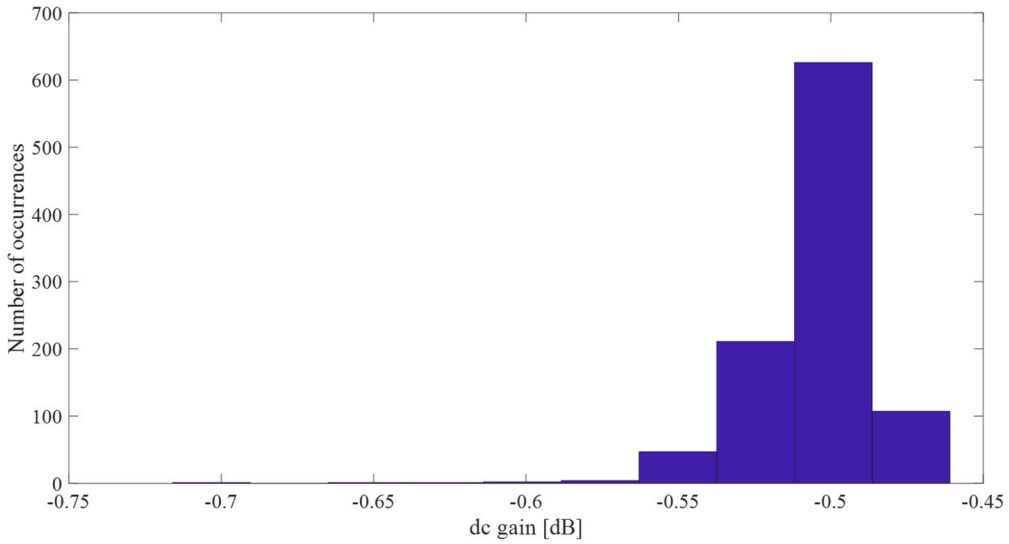

Figure 8. Histogram of DC Gain A_{dc} for 1000 Monte Carlo iterations.

Table 5. Summary of Monte Carlo simulations (1000 iterations).

Name	μ	σ	Unit
A_{dc}	−0.505	0.018	dB
Q	2.071	0.037	-
f_0	6.471	0.100	GHz
f_{3dB}	9.588	0.126	dB

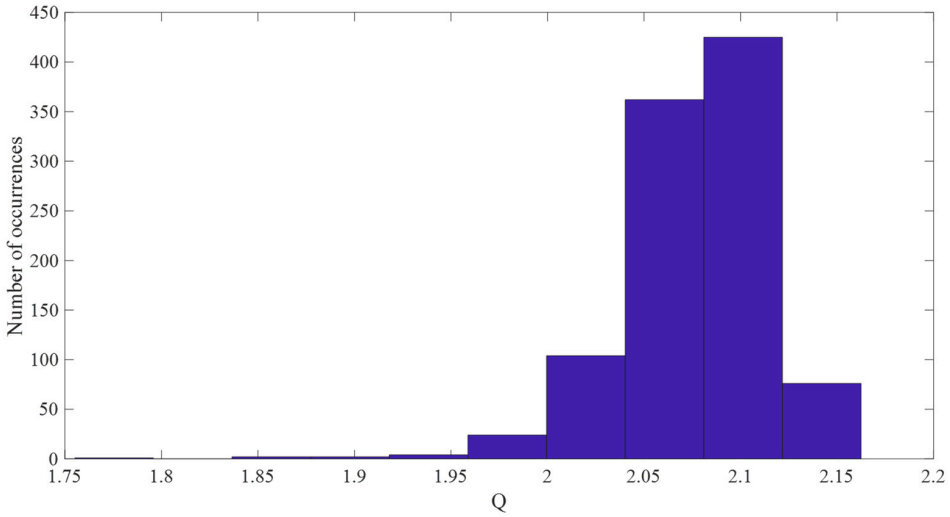

Figure 9. Histogram of quality factor Q for 1000 Monte Carlo iterations.

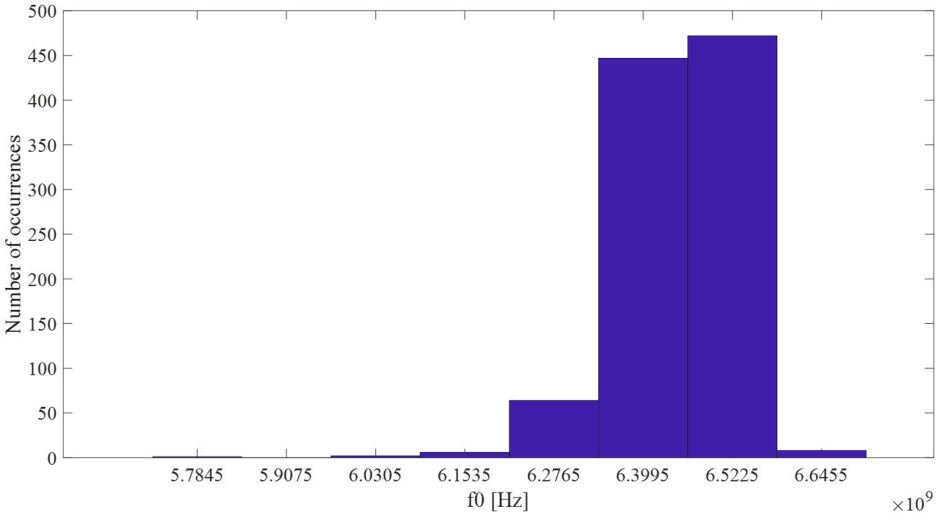

Figure 10. Histogram of resonant frequency f_0 for 1000 Monte Carlo iterations.

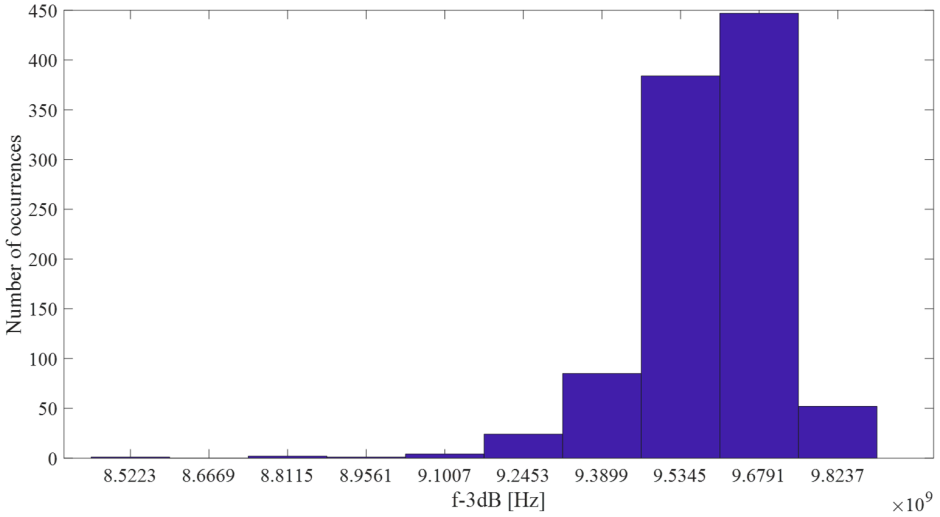

Figure 11. Histogram of 3 dB bandwidth f_{3dB} for 1000 Monte Carlo iterations.

All these results allow us to assess the robustness of the filter under Monte Carlo simulations: the DC gain is almost constant, while the quality factor and resonance frequency of the complex poles vary limitedly.

A comparison with recent technical papers reporting inductorless active lowpass filters with cut-off beyond 1.5 GHz and the proposed filter is reported in Table 6. The proposed filter outperforms all the other designs in terms on SFDR, DR and FOM3, confirming the outstanding linearity performance of our unitary-gain, closed-loop approach.

Table 6. Comparison against the state of the art.

	This Work	[14]	[8]	[18]	[12]	[19]	[11]	[13]
Year	2020	2018	2017	2014	2012	2010	2006	2002
Technology	BiCMOS 55 nm	BiCMOS 55 nm	CMOS 40 nm	CMOS 28 nm	CMOS 65 nm	BiCMOS 180 nm	BiCMOS 250 nm	CMOS 180 nm
Filter Type	*SK*	*AL*	*TT*	*GMC*	*GMC*	*GMC*	*GMC*	*AL*
Supply Voltage [V]	3	3	1.1	1.1	1.4	3.3	3.5	1.8
P_{diss} [mW]	18	13.7	17.6	30	140	300	99.8	1.6
f_{3dB} [GHz]	9.55	10.5	1.6	3.3	10	3.2	4.1	4.6
SFDR [dB])	64	−51	−46	−40	−45	40	-	−57
v_{onoise} [mVrms]	1.36	1.1	1.5	-	0.5	-	-	-
SNR [dB]	46.4	47.2	43.2	39	45	-	-	-
D_R[1] [dB]	49.3	45.5	41.1	37	42	-	20.1	-
Npole	2	2	5	5	3	6	5	5
FOM1 [mW]	9	6.85	3.52	6	46.6	50	19,9	0.32
FOM2 [pW/Hz]	0.94	0.65	2.2	1.81	4.7	15.6	4,8	0.07
FOM3[mW/GHz]	0.0032	0.0035	0.019	0.025	0.037	-	0.47	-
Area (mm^2)	0.0027	0.0056	0.12	0.091	0.01	0.17	0.82	-
Measured	No	No	Yes	Yes	Yes	No	Yes	Yes

[1] D_R has been computed as in [14].

It has to be noted that most papers in the literature are based on the Gm-C approach [11,12,18,19], in which the open-loop input stage often limits linearity, whereas the closed loop approach proposed in this work exploits feedback to reduce nonlinear distortions. Focusing on reference [8], it is based on a closed loop Tow–Thomas (TT) architecture which shows a limited dynamic range owing to the lower bandwidth of CMOS amplifiers, which makes feedback less effective. Reference [14] exploits positive feedback to synthetize an active inductor (AL), and resistive degeneration of the differential pair to improve linearity. Having similar performance and using the same technology, this solution shows lower power consumption but also lower dynamic range; hence, it performs better in the first two FOMs, but worse in the third-one, owing both to worse SNR and SFDR performance. Reference [13] reports a 5th-order filter based on an active circuit which provides a transfer function with two poles and two zeros with only three active devices: this provides for very good power efficiency, as shown by excellent FOM1 and FOM2 performance, but no detailed noise information is provided, so FOM3 cannot be computed. As it reports 100nV/$\sqrt{}$Hz noise for 4.57 GHz of bandwidth, estimated noise is 6.8 mV, which would provide a very low SNR of 25.5 dB. Hence, the dynamic range of such a design is severely limited.

6. Conclusions

A fully differential Sallen–Key filter with a 3-dB bandwidth of about 10 GHz and based on a DDA amplifier which exploits bipolar and MOS devices of the commercial BiCMOS055 technology

from STMicroelectronics has been proposed in this work. Post-layout simulations have shown that the proposed filter outperforms all recently published inductorless active lowpass filters with cut-off frequencies beyond 1.5 GHz in terms of *SFDR*, *DR*, and *FOM3*. Parametric simulations accounting for temperature and supply voltage variations as well as Monte Carlo simulations have confirmed the robustness of the filter to temperature, supply voltage and mismatch variations. The power efficiency of the proposed filter is good and the area footprint is very low. Based on the comparison against the state of the art reported in Table 6, we have demonstrated that the proposed architecture—which exploits a fully differential DDA-based voltage follower as active element—allows the implementation of closed loop biquad filters with a 3-dB bandwidth up to about 10 GHz while guaranteeing better linearity performance with respect to filter architectures based on the Gm-C or the active inductor approach. Furthermore, we can state that it is possible to use the proposed fully differential Sallen–Key closed-loop topology for filters with bandwidths around 10 GHz, exploiting NPN devices with an f_T in the order of 300 GHz and PMOS with an f_T in the order of 100 GHz as active loads. Unity gain feedback across the DDA ensures the highest closed-loop bandwidth, though limiting the achievable maximum quality factor. The resulting filter is also compact, and shows the lowest area occupation among the existing literature.

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