

# KM3NeT front-end and readout electronics system: hardware, firmware and software

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## Abstract.

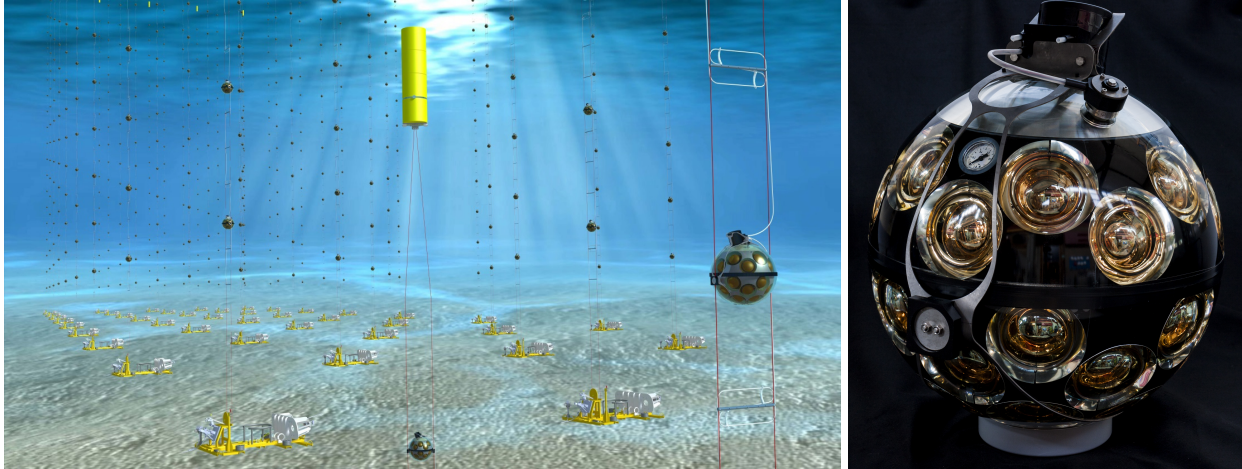
The KM3NeT research infrastructure being built at the bottom of the Mediterranean Sea will host water-Cherenkov telescopes for the detection of cosmic neutrinos. The neutrino telescopes will consist of large volume three-dimensional grids of optical modules to detect the Cherenkov light from charged particles produced by neutrino-induced interactions. Each optical module houses 31 3-inch photomultiplier tubes, instrumentation for calibration of the photomultiplier signal and positioning of the optical module and all associated electronics boards. By design, the total electrical power consumption of an optical module has been capped at seven watts. This paper presents an overview of the front-end and readout electronics system inside the optical module, which has been designed for a 1 ns synchronization between the clocks of all optical modules in the grid during a life time of at least 20 years.

**Keywords:** front-end electronics, readout electronics, neutrino telescope, KM3NeT.

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## 1 Introduction

KM3NeT is a European research facility being built at the bottom of the Mediterranean Sea. It will host the future large volume ARCA and ORCA neutrino telescopes. The ARCA telescope (Astroparticle Research with Cosmics in the Abyss), a cubic kilometer scale detector mainly dedicated to the detection of high energy neutrinos of astrophysical origin, is being installed at a site located offshore the coast of Sicily, Italy, at an approximate depth of 3500 m. The detector of the ORCA telescope (Oscillation Research with Cosmics in the Abyss), located at a depth of about 2400 m offshore Toulon, France, will be optimised for the detection of lower energy neutrinos to allow for the study of fundamental properties of neutrinos. ARCA and ORCA share the same detector technologies.<sup>1</sup> Cherenkov light produced by neutrino-induced charged particles will be



(a) KM3NeT detector, artistic illustration.

(b) Digital Optical Module.

Fig 1: (a) Artistic illustration of the KM3NeT detector. Note that the illustration is not to scale and that actually sunlight will not reach the depths at which the KM3NeT detector is deployed. (b) A picture of the KM3NeT optical module with the fly's eye organisation of the PMTs and the cap of the aluminum cooling 'mushroom' visible. The Titanium collar around the module supports the connection to the ropes of the DU.

detected by a regular array of optical modules in the water volume of the telescope (Figure 1a).

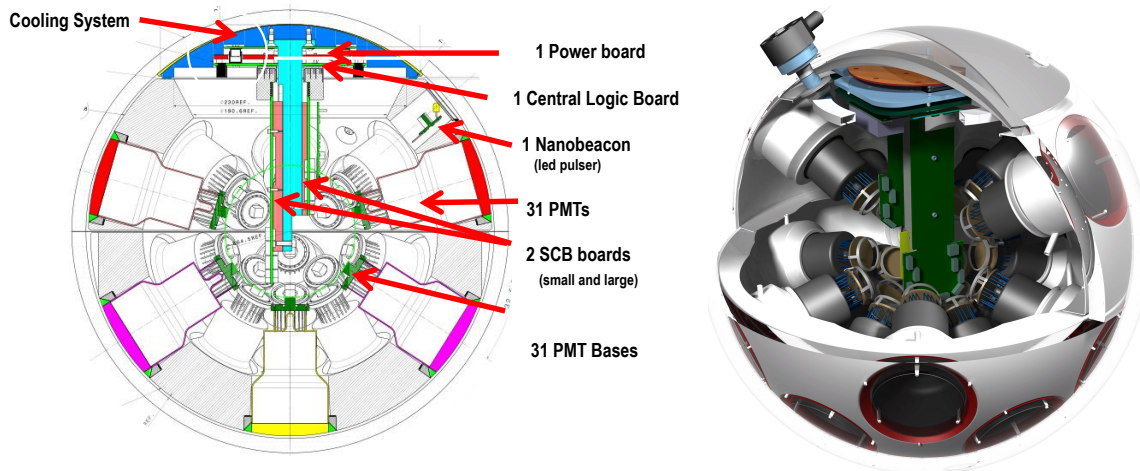
Each module (Figure 1b) is a high-pressure resistant, 17-inch diameter glass sphere containing 31 3-inch photomultiplier tubes (PMTs), instrumentation for calibration and positioning and all associated electronics boards. The modules are called Digital Optical Modules (DOMs).<sup>2,3,4</sup> Eighteen DOMs, uniformly distributed along a vertical slender structure, form a Detection Unit (DU). The DOMs are held into place by means of two thin ropes. The DU is anchored on the seabed and kept in a close to vertical position by a submerged buoy at its top. An electro-optical backbone cable, with breakouts at each DOM, runs along the full DU length providing connection for power feeding and data transmission.

In each DOM, the 31 PMTs are organized in five rings of six PMTs, plus a single one at the bottom pointing downward (Figure 2). The PMTs are kept in place by a 3-D printed support structure. The lower and the upper hemisphere of the module contain 19 and 12 PMTs, respectively. In the upper hemisphere, a mushroom-shape aluminum structure provides support to the electronic



boards of the DOM. The top surface of the mushroom cap is glued to the glass sphere in order to provide heat dissipation to the seawater. Fixed to the mushroom cap is the Power Board, which provides all the DC voltages needed by the electronics. This board will be described in Section 3. The Central Logic Board (CLB), which contains a Field Programmable Gate Array (FPGA), is directly connected to the Power Board. In the FPGA, the Intellectual Property (IP) cores that capture the PMT generated signals are embedded. Also embedded in the FPGA is an implementation of the White Rabbit (WR),<sup>15</sup> a fully deterministic Ethernet-based timing protocol which provides both data transmission and accurate timing. The WR technology allows for a synchronization of the clocks of all CLBs in the telescope at nanosecond precision. The description of the CLB is presented in Section 2. In Section 4, the PMT base board, which generates and adjusts the High Voltage (HV) supply of the PMT and converts the analog signals generated by the PMTs to Low Voltage Differential Signaling (LVDS) is described. Two Signal Collection Boards (SCBs), one for each DOM hemisphere, connect the CLB with the PMTs allowing for command and data signal transfer. The SCB is described in Section 5.

The light detected by a PMT is converted into an electrical pulse. When this electrical pulse surpasses a predetermined threshold, the PMT base board sets its LVDS output. This output is reset when the electrical pulse goes below the threshold. The first crossing of the threshold and the Time over Threshold (ToT) will be measured by the Time to Digital Converters (TDCs) implemented in the CLB. The ToT gives an estimate of the pulse amplitude and its charge. The calibration of the PMT HV provides an average ToT value of 26.4 ns when a single photoelectron impinges on a PMT. The CLB organizes the acquisition of the LVDS signals in frames, or timeslices, of fixed length in time, typically 100 ms. The data acquired, organized in timeslices, are sent to a computer farm onshore via an optical network integrated in the submarine cables and junction boxes. The



(a) 2D vertical cross section of the DOM.

(b) 3D open model of the DOM.

Fig 2: 2D and 3D drawings of the DOM showing the position of the different devices.

DU anchor hosts a base module equipped with a wet-mateable jumper to connect the DU to the seafloor network. The full chain of readout electronics was successfully qualified in a prototype DU of three DOMs deployed at the Italian KM3NeT site in May 2014 and operated more than one year.<sup>5</sup> Mass-produced electronics is operational in full-size deployed DUs with 18 DOMs,<sup>6</sup> thus demonstrating its reliability.

Figure 3 provides a block diagram of the different DOM electronics boards and their interconnections. The power consumption of the DOM is discussed in Section 6 and the reliability studies performed on the DOM electronics boards are presented in Section 7. Finally, a conclusion is given about the front-end and readout electronics system in light of the design goals set out by the KM3NeT Collaboration.

## 2 The Central Logic Board

The DOM CLB<sup>7,8</sup>(Figure 4) is the main electronics board in the readout chain of KM3NeT. The PMT bases generate LVDS signals from the PMT electrical pulses. The corresponding SCB re-

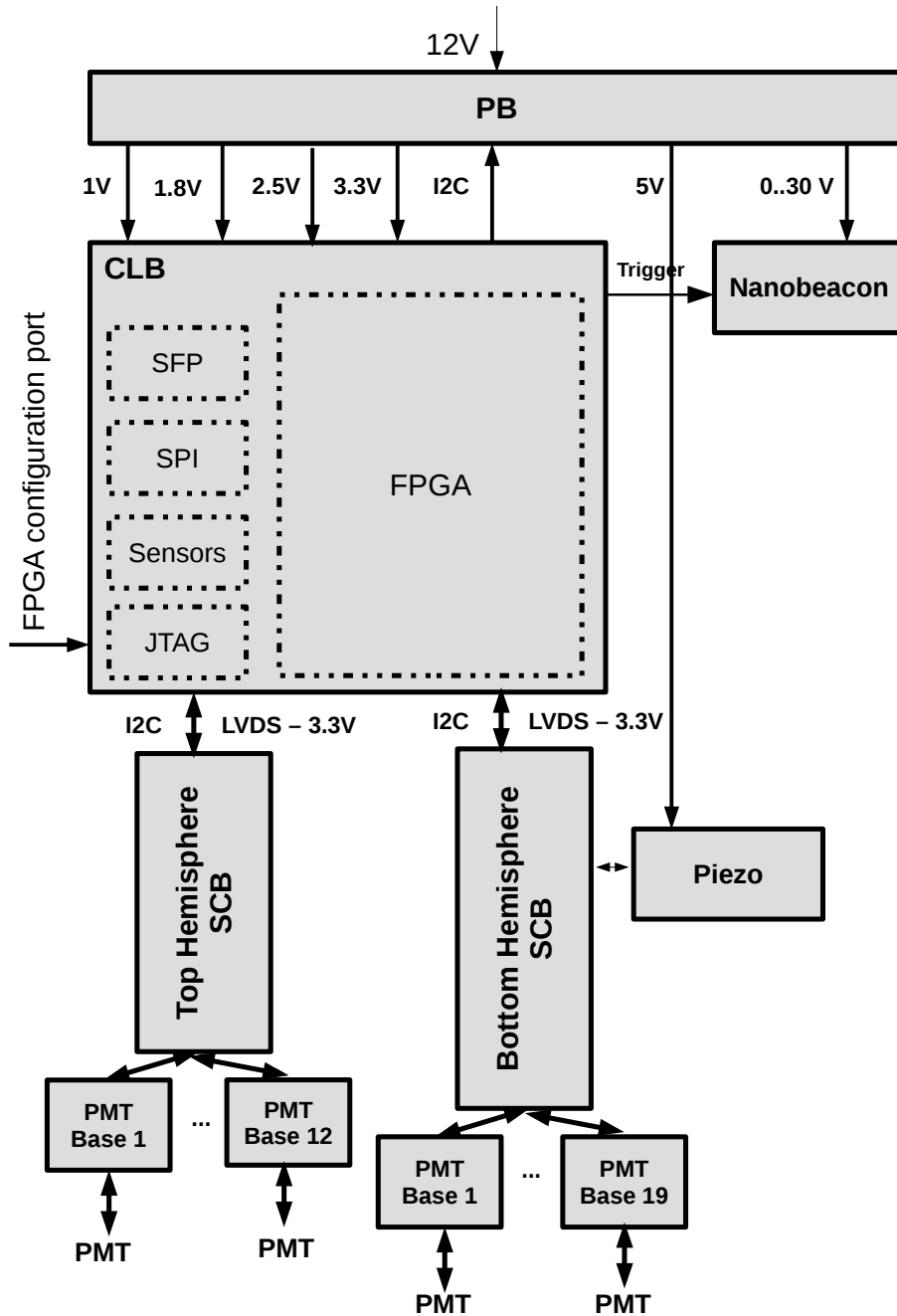


Fig 3: Block diagram of the DOM electronics boards and their interconnections.

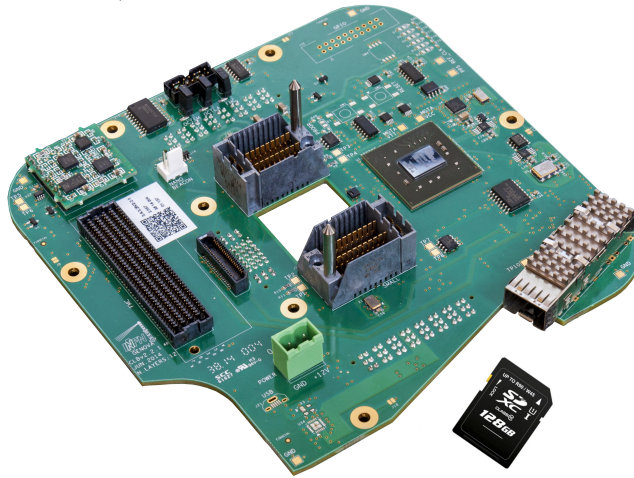


Fig 4: The DOM Central Logic Board. An SD memory is presented close to the CLB as dimension reference.

receives and distributes these signals to the CLB, where they are digitized with a resolution of one nanosecond by TDCs running in the FPGA programmable logic. After being organized and timestamped in the CLB, the TDC data are transferred to the onshore station for further processing and storage. The CLB board also houses a compass/tiltmeter, three temperature sensors and a humidity sensor. In addition, it provides a connection for a LED flasher, called Nanobeacon.<sup>19</sup> Also, a piezo sensor is connected to the CLB via the SCB that serves the lower hemisphere.

The control of the CLB is achieved by means of custom software which runs in a LatticeMico32 (LM32)<sup>9</sup> soft-processor operating in the programmable logic of the CLB FPGA.

In the next subsections the hardware, firmware and software of the CLB are described.

### *2.1 Central Logic Board hardware*

The CLB Printed Circuit Board (PCB) comprises twelve layers: six of them are dedicated to signals, two of them to power planes while the remaining four layers are ground. The ground layers surround the power planes in order to reduce the Electro-Magnetic Interferences (EMI) from the power layers on the signal layers and to improve the signal integrity.<sup>10</sup> For the same

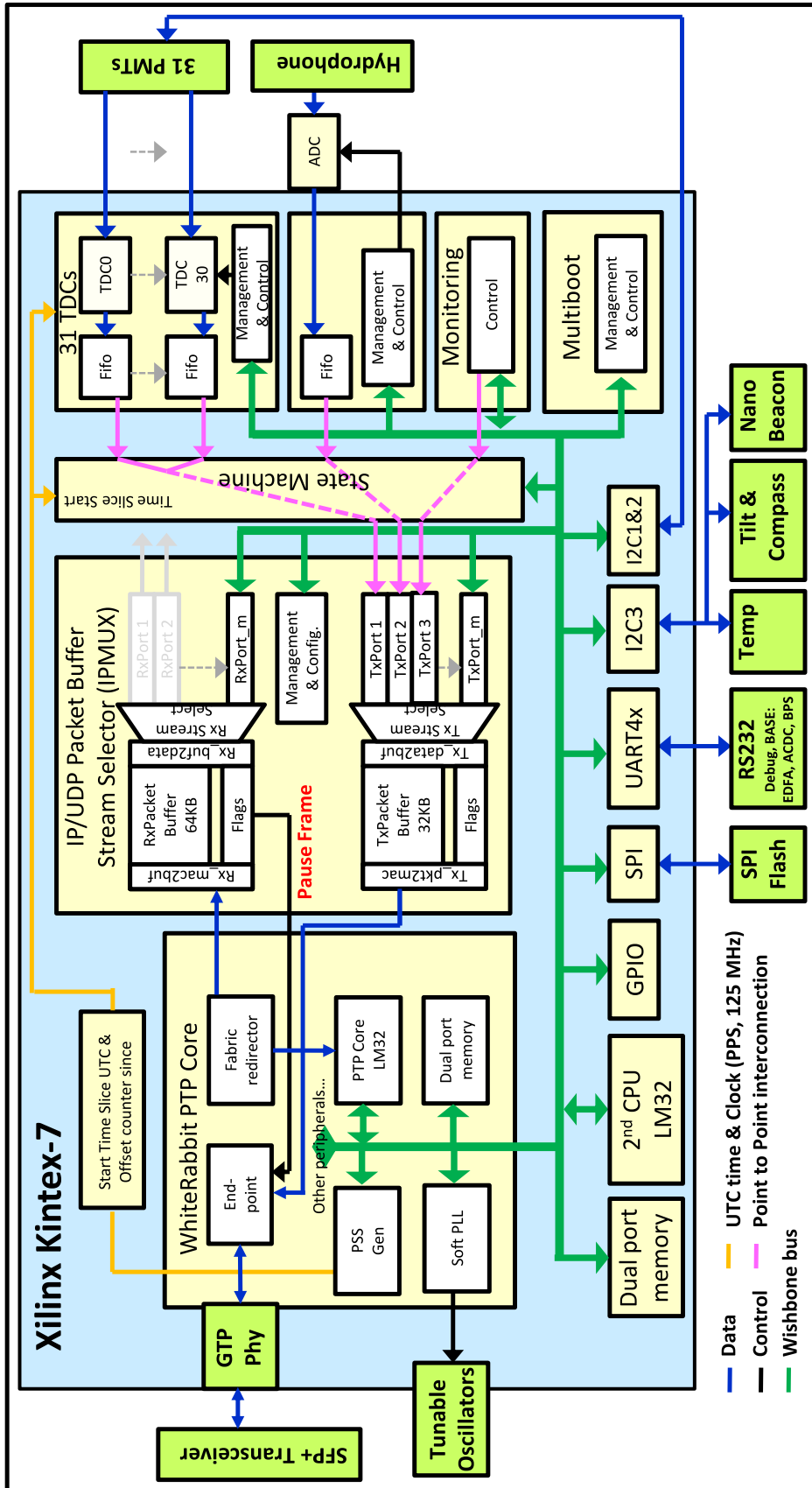


Fig 5: Block diagram of the CLB FPGA firmware.

reasons, the number of vias in these layers has also been minimized wherever possible. Special care has been taken in routing the LVDS signals generated by the PMT base boards. The difference in length between any of the differential pairs has been kept below 100 ps. Moreover, in the case of the clock signals, this difference has been reduced to below 20 ps.

The central coordinating component of the CLB is a Xilinx Kintex-7 FPGA (XC160-T), chosen for its relatively low power consumption. Other relevant components are: the Serial Peripheral Interface (SPI) flash memory, which stores four images of the FPGA and the configuration parameters of the CLB; the programmable oscillators, which provide the appropriated clock signals needed by the WR protocol; two press fit connectors that provide a solid mechanical and electrical connection between the CLB and the SCB. The CLB board includes a 25 MHz crystal oscillator. The oscillator signal is first transferred from a clock pin to a buffer in the FPGA, and then fanned-out to the inner Phase Locked Loop (PLL) to provide two high frequency clocks of 250 MHz but with a 90° phase shift, needed by the TDC core. The main component used for the communications with the onshore station is the Small Form-Factor Pluggable (SFP) transceiver, which interfaces the electronics with the optics system.

## 2.2 *CLB firmware*

The readout logic of the DOM runs in the programmable fabric of the FPGA. A block diagram of the readout logic is shown in Figure 5. Its main blocks are:

- The LM32 soft-processor running the control and monitoring software for the CLB.
- The White Rabbit PTP Core (WRPC) (Precision Time Protocol (PTP)), which implements the WR protocol.
- The TDCs, which digitize and time-stamp the PMT signals arriving at the CLB.



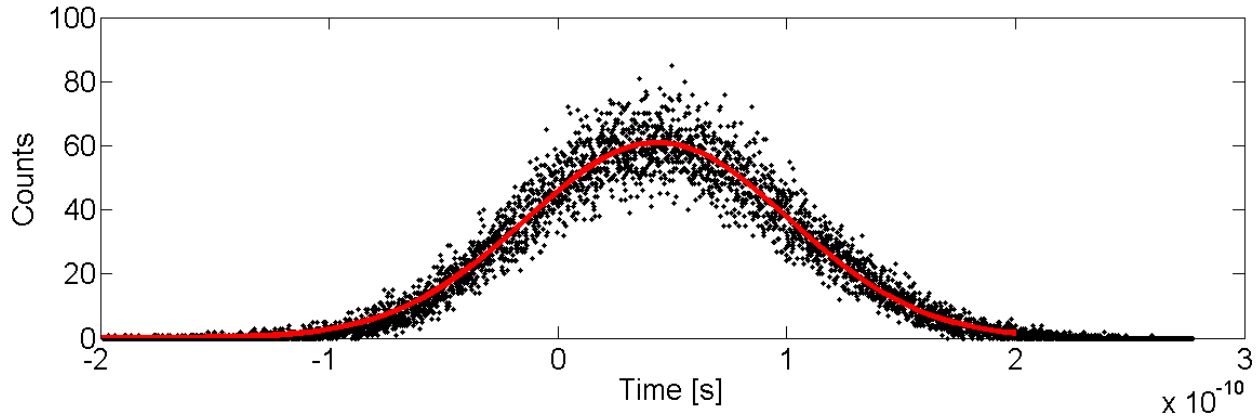


Fig 6: Skew, measured at the laboratory, of the Pulse Per Second of the CLB with respect to the PPS of the Master White Rabbit Switch. The red line is a Gaussian fit to the data with 22 ps standard deviation.

- The state machine and IPMux cores, which collect the TDC data from the PMTs, Audio Engineering Society version 3 (AES3) data from the piezo sensor and the monitoring data from the LM32, and dispatch them over Ethernet to the onshore station.<sup>11</sup>
- The multiboot core, which allows safe remote reconfiguration of the FPGA firmware.
- The different control cores for the instrumentation.

### 2.2.1 Soft-Microcontroller

Central to the control and monitoring of the CLB is the LM32, a subsection of the FPGA fabric consisting of a Central Processing Unit (CPU), Random Access Memory (RAM) and peripherals for timing and communication (Universal Asynchronous Receiver / Transmitter (UART), SPI and Inter Integrated Circuit (I<sup>2</sup>C)). The LM32 was chosen because it uses less FPGA resources than other CPUs<sup>12</sup> and has a wishbone bus<sup>13</sup> master interface. For the wishbone bus many open-source programmable logic peripherals exist, such as SPI/I<sup>2</sup>C controllers, co-processors, timers and counters. In addition, the LM32 CPU is also used in the WRPC, easing the integration and reducing the design complexity. The CPU runs at 62.5 MHz, and has 128 kB of combined program and data

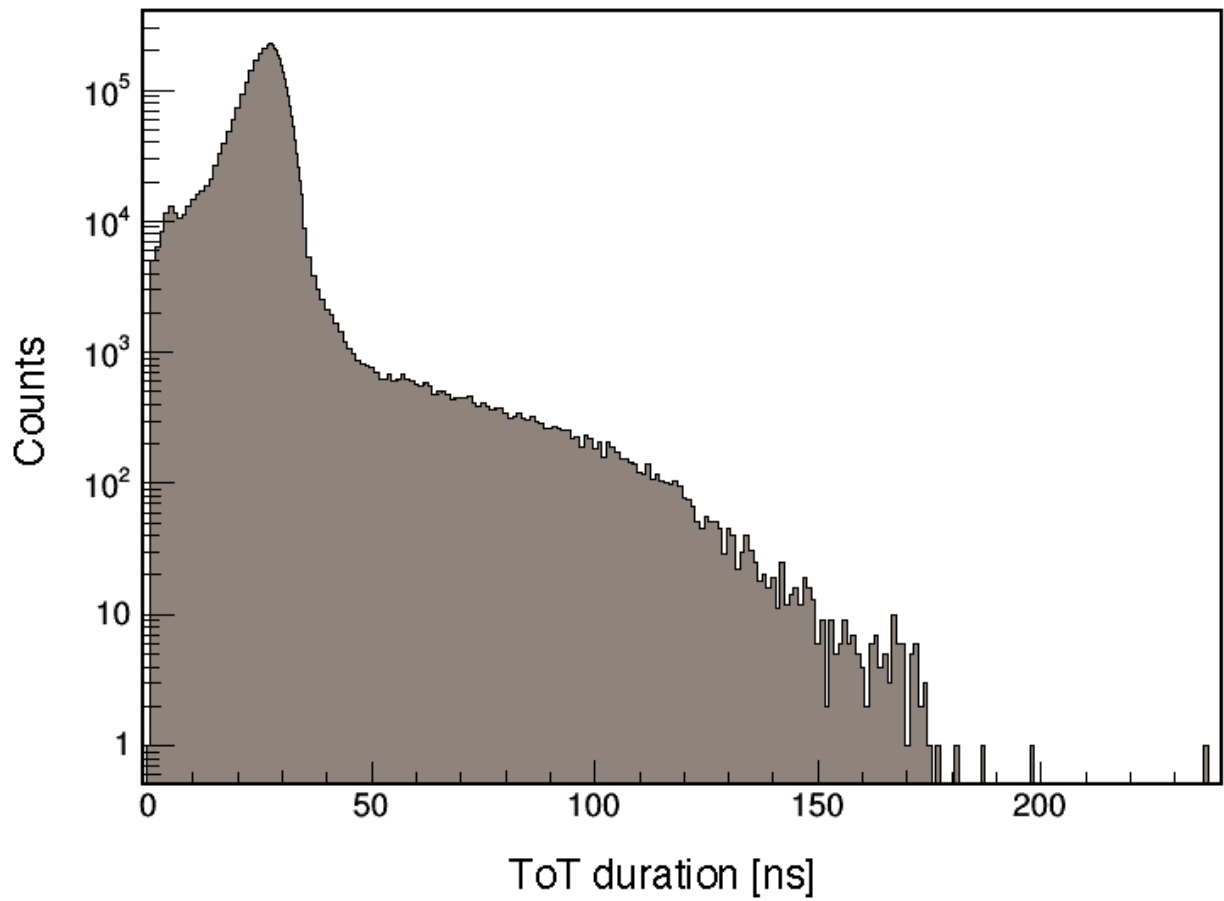


Fig 7: ToT distribution from one DOM of a KM3NeT DU. All the channels have been calibrated in order to harmonise the ToT data arriving from different PMTs

RAM. Moreover, the wishbone bus also connects to the KM3NeT specific programmable logic cores, such that the LM32 can control and monitor the peripherals, which are discussed in the next sections.

### 2.2.2 *White Rabbit PTP core*

The WRPC is an enhanced Ethernet Media Access Controller (MAC), embedded in the CLB FPGA programmable logic. Apart from transferring data, as a regular Ethernet MAC does, the WR protocol synchronizes all CLB clocks in the detector. The protocol is based on the Synchronous Ethernet (SyncE) and PTP standards.<sup>14</sup> The WRPC synchronizes the CLB through the same optical link that is used for data transmission. The global time of the WR network is provided by the WR master switch located onshore, which is synchronized to a Global Positioning System (GPS) receiver. The WRPC IP core synchronizes with the WR master switch and provides a register with the Coordinated Universal Time (UTC), which is used by the rest of the CLB firmware. It also outputs a Pulse Per Second (PPS) signal, which rising edge occurs precisely at the second transition. In order to qualify the stability of the synchronization at the CLB, the skew between the PPS of the CLB and the PPS of a WR switch has been measured at the laboratory using a 50 km optical fiber connection. The skew has a Gaussian distribution with 22 ps standard deviation (Figure 6).

### 2.2.3 *State machine*

The data acquisition is organized in consecutive frames with a period of typically 100 ms, called timeslices. The state machine core orchestrates the data acquisition for the CLB. Firstly, it is responsible for generating the periodic start of the timeslice signal. This signal is synchronized

to the start of a UTC second and repeat at the start of every period. All data acquiring IP cores synchronize their acquisition to this start timeslice signal, and all acquired data are sectioned and timestamped relative to it. Secondly, the state machine is responsible for gathering the acquired data, and merging the UTC time of the timeslice start signal, called the super time, to the acquired data. By combining the relative timeslice time and the super time, the UTC time for all acquired data can be resolved by the onshore Data Acquisition System (DAQ). Once the acquired data are ready, the last responsibility of the state machine is to package the data to be dispatched towards the User Datagram Protocol (UDP) packet generator (IPMux). The data are portioned into frames such that they will fit within the payload of a UDP jumbo packet. A frame header containing metadata, such as the stream identifier or the run number, is also prepared.

#### *2.2.4 Time to Digital Converter*

The TDCs sample the signals from the PMT bases. They are implemented in the CLB FPGA programmable logic with one TDC channel per PMT, totalling 31 IP cores. The cores measure both the pulse arrival time and the duration of the pulse (ToT) using the 1 ns precise UTC WRPC time. The distribution of the ToT data readout as measured by one DOM is shown in Figure 7. The TDC core produces 48 bits per event, where the first eight most significant bits are used for the PMT identifier, the next 32 bits code the arrival time of the event with respect to the timeslice start time, and the last eight bits code the duration. The events are then dispatched to the state machine which also organizes the TDC acquisition in timeslices.

The system clock of the FPGA firmware is derived from the 25 MHz hardware quartz in the PCB. This clock signal is first transferred to a digital PLL to generate the system frequency of 62.5 MHz. The White Rabbit protocol adjusts the phase and frequency of the FPGA system clock

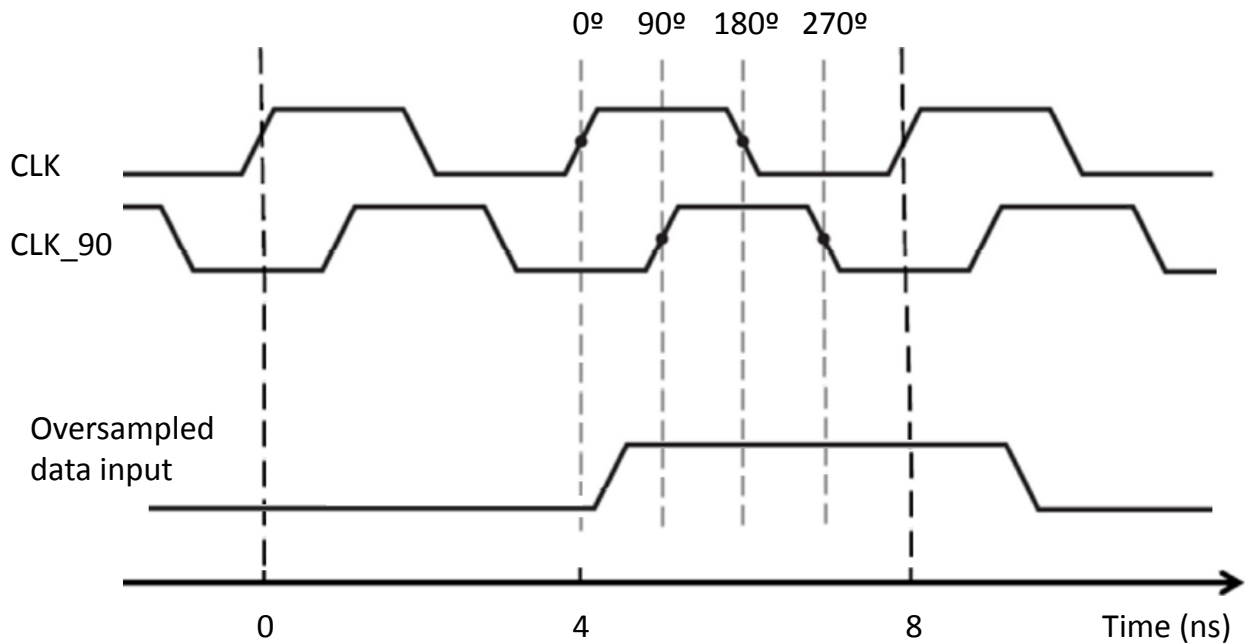


Fig 8: Oversampling technique using two phase-shifted clocks. Technique implemented in the CLB TDCs.

to the reference master clock. Finally, the adjusted system clock is fanned out to the inner PLLs within the FPGA to provide two high frequency clocks of 250 MHz with a phase shift of 90°. The TDC input signals are oversampled at 1 ns rate using the rising and falling edge of the two clocks of 250 MHz as shown in Figure 8.

The information of the sampling is organized by the TDCs, where the arrival time and the pulse length are coded. As all other CLB IP cores connected to the LM32 soft CPU, the TDC core is controlled by the LM32 itself, allowing for enabling/disabling any of the 31 TDC channels.

The TDCs implement the High Rate Veto (HRV) and Multihit features. The HRV limits the total number of acquired hits in a timeslice. If the number of events in a TDC channel surpasses a predetermined threshold, the acquisition is stopped in that channel until the start of the next timeslice. In this way, it is possible to limit the amount of data sent onshore, preventing the blockage of the data acquisition. The Multihit option allows to expand the range of the TDCs,

limited by the ToT codification of eight bits. If this option is active, then the hits with a ToT longer than 255 ns are coded as two or more consecutive events.

### *2.2.5 Acoustic readout*

The CLB also includes a core for the readout of the acoustic piezo sensor,<sup>16</sup> one of the positioning instrumentation devices installed in the DOM. This core reads out the acoustic piezo channel data and timestamps it with respect to the WRPC time. In addition, it generates from the raw acoustic data an AES3 formatted stream, which is dispatched to the state machine.

### *2.2.6 IPMux*

The packets created by the state machine are sent to one of the input ports of the IPMux, an IP/UDP packet buffer stream selector. The IPMux has different input ports for each data sources. For each packet received from the state machine a UDP header is added. By using the Ethernet jumbo frames, a maximum transfer unit of 9014 bytes per frame is possible, consequently reducing protocol overhead significantly when the channel is fully occupied.

The IPMux receives also data from TDCs, the acoustic readout, the monitoring and the slow control LM32 channels. All of them are aggregated on the IPMux and transferred to the WRPC endpoint, where they are routed through the White Rabbit core and sent onshore. Once they arrive to shore, it is possible to discriminate any of the sources of the IPMux (optical, acoustic and monitoring channel) by the port number.

### *2.2.7 Monitoring channel*

The monitoring channel enables transmission of metadata synchronous with the TDC and AES3 channels. However, unlike the TDC and AES3, the monitoring channel is not data driven, and



produces only one packet of content at the timeslice start signal. The header of the packet provides information regarding the TDC First-In First-Out Buffer (FIFO). The monitoring packet consists of two parts. The first part is delivered by programmable logic, containing additional summary information concerning the TDC channel, such as the actual number of hits per channel. The content of the second part is software defined. At initialization, the programmable logic is provided with a pointer to a software defined structure. For each timeslice, the content of this structure is combined before dispatching to the state machine.

The software provides additional information such as the latest reading from the compass and tilt sensor. Also information about the state of the buffers and other system information is inserted into this packet.

### *2.2.8 Multiboot core*

On startup, the FPGA configures itself by loading the first valid image it finds while scanning the SPI flash memory. Up to four images can be stored in the flash memory at subsequent memory locations, reserving the memory regions above those images for storage of settings and logging. The multiboot gives access to the internal Xilinx specific ICAP2 hard-IP block, which allows software initiated reconfiguration of the FPGA at any memory offset. The multiboot is an essential part of the two-stage startup sequence used for fail-safe startup of the CLB. The multiboot mechanism is described in [2.3.3](#).

### *2.3 CLB embedded software*

The FPGA contains two LM32 processors, the WRPC LM32 and the second LM32. Both run a separate software stack. The WRPC LM32 software was developed by the White Rabbit Collabo-

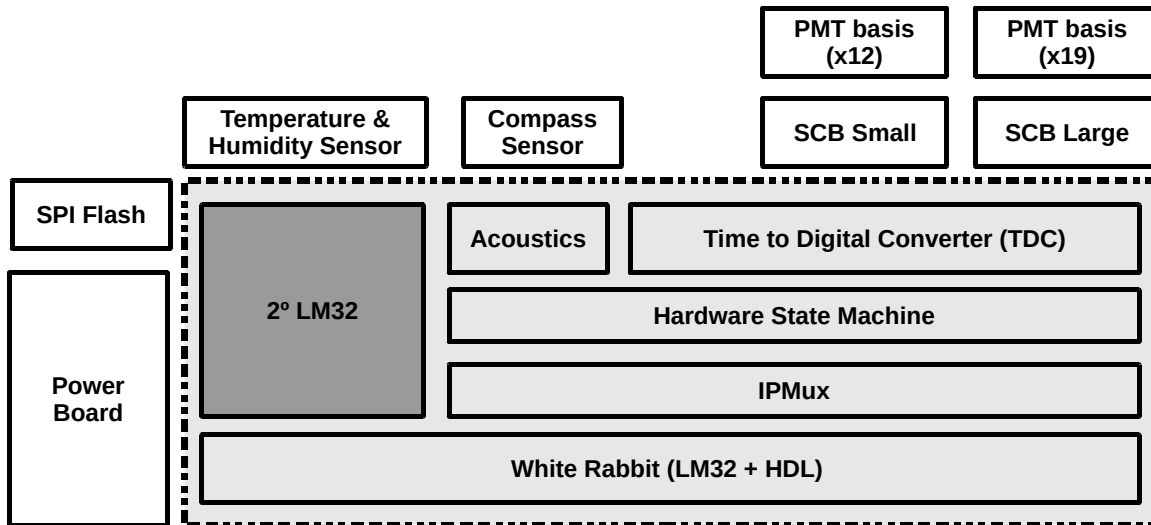


Fig 9: Embedded software location with respect to the main components of the CLB, shown in gray. The dashed line shows the boundaries of the FPGA.

ration,<sup>17</sup> but it has been adapted to the KM3NeT network topology. The second LM32 controls the DOM. The software has been developed by the KM3NeT Collaboration from scratch and designed as control software for the KM3NeT detector. The latter software is discussed in the following sections.

### 2.3.1 Main tasks

The KM3NeT embedded software handles the following tasks:

- Initializing, controlling and monitoring hardware.
- Executing commands issued from the onshore station.
- Sending diagnostic information back to shore.
- Applying firmware updates.

A representation of the hardware directly coupled to the second LM32 is shown in Figure 9. Most of the components inside the dashed line are programmable logic cores, including the CPUs.

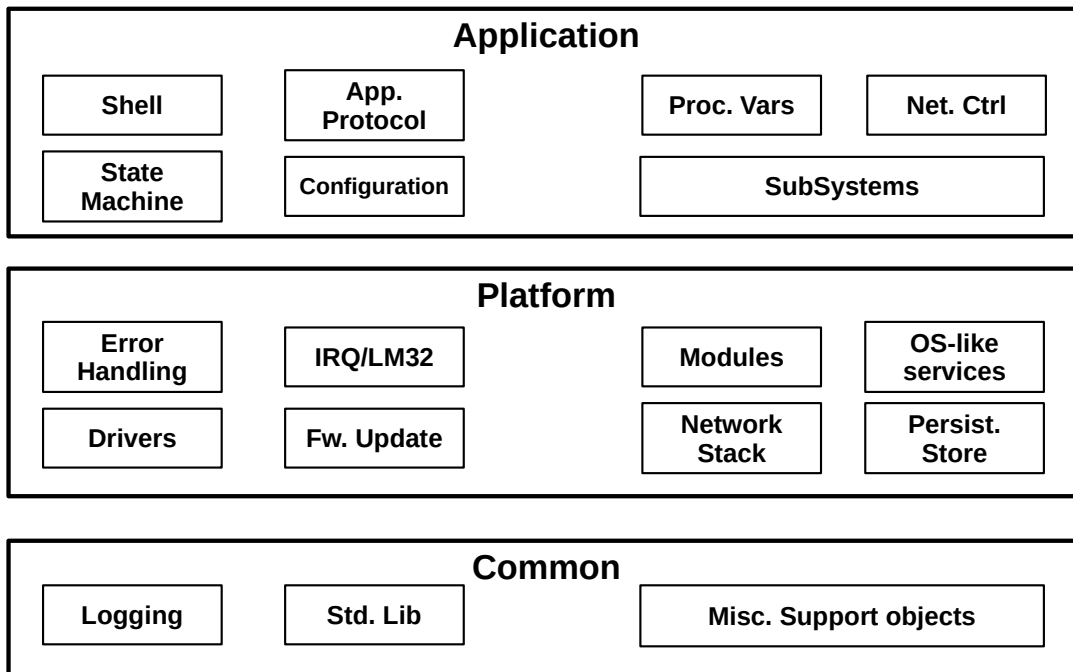


Fig 10: Layers and modules of the CLB embedded software.

The hardware devices lie outside the dashed line boundary. Almost all cores are mapped into the memory space of the LM32. The embedded software reads from or writes to specific memory locations, depending on the device addressed. Outside the dashed lines in Figure 9, the hardware is controlled through external Integrated Circuit (IC) buses like I<sup>2</sup>C or SPI. The interfaces require an additional layer of drivers to communicate with these devices.

### 2.3.2 Software generalities

The software running in the CPU is primarily coded in C, but some bootstrap and interrupt handling code has been written in LM32 assembly. There is no preemptive embedded operating system, but just a simple kernel capable of executing different tasks in a collaborative fashion. The layered structure of the main modules of the software stack is shown in Figure 10.

The Common layer contains functions and objects used throughout the software. They are not

specific to the LM32 platform and could be compiled for any architecture. For example, the logging facilities are placed in this layer. The Platform layer contains all the code required to control the LM32 and all the connected hardware. It consists of hardware control, OS-like services and the network stack. It does not contain application functionality, but it provides convenient functions for the application layer to control and monitor the hardware. Finally, the Application layer contains the high-level functionality of the software. It interprets and executes remote commands, configures and monitors the hardware and implements the software state machine.

### *2.3.3 Firmware update and multiboot*

As explained in subsection [2.2.8](#), the embedded software has, through the multiboot core, the capability of configuring the FPGA from any image located in the serial flash. For the CLB, the flash may contain up to four separate configuration images, starting at address 0 with the startup image, also known as the golden image. The subsequent image is the runtime image, then follow two possible backup images, or test images. After this, the space is reserved for settings and persistent logging. The remaining area of the flash is reserved for storing custom debug and diagnostic information. The complete flash layout is shown in [Figure 11](#).

The golden image is a special image with minimal hardware initialization. The memory region occupied by the golden image is protected from accidental overwrite by write protection feature part of the flash controller. The golden image will start by default a pre-selected image, usually the runtime image, 30 s after a network connection has been established. In exceptional conditions, the startup procedure can be aborted from shore in the 30 s window. The golden image also provides access to diagnostic and recovery features. Each image on the flash can be updated by remote, including the golden image. However, the latter is an exceptional case and should be avoided. To

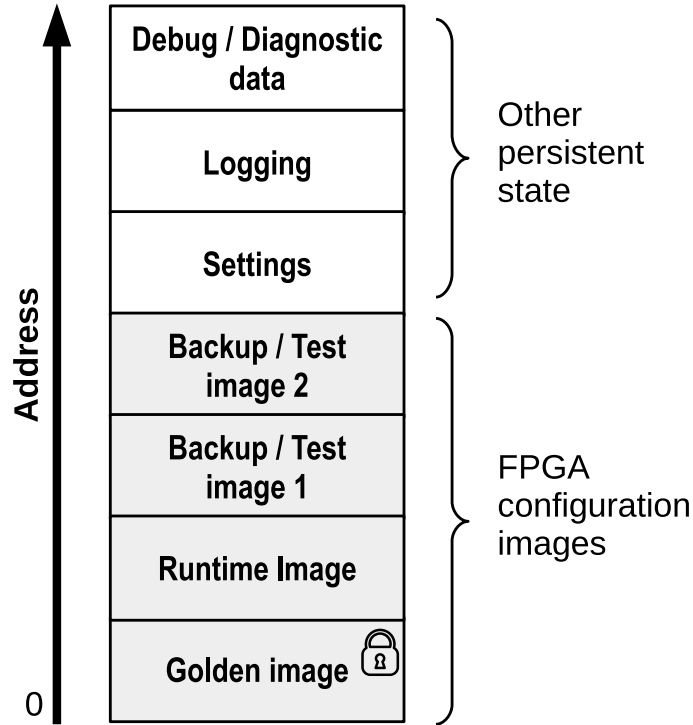


Fig 11: Content of the serial flash memory. At address 0 starts the golden startup image, followed by the primary runtime image, and two backup images. The remainder of the memory contains various types of persistent states.

deal with such cases, a precise and safe procedure has been prepared, which safeguards against accidental loss of CLB due to lack of valid images in the flash. The procedure requires that at least one valid image is always present in the serial flash, even during update.

### 3 Power Board

The Power Board,<sup>18</sup> shown in Figure 12 provides power to the CLB and the full DOM. The schematic view of the Power Board functionality is shown in Figure 13. The input supply to the Power Board is 12 V. Six regulated voltages (1 V, 1.8 V, 2.5 V, 3.3 V, 3.3 V PMT, and 5 V) are generated from the 12 V using DC/DC converters. The 1 V, 1.8 V, 2.5 V and 3.3 V outputs are used by the CLB to supply the FPGA. The 3.3 V PMT output supplies the 31 PMT base boards and the 5 V voltage is used to supply the acoustic piezo sensor. Moreover, the Power Board provides

Table 1: Power Board efficiency for each output voltage.

<b>V(V)</b>	<b>I(A)</b>	<b>Type of DC/DC</b>	<b>Efficiency (%)</b>
2.5	0.13	LTM8021	80
3.3	0.33	OKL-1	90
3.3	0.34	OKL-1	90
1.0	0.80	OKL-3	80
1.8	0.46	OKL-3	80
5.0	0.10	MAX17542G	90

another output, settable via an I<sup>2</sup>C Digital to Analog Converter (DAC), which results in a configurable voltage ranging from 0 V to 30 V. The settable channel is used by the Nanobeacon. The Power Board uses high efficiency DC/DC converters in order to minimize the power consumption in the DOM. The efficiencies of these DC/DC converters are listed in Table 1.

In order to protect the sensitive electronics inside the DOM from the interferences by the high frequency noise produced by the DC/DC converters, the Power Board is located in the shielded part of the cooling mushroom. The chosen location provides also a better cooling of the Power Board. The location of the Power Board in the DOM is shown in Figure 2.

### 3.1 Power startup

One of the functions of the Power Board is to provide a proper voltage startup sequence to the FPGA. For this purpose, a sequencer has been implemented in the Power Board in order to provide the needed sequence of voltages.<sup>20</sup> The sequence of voltages generated by the Power Board is shown in Figure 14. Two power-good signals are generated by the Power Board. The first one indicates that the 3.3 V PMT output has been successfully started (power-good PMT). The second one indicates the successful completion of the power up sequence. The final function implemented in the Power Board is a hysteresis loop to avoid instabilities at the startup. The regulators of the Power Board are enabled only when the input voltage exceeds 11 V, whereas they are disabled



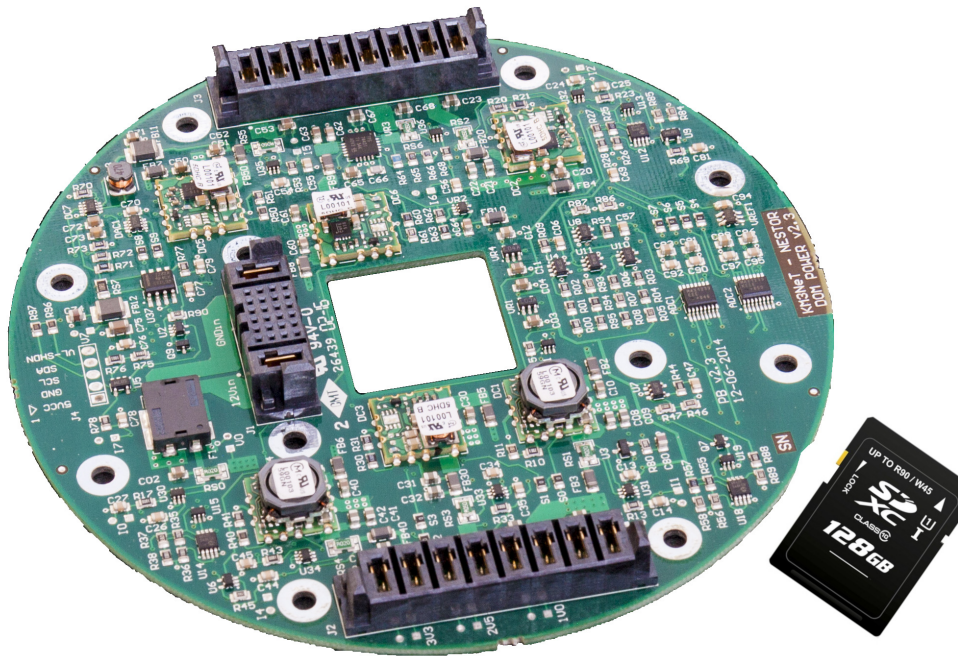


Fig 12: The DOM Power Board. An SD memory is presented close to the Power Board to provide a size reference.

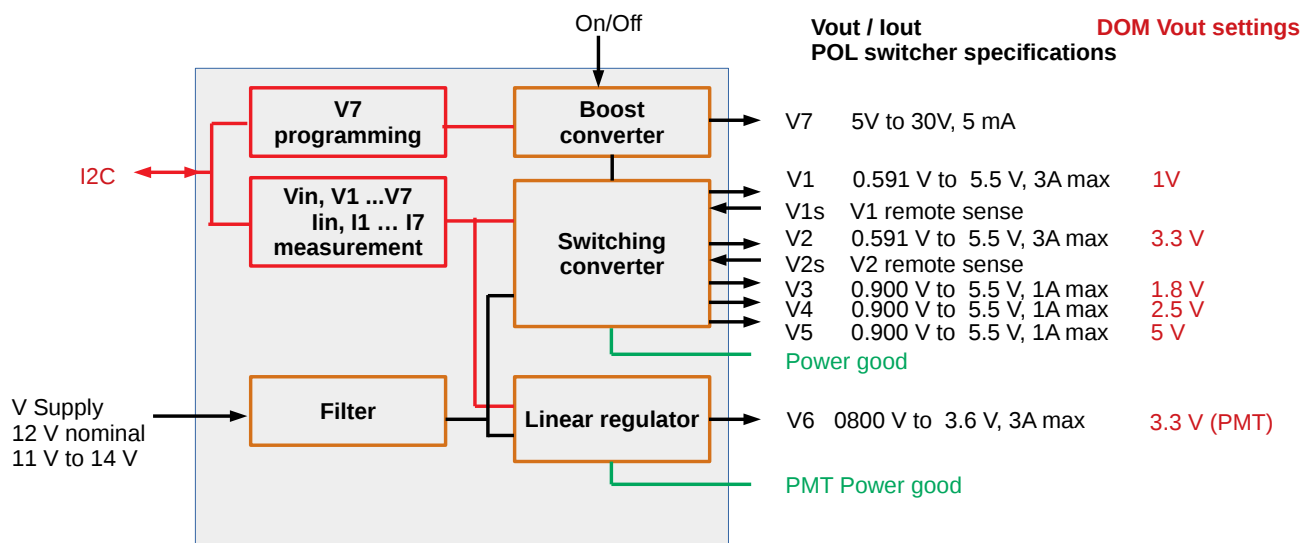


Fig 13: Block diagram of the Power Board functionality. The specification of the DC/DC converters are presented for each power rail. The linear regulator included in the Power Board is used to provide a stable voltage to the PMTs.

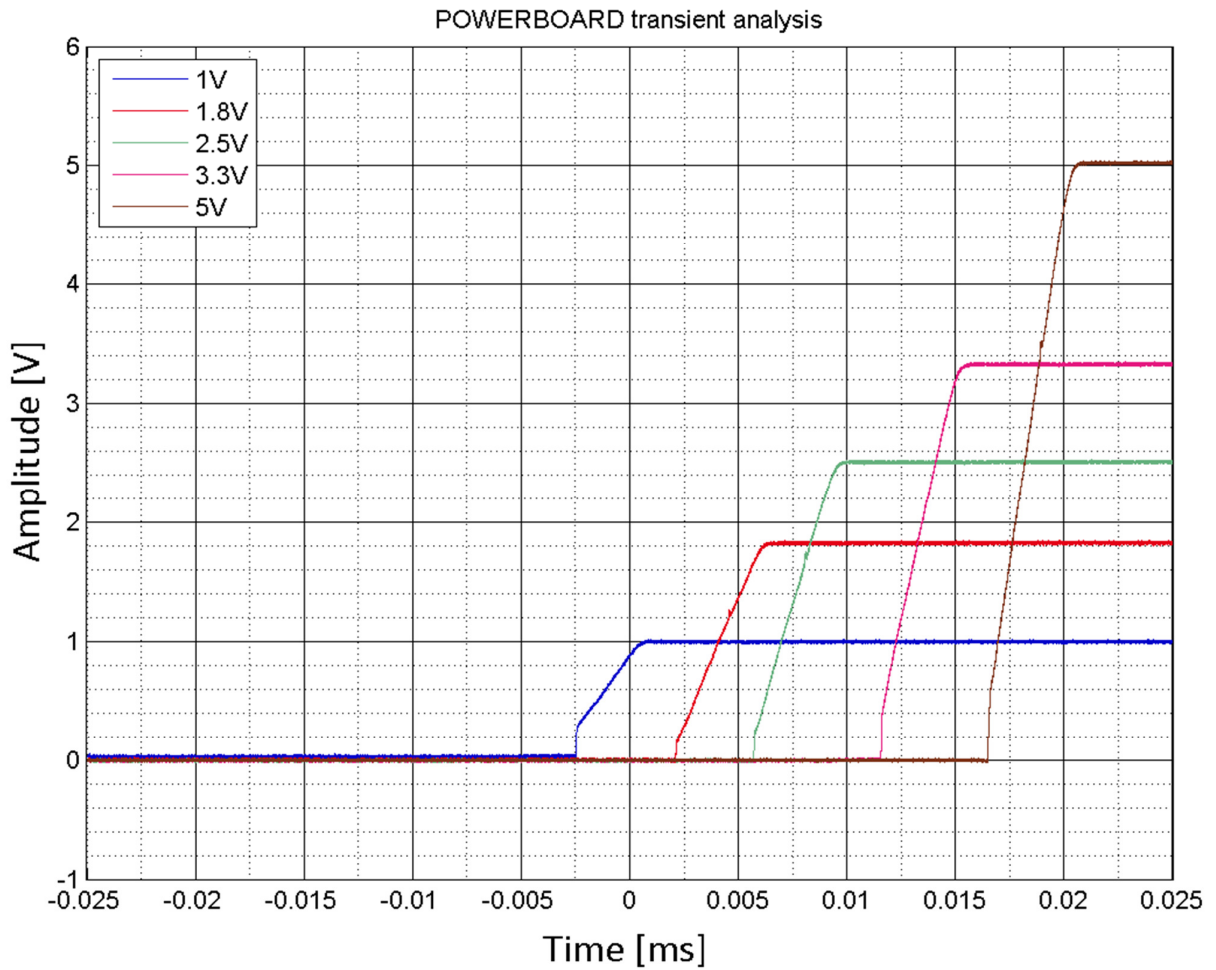


Fig 14: Power up sequence. The picture corresponds to an oscilloscope capture. The oscilloscope trigger, set to 0.9 V, fixes the time reference.

when the input value drops below 9.5 V. In this way, fluctuations in the Power Board regulators are avoided at the start point of the input voltage.

#### **4 Photomultiplier Base**

The PMT base board<sup>21</sup> (see Figure 15) takes care of both the generation of the HV supplied to the PMT and the digitization of the PMT signal. Before being digitized, the PMT signal is amplified by a pre-amplifier built in the PMT base. One of the main components of the PMT base is a comparator, which provides a logical high signal when the PMT output is over the comparator threshold -set through I<sup>2</sup>C-. The duration of the primary signal (ToT) provided by the PMT bases is accurately measured by the CLB TDCs. Apart from the logical signal, the PMT base outputs also the amplified analogue PMT signal, which is only used for testing. The 31 PMT base boards are connected to the SCB by flexible PCB. The HV, which is remotely configurable through I<sup>2</sup>C, is independently generated in each PMT base. This allows for tuning the gain of individual PMTs in order to equalize cross-PMT photon response. The HV value can be adjusted remotely, from -800 to -1400 V. Figure 16 shows a diagram of the PMT base board with its main components.

##### *4.1 Photomultiplier Base ASICs*

In order to reduce the space occupied by the PMT base, as well as its cost and power consumption, two Application Specific Integrated Circuits (ASICs) have been developed.<sup>22</sup> As the DOM is tightly packed with the 31 PMTs and the electronics, compactification is crucial. The first ASIC is the so-called PROMiS ASIC, which performs the readout of the PMT signals and has two different parts, one digital and one analog. The second chip is the CoCo ASIC, which controls the Cockroft-Walton HV power supply providing a gain of  $10^6$ . The main characteristics of both ASICs are listed



Fig 15: The PMT base board mounted on a 3-inch PMT.

Table 2: Specifications of the PROMiS chip.

Time resolution (for a single photon, photomultiplier + electronics)	< 2ns
Two-hit time separation	$\geq 25$ ns
Power consumption	35 mW
Supply voltage, Technology	3.3 V, 0.35 $\mu$ m CMOS AMS
Comparator Threshold Adjustment	8 bits (0.8 V - 2.4 V)
HV feedback control	8 bits (0.8 V - 2.4 V)
Slow-Control Communication, Digital and Analog Output	I <sup>2</sup> C, LVDS and Analog buffer respectively

in Tables 2 and 3.

#### 4.1.1 PROMiS Analog block

The analog section of the PROMiS ASIC includes: a pre-amplifier, which can increase the amplitude signal of the PMT; a two-stage charge amplifier biased at 1 V (feedback:  $R_f = 15$  k $\Omega$ ,  $C_f = 300$

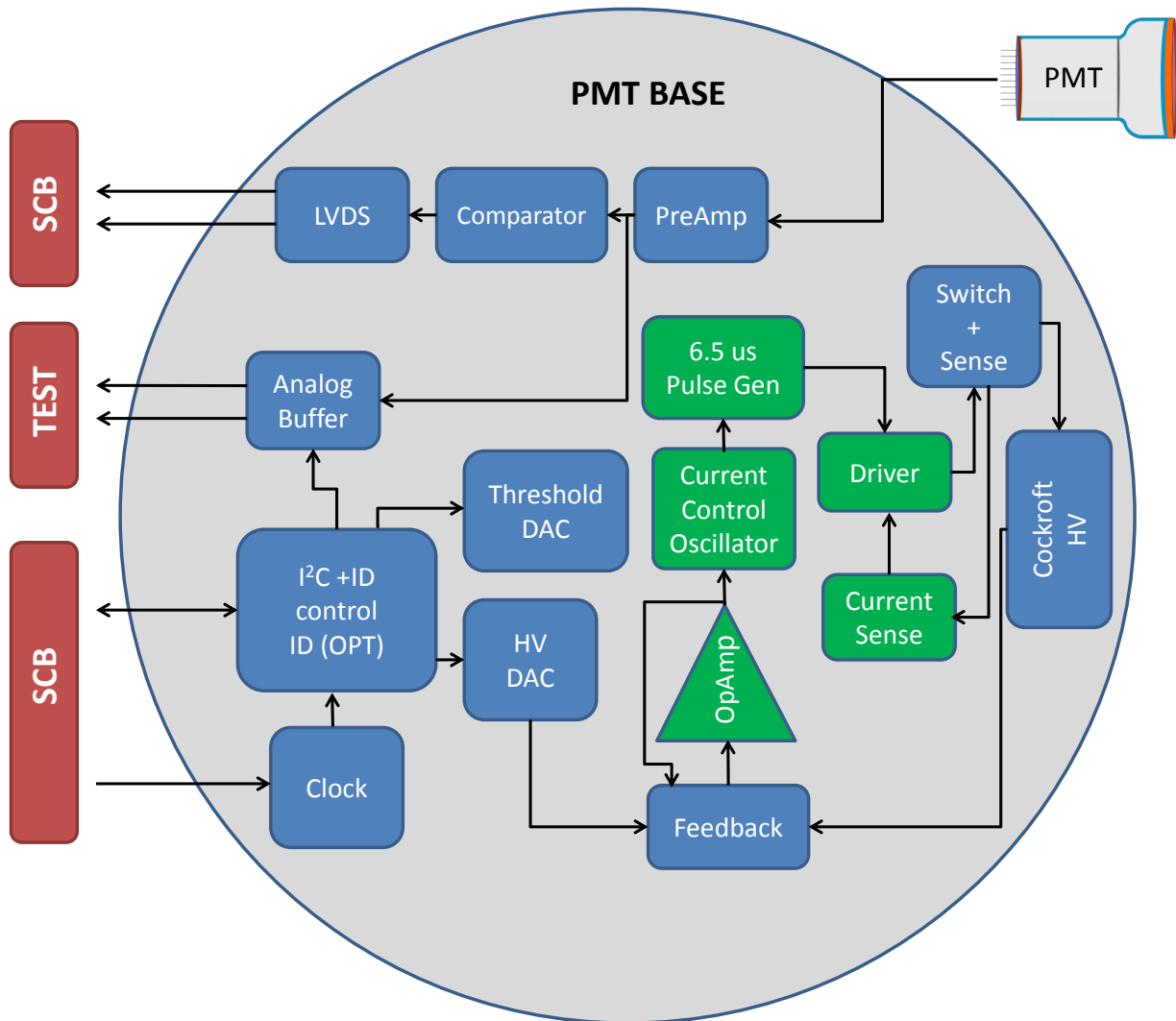


Fig 16: Block diagram of the PMT base.

Table 3: Specifications of the CoCo chip.

Pulse output frequency	< 50 kHz (max.)
Pulse width	< 6.5 $\mu$ s (max.)
Power consumption	< 1 mW
Supply voltage, Technology	3.3 V, 0.35 $\mu$ m CMOS AMS
Current sense	100 mV over 1.5 $\Omega$
Operational amplifier reference (internal)	1.2 V

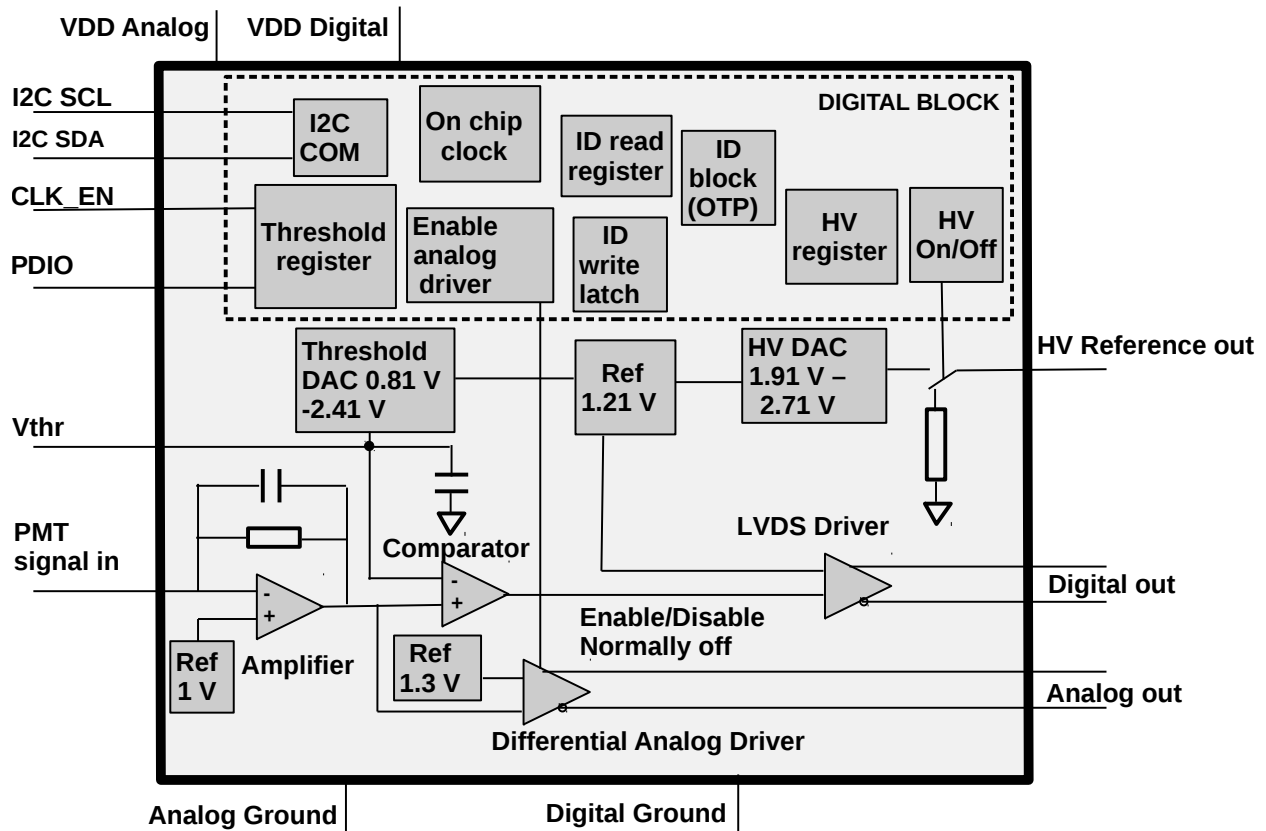


Fig 17: Diagram of the PROMiS chip.

fF); and a discriminator which compares the input signal with a predefined threshold level configured by I<sup>2</sup>C. The PROMiS ASIC generates the LVDS signal. The signal is transmitted via the SCB to the CLB where it is digitized by the corresponding TDC. The LVDS driver, with common mode feedback, feeds the 100 Ω kapton transmission line. The 1.2 V reference voltage is produced by the band gap. From this reference voltage, all the remaining voltages and currents are generated. Figure 17 shows the block diagram of the ASIC.

#### 4.1.2 PROMiS Digital block

The digital block of the PROMiS ASIC includes a clock generator that produces a 10 MHz clock signal with possible fluctuations due to temperature and voltage up to 30 %. The clock accuracy is



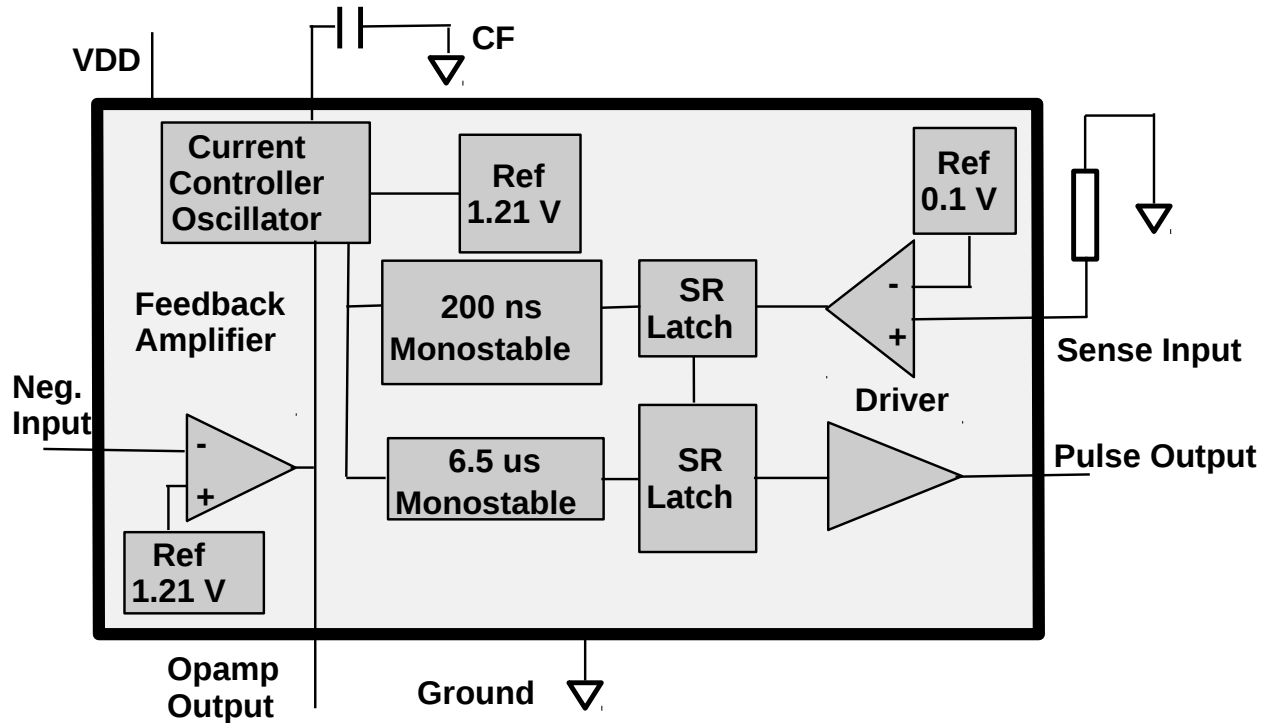


Fig 18: Block Diagram of the CoCo chip.

not critical as it is used by I<sup>2</sup>C interface, whose bus operates at 250 kHz. The PROMiS ASIC also includes an I<sup>2</sup>C slave and One Time Programmable (OTP) memory block. In Figure 17 the block diagram of the PROMiS ASIC, including its digital part, is shown. In order to save power, it is possible to shut off the clock via an enable/disable signal. The ASIC also provides the possibility to test the analog chain via I<sup>2</sup>C as well as to switch on and off the HV circuit.

#### 4.1.3 CoCo - Cockroft Walton multiplier feedback control ASIC

The CoCo ASIC (see block diagram in Figure 18) controls the autotransformer of the PMT base. The autotransformer, which has a ratio of 1:12, couples the 3.3 V power supply provided by the SCB to the Cockroft Walton (CW) multiplier circuit. The CW multiplier circuit generates the stable HV needed by the PMT, whose gain has a linear response to the HV. The ASIC receives feedback from the CW multiplier circuit in order to accurately control the HV. The control is performed by a

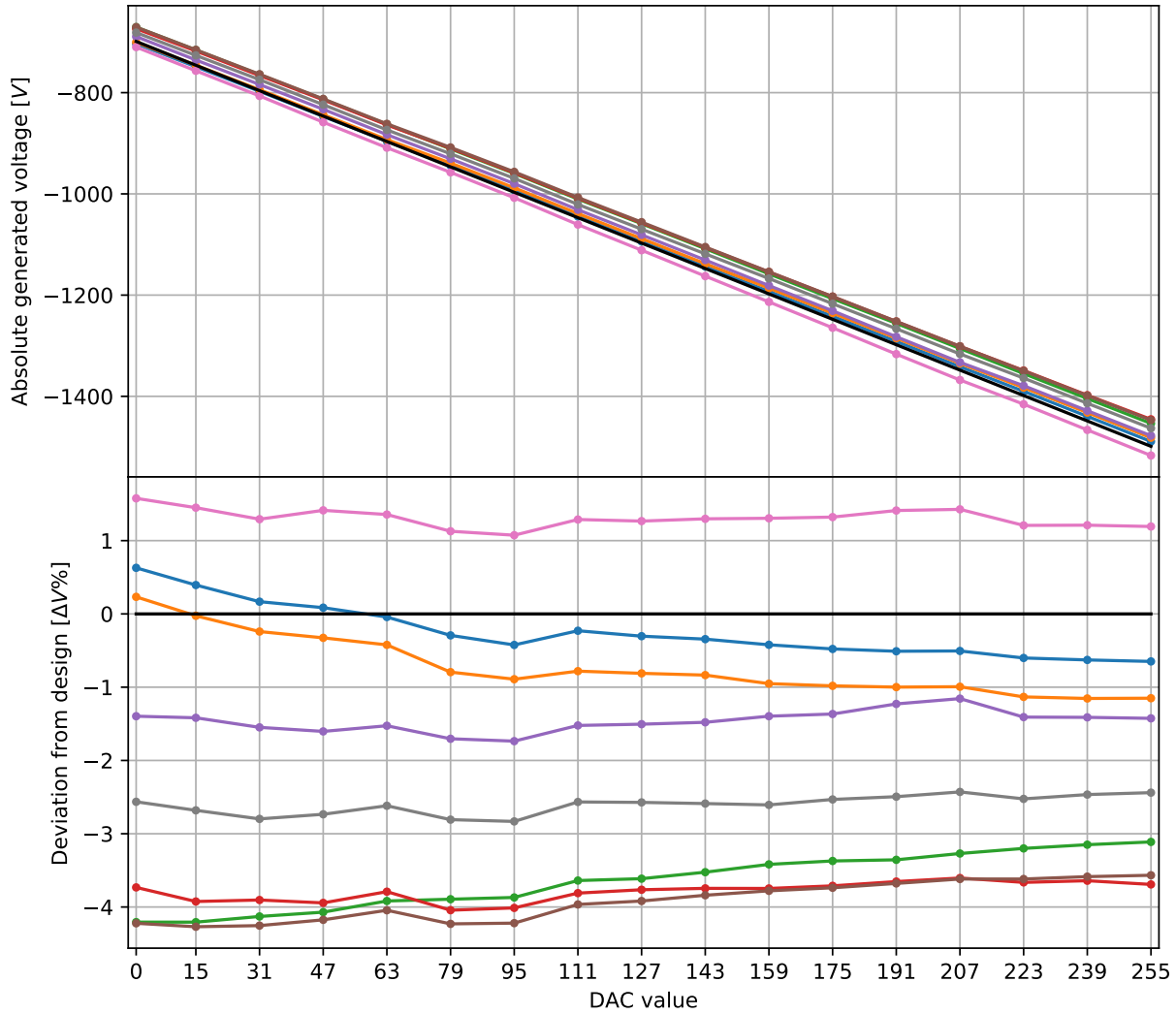


Fig 19: HV produced by a sample of PMT Bases against set PROMiS DAC value. The top plot shows the absolute voltage for eight selected bases, while bottom plot shows the relative deviation from design voltage, where  $\Delta V\% = (V_{DAC} - V_{design}) / V_{DAC} \times 100$ .

series of pulses to the switch that is managing the autotransformer. The characteristic pulse width is  $6.5 \mu s$  and its frequency, which determines the HV, changes according to the HV feedback. The HV feedback voltage is used for charging (or discharging) a capacitor. The value of the capacitor, loaded by the current of the HV feedback, sets the frequency. The triangular wave created by the charge and discharge of the capacitor is also used for generating internal clocks. Another function of the HV feedback is to avoid the autotransformer saturation in case of short circuit.

The relation between the PMT DAC value and the actual produced HV is shown in Figure 19. The relation between the DAC value and the output voltage can be derived from the PMT base HV circuit and is given by

$$V_{HV} = -F(V_{min} - V_{ref} + D \frac{V_{max} - V_{min}}{255}) + V_{ref} \quad (1)$$

where  $D$  is the DAC value (0-255),  $V_{ref}$  is the reference voltage generated by the Cockroft Walton multiplier feedback control ASIC (1.21 V),  $V_{min}$  and  $V_{max}$  are the minimum and maximum output voltages of the DAC (1.91 V and 2.71 V respectively) and  $F$  is the feedback path voltage divider factor, which has been set to 1000.  $V_{HV}$  is the HV generated by the circuit. From this, it follows a range variation of the design output between  $-698.8$  V and  $-1498.8$  V for DAC values 0 and 255 respectively. The observed variation among a sample of PMT bases in Figure 19 is due to resistor tolerances present in the feedback loop, which total to a maximum of  $\pm 6\%$ . The nonlinearity and general offset with respect to the design voltage in the plot is due to the inherent error of the measurement method.

## 5 The Signal Collection Board

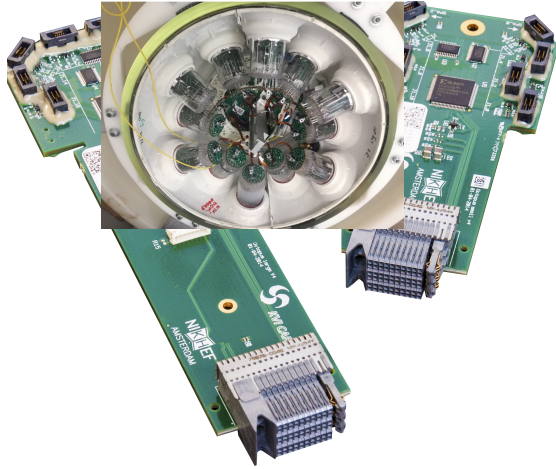
The PMT base generated LVDS signals are collected on a hub board, called the SCB. The main function of the SCB is to transfer the signals from the PMT base to the TDCs embedded in the CLB. The SCB also transfers the I<sup>2</sup>C command signals from the CLB to the PMT bases, in order to monitor and control the PMTs. Each DOM comprises two SCBs, one large and one small (Figure 20a). Figure 20b shows one SCB connected to the PMT bases in half a DOM. The architecture of the SCB consists of the following parts:

- Backplane connector to the CLB.
- Xilinx Coolrunner Complex Programmable Logic Device (CPLD).
- I<sup>2</sup>C multiplexer.
- Current limit switches.
- PMT channels: 19 in the large SCB and 12 in the small SCB.
- One piezo connector (only in the large SCB).

LVDS signaling, as used between the PMT base and the CLB, is not susceptible to cross-talk due to the fact that the two signal lines of the LVDS are electrically tightly coupled with matched impedance throughout the complete route from the PMT base to the CLB. The signal that can be coupled into the LVDS line will be coupled into both signal lines at the same time. Because of this, the distortion becomes common mode and will not affect the signal integrity. For each PMT, a resettable fuse IC, integrated on the SCB, protects individual PMTs and the CLB from short circuit or excessive current draw. For control and monitoring of the SCB, a CPLD, accessible through I<sup>2</sup>C, has been added. The CPLD allows for reading and resetting the current sensors and disabling the PMT base digital clock to eliminate possible interferences from this clock on the PMT signals. The acoustic piezo sensor is also connected to the CLB via the large SCB. As in the case of the PMTs, the SCB supplies the piezo with the needed voltage and transfers the acquired data from the piezo sensor to the CLB. The piezo does not feature a control interface.

The large SCB has 19 equal channels (see Figure 21). The LVDS signals and the 5 V needed to supply the acoustic piezo sensor are connected from the backplane connector to the piezo connector.

The 5 V power is not measured and cannot be switched by the SCB. The small SCB has 12 PMT



(a) The two SCB of the DOM.

(b) An SCB inserted in the DOM.

Fig 20: Signal Collector Boards (SCB).

channels and three spare channels.

## 6 DOM Power budget

The power consumption breakdown of the most consuming DOM electronics boards is shown in Table 4. The component of the DOM with the highest power consumption is the CLB. Inside the CLB, the FPGA and the SFP are the main power consumers, followed by the clock conditioner and the Nanobeacon. The Nanobeacon is only operated when a calibration run is performed, typically a few minutes once a week.

The SCB consumption is negligible and the 31 PMT bases add up to a total of 1 W. The Power Board, mainly because of the DC/DC converter losses, accounts for 10.2% of the total DOM power consumption. In total, the power consumption of the DOM is around 7 W when fully operational. Keeping low the power drain is important both for keeping the overall consumption of the detector low and minimizing the heat production.

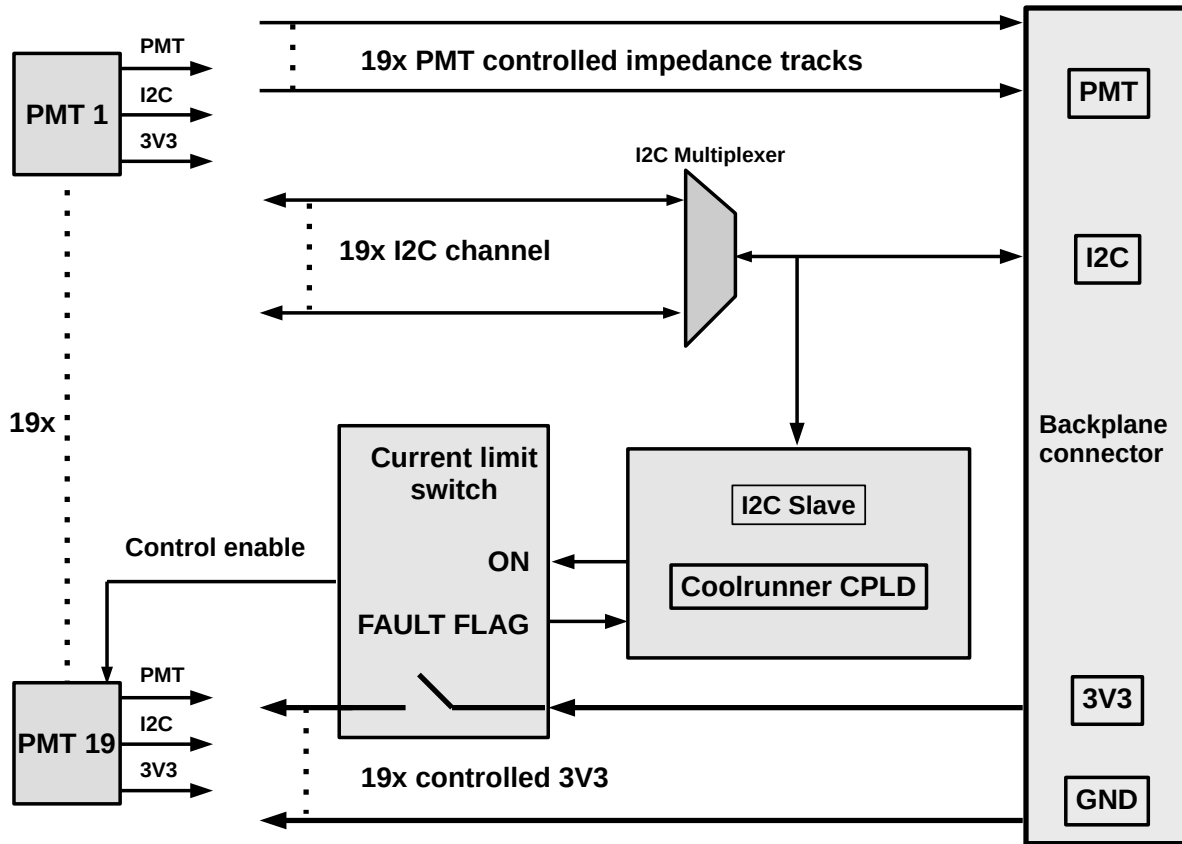


Fig 21: Block diagram of the 19 PMT channel interface of the large SCB. The small SCB is analogous with only 12 channels.

Table 4: DOM power budget.

Power budget		
Board	Sub-component	Power (W)
Power Board		0.72
Central Logic Board		4.45
	<i>FPGA</i>	2.25
	<i>SFP</i>	1.50
	<i>Clock conditioner</i>	0.50
	<i>Tilt and compass</i>	0.20
Small SCB		0.02
Large SCB		0.02
PMT 31×		1.05
Digital Piezo		0.50
Total Budget		6.76

Table 5: FIT and MTTF of the DOM electronics boards of KM3NeT.

Product	FIT	MTTF(years)
PMT Base	1218	94
Large SCB	157	727
Small SCB	156	731
Power Board	1424	80
CLB	417	273

## 7 Reliability

Maintenance of DU operated in deep seawater is difficult. In order to quantify the reliability of the electronics boards used in the detector, the FIDES<sup>23</sup> method is used. The FIDES methodology provides two main engineering tools. The first one consists of a handbook for predicting the reliability of the electronic boards analysed. The second one is a guide to estimate the impact of the design and manufacturing processes on the reliability of the produced boards. FIDES provides a spreadsheet tool to calculate the Failure In Time (FIT) and the Mean Time To Failure (MTTF) of an electronics board. Given a board, each of its components is assigned a FIT, which is either provided by the manufacturer or obtained from the FIDES handbook. The final FIT of a board is the sum of the FITs of each single component and estimates the failure rate per  $10^9$  hours. Once the FIT is obtained, it is possible to calculate the probability of failure in a given time as  $F(t) = 1 - R(t)$ , being  $R(t)$  the probability of a system to be still operational over a time period  $t$ .  $R(t) = e^{-\lambda t}$ ,  $\lambda$  being the board FIT value and  $t$  the time period duration in hours.

The results obtained for the DOM electronics boards are presented in Table 5. To fully quantify the reliability of the boards, it is necessary to evaluate each subsystem included in order to exclude, from the total FIT, those subsystems that are not critical or do not affect the overall performance of the detector in case of failure. The evaluation is called the Failure Mode, Effects, and Criticality Analysis (FMECA). In the case of the Power Board FMECA analysis has shown that the failure

of the Nanobeacon and piezo power supplies has no impact in the overall physics performances of the KM3NeT detector, because there is enough redundancy. The results obtained by the FIDES method show that the electronics boards in the DOM comply with the quality levels required by the KM3NeT Collaboration.<sup>25</sup>

## **8 Conclusions**

In this paper, the electronics front-end and readout system of the KM3NeT telescopes has been presented. The main electronics boards inside the optical modules - the Central Logic Board, the Power Board, the PMT bases and the Signal Collection Boards - have been described in detail, including a description of the readout architecture of the front-end electronics. A challenging requirement of the readout system is the 1 ns accuracy of the synchronization of the clocks inside the individual optical modules deployed in a water volume of about one cubic kilometer scale. Additional challenge is the power budget of maximal 7 W, including the HV of the 31 3-inch PMTs. The full chain of the readout electronics has been successfully qualified in situ during a data taking period from May 2014 to July 2015 at a depth of about 3500 m. The qualification has shown that a sustainable synchronization of 1 ns accuracy between the clocks in the individual optical modules has been achieved. Currently, the first deployed DUs, using the first batch of mass-produced DOM electronics, have been taking data successfully, thus demonstrating the reliability of the KM3NeT front-end and readout electronics system.



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