

Article

Analysis, Modeling, and Control of Half-Bridge Current-Source Converter for Energy Management of Supercapacitor Modules in Traction Applications

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Abstract: In this work, an in-depth investigation was performed on the properties of the half-bridge current-source (HBCS) bidirectional direct current (DC)-to-DC converter, used to interface two DC-link voltage sources with a high-voltage-rating mismatch. The intended implementation is particularly suitable for the interfacing of a supercapacitor (SC) module and a battery stack in a hybrid storage system (HSS) for automotive applications. It is demonstrated that the use of a synchronous rectification (SR) modulation scheme benefits both the power-stage performance (in terms of efficiency and reliability) and the control-stage performance (in terms of simplicity and versatility). Furthermore, an average model of the converter, valid for every operating condition, is derived and utilized as a tool for the design of the control system. This model includes the effects of parasitic elements (mainly the leakage inductance of the transformer) and of the converter snubbers. A 3 kW prototype of the converter was used for experimental validation of the converter modeling, design, and performance. Finally, a discussion on the control strategy of the converter operation is included.

Keywords: hybrid storage systems; power electronic converters; half-bridge current-source converters; supercapacitors

1. Introduction

Among electrical energy storage passive devices, Supercapacitors (SC) stand out as one of the preferred solutions when very high power densities and long life cycles are required. These features also are used in Hybrid Storage Systems (HSS), where SC can be combined with other distinct storage devices, such as electrochemical batteries or fuel cells [1–19]. In these hybrid systems, SC usually operate as power sources, as they provide the required peak power commanded by the load. In turn, the combined device (e.g., the electrochemical battery) work as an energy source, providing the long-term energy required for the given operating conditions, such as islanding operation or back-up energy support after a fault ride-through sequence, etc.

The integration of SC into HSS has been covered extensively in the current state-of-the-art, by analyzing the modeling and operation of power electronic topologies, by proposing control algorithms and methods, and by investigating hierarchical energy management systems [20–27]. Although being the simplest and most inexpensive scheme, the direct connection between the storage systems prevents to fully exploit the high charging and discharging instant power ratings of SCs. This scheme also prevents a tight control on the independent power flows shared among the energy storage devices [28,29]. Therefore, practically every implemented solution found in the technical literature

includes a bidirectional direct current (DC)-to-DC converter. These solutions can be categorized into three different classes: a series connection of the storage devices [6,7], a cascaded connection of the storage subsystems [8,9], and finally a parallel configuration of the storage elements [10–12]. From a detailed analysis of the technical literature, the parallel configuration, depicted in Figure 1, outstands as the most practical solution that allows a full control of the power flow sharing scheme required for the application, as well as a complete SC voltage-range utilization, despite that in this case the bidirectional converter needs to be rated for the peak value of the required power [13,14].

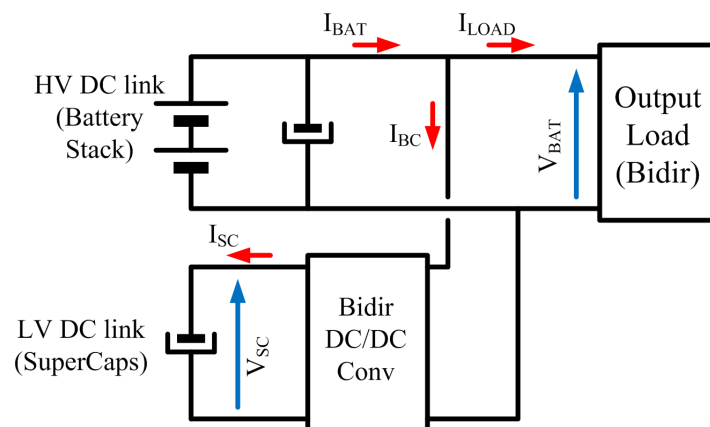


Figure 1. Parallel configuration for interfacing supercapacitors (SCs) with primary energy source (battery stack).

The bidirectional boost converter is formed by the typical connection present in a single phase leg of an inverter. It has two transistors, a series inductor connected between the mid-point of the transistors and the output, plus two capacitors intended to filter the input and the output of the converter. This scheme is generally adopted as the simplest and best-known solution. With this configuration, the peak power ratings required by most applications can be ensured by an assembly of few SC connected in series. This structure is also beneficial in terms of balancing the voltage at each SC module in the assembly. As a consequence, the SC side voltage ratings of the converter are usually much smaller than the voltage levels found at the DC-link. In addition, upon transient variations, the SC side voltage must allow variations from 80 to 20% of the SC ratings, in order to use efficiently the stored energy at the device. On the other side, the voltage at the DC-link may remain almost constant, as to optimize the full system design and operation. Hence, the range of the voltage gain between the input and the output of the bidirectional converter can typically surpass ratios of 1 to 10 and above, depending on the application.

Therefore, the boost converter is no longer a suitable solution, and so alternative topologies that allow for a high voltage gain need to be analyzed. Among these options, the most widely used include the use of a High-Frequency (HF) transformer [30–38]. Studies on the simplest isolated configurations, such as the bidirectional versions of the Flyback converter, the Forward Current-Source converter, the Push-Pull Current-Source converter, and the Half-Bridge Current-Source (HBCS) converter have been carried out [33–35]. These comparative analyses were carried out on the basis of the number of components, the switch stresses at the converters, and other figures of merit such as the utilization factor of the magnetic elements. This comparison shows how the bidirectional HBCS DC-to-DC converter is most suitable in low to medium power applications, for structures that directly interface the storage devices. Thus, the HBCS topology is of interest in HSS with storage devices arranged as shown in Figure 1 with the battery directly forming the DC bus at the converter. This is particularly interesting in traction applications, for which the weight and size of the full system are major concerns, and variable DC-link systems are considered as a suitable option [28,29].

When a given power profile is demanded by the load, the SC converter must react very quickly, in order to prevent the battery from providing the transient power. Given the current-source behavior of the low-voltage side of the HBCS converter, and provided that a tight, fast current control is implemented by generating the adequate SC current reference, the power delivered by this converter can successfully protect the battery from delivering fast, high power peaks, thus enhancing the performance and increasing the reliability of the full system. Other works have investigated the potential use of power converters for interfacing both the battery and the SC module, leading to more complex topologies and control methods [20,24,27,39].

The HBCS topology was introduced in an application to HSS in [11], but the power ratings of the laboratory demonstrator was only 100 W. Later, a 3 kW setup was reported in [35], being able to operate in open-loop, steady-state, both charging and discharging operation modes. A measured efficiency beyond 90% was then reported for the full range of operation. The authors in [35] analyzed the static gain of the HBCS converter, using conventional switching patterns. Furthermore, they considered neither the modeling nor the control stage for closed-loop operation of the converter. On the other hand, the authors of [40,41] showed preliminary research conducted to unify the transfer function of the converter acting in a bidirectional operation scheme, as well as the dynamic behavior.

The present work investigates more in depth the performance of the HBCS converter in vehicle applications. Firstly, a unified control strategy of the converter, on the basis of a synchronous rectification switching pattern, is provided. By using this pattern, the converter can be controlled with a simple, unique control law valid for every operating condition. This allows the implementation of a full bidirectional SC current control, thus enabling a fast, tight power flow control in the storage system. Once this switching pattern is established and validated, the main contribution of this work is the extension of previously existing circuital models of the converter by including non-ideal effects of the parasitic elements in the transformer of the converter, as well as the dissipative effect of the losses in the system. The performance of the proposed model was validated through simulations and experiments carried out on a 3 kW laboratory prototype. The proposed model was also compared against the simplified ideal model. Finally, this work discusses the control strategy that can be implemented in the converter. A basic HBCS current loop was analyzed, designed, and implemented, with the aim to demonstrate its feasibility; finally, a discussion on the possibilities of the high-level control strategy is also included at the end of the paper.

This paper is organized as follows. Section 2 presents the conventional modulation strategy implemented in the state-of-the-art for the HBCS converter. After that, Section 3 evaluates the Synchronous Rectification (SR) scheme in the converter operation, considering both the charging and discharging modes of operation. It also demonstrates experimentally the benefits of SR operation for this topology. Section 4 further discusses the implications of SR in terms of the simplification of the control of the converter; most importantly, this section provides an averaged model of the HBCS converter, suitable to aid in the design of the control stage. Also, this model is validated through simulations. Subsequently, in Section 5 the current control algorithm is discussed and tested through simulations. This section also deals with the overall control scheme of the system. Section 6 validates the full model and the control scheme outlined in the previous sections by showing experimental results obtained with a laboratory prototype of a HBCS converter. Finally, Section 7 discusses the conclusions of the research and proposes some future developments.

2. Special Characteristics of the HBCS Converter

Figure 2 shows the HBCS converter. Because this converter is a bidirectional topology, no predefined input or output are established. For the coming discussion, the SC side is also referred to as the Low-Voltage (LV) side, signifying that this side generally has the lower of the rated voltages involved in the analysis. On the other hand, the alternate energy source (i.e., battery) and the DC-link are referred to as the High-Voltage (HV) side.

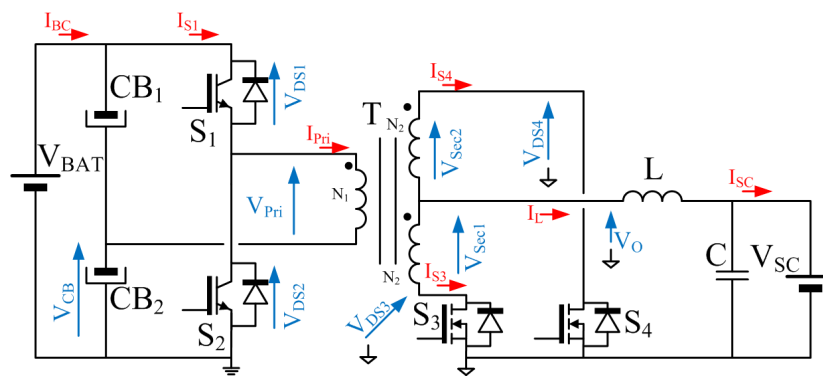


Figure 2. Layout of Half-Bridge Current-Source (HBCS) bidirectional converter. The references for the current and voltage considered for the analysis are shown.

The modulation scheme for the HBCS converter, as presented in [35], is obtained by shifting the command pulse waveforms of each switch in the primary- or secondary-side by 180° . Initially, the control parameters implemented at both charging and discharging operation modes were different. In charging mode, where the energy flows to the SC from the DC link side, switches S_3 and S_4 remain always turned off. This forces the current to flow only through the diodes of S_3 and S_4 . Figure 3 shows the main current and voltage instant waveforms of the converter for charging (a) and discharging (b) modes. The switching pattern is defined by establishing the gate-to-emitter voltages of switches S_1 to S_4 , denoted as V_{GE1} – V_{GE4} , respectively. The rest of the waveforms are consistent with the references in Figure 2. The modulation of switches S_1 and S_2 (Figure 3a) is carried out by shifting by 180° the control pulses, considering a given duty ratio, D :

$$D = \frac{T_{S1\ ON}}{T_s}, \quad (1)$$

where $T_{S1\ ON}$ is the interval when switch S_1 remains turned on and T_s is the switching period. In order to avoid a simultaneous conduction of switches S_1 and S_2 at the battery side, and given that the switching pattern requires a fixed 180° phase shift between the firing signals of V_{GE1} and V_{GE2} , D is restricted to $0 < D < 0.5$. The voltage gain between the LV and HV sides, G_{CHARGE} , is

$$G_{CHARGE} = \frac{V_{SC}}{V_{BAT}} = D \cdot \frac{N_2}{N_1}, \quad (2)$$

where N_1 and N_2 are the primary- and secondary-side number of turns of the HF transformer, respectively; V_{SC} is the voltage across the SC; and V_{BAT} is the DC-link voltage, that is, the battery voltage according to its state of charge. The magnetizing inductance of the transformer is neglected, because it is assumed that it is very high.

Figure 4 shows the current paths for the different switching modes of the converter, during the SC charging operation scheme. When switch S_1 is turned on and S_2 is turned off (Figure 4a), a positive current I_P flows through the primary side, considering the references in Figure 2. Current flows through the portion of the secondary winding connected to switch S_3 , the output filter, and the SC; thus, the anti-parallel diode of switch S_3 carries the secondary-side current. Figure 4b, in turn, shows the switching mode when both transistors S_1 and S_2 are turned off. The inductor current I_L splits equally between the two parts of the secondary winding, flowing through the anti-parallel diodes of S_3 and S_4 . Finally, Figure 4c depicts the current paths when S_2 is turned on and S_1 is turned off. This mode is similar to that shown in Figure 4a but considers the 180° phase shift between S_1 and S_2 .

During the discharging mode, the energy flows back to the DC-link from the the SC. In this case, the switches under control are S_3 and S_4 , while S_1 and S_2 are kept continuously turned off. Again, the modulation of S_3 and S_4 is implemented through a 180° shifting scheme, while the turn-on intervals

are kept equal. Figure 3b shows the key waveforms obtained for this operation mode. The independent parameter for this mode, D' , is defined as:

$$D' = \frac{T_{S3\ ON}}{T_S}, \tag{3}$$

where $T_{S3\ ON}$ is the interval when S_3 is turned on. The constraint for this parameter is now $0.5 < D' < 1$, thus forcing an overlap in the conduction of S_3 and S_4 . This overlapping is required because of the current-source behavior of the LV side of the converter. For this topology, unless at least one switch in the pair S_3 – S_4 is turned on, an abrupt interruption of the current flowing through the inductor would lead to a dangerous overvoltage across the magnetic element, that might damage the converter. For the discharging operation mode, the voltage gain can be defined as:

$$G_{DISCHARGE} = \frac{V_{BAT}}{V_{SC}} = \frac{1}{1 - D'} \frac{N_1}{N_2}. \tag{4}$$

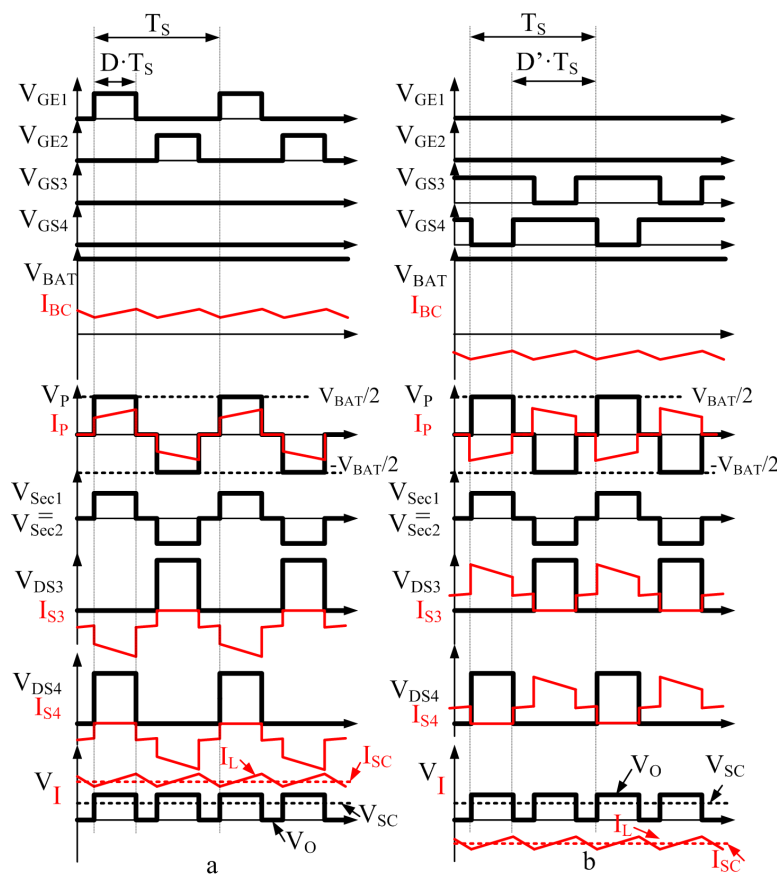


Figure 3. Main voltage (black) and current (red) waveforms of the half-bridge current-source (HBSC) for charging (a) and discharging (b) operation modes.

The switching modes for discharging the SC are represented in Figure 5. The current path when S_4 is turned off and S_3 is turned on is shown in Figure 5a. On the other hand, Figure 5b shows the current flowing through the switches when both S_3 and S_4 are turned on. Finally, it can be seen in Figure 5c how the current flows when switch S_4 is turned on and S_3 remains off. A close look at Figure 5a–c shows that the current paths are the same as those shown in Figure 4a–c, respectively, but with the directions of the currents reversed.

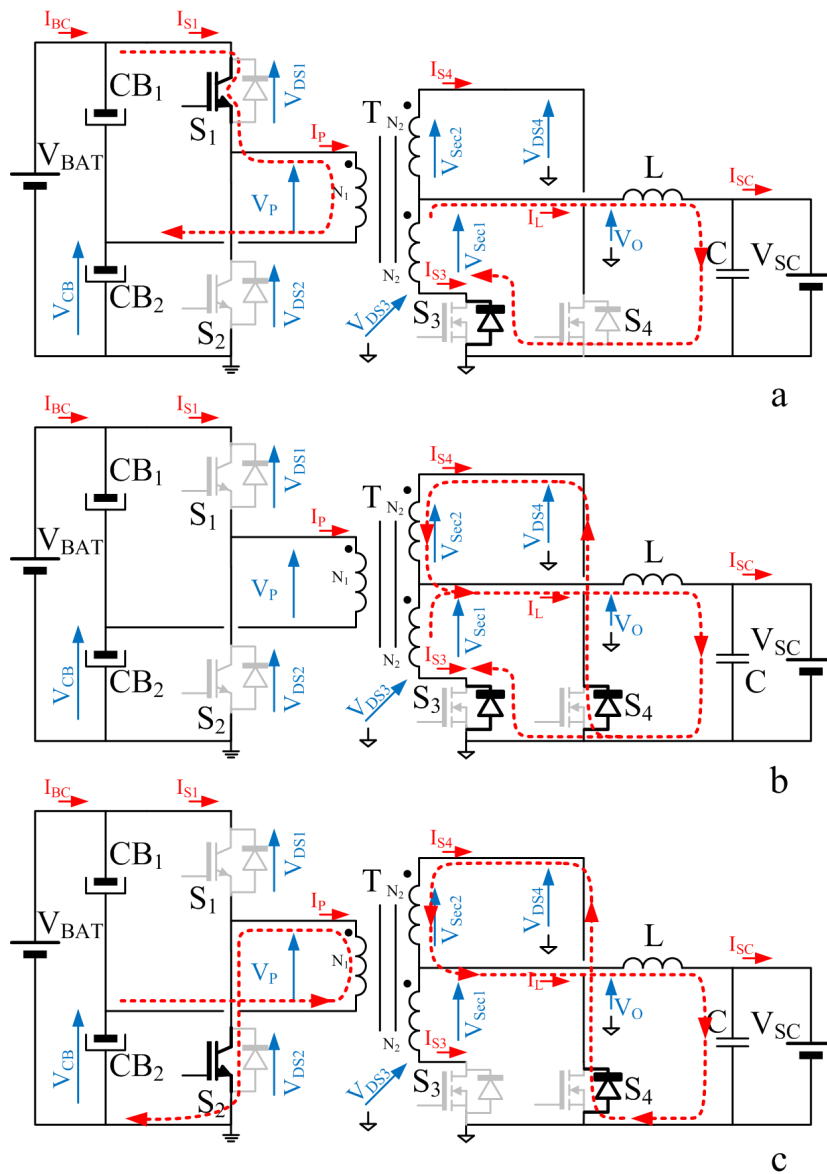


Figure 4. Switching modes of the half-bridge current-source (HBCS) converter operating during supercapacitor (SC) charging operation mode. (a) Switch S_1 on and switch S_2 off. (b) Both switches S_1 and S_2 off. (c) Switch S_1 off and switch S_2 on.

By using the control laws stated in Equations (2) and (4), both the charging and discharging control strategies can be easily designed. However, this modulation pattern requires the calculation of two independent control parameters, defined as the duty cycles of S_1 and S_3 , depending on the operation mode under consideration, given by charging and discharging modes, respectively. This approach, though, yields to some issues at the boundary between these operation modes, given that the switches that must be controlled change abruptly. Therefore, if both control schemes are implemented independently, a smooth transition between modes of operation is prevented. However, this issue is easily avoided provided that SR is implemented. This SR pattern is introduced in the next section for the HBCS converter. The benefits for the control of the converter are discussed in the forthcoming sections.

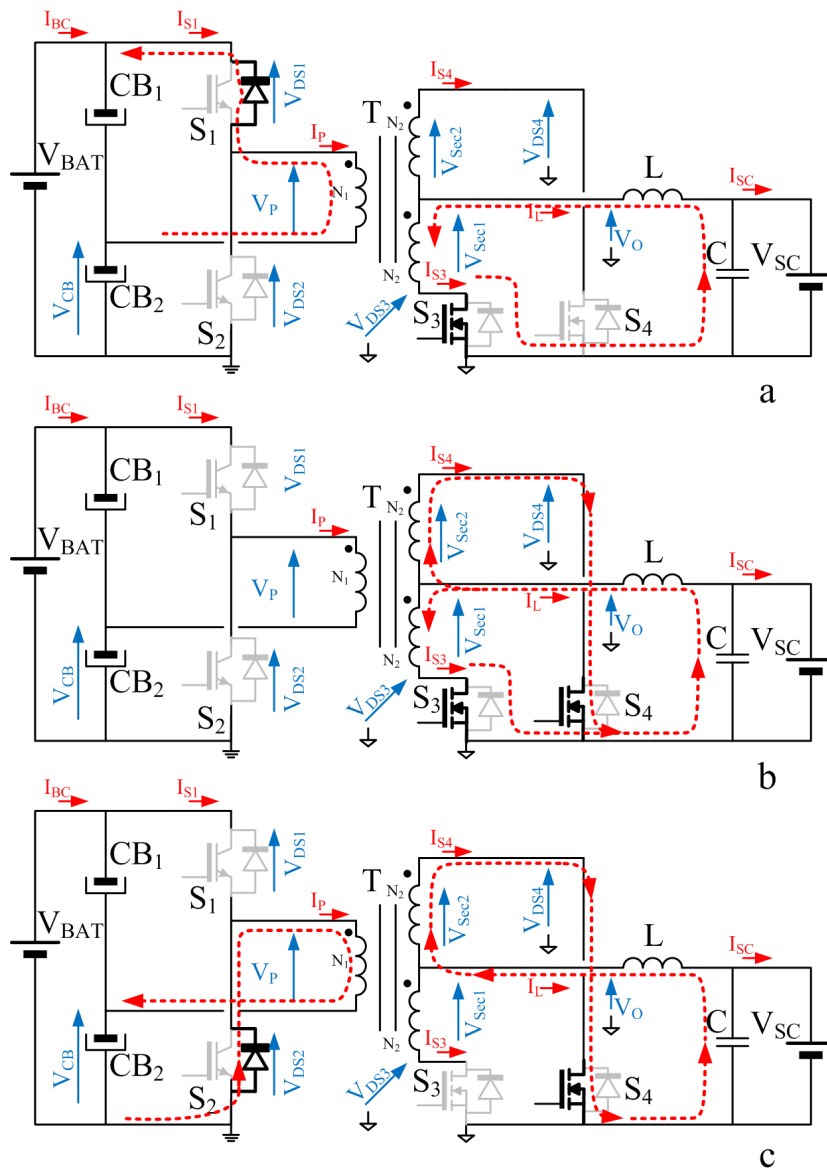


Figure 5. Switching modes of the half-bridge current-source (HBCS) converter operating during supercapacitor (SC) discharging operation mode. (a) Switch S_3 on and switch S_4 off. (b) Both switches S_3 and S_4 turned on. (c) Switch S_3 off and switch S_4 on.

3. Synchronous Rectification in the HBCS Converter

SR is a common strategy that establishes a given switching pattern for the switches in power electronic converters. Upon several conditions, it can decrease conduction losses, thus boosting the efficiency of the converter. This technique has already been described in the technical literature related with hybrid systems applications [36–38]. This technique takes advantage of the low on-state voltage of a MOSFET transistor, when compared to the forward voltage of its body diode. Given the equivalent series circuit of a diode, formed by a threshold voltage, V_{TH} , and a dynamic resistor, R_{DYN} , then the conduction losses, for the diode turned on, are given by:

$$P_{C-DIODE} \propto V_{TH} \cdot I_D + R_{DYN} \cdot I_D^2. \tag{5}$$

Moreover, the conduction losses in a MOSFET can be expressed as:

$$P_{C-MOSFET} \propto R_{DS\ ON} \cdot I_D^2, \quad (6)$$

where $R_{DS\ ON}$ is the drain-to-source on-resistance of the channel. As a result of an analysis of the equivalent circuit of the switch, the current tends to flow through the path with a lower voltage drop. In the HBCS converter depicted at Figure 2, S_3 and S_4 have already been implemented as MOSFET switches, with inherent anti-parallel body diodes. As a consequence, SR can be directly applied.

In order to validate the performance of the SR switching pattern, a reference design is considered for a 3 kW HBCS converter. The main characteristics of the setup are detailed in Table 1.

Table 1. Characteristics of half-bridge current-source (HBCS) design.

Parameter	Max.	Min.
SC voltage	45 V	25 V
HV DC-link voltage	350 V	
Switching frequency	20 kHz	
SC discharge-mode duty ratio	0.75	0.55
SC charge-mode duty ratio	0.45	0.25
Output power (SC disch. mode)	3 kW	1.6 kW
Output power (SC chrg mode)	3 kW	1.6 kW
SC current	65 A	−65 A
Transformer turns ratio	3.5:1:1	

Figure 6 shows a graphical representation of the expression of the drain-to-source voltage, V_{DS} , as well as the power dissipated through conduction losses, P_{COND} , both as a function of the current flowing through the drain of the transistor, I_D . These power and voltage values are given for both the transistor and diode elementary devices. For this study, the actual values given in the datasheets of the real components selected, in this case the SKM121AR power MOSFET modules from SEMIKRON, have been used. The dotted black line shows the voltage at the MOSFET as a function of the current I_D . This line shows the typical load line of a resistive component. As a consequence, the power dissipated as a function of the I_D in the MOSFET is given by a quadratic relationship expressed in Equation (6), drawn as a filled black line in Figure 6. The voltage drop across the diode, in turn, is shown as an horizontal dotted gray line. The power dissipated in the diode, as a function of the current I_D , therefore follows a linear behavior, represented by a filled gray line. As can be seen, both power characteristics, those of the MOSFET and the diode, have an intersection point labeled as I_{LIM} . For I_D current values below I_{LIM} , the MOSFET losses are smaller than the diode losses, and therefore the synchronous rectification implies higher efficiencies compared to the standard switching pattern. For the real values of the devices under consideration, I_{LIM} is equal to

$$I_{LIM} = 70 \text{ A}. \quad (7)$$

From Table 1, the maximum value of the SC current, which is also the maximum currents allowed to flow through S_3 and S_4 , has a value of 65 A. Therefore, and considering Figure 6, the conduction losses at the secondary side of the converter operating in charging mode will be decreased, provided that SR is implemented as the switching pattern. As a consequence, the whole efficiency of the converter will increase. It must be notice that in this case the switches at the DC link side have been implemented by means of IGBT switches. Therefore, and given that for this switch technology the current flowing from the emitter to the collector can only flow through the anti-parallel diode (and not through the transistor itself, as in the previous case), the use of a SR scheme during the SC discharge mode will not mean a decrease in the converter losses. In any case, a critical point for this analysis is to state that SR can still be used in this mode of operation without affecting the performance of the converter. This issue will be discussed in Section 4.

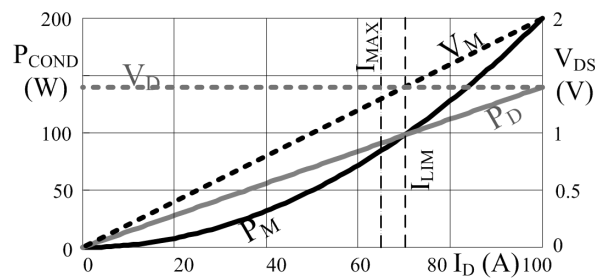


Figure 6. Drain-to-source voltage (V_{DS} , dashed lines) and conduction losses (P_{COND} , filled lines) for both diode conduction (gray) and MOSFET conduction (black), for the half-bridge current-source (HBCS) prototype.

A first set of experiments was carried to validate the feasibility of the SR switching pattern implementation in the HBCS converter. For this validation, and in order to register the steady-state operation of the converter, the setup was configured to supply a resistive load from a voltage source. The values of measured efficiencies in charging operation mode, for the standard and the SR schemes, are given in Figure 7. Three different resistive loads (1.0, 0.67 and 0.5 Ω , respectively), were used in the measurements. The voltage at the power source was kept constant at 300 V_{DC} . Due some practical constraints at the experimental setup, the voltage levels at the LV side were limited to three values, $V_{SC} = 25$ V, $V_{SC} = 30$ V, and $V_{SC} = 34$ V. From the plots at Figure 7, it can be deduced an increase in the converter efficiency in all cases.

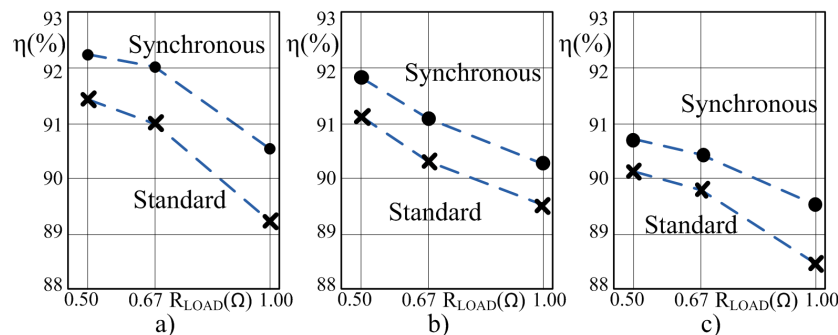


Figure 7. Graphical relationship of experimental efficiency measurements between standard and synchronous rectification switching schemes, as a function of load resistance. (a) $V_{SC} = 25$ V. (b) $V_{SC} = 30$ V. (c) $V_{SC} = 34$ V.

4. Full Model of the Converter under Synchronous Rectification

As a result of the use of SR, the HV and LV side switches, S_1 – S_2 and S_3 – S_4 , present complementary control signals. In particular, the gating signals of S_3 and S_4 , are the complementary signals of S_1 and S_2 , respectively, as it was sketched in the waveforms shown in Figure 3a,b. This condition defines an obvious relationship upon SR scheme between the values of the parameter D of switches S_1 – S_2 and D' of switches S_3 – S_4 . This can be expressed as

$$D = 1 - D' \quad . \quad (8)$$

As a result, a single, independent control parameter can be established for every operation mode in the converter, given that the remaining parameters are calculated automatically. This parameter is the duty ratio of switch S_1 , noted by D . Equation (8), together with Equations (2) and (4), determines

a unique equation to define the voltage gain of the topology, G_{HBSC} . This equation is, as mentioned, true for every mode of operation and charging condition:

$$G_{HBSC} = \frac{V_{SC}}{V_{BAT}} = D \cdot \frac{N_2}{N_1}. \quad (9)$$

Thus, with SR, the control law turns out to be unique, regardless of the mode of operation.

Once the switching strategy is defined, an accurate model of the converter needs to be established in order to properly design the control system. The simplest averaged large-signal model for the converter is shown in Figure 8. This basic model has already been explored in the definition and implementation of a control strategy for the topology [40]. The basic model has been implemented considering ideal switching and reactive devices. For the average circuit, the transistors and the HF transformer have been modeled by the two dependent sources within the dashed frames at Figure 8. The output value of these sources depend on the duty ratio D and on the turns ratio of the transformer, N_2/N_1 . Downstream from these, the second order L - C filter is present.

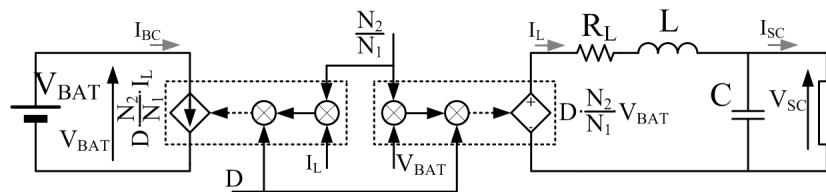


Figure 8. Large-signal averaged model based on ideal components.

In order to check this model, the performance of the circuit depicted in Figure 8 was compared with a full switching model of the HBSC converter, implemented in PSIM. In these simulations, a resistive load replaced the SCs, with the aim of having initial steady-state operation conditions. The dynamic behavior is obtained by imposing a small step in the duty ratio of the converter after reaching the steady state. In the tests shown in Figure 9, the step goes from 0.34 to 0.36. This picture shows the simulated waveforms of the output voltage (V_{SC}), input (I_{BC}) and output (I_{SC}) currents, and the inductor current (I_L), compared with their corresponding averaged values obtained from the basic model. The performance of the basic model differs significantly from the switching converter behavior. Even though the natural frequency is mainly the same, there are two effects of mismatch in the behavior of the model. Firstly, the switching system is more damped than the dynamic response given by the model. Moreover, the equilibrium values after the transient are smaller in the switching circuit.

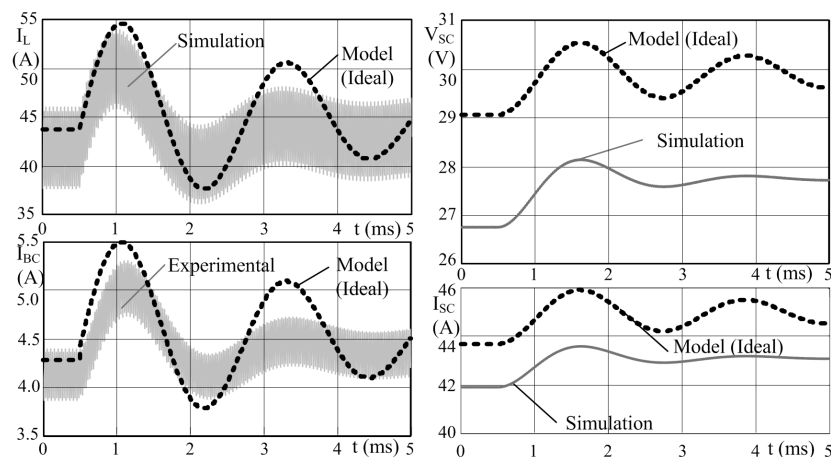


Figure 9. Simulation waveforms (gray) and averaged value of model based on ideal components (black), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}), and input current (I_{BC}).

In order to solve this disagreement between the model and the switching circuit, an improved model has been developed. This model firstly accounts for the effects of the parasitic resistors of the transformer, the R_{DS} of the transistors at the HV side, and the snubbers. These effects are jointly modeled by a series resistance, R_{loss} , which adds a dissipative term in the model that contributes to increase the damping factor. However, the most significant effect is due to the leakage inductance of the transformer, depicted in Figure 10. Some waveforms are depicted in Figure 11 to describe the contribution of this leakage inductance in the full model. For simplicity in this analysis, the overall primary side leakage inductance is obtained as the sum of the measured primary- and reflected measured secondary-side leakage inductances.

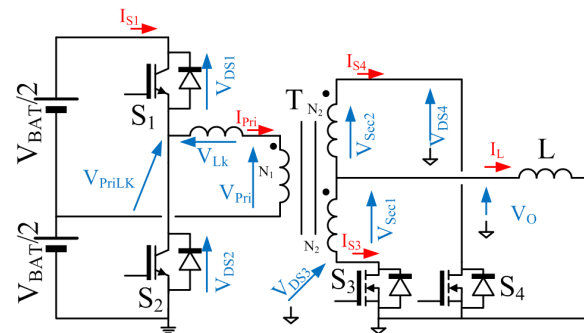


Figure 10. Half-bridge current-source (HBCS) converter equivalent circuit, including the overall leakage inductor at the primary side of the transformer.

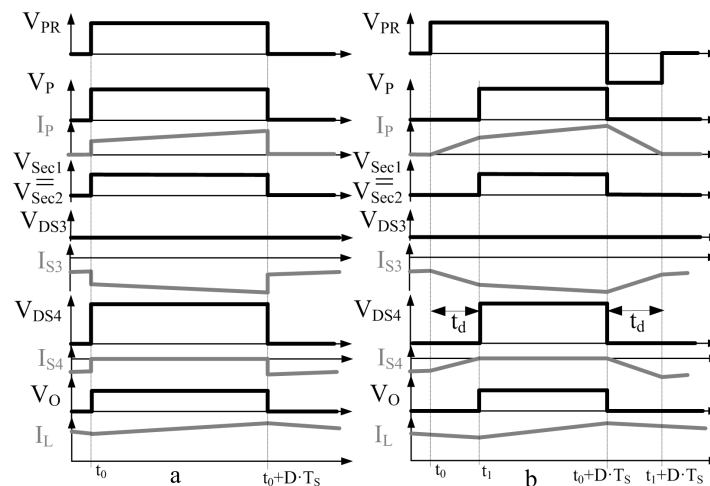


Figure 11. (a) Switching waveforms with ideal transformer. (b) Switching waveforms with overall leakage inductor at the primary side.

The waveform sequence starts when S_1 and S_2 are turned off, and thus there is no current flowing through the primary side of the transformer. In this situation, the output inductor current splits equally through the diodes at switches S_3 and S_4 . At time t_0 , S_1 is turned on, forcing the primary side voltage, V_P , to be half the voltage across the battery:

$$V_P = \frac{V_{BAT}}{2}. \tag{10}$$

The high inductance of the filter, L , causes I_L to keep flowing practically unchanged to the load. For the ideal transformer in Figure 11a, the current immediately flows through S_1 , and thus the diodes

of S_3 and S_4 are instantly turned-off. As a consequence, the secondary side voltages at the transformer instantly are equal to:

$$V_{Sec1} = V_{Sec2} = \frac{V_{BAT} N_2}{2 N_1}. \quad (11)$$

Nonetheless, for the real transformer case depicted in Figure 10, the leakage inductance prevents the secondary side current to change instantly (Figure 11b). Upon this situation current keeps flowing through the secondary sides of the transformer, S_3 and S_4 . The secondary side voltages remain null immediately after turning on S_1 , and thus the voltage at the leakage inductor equals the primary-side voltage. This issue affects the operation of the system. For instance, in charging mode, both HV-side switches, S_1 and S_2 , are in the off-state just before S_1 is turned on. It can be seen in Figures 2 and 3a that each diode at the secondary side carries half I_L , while the voltages at the primary side, V_p , and at the common node of the secondary windings, V_O , are null:

$$I_{S3} = I_{S4} = -\frac{I_L(t)}{2} = -\frac{I_L}{2}, \quad (12)$$

$$V_O = 0, \quad (13)$$

$$V_p = 0. \quad (14)$$

Equation (12) describes as well that the inductor current is considered as constant within a switching interval. When S_1 turns on at t_0 , and given that current keeps on flowing through the LV side diodes, then the voltage V_p does not vary. Instead, because V_{DS1} equals zero, the voltage at the primary side of the real transformer (i.e., considering the parasitic inductance), V_{PR} , equals half the voltage at the battery:

$$V_{PR} = \frac{V_{BAT}}{2}. \quad (15)$$

Therefore, the values of the voltage across the leakage inductor, V_{Lk} , and the current at the primary side of the transformer, I_{Lk} , can be calculated as:

$$V_{Lk} = \frac{V_{BAT}}{2}, \quad (16)$$

$$I_{Lk} = I_{PR} = \frac{1}{L_{Lk}} \frac{V_{BAT}}{2} \cdot t. \quad (17)$$

As mentioned previously, the overall leakage inductance L_{Lk} takes into account the measured leakage inductor at the primary ($L_{Lk_{pri}}$) and secondary ($L_{Lk_{sec}}$) sides of the real transformer, referred to the primary side:

$$L_{Lk} = L_{Lk_{pri}} + \frac{L_{Lk_{sec}}}{2} \left(\frac{N_1}{N_2} \right)^2. \quad (18)$$

Upon these conditions, the inductance L_{Lk} is linearly charged. The currents through S_3 and S_4 are given by:

$$I_{S3} = -\frac{I_L}{2} - \frac{I_{PR} N_1}{2 N_2}, \quad (19)$$

$$I_{S4} = -\frac{I_L}{2} + \frac{I_{PR} N_1}{2 N_2}. \quad (20)$$

At instant t_1 , I_{S4} is null, turning S_4 off, and thus from this instant the current I_L equals the current through the body diode of S_3 :

$$I_{S3} = -I_L, \tag{21}$$

$$I_{S4} = 0. \tag{22}$$

As a consequence, the dead time t_d , defined as the interval between instants t_0 and t_1 ,

$$t_d = t_1 - t_0 \tag{23}$$

is the time it takes for the current I_{S3} to reach $-I_L$ after S_1 is turned on. This condition can be expressed as:

$$\frac{-I_L}{2} - \frac{1}{2} \frac{N_1}{N_2} \frac{V_{BAT}}{2} \frac{1}{L_{Lk}} (t_1 - t_0) = -I_L(t). \tag{24}$$

The explicit expression for t_d can thus be obtained:

$$t_d = 2 \cdot \frac{N_2}{N_1} \frac{I_L(t)}{V_{BAT}} \cdot L_{Lk}. \tag{25}$$

It is important to note that t_d represents a completely different behavior in the full model when compared to the basic one. For the basic model, when switch S_1 is turned on, V_O equals to half the battery voltage, obviously referred to the secondary side. Instead, for the full model, V_O is zero during t_d just after turning S_1 on, and then reaches the same $V_{BAT}/2$ for the rest of the interval when S_1 remains turned on. This situation affects the final voltage gain at the topology, given that the effective duty ratio of the converter, D_{eff} , is actually smaller for the full model than for the basic one. This D_{eff} can be defined now as:

$$D_{eff} = \frac{D_1 \cdot T_S - t_d}{T_S}. \tag{26}$$

As it can be deduced from Equation (25), the expression of the dead time is a non-linear function of a manifold of system parameters. Hence, the resulting model that takes this t_d into account is a non-linear model. The large-signal circuitual model that considers t_d (and also R_{loss}) is shown in Figure 12. Additionally, the Equivalent Series Resistor, ESR_C , of the filter capacitor C has been included.

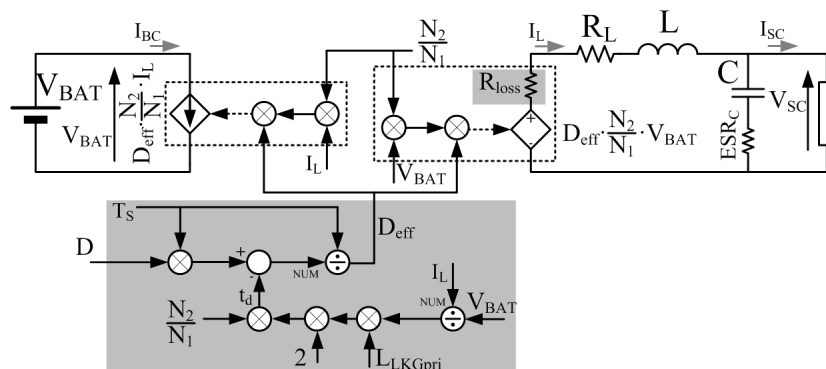


Figure 12. Full averaged large-signal model based on real components, parasitic elements, and snubbers.

The full average model has been simulated and compared with the switching circuit, in order to evaluate its performance. These simulations, shown in Figure 13, have been carried out in the same conditions that were established for the previous simulations of the basic model shown in Figure 9.

It can be seen how the new complete model tracks much more accurately the simulated waveforms at the switching model, again for a duty step from 0.34 to 0.36. Therefore it can be concluded that the dynamic behavior of the HBCS converter with the proposed SR scheme is truly represented by the obtained full model.

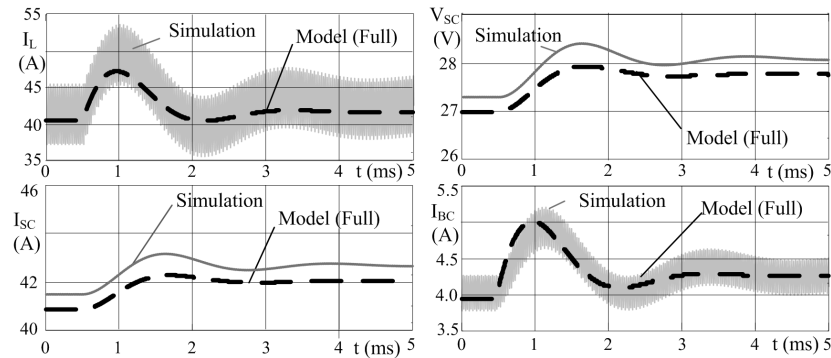


Figure 13. Simulation waveforms (gray) and averaged value of model based on the parameters of real components (black), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}) and input current (I_{BC}).

An important remark on this behavior is that this response corresponds to a second order system, as it is expected from a resistive load at the output of the L - C filter at the LV side. In the proposed application, the load is an assembly of SC. If this assembly is considered as an ideal pure capacitive load, given that the capacitance value of these devices is very large, then the output voltage would remain constant during the transient, and thus the dynamic behavior of the output voltage can be disregarded. For a more realistic approach, the SC assembly will be modeled by an equivalent circuit formed by a series resistor and the SC capacitor. Still, the SC will present a very large capacitance value, and therefore it behaves practically as a DC voltage source. Thus, the AC small signal model of the SC is given by the series resistor only, and the behavior of the full system is again corresponding to a second order system.

At this point, a small-signal model can be derived. Figure 14 shows the model that emerges after linearizing and perturbing the large signal full model, which has the following parameters:

$$R_1 = \frac{t_d}{T_S} \tag{27}$$

$$R_2 = \frac{2 \cdot D \cdot L_{LkPri}}{T_S} \left(\frac{N_2}{N_1} \right)^2 \tag{28}$$

$$K_1 = \frac{N_2}{N_1} \cdot I_L \left(1 - \frac{t_d}{T_S} \right) \tag{29}$$

$$K_2 = 2 \cdot \frac{t_d}{T_S} \cdot D \cdot \frac{N_2}{N_1} \tag{30}$$

$$K_3 = \frac{N_2}{N_1} \cdot V_{BAT} - \frac{2 \cdot I_L^2 \cdot L_{LkPri}}{T_S} \left(\frac{N_2}{N_1} \right)^2 \tag{31}$$

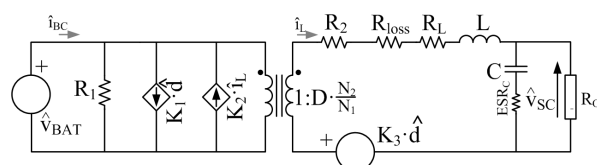


Figure 14. Full Small Signal Model of the system.

This last model finally allows the design and tuning of the control system, since the most significant dynamics of the system are taken into account. The second order behavior of the system, represented in the previous analysis, can be also derived from this model. In fact, the output voltage to duty ratio transfer function, can be calculated as:

$$\left. \frac{\hat{v}_{SC}}{\hat{d}} \right|_{\hat{v}_{BAT}=0} = \frac{K_3 \cdot R_0}{R_0 + ESR_C} \cdot \frac{1 + s \cdot C \cdot ESR_C}{\frac{R_{EQ} + R_0}{R_0 + ESR_C} + s \cdot \left[\frac{L}{R_0 + ESR_C} + C \cdot \left(R_{EQ} + \frac{R_0 \cdot ESR_C}{R_0 + ESR_C} \right) \right] + s^2 \cdot L \cdot C} \quad (32)$$

where

$$R_{EQ} = R_2 + R_{loss} + R_L \quad (33)$$

5. Proposed Control Scheme for the HBCS Converter

An adequate design of the control stage of the converter is needed in order to ensure the required power flows in the hybrid storage system under consideration [20–29]. In order to obtain the desired operating performance of the system, a High Level Control System provides the instant power references that each storage device must supply to the DC link. From this power reference, the HV current value of the HBCS converter, I_{BC}^* can be calculated. This scheme is depicted in Figure 15 [40].

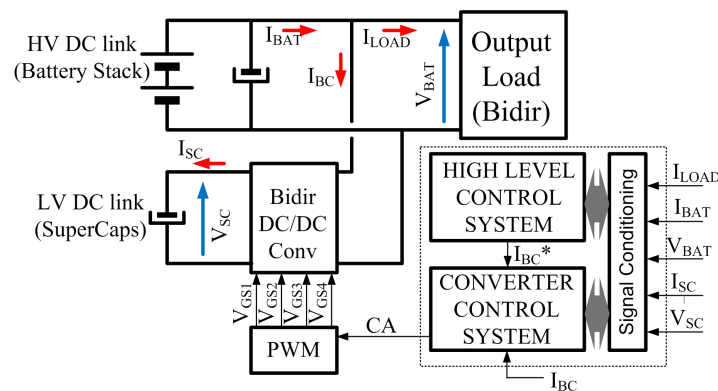


Figure 15. Control Strategy for the HBCS converter.

Considering that the final control parameter is the inductor current, I_L , the converter control stage covers two different aspects: Firstly, it is required that this stage generates a reference for such current, I_L^* , starting from the HV side current, I_{BC}^* . In addition, it implements a feedback control loop for such inductor current.

5.1. Feedback Control Loop for the SC current

This inductor current control loop is shown in Figure 16a. It must be noticed how the average value of I_L equals the average value of I_{SC} . In order to design and tune the regulator, the inductor voltage to inductor current transfer function $G(s)$ can be defined as:

$$G(s) = \frac{1}{R_L + s \cdot L} \quad (34)$$

For the current loop, a standard PI regulator has been designed. This regulator is tuned using the zero-pole cancellation method, and setting the desired bandwidth of the current loop. The regulator consists of a pure integrator and a zero that cancels the pole given by the inductance L and the ESR of the filter inductor, R_L . This ensures that the final bandwidth of the controlled system can be designed to a target value. The characteristic frequency of this zero might change upon eventual variations of the equivalent series resistor due temperature excursions, ageing, or even manufacturing tolerances.

However, assuming an adequate design of this inductor filter, then the ESR of this magnetic element will be relatively small; therefore, the variations in this parameter will not significantly affect the final performance of the controlled system. Once the regulator is tuned, the final implementation needs to obtain the expression of the duty ratio, D , from the control action of the current loop, CA. Considering Equations (25) and (26) and Figure 12, the relationship between D and V_L can be calculated:

$$V_L = D_{eff} \cdot \frac{N_2}{N_1} \cdot V_{BAT} - V_{SC} = D \cdot \left(1 - \frac{t_d}{T_S}\right) \frac{N_2}{N_1} \cdot V_{BAT} - V_{SC}. \tag{35}$$

Finally,

$$D = \frac{N_1}{N_2} \cdot \frac{V_L + V_{SC}}{V_{bat} - \frac{N_2}{N_1} \cdot \frac{2 \cdot I_L \cdot L_{LkPri}}{T_S}}. \tag{36}$$

Figure 16b shows the implemented control scheme. The shaded box implements Equation (36), obtaining the duty ratio D from the control action of the current loop, CA, which is V_L . Figure 17 shows simulations of the performance of this inner loop for a bandwidth of 500 Hz. This plot provides a sequence of current steps as a reference to the current loop, I_L^* . It can be seen how the actual current value tracks perfectly the reference. Moreover, the current can swiftly change its direction, changing automatically from charging to discharging operation modes, even for large relative current steps. This feature is a consequence of using the discussed SR modulation scheme in the topology.

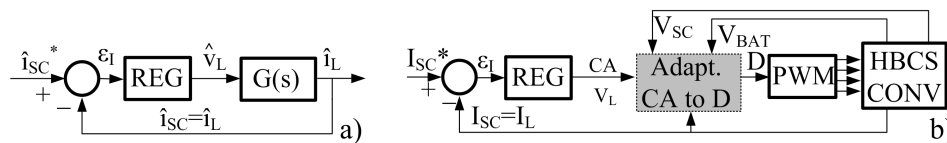


Figure 16. Inner control loop approach (a) for designing and tuning the regulator and (b) for implementing the control scheme.

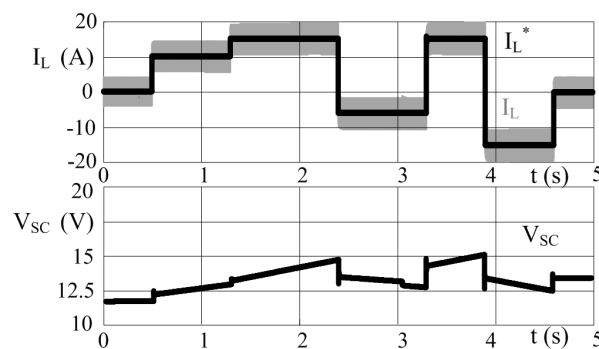


Figure 17. Simulation of inductor current I_L (gray, upper plot) and supercapacitor (SC) voltage V_{SC} (black, lower plot) during step changes in the commanded current (black, lower plot). Positive current corresponds to charging mode, negative to discharging mode.

5.2. Generation of the SC Current Reference

The complete control scheme is shown in Figure 18. An external estimator stage is designed to generate the feedback loop current reference, I_L^* , from the original I_{BC}^* reference. The relationship between the HV-side current and the inductor current can be obtained from the model in Figure 14 as

$$\hat{i}_{BC} = K_1 \cdot \hat{d} + \frac{1}{R_1} \cdot \hat{v}_{BAT} + \left(\frac{N_2}{N_1} \cdot D - K_2 \right) \cdot \hat{i}_L, \quad (37)$$

$$\left. \frac{\hat{i}_{BC}}{\hat{i}_L} \right|_{\substack{\hat{d}=0 \\ \hat{v}_{BAT}=0}} = \frac{N_2}{N_1} \cdot D - K_2. \quad (38)$$

The value of the inductor current reference, I_L^* , is estimated from the HV-side current, I_{BC}^* , by means of the model, as is given in Equation (38). Other control strategies based on additional feedback loops, such as a cascaded control loop to generate the inductor current reference, would imply a more complex implementation of the controller, in terms of computation, number of sensors, filtering and signal conditioning stages, and so on. In addition, they would provide a decrease in the dynamics, given that the external loop dynamics requires a bandwidth significantly smaller than that of the inner loop, in order to ensure a good overall performance.

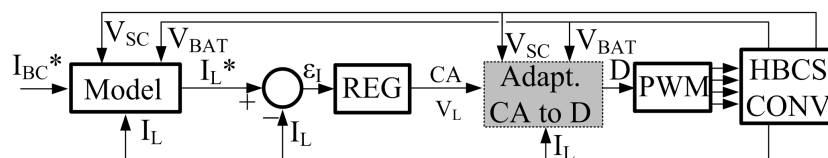


Figure 18. Complete control scheme for the half-bridge current-source (HBCS) converter.

6. Experimental Results

Figure 19 shows a 3 kW laboratory prototype of the HBCS, used in this work for the practical demonstration of the system performance. The main characteristics of the setup are detailed in Table 1. Preliminary results of the performance of this setup were reported in [35].

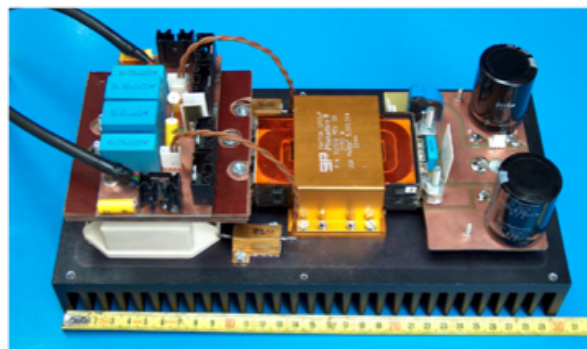


Figure 19. Laboratory prototype of the half-bridge current-source (HBCS) converter.

Figure 20 shows the experimental waveform of the converter, with the same operating conditions as reported in Figure 9. It can be seen how the experimental waveforms were very similar to the simulated waveforms for the switching converter. It also can be seen how the ideal model failed to track the real waveforms properly.

Similarly, Figure 21 compares the proposed complete model, including the effects of the parasitic leakage inductance of the transformer and the resistance to account for the losses, against the experimental waveforms, resembling the conditions stated for Figure 13. This validates the obtained model for the HBCS converter, as the complete model tracked the real converter waveforms very accurately.

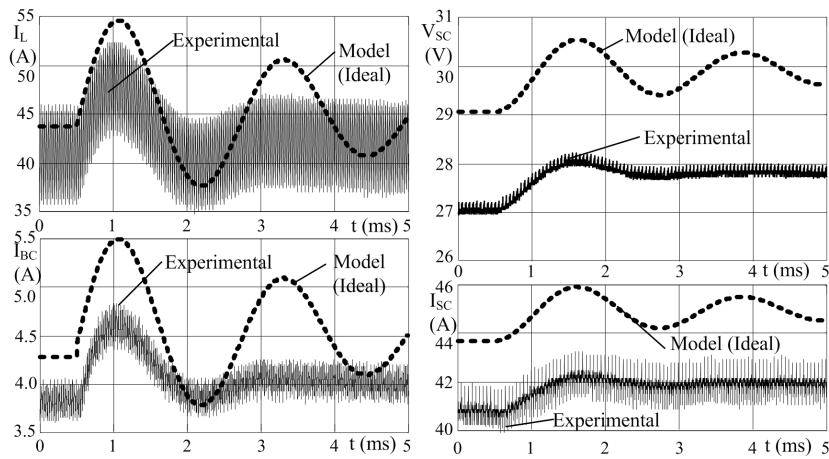


Figure 20. Experimental waveforms (gray) and averaged value of model based on ideal components (black, dashed), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}), and input current (I_{BC}).

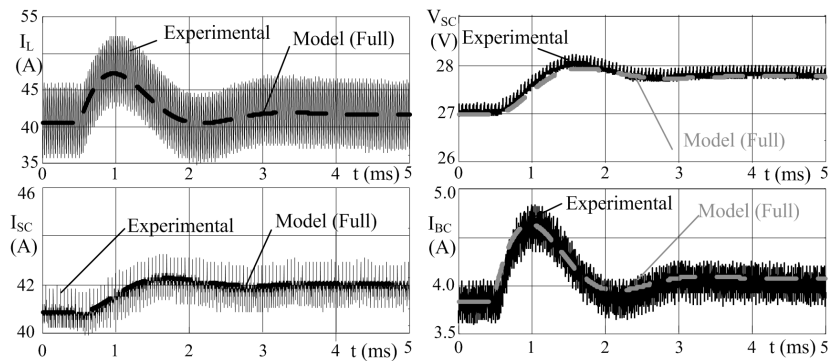


Figure 21. Experimental waveforms (gray) and averaged value of model based on real components (black), for filter current (I_L), load output current (I_{SC}), load voltage (V_{SC}), and input current (I_{BC}).

In order to validate experimentally the implementation of the control scheme, a series of current reference steps were implemented in the converter. The reference steps that were provided to the simulations, shown in Figure 17, were also supplied to the laboratory prototype. Figure 22 shows the performance of the experimental setup. It can be seen how the real converter performed as expected, thus validating the converter control scheme.

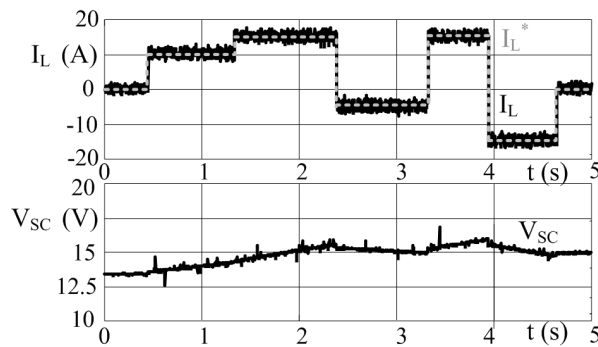


Figure 22. Inductor current I_L (black, upper plot) and supercapacitor (SC) voltage V_{SC} (black, lower plot) during step changes in the commanded current I_L^* (referenced by dashed gray lines). Positive current corresponds to charging mode, negative to discharging mode.

In order to check the dynamics of the inner control loop, a detailed experimental response of one of such current steps is shown in Figure 23.

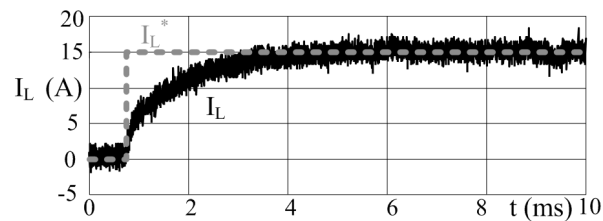


Figure 23. Inductor current I_L (black) and reference I_L^* (grey) during one step change.

7. Conclusions and Future Developments

This research has demonstrated the feasibility of the HBCS converter as a bidirectional power converter for HSS systems in traction applications, where the DC-link is directly connected to the battery bank. The main topics covered include the analysis and design of the power and control stages, the modeling including parasitic elements of the topology, and a validation procedure through a laboratory prototype.

As a first contribution, it has been demonstrated that the use of SR is a suitable switching scheme in the converter, given the demonstrated benefits in the efficiency and the enhancement in the control system implementation. By means of this switching pattern, a full, bidirectional power flow control can be simply implemented in the converter. Moreover, this feature is obtained at no cost, since the required hardware elements to implement SR pattern are present in the conventional HBCS topology.

Another key contribution is to include the parasitic elements in the topology aiming to obtain a highly representative circuital model of the converter. This model has been demonstrated by means of simulations and through experiments in a 3 kW laboratory setup. With the information derived from this dynamic model, the design of the control stage for the HSS can be easily implemented. This research also has provided a design example of a current control loop in order to govern the power flow in the HSS outlined.

A series of future developments arise from this research. One of these developments is the implementation of the HSS in a full powertrain for vehicle applications, including the integration of the HBCS converter control with the complete high-level control system. Another development covers the optimization of the converter power topology and control system, including the definition of the control strategy for the complete system. Additionally, the extension of the application of the HBCS converter to other types of loads (e.g., inductive loads) can be considered in future research.

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Abbreviations

The following abbreviations are used in this manuscript:

CA	Control action
DC	Direct current
ESR	Equivalent series resistor
LV	Low-voltage
HBCS	Half-bridge current-source
HF	High-frequency
HSS	Hybrid storage system
HV	High-voltage
IGBT	Insulated-gate bipolar transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
SC	Supercapacitor
SR	Synchronous rectification

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