

PAPER

## Status of the Level-0 ATLAS barrel muon trigger for High-Luminosity LHC

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## Status of the Level-0 ATLAS barrel muon trigger for High-Luminosity LHC

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**F. Morodei on behalf of the ATLAS TDAQ collaboration**

*Dipartimento di Fisica, Università La Sapienza & INFN Sezione di Roma,  
Piazzale Aldo Moro 5, 00185, Roma, Italy*

*E-mail:* [federico.morodei@cern.ch](mailto:federico.morodei@cern.ch)

**ABSTRACT:** The Muon Spectrometer of the ATLAS detector will be substantially modified during the Phase-II Upgrade to cope with the higher particle rates and radiation levels of the High-Luminosity LHC. The entire trigger and readout electronics of the Resistive Plates Chambers will be replaced. The Resistive Plate Chambers' hit data will be collected by on-detector Data Transmitter and Collector boards and will be sent off-detector to the Sector Logic boards, which will perform the Level-0 barrel muon trigger algorithm and the readout logic. This contribution presents the design of the Phase-II barrel muon trigger and data acquisition system and the development of the barrel Sector Logic board firmware and its challenges.

**KEYWORDS:** Data acquisition concepts; Muon spectrometers; Trigger concepts and systems (hardware and software)

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## Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
<b>2</b>	<b>The Phase-II RPC-based trigger and readout system</b>	<b>2</b>
<b>3</b>	<b>The SL FPGA firmware</b>	<b>3</b>
3.1	Resource floorplanning	3
3.2	Firmware logic	4
3.3	Firmware implementation	5
<b>4</b>	<b>Conclusion</b>	<b>6</b>

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## 1 Introduction

For the High-Luminosity phase of the Large Hadron Collider (HL-LHC), foreseen to start with Run 4 in 2029, the instantaneous luminosity delivered to the LHC experiments will increase from 5 to 7.5 times the nominal value of  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . The much higher pile-up and radiation levels due to the new instantaneous luminosity values constitute a tough challenge for the LHC experiments, especially for what concerns the on-detector electronics of the Trigger and Data Acquisition (TDAQ) systems. For this reason, during the Long Shutdown 3 (2026–2028), the ATLAS detector [1] will undergo a major upgrade (Phase-II Upgrade) in which many detector components will be replaced.

The ATLAS Muon Spectrometer (MS) will undergo several changes in order to retain its excellent trigger and tracking performance even with the extremely high particle rates of the HL-LHC [2]. The entire trigger and readout electronics of the Resistive Plate Chambers (RPCs) of the barrel region will be replaced. Data Collector and Transmitter (DCT) boards will be installed on-detector in substitution of the current Pad and Splitter boxes. They will collect the RPC data and send them to the off-detector Sector Logic (SL) boards, which will perform the Level-0 (L0) trigger algorithm and the readout logic. The current ATLAS two-level trigger scheme will also be kept at HL-LHC. However, the trigger rate and latency of the first level trigger will increase from 100 kHz to 1 MHz and from 3  $\mu\text{s}$  to 10  $\mu\text{s}$  respectively [3]. This will allow more complex trigger algorithms, as well as to maintain the current trigger thresholds. Moreover, the trigger acceptance and efficiency will be increased by the installation of a new RPC station in the barrel inner region.

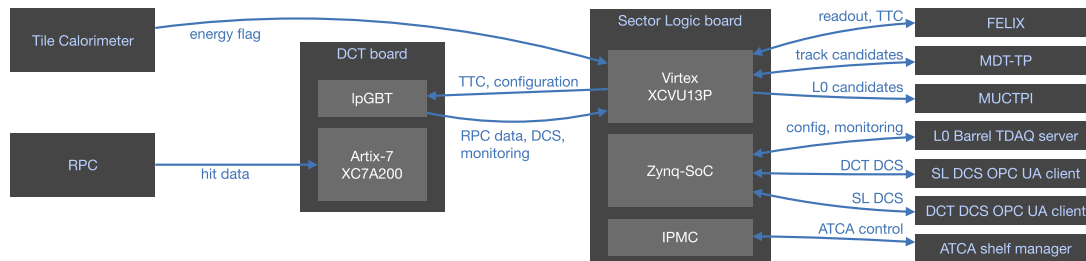
After the description of the major Phase-II changes to the ATLAS RPC TDAQ system, the SL FPGA firmware development and the related challenges are presented in detail.

## 2 The Phase-II RPC-based trigger and readout system

The current ATLAS RPC system of the barrel MS is made of three stations of doublet RPC chambers. Two RPC doublets are situated in the barrel medium (BM) region and the third one in the outer (BO) region. The front-end boards of the BM and BO RPCs, which collect the RPC signals, perform the ASD (Amplifier Shaper Discriminator) functionality and transmit them to the TDAQ chain, will also be kept for the HL-LHC. During the Phase-II Upgrade a new station of RPC triplet chambers will be installed in the barrel inner (BI) region to increase the redundancy of the trigger system, and at the same time to cover the current acceptance holes due to the barrel toroid coils and their support structures. A new front-end board, which will perform both the ASD and TDC logic (100 ps time resolution), will be used for the BI chambers. With the addition of the BI station, any muon with a coincidence of hits in at least three chambers out of four will be considered a valid candidate by the RPC-based L0 trigger algorithm. Furthermore, a coincidence of hits in the BI and BO chambers will be used to cover the current acceptance holes. In this way, the average trigger efficiency will increase to 92%.

In order to satisfy the Phase-II requirements, all the RPC trigger and readout electronics, except for the front-end boards, will be replaced. 1572 DCT boards will be installed to collect the RPC front-end signals and send them to the SL boards. The DCT is a board based on a FPGA from the Xilinx Artix-7 family (XC7A200). The DCT FPGA will implement the logic to collect the RPC signals coming from up to 288 front-end channels, digitize them with 800 ps time resolution (only in BM and BO case) and transmit zero-suppressed data to the barrel SL boards placed in the counting room. The data transmission between DCT and SL will be handled by the Low Power Gigabit Transceiver (lpGBT) [4], a radiation tolerant ASIC working as a serializer/deserializer. The link from the SL board to the DCT, used for TTC data and firmware upload, is called *downlink* and has a bandwidth of 2.56 Gb/s with a user bandwidth of 1.28 Gb/s, while the link from the DCT to the SL board, used to transmit timing and monitoring data, is called *uplink* and has a bandwidth of 10.24 Gb/s with a user bandwidth of 8.96 Gb/s.

In the counting room there will be 32 barrel SL boards, one for each barrel sector, and each of them will be connected with up to 50 DCTs via bidirectional optical fibres. The SL board consists of a Xilinx Virtex Ultrascale+ XCVU13P FPGA which implements the SL firmware; a Xilinx Zynq Ultrascale+ SoC module to communicate with the Detector Control Systems (DCS) and the L0 barrel TDAQ server; and an IPMC module to communicate with the ATCA shelf manager. Using information from the RPCs and the Tile calorimeter, the barrel SL boards will generate trigger candidates within 390 ns and will pass them to the MDT Trigger Processor (MDT-TP), which will perform an improved measurement of muon momentum and will confirm or reject the candidates. The barrel SL boards will then send the trigger decision to the Muon Central Trigger Processor Interface (MUCTPI). The SL boards will also store the DCT data and send them to the readout system through the Front-End Link Interface eXchange (FELIX) modules upon the decision to accept the event from the Central Trigger Processor. The barrel RPC TDAQ system is schematically shown in figure 1.



**Figure 1.** Scheme of the barrel RPC TDAQ system for the HL-LHC [5].

The hardware and firmware of the first DCT prototype have been successfully tested with an RPC station. The prototype SL board is still in a preliminary test phase. Functional tests of the hardware have been performed, while firmware verification and hardware performance tests are foreseen in 2023<sup>1</sup>.

### 3 The SL FPGA firmware

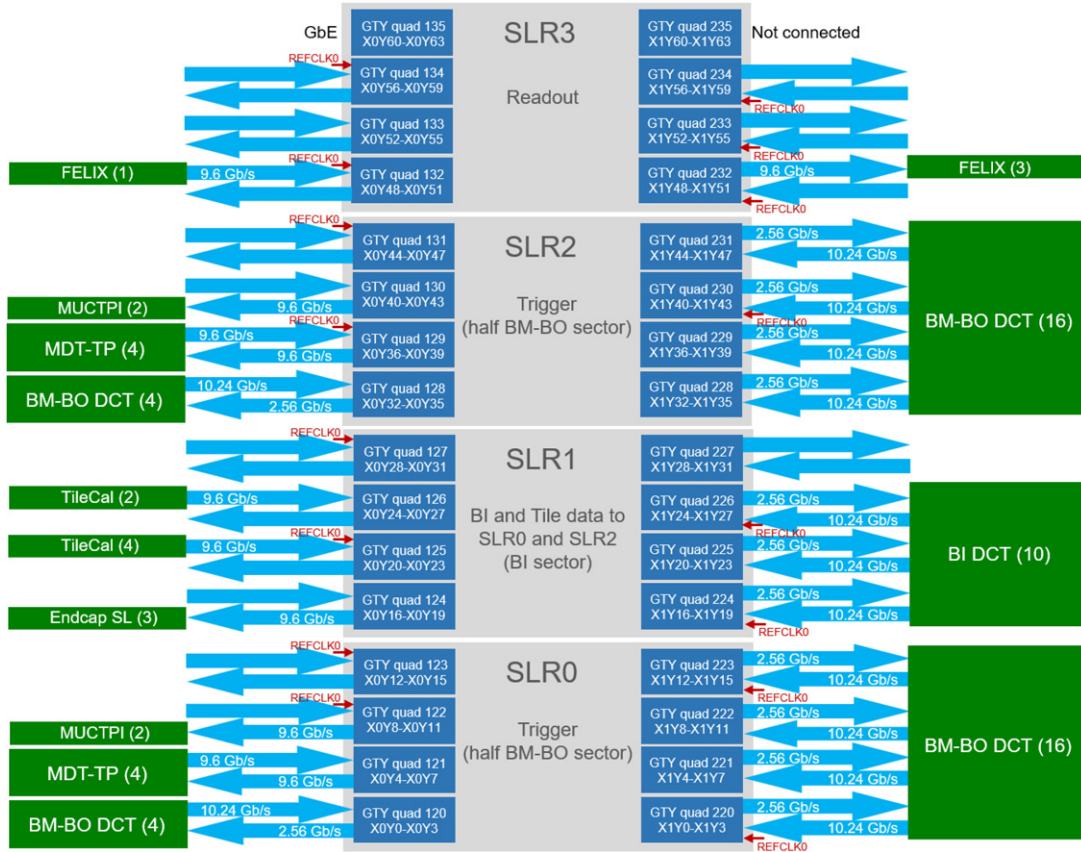
The development and implementation of the SL FPGA firmware was challenging because of the high clock frequencies used (typically 320 MHz) and the location of resources within the FPGA. The Virtex Ultrascale+ XCVU13P device, where the SL FPGA firmware will be uploaded, is divided into four die slices called Super Logic Regions (SLRs), so a careful choice has been made for the I/O port and logic placement among them, in order to optimize the device resource utilization. The firmware has been validated with VHDL simulations using Monte Carlo data for DCT inputs.

#### 3.1 Resource floorplanning

The Barrel SL connections with the external systems are handled by the FPGA embedded high speed transceivers (GTY). Samtec Firefly modules are used on the board for the optical connection to the GTY, each Firefly module providing 12 TX and 12 RX optical fibres. GTY transceivers are organised in groups of four, called Quads. 32 Quads are present in this FPGA (eight for each SLR), for a total of 128 TX and 128 RX fibres. Figure 2 shows the FPGA GTY usage, bandwidth and connectivity with the external systems, as well as how the firmware logic has been divided among the four SLRs.

SLR1 receives the BI RPC data through 10 GTYs and the Tile Calorimeter data through 6 GTYs and passes all of them to the trigger logic blocks in SLR0 and SLR2. SLR0 and SLR2 each receive BM/BO RPC data from a half barrel sector (20 GTYs for each SLR) and perform the L0 RPC-based trigger algorithm. SLR0 and SLR2 then send trigger candidates to the MDT-TP through 4 TX fibres each and receive back confirmation through 4 RX fibres. The final trigger candidates are sent to the MUCTPI via 2 fibres for each of the two SLRs. Moreover, SLR0, SLR1 and SLR2 pass all the RPC DCT data to SLR3, which performs readout logic and sends readout data to FELIX modules through 3 GTYs. Finally, a GTY in SLR1 is reserved for LHC TTC signals.

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**Figure 2.** FPGA transceiver usage, bandwidth and connections with the external systems. The numbers in brackets refer to the number of GTYs used for connections [5].

Tile Calorimeter, MDT-TP, MUCTPI, Endcap SL and FELIX Quads are configured to use the 8b10b decoding/encoding logic and have a line rate of 9.6 Gb/s both for TX and RX, while the DCT Quads use the lpGBT encoding logic and have a TX and a RX line rates of 2.56 and 10.24 Gb/s respectively. The reference clock frequency for all GTYs is 160 MHz for the current implementation. All the logic described below works with a 320 MHz clock obtained from the LHC 40 MHz clock.

### 3.2 Firmware logic

DCT data are encoded with the lpGBT encoding logic, therefore for each DCT GTY in SLR0, SLR1 and SLR2 an lpGBT-FPGA logic block [6], provided by CERN, is instantiated to decode the data (uplink logic). The lpGBT-FPGA logic blocks also encode the control data sent towards the DCTs (downlink logic). The uplink logic is followed by a logic block which divides the uplink output frames to obtain the original DCT 28-bit frames. A logic block, referred to as derandomizing block, reorders the DCT hit data by Bunch Crossing (BC), since they arrive at the SL with a non-fixed latency (from 5 to 20 BCs later with respect to the BC the hit occurred in). Since the BI RPCs have only  $\eta$  strips (read out on both sides), the  $\phi$  coordinate is derived from

the  $\eta$  hit timing. Every BC, the oldest data are sent to a logic block which performs the local coincidence between layers of one RPC chamber (1 out of 2 for BM/BO and 2 out of 3 for BI case). The output of this block is then sent to the trigger logic.

The trigger logic blocks in SLR0 and SLR2 generate up to four trigger candidates per BC, requiring a coincidence in at least three RPC layers out of four independently for  $\eta$  and  $\phi$  strips. Then a logical AND between  $\eta$  and  $\phi$  candidates is applied and the result is sent to the MDT-TP. The candidates are 128-bit frames which include information on  $\eta$  and  $\phi$  coordinates, transverse momentum, charge and highest  $p_T$  threshold satisfied.

The DCT data, after being decoded in SLR0, SLR1 and SLR2, are also sent to SLR3, where the readout logic stores and reorders them by BC using 50 RAM memories (one RAM for each DCT). The memories have a 32-bit width and a depth of 8192 words (16 words per BC, for a maximum of 512 BCs). The writing rate is 10.24 Gb/s. When a L0-Accept signal for a certain BC is received, the corresponding data are sent to the FELIX modules in the order they arrived. Otherwise, 10  $\mu$ s after the collision BC the corresponding data are deleted.

### 3.3 Firmware implementation

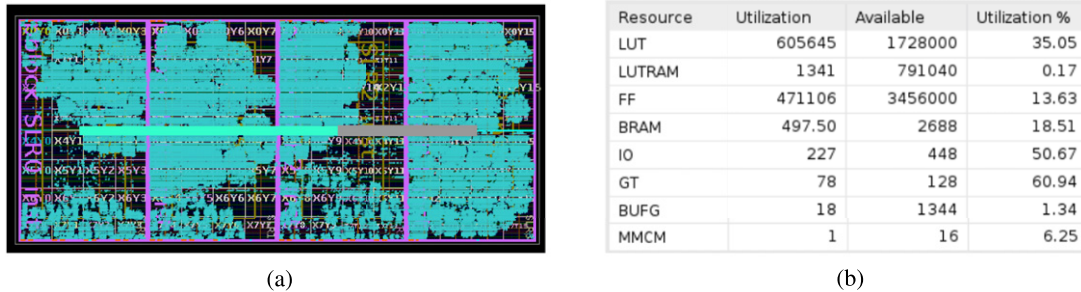
The VHDL simulations and firmware implementation have been performed with Vivado software using the Xilinx Virtex Ultrascale+ XCVU13P device, which is divided into four SLRs, each of them made of one fourth of the FPGA resources. Such a multi-die structure posed a challenge to the firmware implementation: the logic and the I/O pins had to be divided among the four SLRs to minimize the number of signal crossings, because signals can be transmitted between different SLRs only through dedicated routes called Super Long Line (SLL) routes, placed mostly in the central part of the die. Ideally each SLR could work independently from the others, since the L0 trigger algorithm is run independently for the two halves of the ATLAS barrel. However this is not possible, because the number of GTYs in each SLR (32) is not sufficient for all the input and output connections needed by the L0 trigger and readout logic of half the ATLAS barrel, besides the fact that the single SLR occupancy would become close to 100%. The floorplanning design that optimizes the FPGA resource utilization is the one described in section 3.1, and has been implemented assigning the various firmware logic blocks to four different Pblocks,<sup>2</sup> each one covering an entire SLR. Besides these resource issues, there were also problems with the timing closure due to SLR signal crossings. Therefore pipeline registers have been added according to the number of SLR crossings: one register for signals making one crossing (BI DCT data from SLR1 to SLR0 and SLR2, and BM/BO DCT data from SLR2 to SLR3); two registers for signals making two crossings (BI DCT data from SLR1 to SLR3); three registers for signals making three crossings (BM/BO DCT data from SLR0 to SLR3). The availability of SLR crossings is not a concern: the current design uses a maximum of 2600 of the 23040 possible SLR crossings.

The FPGA device after implementation looks as shown in figure 3(a), where the physical cells used for the logic are highlighted in turquoise, while the four Pblocks are contoured in purple.

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<sup>2</sup> A Pblock is a region of the device that constrains the logic assigned to it during Vivado placement process.

The overall post-implementation device resource utilization is shown in figure 3(b). The work presented here, besides the firmware development, demonstrates that the target FPGA has adequate logic resources for the firmware design.



**Figure 3.** SL FPGA device after firmware implementation (a) and overall post-implementation resource utilization of SL FPGA device (b) [5].

#### 4 Conclusion

The TDAQ system of the ATLAS barrel Muon Spectrometer will undergo a substantial upgrade during LS3 to cope with the harsher operation conditions at HL-LHC. The RPC trigger and readout electronics will be replaced with DCT boards, to collect RPC data, and SL boards, which will perform trigger and readout logic. The DCT and SL board prototypes are available and their basic functionalities have been tested. The development of the SL FPGA firmware has represented a tough challenge, because of the large amount of data to be stored and processed, the high number of systems to interface with and the very strict timing constraints. Floorplanning has allowed the logic to meet timing. The next step is the validation of SL FPGA firmware using the SL prototype.

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