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A 0.3 V OTA with Enhanced CMRR and High Robustness to PVT Variations

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Abstract: In this paper, we present a 0.3 V body-driven operational transconductance amplifier (OTA) that exploits a biasing approach based on the use of a replica loop with gain. An auxiliary amplifier is exploited both in the current mirror load of the first stage of the OTA and in the replica loop in order to achieve super-diode behavior, resulting in low mirror gain error, which enhances CMRR, and robust biasing. Common-mode feedforward, provided by the replica loop, further enhances CMRR. Simulations in a 180 nm CMOS technology show 65 dB gain with 2 kHz unity-gain frequency on a 200 pF load when consuming 9 nW. Very high linearity with a 0.24% THD at 90% full-scale and robustness to PVT variations are also achieved.

Keywords: ultra-low voltage; ultra-low power; IoT; OTA; body-driven; replica bias; CMFF

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1. Introduction

The evolution of technology leads to increasingly pervasive electronics, not only in the computing and communication fields, but also in biomedical applications [1–3] and in all aspects of daily life. In particular, the Internet of Things (IoT) [4], making objects 'smart' and able to intercommunicate, represents a milestone from the point of view of the pervasiveness of electronics. IoT nodes include sensor capabilities, computing, and wireless communications, thus presenting potential applications in a very broad range of fields such as healthcare, agriculture, automotive, and industrial manufacturing [5–10].

IoT nodes are mixed-signal systems that include analog signal conditioning, digital processing, and wireless communication, and are often energy-autonomous. They therefore require a drastic reduction of power consumption, since they take their energy from batteries that are required to be small [11] or directly from the environment, exploiting energy harvesting techniques [12–14]. Things are similar in the case of biomedical devices, particularly implantable ones [15–17], for which substitution of the battery is not a viable solution or at least requires a surgical operation.

Reduction of the supply voltage is one of the available options to reduce power dissipation; moreover, in the case of energy-harvesting systems, which typically provide voltages in range of hundreds of mV [13], reduction of supply voltage would reduce the need for step-up converters and simplify power management. In CMOS technology, reduction of the supply voltage to 0.3–0.5 V leads the devices to operate in moderate or weak inversion. This results in a drastic drop in power consumption and transistor speed that is still compatible with applications utilizing signals with bandwidth up to hundreds of kHz and however no more than some MHz. This context has led to a boost of research interest in the field of ultra-low voltage (ULV) and ultra-low power (ULP) electronics [18,19].

Analog interfaces are a critical function in IoT nodes and biomedical circuits, and the unbuffered operational amplifier (UOPA), also often denoted as the "operational transconductance amplifier" (OTA) in the literature, is a fundamental building block in such ap-

plications. The UOPA is also one of the most challenging blocks to design in ULV/ULP applications due to the competitive requirements for gain, bandwidth, efficiency and robustness under process, supply voltage, and temperature (PVT) variations [20,21]. UOPAs and proper OTAs have widespread applications in biomedical and IoT systems, including in the analog input interface, in the design of amplifiers and filters, in drive actuators, as buffer references for the analog-to-digital converter (ADC), and in the design of low-dropout regulators (LDOs). Limited bandwidths are often needed, but some of these applications require the driving of large capacitive loads. The extremely low supply voltage does not allow for the exploitation of traditional design approaches such as tailed differential pairs and cascoding, and several design techniques have been studied for the design of efficient ULV OTAs. Solution based on a fully-digital approach (DIGOTA) [22–24] or operating in the time domain [25,26] have been proposed, but most of these techniques exploit analog approaches such as body-driving [27–45], floating-gate [46] and floating-body [47] devices, and inverter-based architectures [48–51]. The latter are often suitable for implementation using digital standard-cell libraries [52–55], thus simplifying the layout through the use of automatic place-and-route CAD tools and easing design portability among different technologies.

The lack of a tail current source makes biasing more sensitive to PVT variations and results in a drastic worsening of the common-mode rejection ratio (CMRR). Body biasing [21] has been proposed in the literature as a substitute for the tail generator, but the reduced supply voltage and the low body transconductance gain limit its performance in coping with PVT variation. In the case of body-driven OTAs, the gate terminals are available for biasing, and this places the bias current within the limit of the precision of the resulting current mirror. This is affected not only by device mismatches but also by different drain-source voltages, resulting in the dispersion of performance under PVT variations.

In the case of fully differential stages, CMRR is determined by the common-mode feedback (CMFB) loop gain. Differential-to-single-ended (D2S) stages are typically designed with a (pseudo)-differential pair loaded by a current mirror; without the tail current generator, CMRR entirely relies on the precision of the current mirror load. Even in the ideal case of perfectly matched devices, the output resistance of the transistors results in a gain error and hence limits CMRR. Using a fully differential input stage with common-mode feedback [40,44] improves CMRR in the nominal case but results in larger variations under mismatches due to common-mode to differential-mode conversion. A common-mode feedforward (CMFF) approach [29,38,56–58] can be used to improve CMRR in typical conditions, also reducing variability under PVT. In [43], an improved body-driven current mirror was proposed and applied to a ULV differential-to-single-ended (D2S) converter stage to improve its CMRR; a similar idea was applied in [53] to achieve high CMRR in a standard-cell-based OTA. The idea was to exploit an auxiliary amplifier to attenuate the gain error of the current mirror.

In this paper, we develop on this approach, and propose a two-stage body-driven ULV OTA with high CMRR and robust bias. The improvement of the auxiliary amplifier is exploited by the gate-driven current mirror of the input D2S stage to improve its CMRR; moreover, the same technique, together with a CMFF approach, is used in the biasing branch that generates the gate voltage for the gate biasing of the input stage. This not only allows for improvement of the CMRR, but also for the achievement of a bias point that is robust under PVT variations, thanks to the reference voltage exploited by the auxiliary amplifiers. The proposed solution entails utilizing an enhanced gate-driven current mirror (previously published in a body-driven configuration [43]) alongside a biasing approach that accurately fixes current and voltage.

The paper is structured as follows: Section 2 presents the proposed topology and discusses its advantages. Section 3 reports circuit simulations conducted using a CMOS 180 nm technology and compares the performance with the state of the art. Finally, Section 4 concludes this paper.

2. Proposed Amplifier

This section introduces the proposed topology and presents a detailed analysis of its performance. Key features of the topology are the use of an enhanced current mirror, which helps with improving the common-mode rejection ratio (CMRR), and a replica bias loop that exploits auxiliary amplifiers to set bias current and node voltage with great robustness against variations. The bias approach is described in Section 2.2 to highlight its advantages in terms of robustness. The circuit is then analyzed considering its small-signal performance from the point of view of noise and differential-mode and common-mode behavior. This analysis shows how the proposed approach improves the CMRR of the proposed OTA, thanks to both the enhanced current mirror and the common-mode feedforward approach achieved through the replica bias. This approach also helps with reducing distortions, as shown in Section 2.6.

2.1. Topology Description

The proposed amplifier features a standard two-stage architecture, as shown in Figure 1; body-driving is exploited in both stages to allow for a rail-to-rail input common-mode range (ICMR) and keep gate terminals available for robust biasing. Both NMOS and PMOS body terminals are exploited as inputs of the second stage to enhance gain.

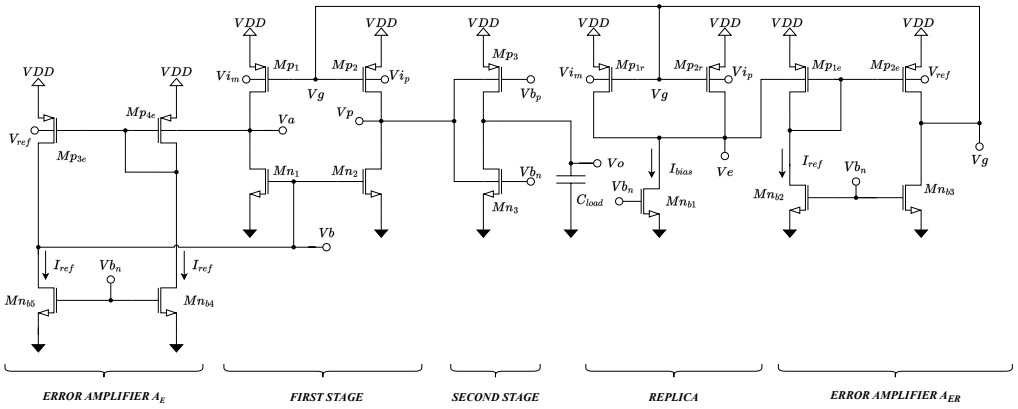

Figure 1. Proposed two-stage OTA architecture with enhanced current mirror and replica bias.

With reference to Figure 1, the input stage is composed of transistors $Mn_{1,2}$ and $Mp_{1,2}$. The input is applied to the body terminals of the PMOS devices, whose gate terminal is exploited to set the bias point. NMOS devices are used to form a current mirror load. To improve CMRR, the NMOS current mirror is enhanced through the use of an auxiliary amplifier A_E that helps with reducing gain error. A simple single-stage body-driven auxiliary amplifier is used; it exploits a reference voltage V_{ref} that helps with achieving a robust bias point.

The first stage of the OTA is critical in achieving robust bias and high CMRR. To improve performance, the bias point is set through the use of a replica bias stage ($Mp_{1r,2r}$ in Figure 1). The input signal is applied to the body terminals of the replica bias stage, whose role is to keep the bias current constant at I_{bias}, counteracting the variations of PVT and of the input common-mode voltage. Additionally, an auxiliary amplifier is exploited to improve the diode connection of $Mp_{1r,2r}$, and it is designed identically to the auxiliary amplifier of the input stage. The voltage reference applied to the amplifier keeps the drains of $Mp_{1r,2r}$ at the desired voltage (typically $V_{DD}/2$), equal to the drain voltage of $Mp_{1,2}$, controlled by the auxiliary amplifier of the input stage (the same reference V_{ref} is applied to both amplifiers). The replica bias stage thus implements common-mode feedforward (CMFF) to improve CMRR and yields a robust bias point against PVT variations.

It has to be noted that the proposed approach, based on the use of auxiliary amplifiers with an explicit reference voltage, enables setting the gate-source voltages of the transistors independently from their drain-source voltages; hence, the operating point of the transistors

can be optimized while still keeping their drain-source voltages at $V_{DD}/2$. Moreover, this approach can also be applied in simple p-well CMOS technologies that do not allow isolated wells for NMOS devices.

With reference to a more common triple-well technology, a simple body-driven inverter is exploited as the second stage, and its bias point is set through the gate terminals. Bias voltages Vb_n and Vb_p in Figure 1 are generated through current mirror connections (diode-connected devices driven by current sources) in order to retain the current constant notwithstanding PVT variations.

2.2. Analysis of Biasing Approach

A replica-bias approach is exploited to precisely set the bias current of the first stage of the OTA, making it independent on PVT and input common-mode variation. With reference to Figure 1, the replica bias stage, composed of $Mp_{1r,2r}$, the current source Mn_{b1}, and the auxiliary amplifier A_{ER}, is used to set the bias current of $Mp_{1,2}$ to $KI_{bias}/2$, where K is the ratio of the form factors of devices in the main and replica stages.

Recall that the drain current of an MOS device operating in sub-threshold is given by

$$I_D = I_0 exp\left(\frac{Vgs - V_{th}}{nU_T}\right)\left(1 - exp(\frac{-Vds}{U_T})\right) \tag{1}$$

where Vgs and Vds are gate-source and drain-source voltages; V_{th} is the threshold voltage and depends on the body-source voltage Vbs (body-effect) and on Vds (DIBL, drain-induced barrier lowering); U_T is the thermal voltage, n is the subthreshold slope. Recall as well that the current I_0 is given by

$$I_0 = \mu C_{ox}(n-1)U_T^2\frac{W}{L} \tag{2}$$

where μ is the mobility of electrons (holes), C_{ox} is the oxide capacitance per unit area, and W and L are the width and length of the gate, respectively.

The replica bias loop adjusts the gate voltage of $Mp_{1r,2r}$ so as to keep the sum of their currents equal to I_{bias}, contrasting PVT variations. that affect I_0 and V_{th} in (1), and variations of the input common-mode voltage, that changes Vbs. The same gate voltage is applied to the gates of $Mp_{1,2}$, thus controlling their current. Instead of a simple diode connection, a feedback loop involving the auxiliary amplifier A_{ER} is exploited in the replica stage. This approach not only improves the precision of the replica stage, but also enables keeping the drain-source voltages of $Mp_{1r,2r}$ constant and equal to V_{ref}, within the limits of finite loop gain. This results in better matching of devices in the main and replica stages, and hence, a more robust biasing.

The replica bias loop is schematized in Figure 2, where i_{in} represents the variation of the current of $Mp_{1r,2r}$ with respect to its nominal value, $i_{ref} = 0$ is the small-signal component of the reference current (we are assuming an ideal current source I_{ref}), $v_{ref} = 0$ is the small-signal component of the reference voltage, and A_E is the voltage gain of the auxiliary amplifier:

$$A_E = \frac{gmb_{pe}}{G_{oE}}\frac{2gm_{pe} + G_{oE}}{2(gm_{pe} + G_{oE})} = \frac{gmb_{pe}}{G_{oE}} \tag{3}$$

where $G_{oE} = gds_{pe} + gds_{ne}$ is its output conductance, and Z_e is the impedance at the output of the replica stage:

$$Z_e = \frac{1}{2gds_r + gds_G} \tag{4}$$

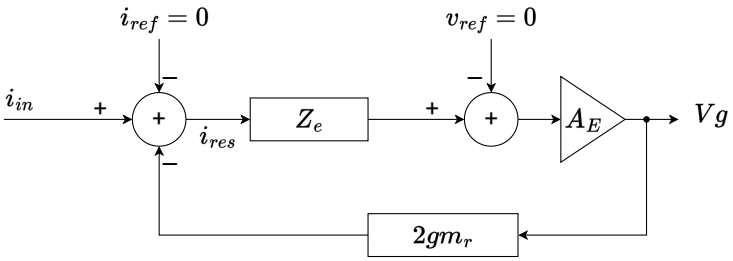

Figure 2. Block scheme of the replica bias loop.

In the previous equations, standard nomenclature is used for the small-signal parameters of the MOS devices. Subscript r refers to $Mp_{1r,2r}$. Subscripts pe and ne refer to the PMOS and NMOS devices af the auxiliary error amplifier, and gds_G is the output conductance of the current source in the replica stage.

The scheme in Figure 2 enables calculation of the residual current error of the replica stage i_{res} as

$$i_{res} = \frac{i_{in}}{1 + 2gm_r A_E Z_e} \tag{5}$$

The same error is achieved in the main stage, in the limit of matched drain-source voltages.

Looking at the main amplifier, the voltage generated by the replica loop is applied to the gate terminals of the input devices $Mp_{1,2}$. The enhanced current mirror load exploits an auxiliary amplifier that sets the drain voltage of Mp_1 (and, by symmetry, of Mp_2) to V_{ref}, within the limit of its finite loop gain. The input devices thus present the same gate-source, drain-source, and body-source voltages as their replica counterparts, resulting in robust biasing.

This approach mimics the behavior of a tailed differential pair: within the limit that the replica stage correctly estimates the common-mode current, when a differential input signal is applied, the replica loop keeps the sum of the drain currents of Mp_1 and Mp_2 constant, thus transforming the input stage into a truly differential stage.

2.3. Differential-Mode Analysis

To analyze the small-signal behavior of the proposed amplifier, we can refer to Figure 3, where the capacitances at the different nodes have been explicitly shown.

$$C_A = Cgd_n + Cdb_n + Cgd_p + Cdb_p + C_{inE} \tag{6}$$

$$C_B = 2Cgs_n + Cgd_n\left(2 + \frac{gm_n}{Go_1}\right) + C_{oE} \tag{7}$$

$$C_1 = Cgd_n + Cgd_p + Cdb_n + Cdb_p + Csb_{p2} + Csb_{n2} + (Cdb_{n2} + Cdb_{p2})\left(1 + \frac{Gm_2}{Go_2}\right) \tag{8}$$

$$C_L = C_{load} + Ggd_{n2} + Cdb_{n2} + Cgd_{p2} + Cdb_{p2} \tag{9}$$

where C_{inE} and C_{oE} are the input and output capacitances of the auxiliary amplifier, $Go_1 = gds_n + gds_p$ is the output conductance of the first stage, and $Gm_2 = gmb_{n2} + gmb_{p2}$ and $Go_2 = gds_{n2} + gds_{p2}$ are transconductance and output conductance of the second stage. Standard nomenclature is used for the small-signal parameters of the MOS devices. Subscript p refers to $Mp_{1,2}$, subscript n refers to $Mn_{1,2}$, and subscripts $n2$ and $p2$ refer to NMOS and PMOS devices of the second stage. The same auxiliary amplifier as in the replica stage has been used; hence, A_E is given by (3) (we are neglecting the pole-zero doublet due to the current mirror) and

$$C_{inE} = Csb_{pe} \tag{10}$$

$$C_{oE} = Cgd_{ne} + = Cgd_{pe} + Cdb_{ne} + = Cdb_{pe} \tag{11}$$

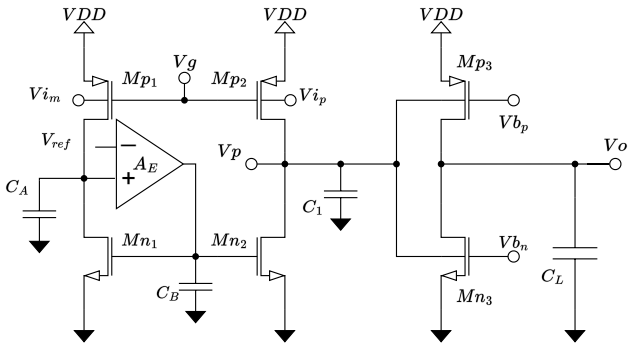

Figure 3. Schematic of the amplifier for small-signal analysis.

Let us consider initially the differential-mode transfer function ($v_{ip} = -v_{im} = v_{id}/2$). The gate terminals of $Mp_{1,2}$ can be assumed at virtual ground; hence, $v_g = 0$. From Figure 3, the transfer function of the first stage, exploiting the Miller approximation, can be obtained as

$$A_{d1} = -\frac{gmb_p}{Go_1 + sC_1} \frac{gm_n A_E + Go_1/2 + s(C_A + C_B \frac{Go_1}{Go_E})/2 + s^2 \frac{C_A C_B}{2Go_E}}{gm_n A_E + Go_1 + s(C_A + C_B \frac{Go_1}{Go_E}) + s^2 \frac{C_A C_B}{Go_E}} \approx -\frac{gmb_p}{Go_1 + sC_1} \tag{12}$$

where the two pole-zero doublets due to the enhanced current mirror can be neglected, and the transfer function of the second stage is given by

$$A_2 = -\frac{Gm_2}{Go_2 + sC_L} \tag{13}$$

The differential-mode gain is therefore

$$A_d = A_{d1} A_2 = \frac{gmb_p Gm_2}{Go_1 Go_2} \frac{1}{1 + s\tau_1} \frac{1}{1 + s\tau_2} \tag{14}$$

where the two poles are

$$\frac{1}{\tau_1} = \frac{Go_2}{C_L} \tag{15}$$

$$\frac{1}{\tau_2} = \frac{Go_1}{C_B} \tag{16}$$

For a sufficiently large load capacitance C_L, the dominant pole is given by $1/\tau_1$, and an adequate phase margin is achieved, otherwise some form of compensation is needed. Assuming to be in the large-capacitance case, the gain-bandwidth product (GBW) can be easily calculated as

$$GBW = \frac{gmb_p Gm_2}{Go_1 C_B} \tag{17}$$

2.4. Common-Mode Analysis

The common-mode gain of the proposed amplifier is affected both by the enhanced current mirror used for differential to single-ended conversion and by the replica loop. To separately analyze these two effects, we can start analyzing the scheme in Figure 3 in the case of common-mode excitation ($v_{ip} = v_{im} = V_{ic}$) with $v_g = 0$. The analysis yields the common-mode gain of the first stage as

$$A_{c1} = -\frac{gmb_p}{Go_1 + sC_1} \frac{Go_1 + s(C_A + C_B \frac{Go_1}{Go_E}) + s^2 \frac{C_A C_B}{Go_E}}{gm_n A_E + Go_1 + s(C_A + C_B \frac{Go_1}{Go_E}) + s^2 \frac{C_A C_B}{Go_E}} \approx -\frac{gmb_p}{gm_n A_E} \frac{1}{1 + s\tau_2} \tag{18}$$

Equation (18) highlights the effect of the enhanced current mirror. We note that A_{c1} is given by the differential mode gain (12) times the reciprocal of the current gain error of the mirror. Using a simple current mirror (with gate and drain of Mn_1 connected together), the current gain error is inversely proportional to gm/gds, whereas in this case the error is scaled down by the gain of the auxiliary amplifier A_E.

The replica bias loop keeps constant the sum of the drain currents of $Mp_{1,2}$, counteracting the effect of the input common-mode signal. Hence, voltage v_g depends on the input common-mode signal v_{ic}, and the overall common-mode transconductance gain of the pair $Mp_{1,2}$ results lower than the value of gmb_p used in (18). The effect is similar to a tailed differential pair, where the common-mode input signal sees a source degeneration that reduces the transconductance.

The block scheme in Figure 2 can be used to calculate v_g as a function of v_{ic}, observing that current i_{in} in Figure 2 is given by $2gmb_r v_{ic}$. A simple analysis yields

$$v_g = -\frac{2gmb_r Z_e A_E}{1+2gm_r Z_e A_E} v_{ic} \approx -\frac{gmb_r}{gm_r} \frac{1}{1+\frac{1}{2gm_r Z_e A_E}} v_{ic} \tag{19}$$

The common-mode transconductance of $Mp_{1,2}$ therefore becomes

$$Gm_{c1} = \frac{gmb_p}{2gm_r Z_e A_E + 1} \tag{20}$$

and this is the correct value to be used in (18). The overall common-mode gain of the amplifier is thus given by

$$A_c \approx \frac{gmb_p}{2gm_r Z_e gm_n A_E^2} \frac{1}{1+s\tau_2} |A_2| \tag{21}$$

and CMRR results as

$$CMRR = 2gm_r Z_e \frac{gm_n}{Go_1} A_E^2 \tag{22}$$

2.5. Noise Analysis

To analyze the noise performance of the proposed OTA, we consider for each transistor M_X in Figure 1 a noise current source i_X that includes a thermal noise component with spectral density

$$S_{X,t} = 4KT\gamma gm_X \approx 2qI_{DX} \tag{23}$$

(where I_{DX} is the bias current of the device) and a flicker noise component with spectral density

$$S_{X,f} = \frac{K_F gm_X^2}{fC_{ox}WL} \tag{24}$$

We calculate the open-circuit output voltage due to the different noise sources, and dividing it by the differential gain (14), we obtain the equivalent input-referred noise voltage.

Noise sources of transistors of the second stage (Mn_3 and Mp_3) are directly connected to the output and yield an output voltage

$$\frac{i_{n3} + i_{p3}}{Go_2} \tag{25}$$

Neglecting the gain error of the current mirror, the noise sources of the main devices of the first stage ($Mn_{1,2}$ and $Mp_{1,2}$) yield an output voltage

$$\frac{i_{n1} - i_{n2} + i_{p1} - i_{p2}}{Go_1} A_2 \tag{26}$$

that is the main noise contribution of the OTA. Noise sources in the auxiliary amplifier (devices $Mp_{3e,4e}$ and $Mn_{4,5}$) yield a common-mode contribution that is attenuated by the CMRR. Noise in the replica stage appears at the gates of $Mp_{1,2}$ and is amplified by the common-mode gain (21), resulting in a very small contribution that can be neglected.

As a result, the equivalent input noise spectrum is given by

$$S_{Veq} = \frac{S_{n1} + S_{n2} + S_{p1} + S_{p2}}{gmb_p^2} + \frac{S_{n4} + S_{n5} + S_{p3e} + S_{p4e}}{A_{d1}^2 gmb_{pe}^2} + \frac{S_{n3} + S_{p3}}{A_{d1}^2 Gm_2^2} \tag{27}$$

and by using (23) and (24), it can be written as

$$\begin{aligned} S_{Veq} \approx \frac{4q}{gmb_p^2}\left[2I_{D1} + 2I_{AUX}\left(\frac{Go_1}{gmb_{pe}}\right)^2 + I_{D2}\left(\frac{Go_1}{Gm_2}\right)^2\right] \\ + \frac{1}{fC_{ox}gmb_p^2}\left[\frac{2K_{Fp}gm_p^2}{W_pL_p} + \frac{2K_{Fn}gm_n^2}{W_nL_n} + \left(\frac{Go_1}{gmb_{pe}}\right)^2\left(\frac{2K_{Fp}gm_{pe}^2}{W_{pe}L_{pe}} + \frac{2K_{Fn}gm_{ne}^2}{W_{ne}L_{ne}}\right)\right. \\ \left. + \left(\frac{Go_1}{Gm_2}\right)^2\left(\frac{K_{Fp}gm_{p2}^2}{W_{p2}L_{p2}} + \frac{K_{Fp}gm_{n2}^2}{W_{n2}L_{n2}}\right)\right] \end{aligned} \tag{28}$$

where I_{D1}, I_{D2}, and I_{AUX} are the bias currents of devices in the first stage, in the second stage, and in the auxiliary amplifier, respectively.

2.6. Distortions

To analyze distortions, we model the transconductance gain of the transistors as a power series, limiting it to the third order:

$$I \approx \sum_{i=1}^{3} a_i Vgs^i + \sum_{i=1}^{3} b_i Vbs^i \tag{29}$$

(a_1 is the small-signal transconductance gm, and b_1 is gmb). The differential input signal is assumed to be a pure sinusoidal tone

$$V_{in} = Acos(\omega t) \tag{30}$$

Analysis of the replica bias loop shows that the gate voltage V_g contains only a second-harmonic component

$$V_g^{(2)} = \left(\frac{b_2 A_E Z_e}{1 - 2a_1 A_E Z_e} A^2\right) cos(2\omega t) \tag{31}$$

Applying this signal to the main amplifier, and considering a gain error ϵ for the current mirror, the output voltage V_p of the first stage can be calculated as

$$V_p = \left(1 + \frac{\epsilon}{2}\right)\frac{b_1}{Go_1}Acos(\omega t) + \frac{\epsilon}{1 - 2a_1 A_E Z_e}\frac{b_2}{2Go_1}A^2 cos(2\omega t) + \left(1 + \frac{\epsilon}{2}\right)\frac{b_3}{4G_o 1}A^3 cos(3\omega t) \tag{32}$$

Equation (32) shows that the use of the CMFF attenuates the second harmonic distortion, which is usually the dominant component in single-ended OTAs.

3. Circuit Design and Simulation

The proposed OTA was designed and simulated using a triple-well 180 nm CMOS technology by TSMC. A 0.3 V supply voltage was adopted, and the amplifier was sized to drive a 200 pF load, rendering it stable without the need of compensation. The design goal was a gain-bandwidth product in the order of 1.5–2 kHz suitable for biomedical and IoT applications and requiring extremely low power consumption. Table 1 reports the sizing of the devices (standard 1.8 V devices of the selected technology) and the bias currents. The design guidelines taken into consideration ensure that the nominal values of Vds and Vgs

are set to $V_{DD}/2$. This choice serves to center the dynamic range of each transistor while also enhancing the effectiveness of control amidst PVT variations. The external reference voltage Vref is set to $V_{DD}/2$.

Table 1. Transistor sizing.

	W [µm]	L [µm]	I_{DC} [nA]
$Mp_{1,2}$	65	1	10
$Mn_{1,2}$	10	2.53	10
Mp_3	26	1	4
Mn_3	4	2.53	4
Mn_{b1}	4	2.53	1
$Mp_{1r,2r,1e,2e,3e,4e}$	6.5	1	1
$Mn_{b2,b3,b4,b5}$	2	2.53	1

Simulations were performed in the Cadence Virtuoso design environment, considering both nominal conditions and PVT and mismatch variations. The performance of the amplifier under typical conditions (nominal process corner, 27 °C, 0.3 V supply) is reported in Table 2. Figure 4 shows the differential-mode transfer function, highlighting a DC gain A_{d0} of 65.54 dB and a unity-gain bandwidth of about 2 kHz; a phase margin of 50° was achieved. Figure 5 reports the frequency behavior of CMRR, highlighting the extremely good performance that was achieved. Figure 6 shows the input-referred noise (IRN) spectrum, which indicates a white noise level of 1.46 µV/$\sqrt{\text{Hz}}$ at 1 kHz and a noise corner frequency of about 800 Hz. Power consumption is 9 nW.

Table 2. PVT Characterization of the proposed OTA.

	Typ	FF	SS	SF	FS	Temp = 0	Temp = 80	Alim = 270 mV	Alim = 330 mV
A_{d0} [dB]	65.54	64.64	66.49	65.07	66.02	66.43	61.45	63.28	66.91
GBW [kHz]	1.98	1.85	2.135	1.92	2.05	2.23	1.33	1.73	2.2
$m\varphi$ [deg]	49.87	52.66	51.29	47.07	48.47	48.23	60.77	46.51	54.56
A_{c0} [dB]	−54.76	−24.08	−25.17	−36.64	−39.85	−22.78	−16.14	−26.16	−27.44
$CMRR$ [dB]	120.3	88.72	91.66	101.71	105.87	89.21	77.59	89.44	94.35
$PSRR$ [dB]	121.06	120.96	120.39	119.79	121.59	119.79	117.8	114.36	125.07
P_D [nW]	9	9.05	8.96	8.98	9.02	8.95	9.19	8.07	9.93
I_{in} [fA]	349.7	349.9	349.5	350.3	349.1	302.9	3406	225.9	544.2
V_{off} [mV]	0	0.1	0.1	0	0	0.1	0.3	0.1	0
SR_p [V/s]	83.89	73.99	89.76	85.49	79.51	100.1	43.23	70.68	100.1
SR_m [V/s]	59	122.3	26.34	30.83	107.4	23.93	207.1	28.8	113.1
SR_{avg} [V/s]	71.445	98.145	58.05	58.16	93.455	62.015	125.165	49.74	106.6
IRN [µV/$\sqrt{\text{Hz}}$]	1.43	1.45	1.41	1.46	1.41	1.33	1.61	1.46	1.40
THD (10 Hz, 270 mVpp) [%]	0.24	0.239	0.238	0.242	0.237	0.238	0.248	0.241	0.247

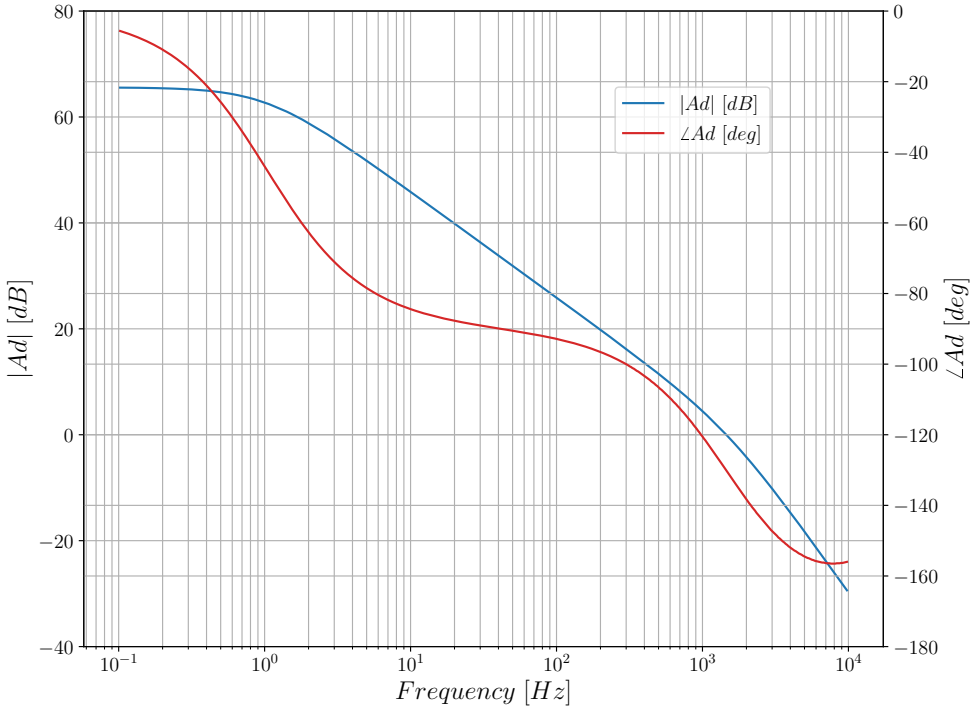

Figure 4. Differential-mode transfer function.

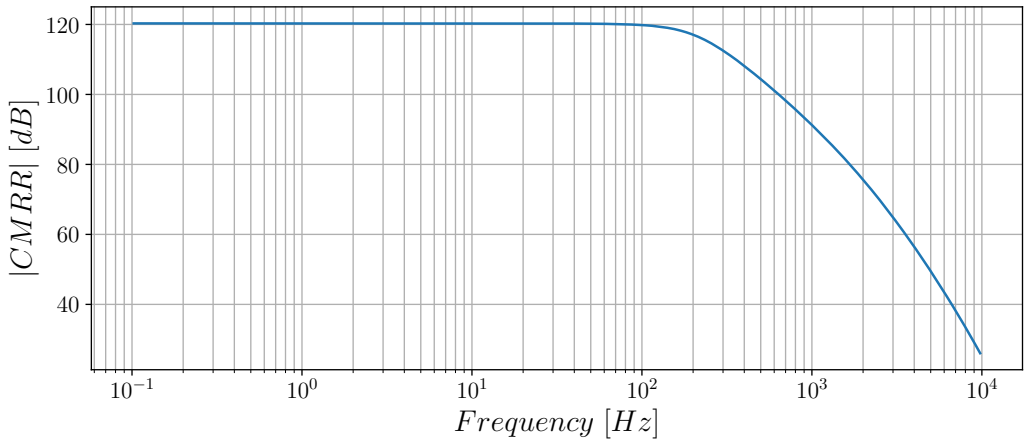

Figure 5. Common-mode rejection ratio.

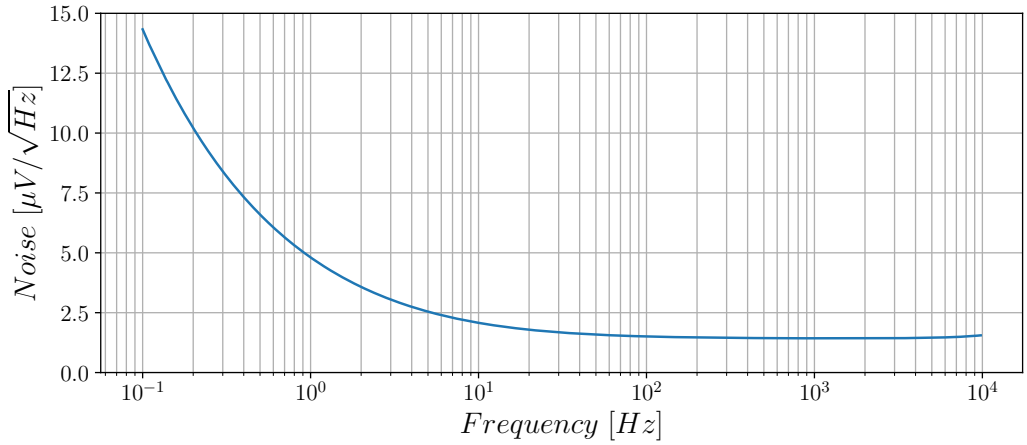

Figure 6. Input-referred noise spectrum.

The OTA was also tested in a closed-loop unity-gain configuration. Figure 7 reports the response to a full-swing input voltage step, whereas Figure 8 shows the total harmonic distortion (THD) vs. input signal amplitude when a 10 Hz sinusoidal input signal was applied. Very low distortions were achieved, with a THD as low as 0.24% for a 270 mVpp input (90% of full swing), thanks to the use of the enhanced current mirror and of the replica loop. Figure 9 shows the output signal when a 10 Hz 270 mVpp sine wave was applied.

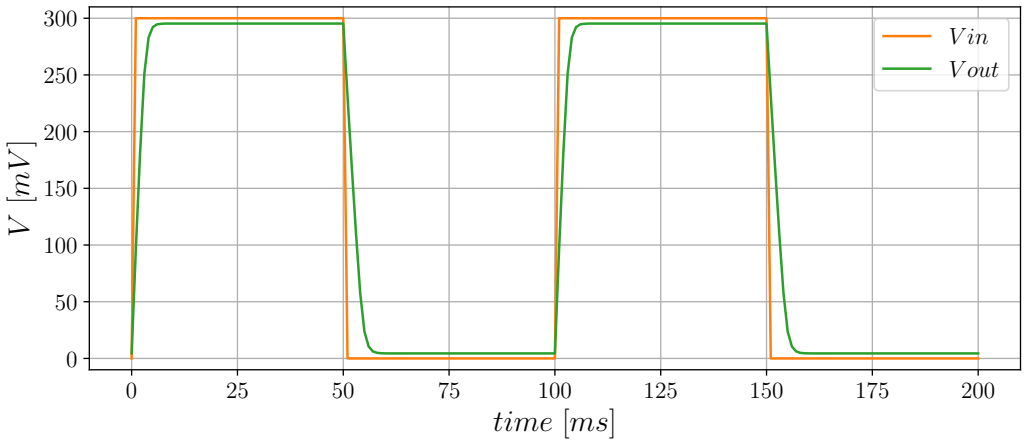

Figure 7. Step response in unity-gain closed-loop configuration.

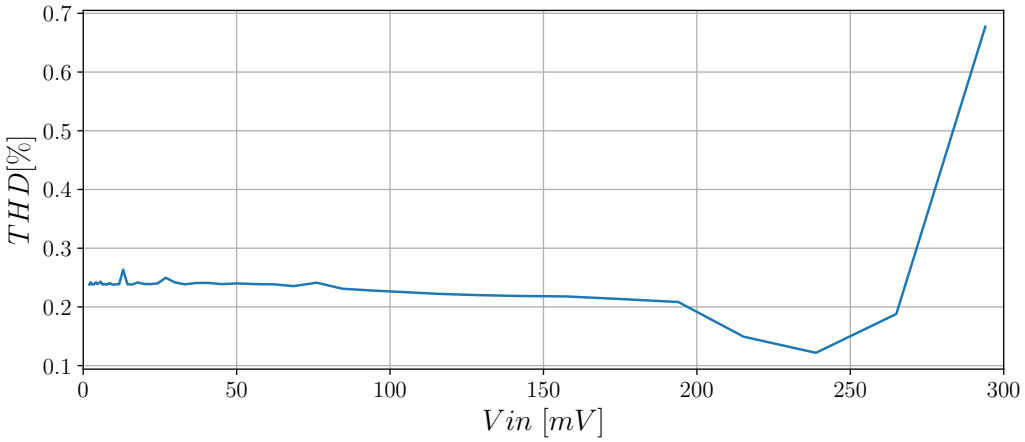

Figure 8. Total harmonic distortion vs. input peak-to-peak voltage.

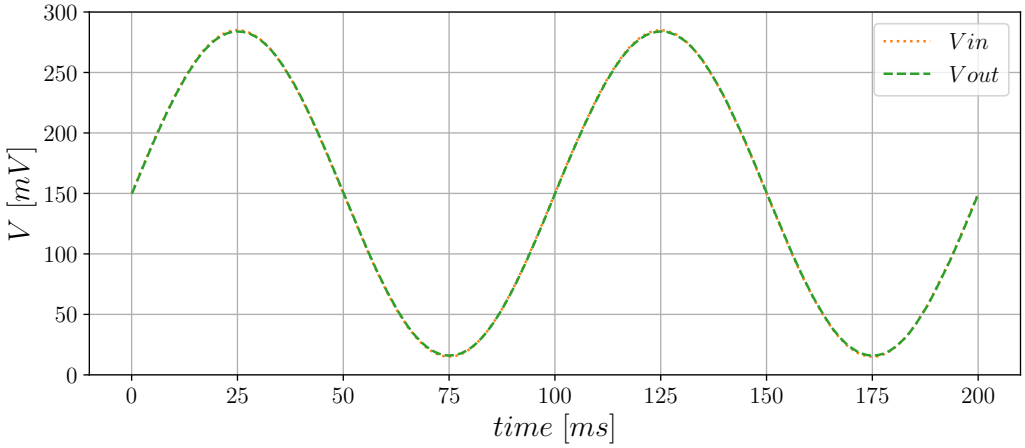

Figure 9. Response of the proposed OTA to a 10 Hz 270 mVpp sinusoidal input signal.

The input common-mode range is rail-to-rail, as can be observed from Figure 10 which reports the input–output DC characteristic when the OTA is closed in a non-inverting buffer configuration.

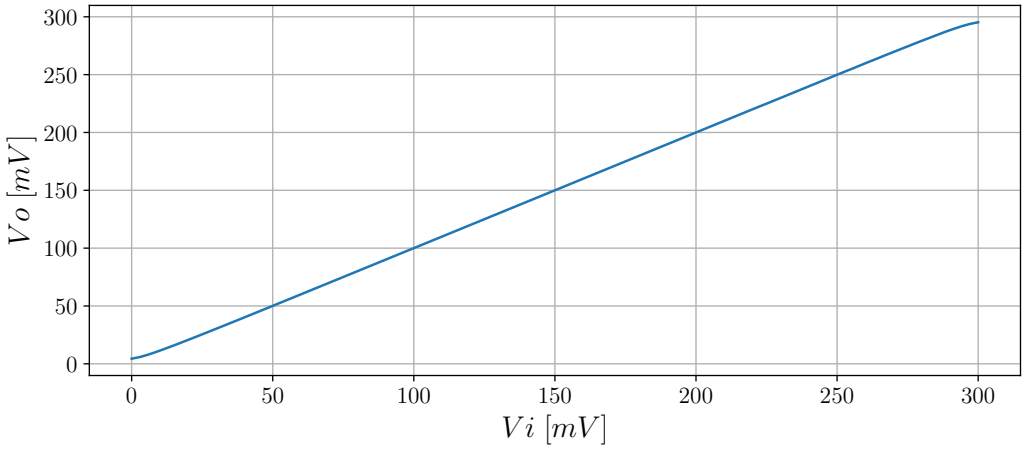

Figure 10. Input–output DC characteristic in a non-inverting buffer configuration.

Table 2 also reports the effects of variation of process corners, temperature (0 °C and 80 °C), and supply voltage (±10%). Biasing is extremely robust, as evidenced by values of (systematic) offset and power consumption that remain fairly constant, and this reflects on OTA performance. Larger variations are reported for the slew rate, which depends on the second stage, where the proposed bias approach was not applied. The table also includes the input bias current I_{in}, the value of which remains extremely low under PVT variations, justifying the body-driven approach in this ultra-low voltage environment. Table 3 also shows the combined effect of process and supply/temperature variations, highlighting the good robustness of the proposed approach.

Table 3. Characterization of the proposed OTA under voltage and temperature variations combined with corners.

Corner	**FF**				**SS**				**SF**				**FS**			
VDD	**0.27**		**0.33**		**0.27**		**0.33**		**0.27**		**0.33**		**0.27**		**0.33**	
Temp	**0**	**80**	**0**	**80**	**0**	**80**	**0**	**80**	**0**	**80**	**0**	**80**	**0**	**80**	**0**	**80**
A_{d0} [dB]	58.96	63.71	61.59	66.83	60.56	65.54	63.01	68.77	59.35	64.13	61.89	67.26	60.04	65.10	62.56	68.33
GBW [kHz]	1.199	1.842	1.393	2.288	1.292	2.126	1.408	2.658	1.205	1.910	1.359	2.374	1.256	2.044	1.393	2.550
$m\varphi$ [deg]	65.850	55.190	63.240	47.970	60.930	49.870	58.690	42.460	64.330	53.910	61.630	46.660	62.770	51.050	60.540	43.730
A_{c0} [dB]	−54.060	−25.610	−58.620	−31.920	−30.440	−9.590	−26.270	−20.700	−10.510	−16.030	−29.370	−32.120	−21.430	−14.320	−18.470	−26.970
$CMRR$ [dB]	113.020	89.320	120.210	98.750	91.000	75.130	89.280	89.470	69.860	80.160	91.260	99.380	81.470	79.420	81.030	95.300
$PSRR$ [dB]	82.090	76.450	95.380	95.503	51.834	101.320	75.120	81.980	78.660	87.160	90.890	78.420	44.780	93.240	74.240	79.780
P_D [nW]	8.563	8.065	10.990	9.919	8.131	7.940	10.050	9.839	8.177	8.015	10.190	9.858	8.416	8.009	10.620	9.899
V_{off} [mV]	−0.194	0.135	−0.103	0.165	−0.195	0.135	−0.105	0.165	−0.194	0.135	−0.104	0.165	−0.195	0.135	0.165	0.165
SR_p [V/s]	75.750	58.060	116.400	85.030	79.970	55.320	122.800	76.530	76.150	57.220	116.700	81.620	79.100	54.860	121.800	75.840
SR_m [V/s]	52.700	40.030	75.230	52.170	57.600	41.700	82.980	49.670	56.910	40.740	82.340	51.970	53.160	38.250	75.690	48.620
SR_{avg} [V/s]	64	49	96	69	69	49	103	63	67	49	100	67	66	47	99	62
IRN [µV/$\sqrt{\text{Hz}}$]	1.650	1.369	1.582	1.318	1.629	1.338	1.570	1.288	1.686	1.379	1.625	1.328	1.601	1.331	1.527	1.282
THD (10 Hz, 1 mVpp) [%]	0.241	0.241	0.238	0.239	0.240	0.239	0.238	0.241	0.240	0.239	0.240	0.239	0.242	0.239	0.238	0.239

The effect of mismatches has also been considered by running 200 Monte Carlo mismatch simulations to evaluate the robustness of the design. A summary of the Monte Carlo simulation results is reported in Table 4, together with the nominal values of the different performances for comparison. Overall, a low offset voltage and robust performance are achieved. Furthermore, linearity performance remains good when mismatches are considered. Mismatches mostly affect the common-mode gain, resulting in a worsening of CMRR and similarly of PSRR. In the presence of mismatches, the common-mode cancellation due to the current mirror load is no longer effective, as is common in all structures of this kind; however, the effect of the replica loop, as shown in (20), remains and provides performance that is still acceptable, similarly to the case of standard tailed differential pairs.

Table 4. Mismatch Monte Carlo simulations.

	Typ	**μ**	σ
V_{off} [mV]	0.013	0.187	1.95
A_{d0} [dB]	65.54	65.53	0.009
GBW [kHz]	1.98	1.98	0.045
$m\varphi$ [deg]	49.87	49.88	0.86
$CMRR$ [dB]	120.3	62.82	7.141
$PSRR$ [dB]	121.06	75.58	8.75
SR_p [V/s]	83.89	83.63	3.57
SR_m [V/s]	59	58.87	1.99
SR_{avg} [V/s]	71.445	71.25	2.78
P_D [nW]	9	9.00	0.323
I_{in} [fA]	349.7	349.5	7.245
THD (10 Hz, 270 mVpp) [%]	0.24	0.233	0.016

Table 5 compares the performance of the proposed OTA with state-of-the-art sub-0.4V results from recent literature. Commonly used figures-of-merit

$$FOM_S = \frac{GBW \cdot C_L}{P_D} \tag{33}$$

$$FOM_L = \frac{SR \cdot C_L}{P_D} \tag{34}$$

are calculated and reported to allow a fair comparison. The proposed OTA presents values of FOM_S, $CMRR$, and noise that compare well to the state-of-the-art, and presents the best results in terms of linearity. The output stage was not optimized for slew rate, resulting in a low value of FOM_L that is, however, comparable to some of the reported results [30,35,43].

Table 5. Comparison with state-of-the-art sub-0.4V OTAs.

	This Work	[24]	[44]	[43]	[41]	[39]	[59]	[22]	[35]	[34]	[33]	[31]	[30]
Year	**2023**	**2023**	**2023**	**2022**	**2022**	**2022**	**2021**	**2021**	**2020**	**2020**	**2020**	**2018**	**2017**
Tech [nm]	180	28	130	130	65	130	180	180	65	180	180	180	130
V_{DD} [V]	0.3	0.3	0.3	0.3	0.25	0.3	0.35	0.3	0.25	0.3	0.3	0.3	0.25
V_{DD}/V_{th}	0.6	–	0.86	0.86	–	0.86	0.7	0.6	–	0.6	0.6	0.6	–
A_{d0} [dB]	65.54	66.39	86.83	41.28	90.88	52.92	83	30	70	98.1	68.9	65.8	63
C_L [pF]	200	250	35	250	100	50	10	150	15	30	30	20	15
GBW [kHz]	1.981	12.29	10.32	7.95	31.22	35.16	24.78	0.25	9.5	3.1	2.96	2.78	6.23
$m\varphi$ [deg]	49.87	68.42	58.27	52	78.18	52.4	61.48	90	89.9	54.2	52	61.2	62.5
$CMRR$ [dB]	62.82 *	105.7 **	57.8 *	35.28 **	74.8 **	42.11 *	98.59 **	41 ***	62.5 **	60 ***	110 ***	72 ***	69.8 **
$PSRR$ [dB]	75.58 *	74.59 **	46.59 *	74.41 **	113.75 **	56.13 *	94.74 **	30 ***	38 **	61 ***	56 ***	62 ***	66.5 **
SR_p [V/ms]	0.08389	3.51	2.5	1.25	8.61	18.61	2951	–	2	14	1.9	6.44	–
SR_m [V/ms]	0.05898	2.87	5	1.25	8.61	11.51	2869	–	2	4.2	6.4	7.8	–
SR_{avg} [V/ms]	0.072	3.19	3.75	1.25	8.61	15.06	2910	0.085	2	9.1	4.15	7.12	2.15
THD [%]	0.24	1.72	0.2	3.15	–	0.673	–	2	–	0.49	–	1	0.3
at swing [%]	90	83	73	90	–	90	–	90	–	83	–	93	60
IRN [$\mu V/\sqrt{Hz}$]	1.43	2	2.85	1.4	4.36	1.6	0.18	21	–	1.8	1.6	1.85	17.6
at freq [Hz]	1000	1000	10,000	10,000	1000	1000	1000	–	–	–	–	–	0.1
P_D [nW]	9	44	33.73	120	32.77	21.89	35.04	2.4	26	13	12.6	15.4	20
Mode	BD	DIG	BD	BD	BD	BD	GD	DIG	BD	BD	BD	BD	BD
Area [μm^2]	1410	625	2340	2350	3300	5200	13470	982	2000	9840	8500	8200	–
FOM_S	44.022	69.83	10.709	16.563	95.27	80.311	7.072	15.625	5.481	7.154	7.048	3.61	4.673
FOM_L	1.6	18.125	3.891	2.604	26.274	34.399	830.479	5.313	1.154	21	9.881	9.247	1.613

BD = body-driven; GD = gate-driven; DIG = digital. * = Monte-Carlo mean; ** = typical; *** = measured.

4. Conclusions

Robust biasing is critical in ULV environments, where tail current generators cannot be used, making it difficult to control the bias current of (pseudo)-differential stages. Moreover, the lack of tail current generators affects CMRR, which relies solely on the cancellation of identical paths and is limited by the gain error of the current mirror. In this paper, we have proposed a biasing approach based on a replica loop and the use of auxiliary amplifiers. The amplifiers provide super-diodes to minimize the gain error of the current mirrors, and the replica loop allows the sum of the currents of the input devices of the OTA to be kept constant against PVT and input common-mode variations. The use of the auxiliary amplifiers maximizes the matching of the drain-source voltages of devices in the main and replica pairs, and allows different values for drain-source and gate-source voltages to be set, optimizing the bias point. Simulations in a 180 nm CMOS technology show high robustness of bias point and performance in the face of PVT variations, high CMRR, though it is still affected by mismatches, and very high linearity. A two-stage OTA provides about 65 dB gain, 2 kHz unity-gain bandwidth on a 200 pF load, 9 nW power consumption, and FOM_S and noise levels comparable with the state-of-the-art.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-Digital Converter
BD	Body-driven
CAD	Computer-Aided Design
CMFB	Common-Mode Feedback
CMFF	Common-Mode Feedforward
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
D2S	Differential-to-Single-Ended
DIBL	Drain-Induced Barrier Lowering
DIGOTA	Digital Operational Transconductance Amplifier
GBW	Gain-bandwidth product
GD	Gate-driven
IB	Inverter-based
IoT	Internet-of-Things
LDO	Low-Dropout Regulator
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
PVT	Process, supply voltage and temperature
SR	Slew Rate
THD	Total Harmonic Distortion
ULP	Ultra-Low Power
ULV	Ultra-Low Voltage
UOPA	Unbuffered Operational Amplifier

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