Compact E-band I/Q Receiver in SiGe BiCMOS for 5G backhauling applications

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***Abstract*— The implementation of backhauling links poses several challenges to the designers which are requested to limit the hardware costs in the framework of complex millimeter wave radio systems. This work presents a monolithically integrated E-band I/Q receiver covering the whole bandwidth from 71 to 86 GHz. The chip was implemented in a 55 nm SiGe BiCMOS technology which allows reaching a high level of integration. The receiver is based on a Low Noise Amplifier (LNA) stage and a Variable-Gain Amplifier (VGA) which provide a -11 dBm IP1dB. A double balanced mixer provides I/Q baseband outputs through a reduced-size differential phase shifter which allows to contain the chip size to 1.8 mm².**

***Index Terms*—Backhaul, BiCMOS integrated circuits, E-band, Point to point communication, SiGe, Wideband receiver front-end**

I. Introduction

Backhauling links are the interconnections between the core of a telecommunication network and its peripheral nodes (e.g. base stations), shown in Fig. 1. They are receiving increasing attention as they play a key role in sustaining the huge fronthaul data rate [1], [2]. This aspect will be further augmented in 5G networks where the proliferation of the number of cells will demand the use in large scale of high-capacity wireless backhauling links [3]. In this context, the use of point-to-point (P2P) millimeter wave radio links (i.e. E-band, 71–76 and 81–86 GHz) is a very promising technology for several reasons: i) the high capacity that can be reached (with 10 GHz of spectrum available), ii) the very large channel bandwidths (up to 2 GHz), and iii) the links are often licensed under a "light license" process that can be obtained quickly and at a fraction of the cost of traditional link licenses.

One of the key cost drivers of the E-band backhauling networks is related to the transceiver which became a key research topic over the last few years. Transceivers should be monolithically integrated and should adapt to various

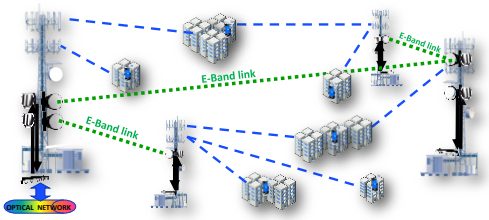

Fig. 1 Targeted application: SiGe E-band Receiver for 5G backhaul.

modulation transmission formats, including low-power high quadrature amplitude modulation (QAM) and high-power constant envelop modulation. Therefore, the key elements of innovation are the linearity of its response, the dynamic range, and also the area from which depends the chip cost. Several examples of monolithically integrated chipsets were proposed in different technologies. In [4] and [5], examples of E-band receivers in 0.1µm GaAs pHEMT are presented. More recently, a 2x2 transceiver module in 22nm FinFET CMOS process [6], and a W-band receiver based on 90 nm CMOS technology [7] have been also demonstrated. The specific application context makes SiGe BiCMOS technologies a breakthrough in the system concept enabling a mixed signal design including mmWave, baseband, and digital functionalities embedded into a single chip. First examples of fully integrated SiGe E-band transceiver chipsets for broadband P2P communication were presented in [8] and [9]. An E-band quadrature receiver in 0.35-µm SiGe BiCMOS process [10], and a receiver front-end for phased-array applications [11] were also reported.

In this paper, a highly integrated SiGe BiCMOS E-band I/Q receiver is presented. The proposed design covers the mmWave band from 70 to 88 GHz continuously, based on the SiGe BiCMOS 55nm semiconductor technology [12], [13]. The proposed design fully exploits the mixed-signal capabilities of the selected technology, and it features an ultra-compact broadband differential phase shifter. In Section II, a brief overview of the technology is shown. In Section III, the IC building block implementation is presented, and its peculiarities

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are highlighted. In Section IV, the measurement results are reported and the comparison with the state of the art is carried out. Finally, in Section V, the conclusions are drawn.

II. TECHNOLOGY OVERVIEW

In radio access, backhauling, and core networks field, silicon technology has enabled the development of high-frequency critical subsystems: *i)* RF and mmWave front-end modules in massive MIMO antennas and in multiband P2P radios, and *ii)* high-speed optical modules. This has allowed the so-called front-end module (FEM) to support new IC active devices operating at a higher frequency and larger bandwidth [14].

Si/SiGe:C Heterojunction Bipolar Transistor (HBT) based BiCMOS technologies, mainly addressed the automotive radar market, have gained increasing interest for emerging mmWave markets, as f_T and f_{MAX} of the HBTs have exceeded 200 GHz. The combination of: *i)* high frequency performance of the bipolar transistors, providing high speed and gain that are critical for high-frequency analog sections, *ii)* CMOS technology, excellent for building low-power logic functions, and *iii)* Back End Of Line (BEOL) that includes an upper layer with thicker copper for improved quality factor at mmWave of the passive devices (inductor, capacitors and transmission lines), makes the 55-nm SiGe BiCMOS (BiCMOS055) developed by STMicroelectronics [12] the process technology optimized for mixed-signal high frequency IC chip sets, for applications in cellular network, mmWave backhauling, front-hauling, satellite communication and radar.

The E-band receiver presented in this paper has been designed on this process. The technology, developed on a 300 mm wafer, allows the design of RF circuits for applications up to 0.5 THz. In fact, the BEOL has been developed to meet the requirements of mmWave applications and it consists of eight metallic layers and a final layer of aluminum. Moreover, the technology features Low Power (LP) and General Purpose (GP) CMOS transistors, high quality MIM capacitors with 5fF/μm² and High-Speed HBT that exhibits f_T and f_{MAX} of 320 and 370 GHz, respectively. The collector–emitter breakdown voltage (BVCEO) and the collector–base breakdown voltage (BVCBO) of the bipolar transistors are 1.5 V and 5.2 V, respectively. It is worth noting that there is a strong push to continuously improve SiGe HBT performances to provide high speed and gain that are critical for high-frequency analog sections. Such a request has a first answer with the architecture that is being developed in the new envisaged process, named ST BiCMOS055X, to target 400 GHz f_T and 600 GHz f_{MAX}, which is mandatory for 6G [14].

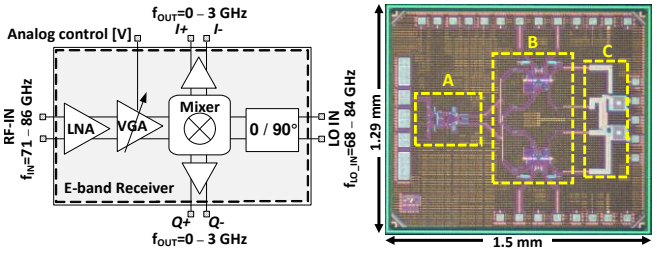


Fig. 2. a) Proposed SiGe E-band receiver block diagram, b) Die photograph of the E-band Receiver fabricated in BiCMOS055. In detail: A) LNA-VGA, B) I/Q mixer and output buffers, and C) 0/90° hybrid on LO chain. Die size is (1.5 x 1.29) mm².

III. SIGE E-BAND RECEIVER

The E-band receiver consists of a Low Noise Amplifier (LNA), a Variable-Gain Amplifier (VGA), a differential phase shifter on the local oscillator chain, and a double balanced mixer that provide I and Q outputs. The block diagram of the receiver and chip photo are shown in Fig. 2-a and 2-b, respectively.

A. E-band LNA-VGA chain

The front-end stage at E-band has been designed to provide more than 20 dB gain control, by exploiting the chain of a tuned LNA stage at fixed gain followed by a broadband VGA, as shown in Fig. 3. The LNA and VGA blocks have been designed as two sub-sections of the front-end with separate specifications, in order to achieve the overall front-end requirements. In particular, the first stage shows more gain and is biased at a lower current to reduce overall Noise Figure (NF), while the second stage has been designed with larger emitter degeneration to improve linearity performance. Most of the gain for the LNA-VGA front-end has been specified for the first LNA cell, in order to set the required NF value even in receiver attenuation mode. The VGA has been designed to show a loaded gain as low as 3 dB by means of a larger degeneration, so that receiver linearity at maximum input power level is guaranteed. It has been designed without tuned load in order to achieve a larger overall bandwidth for the receiver. The LNA stage is implemented as a tuned cascode differential cell to get the best performance at mmWaves in terms of gain, bandwidth, stability, linearity, and reverse isolation. The Q-factor and the bandwidth of the LNA stage is set by means of a bridge resistor placed between the collectors of the common-base devices. A T-network, not shown in Fig. 3, allows matching to the input transition. Linearization of both LNA and VGA cells is provided by inductive degeneration, synthesized by means of low-width microstrip lines. The second stage has been designed with larger bias current and larger degeneration with respect to the first stage, to improve linearity: second stage degeneration L_{E2} corresponds to 19 Ω at 80 GHz, and has to be compared to R_{C2} = 27 Ω; first stage degeneration L_{E1} is about 5 Ω at 80 GHz, much lower than the parallel between L_C and $R_C/2$ (about 11.5 Ω at 80 GHz). The VGA circuit, based on Gilbert cell topology, works also as the buffering stage to the following I/Q down-conversion mixer: VGA output termination was specified to 50 Ω differential in order to permit easier matching to the

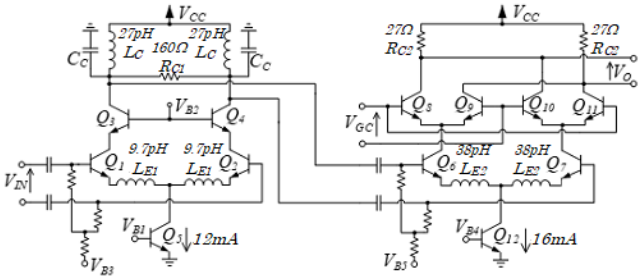


Fig. 3. Simplified schematic of the E-band LNA-VGA stages.

50 Ω mixer input termination. The VGA topology in Fig. 3 is based on current cancellation on R_{C2} resistors: when control voltage V_{GC} is set to 0, devices Q_8-Q_{11} drain the same current, and maximum attenuation is achieved; maximum gain is obtained when Q_9 and Q_{10} devices are switched-off. A MOS differential pair produces the proper V_{GC} value from an external control voltage. The chosen VGA topology has allowed to guarantee proper operation of the receiver at worst-case condition for linearity: at maximum attenuation, where a max-power input signal is expected, all devices of the Gilbert cell are operated in active region, so leading to better linearity. All passive structures are designed by EM simulations. Special care has been paid in preserving layout symmetry: in particular, for the VGA stage it is essential to provide current cancellation at maximum attenuation. Simulations have highlighted 8.8 dB peak gain at minimum attenuation. In the 70–90 GHz band, NF is ranging from 8.7 to 10 dB. At -12.5 dB peak gain, the IIP3 is higher than 6.7 dBm.

B. *I/Q Mixer and DC-coupled output buffers*

The I/Q down-conversion stage is composed of two Gilbert cells driven by inductive degenerated transconductors and loaded by output buffers. DC-coupling has been chosen to allow down-conversion function both at IF and at base-band. A passive matching network provides driving of the two transconductors at the I/Q mixer inputs, and a wideband matching network has been designed also at the LO differential ports. All matching networks have been designed as low-Q T-shape networks, composed of series low-width microstrip lines working as inductors, and MIM shunt capacitors. The density currents and sizes of the active devices have been chosen to provide the best compromise between conversion gain value and flatness in the 70–90 GHz band, and intermodulation and noise minimization. The DC-coupled buffer stages are differential pairs with 50 Ω resistive loads, to provide output matching to the external 100 Ω differential termination up to at least 12 GHz. Post layout simulations have shown conversion-gain higher than 8.3 dB, NF with a maximum of 14.6 dB at 90 GHz, and minimum IIP3 value of 5.7 dBm at 70 GHz.

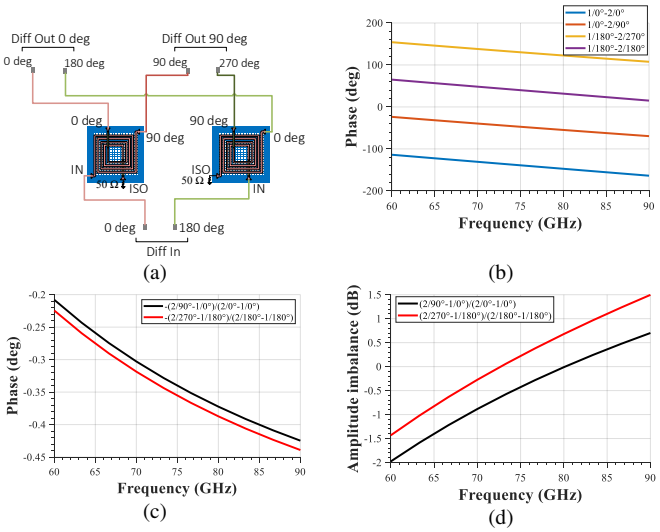


Fig. 4. E-band phase shifter: a) layout and simulated b) output phases, c) phase imbalance and, d) amplitude imbalance.

C. *LO E-band phase shifter*

The E-band differential phase shifter block has been designed to split the differential input signal from the LO input into two differential pairs in phase quadrature. To minimize the occupied area while providing a wideband response, a configuration using a pair of single-ended quadrature couplers implemented using intertwined coils was taken into account, as shown in Fig. 4-a. Compared to other solutions [15], the one proposed in this work reduces the area required for the phase delay transmission line networks, which are only required in the final routing stage. On the other hand, the two hybrid quadrature couplers are designed to provide a wideband phase response. The entire architecture was analyzed through full-wave simulations [16]. The evaluation of the performance was done taking into account different parameters, the first of which is related to the phase offset between the input and output ports. The simulated values, reported in Fig. 4-b, show the phase of the transmitted signal. The imbalance of phase offset does not exceed 8 degrees over the entire band of interest (Fig.4-c). The transmission losses, shown in Fig. 4-d, indicate an amplitude imbalance between the two ports which does not exceed ±0.4 dB at the two extremes of the band (60.84–87 GHz). The overall size of the hybrid is 638.2 × 249.63 μm^2.

IV. Measurements Results

In order to characterize the proposed E-band receiver (RX) developed in ST BiCMOS055 process, a demonstrator has been assembled on a test board specifically developed. Simplified block diagram and microphotograph of the receiver chain are shown in Fig. 5 and Fig. 6, respectively.

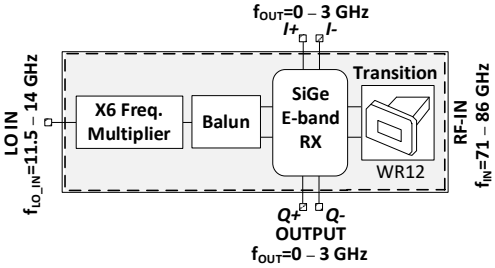


Fig. 5. Block diagram of SiGe E-band receiver chain.

The structure is composed by: *i)* E-band RX, *ii)* GaAs X6 frequency multiplier, *iii)* RF input transition, from waveguide to die, developed on Alumina substrate, *iv)* E-band balun on Alumina for the LO chain and a microstrip line on Alumina to connect the LO input signal to the external LO. System measurements are carried out by using single tone signal generators and E-band radios (SIAE ALFO Plus 80HDX). Moreover: *i)* a signal generator has been used to drive the LO input of the demo board to generate the proper LO input of the E-band RX by driving the X6 frequency multiplier, and *ii)* a spectrum analyzer and a NF meter have been used to record signal spectrum which are shown in all the following graphs. Twelve power supplies and a full set of passive structures over alumina, teflon-based (PCB) and GaAs substrates have been

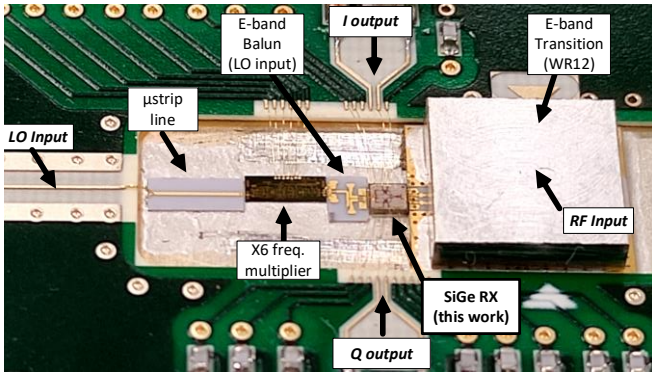


Fig. 6. Microphotograph of the SiGe E-band receiver chain.

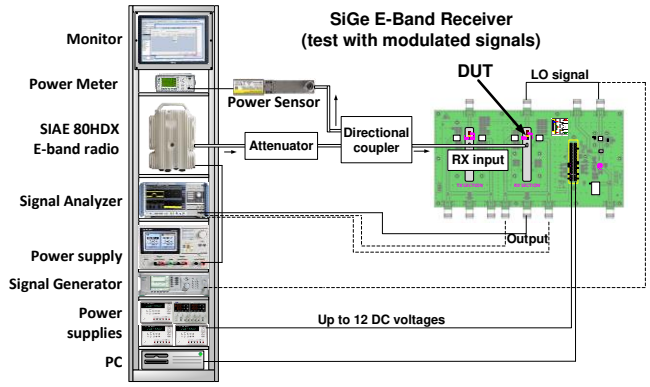


Fig. 7. Experimental setup for the characterization of the SiGe E-band receiver chain with modulated signals.

designed. I.e.: *i)* microstrip lines, *ii)* matching networks, *iii)* baluns, *iv)* attenuators, and *v)* die-to-waveguide transitions for both 71–76 GHz and 81–86 GHz frequency bands. In Fig. 7 one of the testbenches used to characterize the demonstrator is shown. E-band RX has shown conversion gain (I or Q output) in the range of 10-15 dB, NF between 11.7 and 14.5 dB, and more than 30 dB of gain-control dynamic range in the whole E-band.

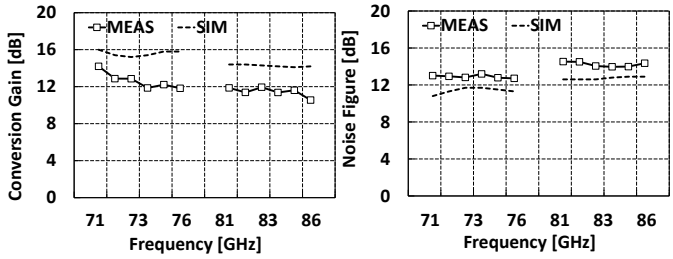


Fig. 8. a) Measured vs simulated Conversion Gain of the receiver, and b) Measured vs simulated NF of the receiver @Max-Gain.

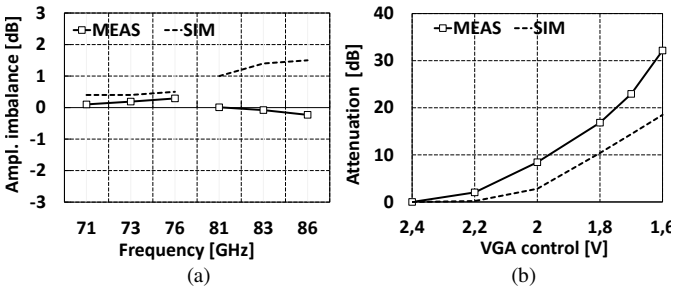


Fig. 9. a) Measured I/Q imbalance of the receiver, and b) Gain variation as a function of VGA control voltage at 72 GHz.

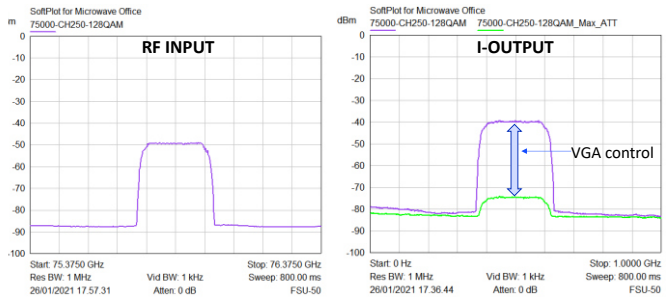


Fig. 10. Test #1 – RF freq. =75 GHz and IF out = 500 MHz (I-output).

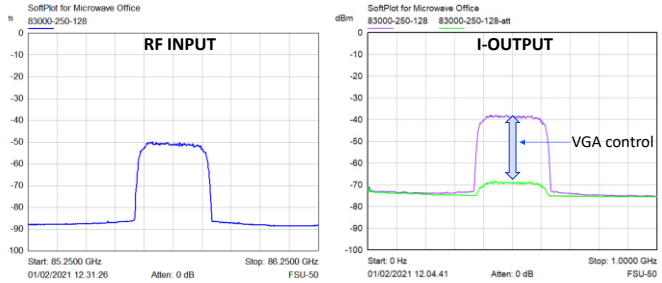


Fig. 11. Test #2 – RF freq. =83 GHz and IF out = 500 MHz (I-output).

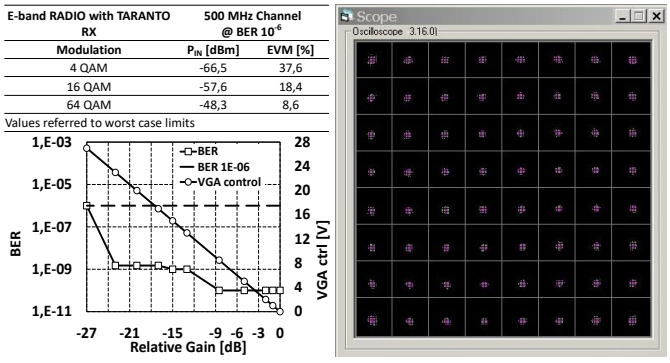


Fig. 12. Test #3 Input freq.= 73 GHz – EVM [%], BER VS RF input control with P_{IN}=-19.5dBm, and 64 QAM received modulation.

Measurement results of conversion gain and NF compared to post-layout simulations are shown in Fig. 8-a and 8-b, respectively. In Fig. 9-a and 9-b the I/Q amplitude imbalance for both the lower and the upper bands and the gain variation as a function of VGA control voltage at 72 GHz, respectively, are shown. Another set of measurements have been performed by using E-band radios as signal generators. Several modulated signals have been sent to the E-Band RX. Measurement results have been shown in Fig. 10-13, and in particular: *i)* Fig. 10 and Fig. 11 show the measurement results with modulated signals (250 MHz and 128 QAM), RF inputs at 75 and 82 GHz and IF output at 500 MHz (at max and min attenuation), *ii)* Fig. 12 shows the results of a setup where EVM values up to 64 QAM, Bit Error Rate (BER) VS RF input control with P_{IN}=-19.5 dBm to check the link robustness, and 64 QAM received modulation at 73 GHz have been measured, and *iii)* Fig. 13 shows the base-band I-output with RF modulated signals (RF input signals at 72 and 83 GHz, 250–500–1000–2000 MHz channels and 128 QAM modulation scheme). Finally, by considering the performance of the E-band RX, the specification of a typical E-band transmitter, the rain factor of about 42 mm/h, and an

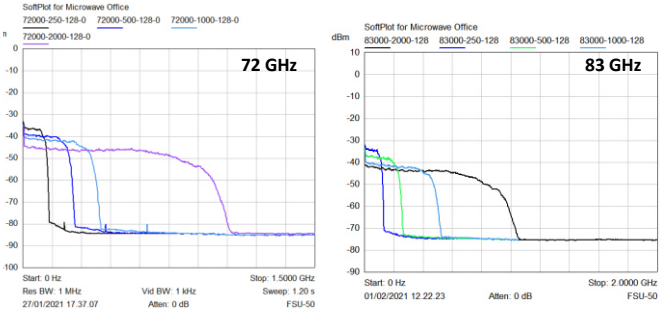
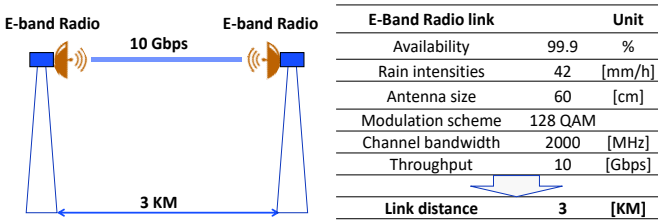


Fig. 13. Test #4 – BB I-Output (250, 500, 1000, and 2000 MHz channels).



E-Band Radio link		Unit
Availability	99.9	%
Rain intensities	42	[mm/h]
Antenna size	60	[cm]
Modulation scheme	128 QAM	
Channel bandwidth	2000	[MHz]
Throughput	10	[Gbps]
Link distance	**3**	**[KM]**

Fig. 14. Point-to-point link by using the developed SiGe E-band Receiver.

availability of 99.9%, it is possible to set a 3 Km link, as reported in the Fig. 14. The receiver performance is compared in Table I to BiCMOS E-band receivers presented in recent years. The chip size and power dissipation are compatible, while better linearity is observed at the expense of higher NF. It is worth noting that the presented demonstrator also includes the die-to-waveguide input transition. The high gain control range is the other distinguishing feature, which allows for a high input linear dynamic range of the receiver.

TABLE I
COMPARISON TO OTHER BICMOS E-BAND RXS

	[9]	[8]	[10]	[11]	**This work**
Bandwidth [GHz]	71–76 & 81–86	71–76 & 81–86	70–90	56–79	**70–88**
Gain [dB]	60	70	17–23	18.5	**10-15**[4]
NF [dB]	8.5	< 7	8-12	9	**13–14**[4]
Gain control [dB]	yes	> 65	no	yes	**> 30**
IP_{-1dB} [dBm]	-	-	-22	-24	**-11.5**[3]
IIP3 [dBm]	-30	-12	-	-	**-**
P_{DC} [mW]	600	650	760	116	**470**
Size [mm²]	4.9[1]	6.1[1]	2.5[1]	0.86[2]	**1.8**
Technology	130 nm	130 nm	350 nm	130 nm	**55 nm**

[1]LO generator is included, [2]Core area only, [3]Measured on a stand-alone LNA-VGA block, [4]Die-to-waveguide input transition included.

V. CONCLUSION

This work presents a first example of a highly integrated E-band receiver covering the frequency range from 70 to 88 GHz and realized using a 55nm SiGe BiCMOS technology. The chip was implemented to cover the whole backhauling bandwidth for telecommunication applications. An exhaustive experimental assessment was conducted to validate the chip performance. Measured results have confirmed that the chip offers a highly linear response with an IP1dB of the amplification stage of -11.5 dBm. Moreover, thanks to the optimization of each building block, the chip area is limited to 1.8 mm^2. The proposed device represents a valid alternative for high-capacity backhauling links, and it is capable to handle a 10 Gbps link.

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Compact E-band I/Q Receiver in SiGe BiCMOS for 5G backhauling applications

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***Abstract*— The implementation of backhauling links poses several challenges to the designers which are requested to limit the hardware costs in the framework of complex millimeter wave radio systems. This work presents a monolithically integrated E-band I/Q receiver covering the whole bandwidth from 71 to 86 GHz. The chip was implemented in a 55 nm SiGe BiCMOS technology which allows reaching a high level of integration. The receiver is based on a Low Noise Amplifier (LNA) stage and a Variable-Gain Amplifier (VGA) which provide a -11 dBm IP1dB. A double balanced mixer provides I/Q baseband outputs through a reduced-size differential phase shifter which allows to contain the chip size to 1.8 mm².**

***Index Terms*—Backhaul, BiCMOS integrated circuits, E-band, Point to point communication, SiGe, Wideband receiver front-end**

I. Introduction

Backhauling links are the interconnections between the core of a telecommunication network and its peripheral nodes (e.g. base stations), shown in Fig. 1. They are receiving increasing attention as they play a key role in sustaining the huge fronthaul data rate [1], [2]. This aspect will be further augmented in 5G networks where the proliferation of the number of cells will demand the use in large scale of high-capacity wireless backhauling links [3]. In this context, the use of point-to-point (P2P) millimeter wave radio links (i.e. E-band, 71–76 and 81–86 GHz) is a very promising technology for several reasons: i) the high capacity that can be reached (with 10 GHz of spectrum available), ii) the very large channel bandwidths (up to 2 GHz), and iii) the links are often licensed under a "light license" process that can be obtained quickly and at a fraction of the cost of traditional link licenses.

One of the key cost drivers of the E-band backhauling networks is related to the transceiver which became a key research topic over the last few years. Transceivers should be monolithically integrated and should adapt to various

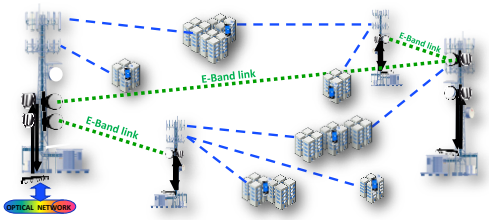

Fig. 1 Targeted application: SiGe E-band Receiver for 5G backhaul.

modulation transmission formats, including low-power high quadrature amplitude modulation (QAM) and high-power constant envelop modulation. Therefore, the key elements of innovation are the linearity of its response, the dynamic range, and also the area from which depends the chip cost. Several examples of monolithically integrated chipsets were proposed in different technologies. In [4] and [5], examples of E-band receivers in 0.1µm GaAs pHEMT are presented. More recently, a 2x2 transceiver module in 22nm FinFET CMOS process [6], and a W-band receiver based on 90 nm CMOS technology [7] have been also demonstrated. The specific application context makes SiGe BiCMOS technologies a breakthrough in the system concept enabling a mixed signal design including mmWave, baseband, and digital functionalities embedded into a single chip. First examples of fully integrated SiGe E-band transceiver chipsets for broadband P2P communication were presented in [8] and [9]. An E-band quadrature receiver in 0.35-µm SiGe BiCMOS process [10], and a receiver front-end for phased-array applications [11] were also reported.

In this paper, a highly integrated SiGe BiCMOS E-band I/Q receiver is presented. The proposed design covers the mmWave band from 70 to 88 GHz continuously, based on the SiGe BiCMOS 55nm semiconductor technology [12], [13]. The proposed design fully exploits the mixed-signal capabilities of the selected technology, and it features an ultra-compact broadband differential phase shifter. In Section II, a brief overview of the technology is shown. In Section III, the IC building block implementation is presented, and its peculiarities

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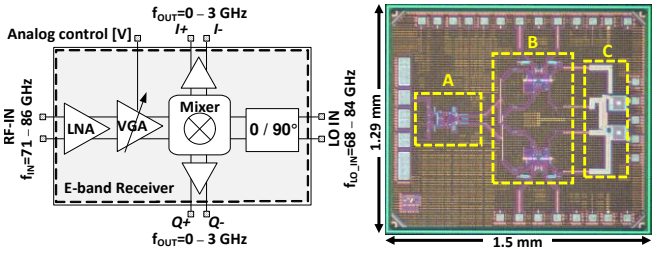
are highlighted. In Section IV, the measurement results are reported and the comparison with the state of the art is carried out. Finally, in Section V, the conclusions are drawn.

II. TECHNOLOGY OVERVIEW

In radio access, backhauling, and core networks field, silicon technology has enabled the development of high-frequency critical subsystems: *i)* RF and mmWave front-end modules in massive MIMO antennas and in multiband P2P radios, and *ii)* high-speed optical modules. This has allowed the so-called front-end module (FEM) to support new IC active devices operating at a higher frequency and larger bandwidth [14].

Si/SiGe:C Heterojunction Bipolar Transistor (HBT) based BiCMOS technologies, mainly addressed the automotive radar market, have gained increasing interest for emerging mmWave markets, as f_T and f_{MAX} of the HBTs have exceeded 200 GHz. The combination of: *i)* high frequency performance of the bipolar transistors, providing high speed and gain that are critical for high-frequency analog sections, *ii)* CMOS technology, excellent for building low-power logic functions, and *iii)* Back End Of Line (BEOL) that includes an upper layer with thicker copper for improved quality factor at mmWave of the passive devices (inductor, capacitors and transmission lines), makes the 55-nm SiGe BiCMOS (BiCMOS055) developed by STMicroelectronics [12] the process technology optimized for mixed-signal high frequency IC chip sets, for applications in cellular network, mmWave backhauling, front-hauling, satellite communication and radar.

The E-band receiver presented in this paper has been designed on this process. The technology, developed on a 300 mm wafer, allows the design of RF circuits for applications up to 0.5 THz. In fact, the BEOL has been developed to meet the requirements of mmWave applications and it consists of eight metallic layers and a final layer of aluminum. Moreover, the technology features Low Power (LP) and General Purpose (GP) CMOS transistors, high quality MIM capacitors with 5fF/μm² and High-Speed HBT that exhibits f_T and f_{MAX} of 320 and 370 GHz, respectively. The collector–emitter breakdown voltage (BVCEO) and the collector–base breakdown voltage (BVCBO) of the bipolar transistors are 1.5 V and 5.2 V, respectively. It is worth noting that there is a strong push to continuously improve SiGe HBT performances to provide high speed and gain that are critical for high-frequency analog sections. Such a request has a first answer with the architecture that is being developed in the new envisaged process, named



(a) (b)

Fig. 2. a) Proposed SiGe E-band receiver block diagram, b) Die photograph of the E-band Receiver fabricated in BiCMOS055. In detail: A) LNA-VGA, B) I/Q mixer and output buffers, and C) 0/90° hybrid on LO chain. Die size is (1.5 x 1.29) mm².

ST BiCMOS055X, to target 400 GHz f_T and 600 GHz f_{MAX}, which is mandatory for 6G [14].

III. SIGE E-BAND RECEIVER

The E-band receiver consists of a Low Noise Amplifier (LNA), a Variable-Gain Amplifier (VGA), a differential phase shifter on the local oscillator chain, and a double balanced mixer that provide I and Q outputs. The block diagram of the receiver and chip photo are shown in Fig. 2-a and 2-b, respectively.

A. E-band LNA-VGA chain

The front-end stage at E-band has been designed to provide more than 20 dB gain control, by exploiting the chain of a tuned LNA stage at fixed gain followed by a broadband VGA, as shown in Fig. 3. The LNA and VGA blocks have been designed as two sub-sections of the front-end with separate specifications, in order to achieve the overall front-end requirements. In particular, the first stage shows more gain and is biased at a lower current to reduce overall Noise Figure (NF), while the second stage has been designed with larger emitter degeneration to improve linearity performance. Most of the gain for the LNA-VGA front-end has been specified for the first LNA cell, in order to set the required NF value even in receiver attenuation mode. The VGA has been designed to show a loaded gain as low as 3 dB by means of a larger degeneration, so that receiver linearity at maximum input power level is guaranteed. It has been designed without tuned load in order to achieve a larger overall bandwidth for the receiver. The LNA stage is implemented as a tuned cascode differential cell to get the best performance at mmWaves in terms of gain, bandwidth, stability, linearity, and reverse isolation. The Q-factor and the bandwidth of the LNA stage is set by means of a bridge resistor placed between the collectors of the common-base devices. A T-network, not shown in Fig. 3, allows matching to the input transition. Linearization of both LNA and VGA cells is provided by inductive degeneration, synthesized by means of low-width microstrip lines. The second stage has been designed with larger bias current and larger degeneration with respect to the first stage, to improve linearity: second stage degeneration L_{E2} corresponds to 19 Ω at 80 GHz, and has to be compared to R_{C2} = 27 Ω; first stage degeneration L_{E1} is about 5 Ω at 80 GHz, much lower than the parallel between L_C and $R_C/2$ (about 11.5 Ω at 80 GHz). The VGA circuit, based on Gilbert cell topology, works also as the buffering stage to the following I/Q down-conversion mixer: VGA output termination was specified to 50 Ω differential in order to permit easier matching to the

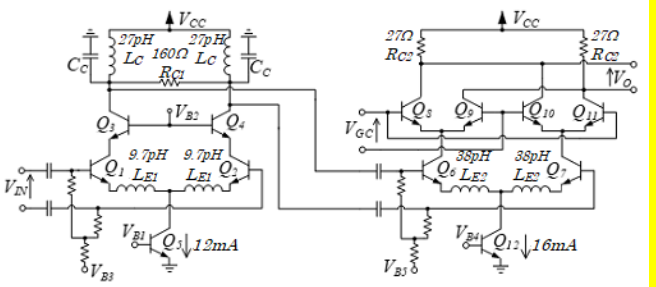


Fig. 3. Simplified schematic of the E-band LNA-VGA stages.

50 Ω mixer input termination. The VGA topology in Fig. 3 is based on current cancellation on R_{C2} resistors: when control voltage V_{GC} is set to 0, devices Q_8-Q_{11} drain the same current, and maximum attenuation is achieved; maximum gain is obtained when Q_9 and Q_{10} devices are switched-off. A MOS differential pair produces the proper V_{GC} value from an external control voltage. The chosen VGA topology has allowed to guarantee proper operation of the receiver at worst-case condition for linearity: at maximum attenuation, where a max-power input signal is expected, all devices of the Gilbert cell are operated in active region, so leading to better linearity. All passive structures are designed by EM simulations. Special care has been paid in preserving layout symmetry: in particular, for the VGA stage it is essential to provide current cancellation at maximum attenuation. Simulations have highlighted 8.8 dB peak gain at minimum attenuation. In the 70–90 GHz band, NF is ranging from 8.7 to 10 dB. At -12.5 dB peak gain, the IIP3 is higher than 6.7 dBm.

B. *I/Q Mixer and DC-coupled output buffers*

The I/Q down-conversion stage is composed of two Gilbert cells driven by inductive degenerated transconductors and loaded by output buffers. DC-coupling has been chosen to allow down-conversion function both at IF and at base-band. A passive matching network provides driving of the two transconductors at the I/Q mixer inputs, and a wideband matching network has been designed also at the LO differential ports. All matching networks have been designed as low-Q T-shape networks, composed of series low-width microstrip lines working as inductors, and MIM shunt capacitors. The density currents and sizes of the active devices have been chosen to provide the best compromise between conversion gain value and flatness in the 70–90 GHz band, and intermodulation and noise minimization. The DC-coupled buffer stages are differential pairs with 50 Ω resistive loads, to provide output matching to the external 100 Ω differential termination up to at least 12 GHz. Post layout simulations have shown conversion-gain higher than 8.3 dB, NF with a maximum of 14.6 dB at 90 GHz, and minimum IIP3 value of 5.7 dBm at 70 GHz.

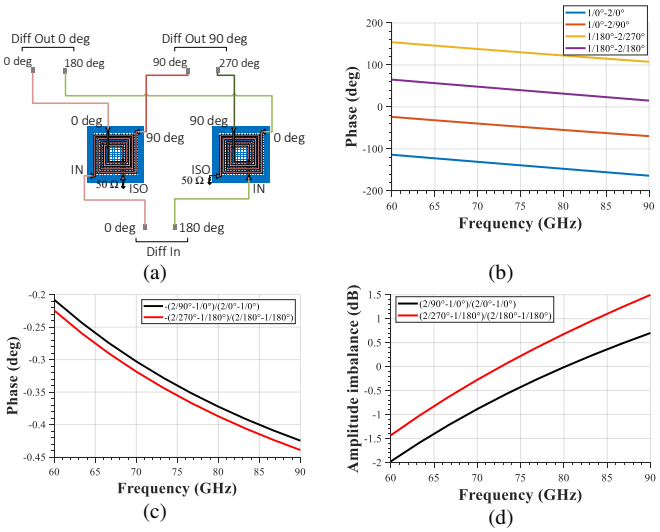


Fig. 4. E-band phase shifter: a) layout and simulated b) output phases, c) phase imbalance and, d) amplitude imbalance.

C. *LO E-band phase shifter*

The E-band differential phase shifter block has been designed to split the differential input signal from the LO input into two differential pairs in phase quadrature. To minimize the occupied area while providing a wideband response, a configuration using a pair of single-ended quadrature couplers implemented using intertwined coils was taken into account, as shown in Fig. 4-a. Compared to other solutions [15], the one proposed in this work reduces the area required for the phase delay transmission line networks, which are only required in the final routing stage. On the other hand, the two hybrid quadrature couplers are designed to provide a wideband phase response. The entire architecture was analyzed through full-wave simulations [16]. The evaluation of the performance was done taking into account different parameters, the first of which is related to the phase offset between the input and output ports. The simulated values, reported in Fig. 4-b, show the phase of the transmitted signal. The imbalance of phase offset does not exceed 8 degrees over the entire band of interest (Fig.4-c). The transmission losses, shown in Fig. 4-d, indicate an amplitude imbalance between the two ports which does not exceed ±0.4 dB at the two extremes of the band (60.84–87 GHz). The overall size of the hybrid is 638.2 × 249.63 μm^2.

IV. Measurements Results

In order to characterize the proposed E-band receiver (RX) developed in ST BiCMOS055 process, a demonstrator has been assembled on a test board specifically developed. Simplified block diagram and microphotograph of the receiver chain are shown in Fig. 5 and Fig. 6, respectively.

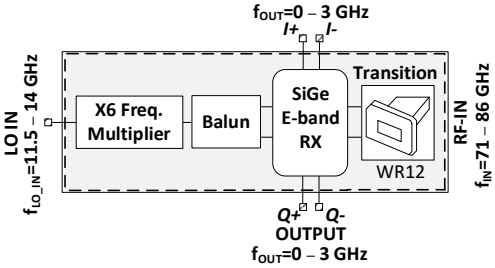


Fig. 5. Block diagram of SiGe E-band receiver chain.

The structure is composed by: *i)* E-band RX, *ii)* GaAs X6 frequency multiplier, *iii)* RF input transition, from waveguide to die, developed on Alumina substrate, *iv)* E-band balun on Alumina for the LO chain and a microstrip line on Alumina to connect the LO input signal to the external LO. System measurements are carried out by using single tone signal generators and E-band radios (SIAE ALFO Plus 80HDX). Moreover: *i)* a signal generator has been used to drive the LO input of the demo board to generate the proper LO input of the E-band RX by driving the X6 frequency multiplier, and *ii)* a spectrum analyzer and a NF meter have been used to record signal spectrum which are shown in all the following graphs. Twelve power supplies and a full set of passive structures over alumina, teflon-based (PCB) and GaAs substrates have been

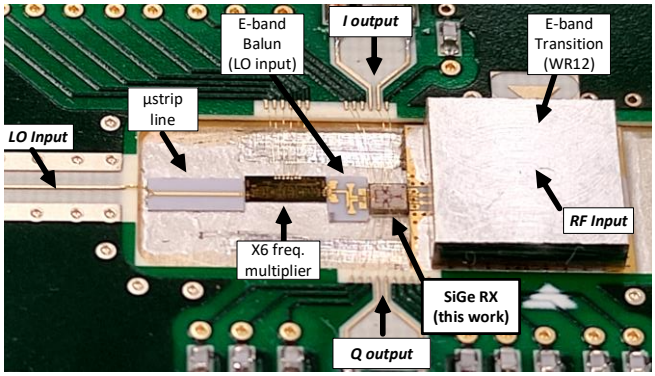


Fig. 6. Microphotograph of the SiGe E-band receiver chain.

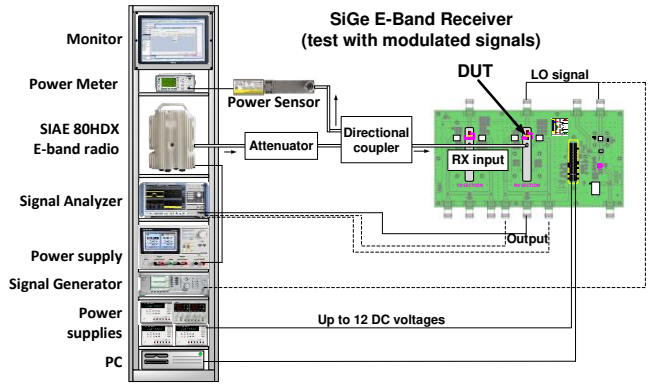


Fig. 7. Experimental setup for the characterization of the SiGe E-band receiver chain with modulated signals.

designed. I.e.: *i)* microstrip lines, *ii)* matching networks, *iii)* baluns, *iv)* attenuators, and *v)* die-to-waveguide transitions for both 71–76 GHz and 81–86 GHz frequency bands. In Fig. 7 one of the testbenches used to characterize the demonstrator is shown. E-band RX has shown conversion gain (I or Q output) in the range of 10-15 dB, NF between 11.7 and 14.5 dB, and more than 30 dB of gain-control dynamic range in the whole E-band.

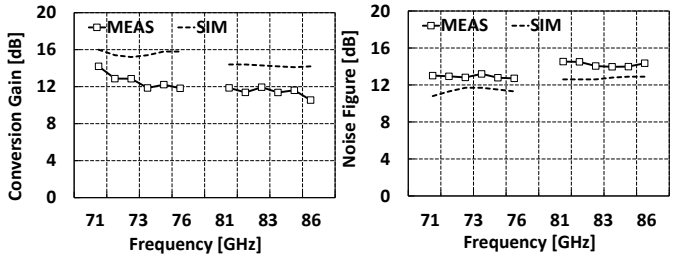


Fig. 8. a) Measured vs simulated Conversion Gain of the receiver, and b) Measured vs simulated NF of the receiver @Max-Gain.

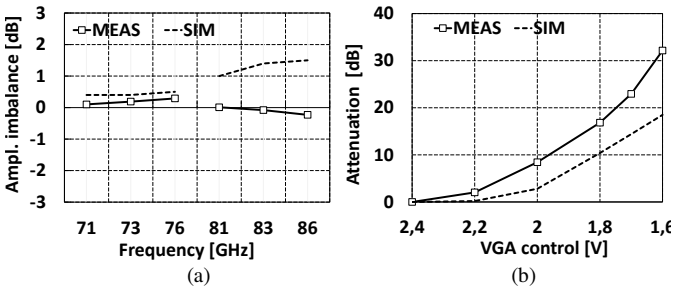


Fig. 9. a) Measured I/Q imbalance of the receiver, and b) Gain variation as a function of VGA control voltage at 72 GHz.

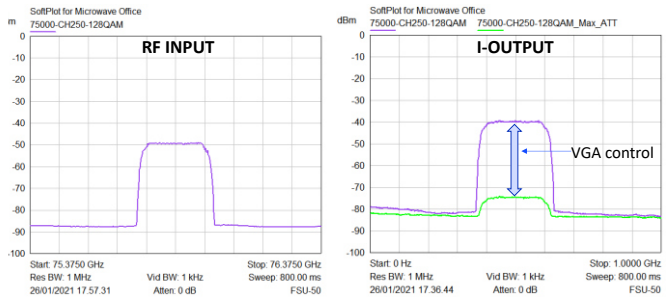


Fig. 10. Test #1 – RF freq. =75 GHz and IF out = 500 MHz (I-output).

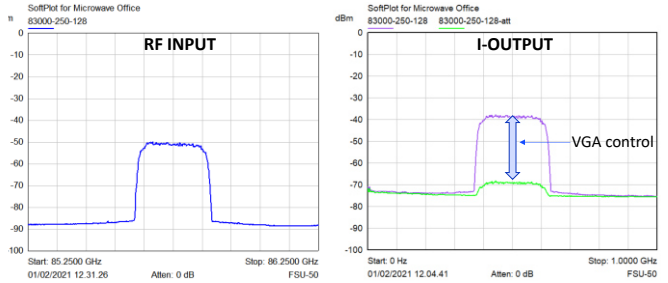


Fig. 11. Test #2 – RF freq. =83 GHz and IF out = 500 MHz (I-output).

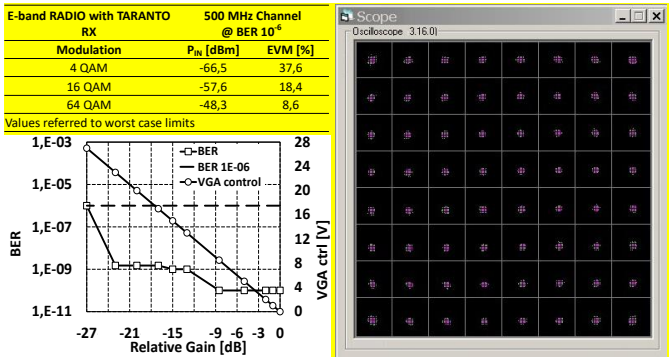


Fig. 12. Test #3 Input freq.= 73 GHz – EVM [%], BER VS RF input control with P_{IN}=-19.5dBm, and 64 QAM received modulation.

Measurement results of conversion gain and NF compared to post-layout simulations are shown in Fig. 8-a and 8-b, respectively. In Fig. 9-a and 9-b the I/Q amplitude imbalance for both the lower and the upper bands and the gain variation as a function of VGA control voltage at 72 GHz, respectively, are shown. Another set of measurements have been performed by using E-band radios as signal generators. Several modulated signals have been sent to the E-Band RX. Measurement results have been shown in Fig. 10-13, and in particular: *i)* Fig. 10 and Fig. 11 show the measurement results with modulated signals (250 MHz and 128 QAM), RF inputs at 75 and 82 GHz and IF output at 500 MHz (at max and min attenuation), *ii)* Fig. 12 shows the results of a setup where EVM values up to 64 QAM, Bit Error Rate (BER) VS RF input control with P_{IN}=-19.5 dBm to check the link robustness, and 64 QAM received modulation at 73 GHz have been measured, and *iii)* Fig. 13 shows the base-band I-output with RF modulated signals (RF input signals at 72 and 83 GHz, 250–500–1000–2000 MHz channels and 128 QAM modulation scheme). Finally, by considering the performance of the E-band RX, the specification of a typical E-band transmitter, the rain factor of about 42 mm/h, and an

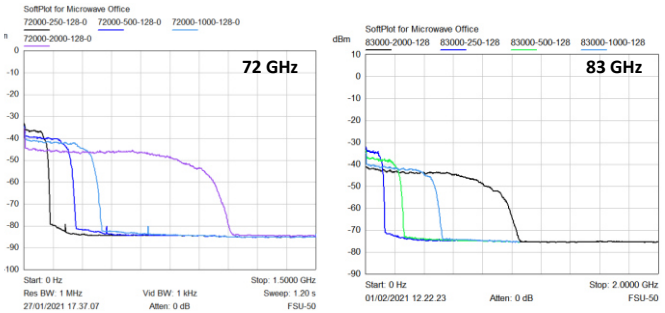
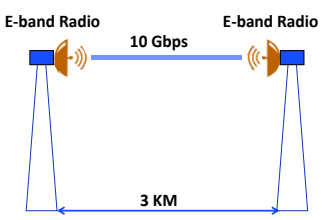


Fig. 13. Test #4 – BB I-Output (250, 500, 1000, and 2000 MHz channels).



E-Band Radio link		Unit
Availability	99.9	%
Rain intensities	42	[mm/h]
Antenna size	60	[cm]
Modulation scheme	128 QAM	
Channel bandwidth	2000	[MHz]
Throughput	10	[Gbps]
Link distance	**3**	**[KM]**

Fig. 14. Point-to-point link by using the developed SiGe E-band Receiver.

availability of 99.9%, it is possible to set a 3 Km link, as reported in the Fig. 14. The receiver performance is compared in Table I to BiCMOS E-band receivers presented in recent years. The chip size and power dissipation are compatible, while better linearity is observed at the expense of higher NF. It is worth noting that the presented demonstrator also includes the die-to-waveguide input transition. The high gain control range is the other distinguishing feature, which allows for a high input linear dynamic range of the receiver.

TABLE I
COMPARISON TO OTHER BICMOS E-BAND RXS

	[9]	[8]	[10]	[11]	**This work**
Bandwidth [GHz]	71–76 & 81–86	71–76 & 81–86	70–90	56–79	**70–88**
Gain [dB]	60	70	17–23	18.5	**10-15**[4]
NF [dB]	8.5	< 7	8-12	9	**13–14**[4]
Gain control [dB]	yes	> 65	no	yes	**> 30**
IP_{-1dB} [dBm]	-	-	-22	-24	**-11.5**[3]
IIP3 [dBm]	-30	-12	-	-	**-**
P_{DC} [mW]	600	650	760	116	**470**
Size [mm²]	4.9[1]	6.1[1]	2.5[1]	0.86[2]	**1.8**
Technology	130 nm	130 nm	350 nm	130 nm	**55 nm**

[1]LO generator is included, [2]Core area only, [3]Measured on a stand-alone LNA-VGA block, [4]Die-to-waveguide input transition included.

V. CONCLUSION

This work presents a first example of a highly integrated E-band receiver covering the frequency range from 70 to 88 GHz and realized using a 55nm SiGe BiCMOS technology. The chip was implemented to cover the whole backhauling bandwidth for telecommunication applications. An exhaustive experimental assessment was conducted to validate the chip performance. Measured results have confirmed that the chip offers a highly linear response with an IP1dB of the amplification stage of -11.5 dBm. Moreover, thanks to the optimization of each building block, the chip area is limited to 1.8 mm^2. The proposed device represents a valid alternative for high-capacity backhauling links, and it is capable to handle a 10 Gbps link.

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Authors' replies

Reviewer: 1

R1.0 This manuscript describes an E-band I/Q receiver fabricated in a 55nm SiGe BiCMOS technoloy. Overall, the paper is well written and provides valuable insight in the design choises.

R1.1 What is the 3 dB BW of the VGA Gilbert cell? Since you terminate the Gilbert cell with a resistor, you are making a broadband circuit and given the high operating frequency, this would give a difficult to achieve constraint on the BW.

The VGA Gilbert cell has been designed to show a loaded gain as low as 3dB, so that indeed it works as a buffer. Most of the gain for the LNA-VGA front-end has been specified for the first LNA cell, in order to achieve a lower NF for the overall receiver. The VGA has been designed with larger degeneration for better overall linearity, so leading to lower gain. This choice has allowed to get a simulated high-frequency cut-off of about 100GHz.

R1.2 Related to the previous question, why did you choose to have a tuned first stage and a broadband second stage?

The first stage is tuned to get higher gain and lower NF for the overall receiver: as the second stage shows low gain, we have chosen to design it as a broadband stage in order to easier achieve a larger overall bandwidth.

R1.3 What are the values of IBias, R_E and L_E? It seems that both the LNA and the VGA have the same tail current, however, the differential pair Q6 and Q7 need to have a larger linearity, dealing with the largest signals of the mmWave front-end. This means that the degeneration of Q6 and Q7 at the target frequency needs to be larger. Is this the case in your design?

Yes, this is the case. The second stage has been designed (and measured) with larger bias current (16mA) and larger degeneration with respect to the first stage (12mA bias current), due to the different requirements in terms of NF and linearity. Second stage degeneration is L_{E2} = 38pH (19Ω at 80GHz) for Q6 and Q7 (to be compared to R_{C2} = 27Ω), while L_{E1} = 9.7pH (about 5Ω at 80GHz, to be compared with L_C = 27pH in parallel to $R_C/2$ = 80Ω, about 11.6Ω at 80 GHz).

In the revised version, the Authors have corrected Fig. 3 in which, erroneously, the output resistors R_{C2} were set to 50Ω and the second stage degeneration was resistive (it is inductive, indeed). The goal output termination for the VGA was specified to 50Ω differential (instead of 100Ω) in order to permit easier matching to the mixer input termination (again specified to 50Ω differential). Now all the values of the passive components are visible in Fig. 3.

R1.4 If possible, can you provide the EVM of the transmission experiments?

At the time of the submission, the measurements were still ongoing. We have continued the measurement session by improving the integration of TARANTO RX in the SIAE E-band radio and closing a point-to-point link with another E-band radio. With the latest system characterization, the EMV was measured (see following table), the sensibility of the system was checked, and the constellation (at the moment up to 64 QAM and with a 500 MHz channel bandwidth) was monitored. We have added this information in the last version of the paper.

E-band RADIO with TARANTO RX	500MHz Channel @ BER 10^{-6}	
Modulation	P_{IN} [dBm]	EVM [%]
4 QAM	-66.5	37.6
16 QAM	-57.6	18.4
64 QAM	-48.3	8.6
Values referred to worst case limits		

R1.5 The stated P1dB of the LNA-VGA is, if I'm not mistaken, the simulated P1dB. Please, if you use simulations in your table, indicate it to avoid confusion. Since your conversion gain is almost 4 dB lower than simulated, the actual P1dB might be different. Could you also try to measure the IIP3 of the receiver?

Indeed, the P1dB was measured for the LNA-VGA front-end only, fabricated as a stand-alone block for characterization purpose. It has been better specified in the revised version of the paper. Unfortunately, the Authors have not been able to perform measurements of receiver IP3 in these days.

Reviewer: 2

Comments to the Authors (Mandatory)

R2.0 The paper present an interesting implementation of an integrated front end for E-band receivers. Extended measurements have shown. The weak point of the paper are the following:

R2.1 circuit novelty is poor, but at this frequency it is interesting to see the design choice which has been made.

The Authors wish to thank the reviewer: a more detailed description has been added in the revised version, to better clarify to the reader the main design choices.

R2.2 in Fig. 2 LNA and VGA are described as two separated blocks, while it seems that they are an unified circuit block. It is not well explained how the gain programability is obtained. I believe this is a fundamental part of the paper.

The LNA and VGA blocks have been designed as 2 sub-sections of the front-end with separate specifications, in order to achieve the overall front-end requirements. In particular, the first stage shows more gain and is biased at a lower current to reduce overall NF, while the second stage has been designed with larger emitter degeneration to increase linearity performance. In the revised version, more details have been added about gain control.

R2.3 the schematic of the phase shifter is not shown. Please provide it.

Considering the limited space, the authors have included a conceptual layout of the phase shifter which provides both layout and schematic information. Now the description of the design principles of the differential phase shifter should be more clear. A comment was also added in the manuscript text. A further sentence was added in the introduction to remark that the phase shifter is a key enabling block of the proposed design.