A novel FVF-based GHz-range biquad in a 28nm CMOS FD-SOI technology

Matteo Lombardo, Francesco Centurelli, Pietro Monsurrò, Alessandro Trifiletti

DIET Dip. Ingegneria dell'Informazione, Elettronica e Telecomunicazioni
Sapienza Università di Roma
Via Eudossiana 18, 00184 Roma ITALY

Corresponding author: Matteo Lombardo (matteo.lombardo@uniroma1.it)

Abstract

Inductor-less CMOS filters with bandwidth exceeding several GHz are required in high-speed data converter applications. This paper introduces two complementary biquad filters, one N-based and the other P-based, utilizing the well-established flipped voltage follower (FVF) stage. These filters exhibit more than 7 GHz cut-off frequency and a low power consumption of 0.54 mW/pole for the N-type biquad, and 0.3 mW/pole for the P-type one, demonstrating impressive figures-of-merit (FOMs) even considering bandwidth and dynamic range. The implementation of these biquads in the STMicroelectronics FD-SOI 28-nm CMOS process, along with extensive simulations, ensures stable performance under process, supply voltage and temperature (PVT) variations and mismatches, as confirmed by post-layout simulations. Notably, the area occupied by each biquad is merely 246 μm^2 for N-type biquad and 193 μm^2 for P-type, marking one of the smallest footprints in the existing literature. The achieved figures-of-merit are noteworthy, showcasing excellent power efficiency, minimal area occupation, and commendable dynamic range.

Keywords

Analog filters, anti-aliasing, inductor-less filters, CMOS integrated circuits

1. Introduction

High speed analog-to-digital converters (ADC) [1]-[3] and digital to analog converters (DAC) [4] are required in many applications, such as wideband RF and optical communication systems [5]-[6] and wideband instrumentation [7]. These converters require lowpass filters with cut-off frequencies of several GHz as aliasing filters in ADCs and pulse-shaping filters in DACs. Wideband lowpass filters are also required in advanced ADC architectures such as multiply-filter-processing (MFP) digitizers [7]-[9].

High-speed filters for these applications require sufficient signal-to-noise-and-distortion ratio (SNDR), comparable with the ADC and DAC specifications, to avoid hampering noise and linearity performance for the whole system. Integration requires a small area footprint, thus avoiding the use of large integrated inductors: the area reduction is also important to reduce parasitic effects, and allow lumped-element analyses for multi-GHz circuits. Finally, the filter design must be based on low-Q stages, to avoid issues with parasitic elements and process variations [10].

Even if filters in the GHz range are often based on active or passive RLC structures [11]-[12] or on a microstrip approach [13], there is a research interest in designing active filters in the GHz range that do not exploit physical inductors, to minimize area and power consumption. Filters based on low-frequency design approaches are quite common in the low-GHz range (1-2 GHz) [14]-[15], but design at higher frequencies have been proposed in the literature, using both BiCMOS and CMOS multi-GHz technologies.

Filters are designed using the gyrator synthesis approach [16]-[17], the leapfrog LC-ladder simulation technique [18] or as a cascade of biquad stages [10]; the adopted topologies often exploit RLC reference structures, where the inductance is implemented by an active inductor [19]-[24], or Gm-C and active-C approaches [16]-[18], [25]. Filters based on closed-loop Sallen-Key [26]-[28] or Tow-Thomas [29] architectures have also been reported.

Using BiCMOS technologies, some of the authors have reported a 6-th order lowpass filter exploiting active inductors with a cutoff frequency of 10 GHz [30] and a Sallen-Key biquad with a cutoff frequency of 17 GHz [31]. Houfaf [17] has reported a Gm-C lowpass filter with a cutoff frequency of 10 GHz in 65-nm CMOS, with a power dissipation of 140 mW, and Gannedahl [32] has presented a 4.9-GHz Gm-C lowpass filter dissipating 20 mW in a 22-nm CMOS technology.

Even if BiCMOS technologies have the potential for higher operating frequencies, implementing GHz-bandwidth lowpass filters in CMOS is an attractive goal for an easy integration of the whole system; CMOS also offer the potential for minimizing power consumption. With the aim of achieving a GHz-range lowpass filter with very low power consumption and a suitable dynamic range, active-C CMOS filters are considered. In particular, filters based on the flipped voltage

follower (FVF) and super source follower (SSF) voltage buffer stages have been proposed for low-frequency applications [33]-[39], as they require very little power consumption with respect to filters based on operational amplifiers. These filters are a good fit for high-speed filter design because of their simplicity.

This paper presents biquad filters based on the use of the FVF that allows achieving a 3-dB bandwidth of more than 7 GHz in a 28-nm FD-SOI CMOS technology [40] with a power consumption of about 1 mW. Two complementary (i.e., with PMOS and NMOS input) stages are proposed, allowing the cascading of multiple stages, as the use of complementary stages overcomes the problem arising from the different input and output voltage levels in the FVF topology. Hence, multi-stage filters can be synthetized using a power efficient architecture.

This paper is organized as follows: Section II describes the filter topology and analyzes its performance. Section III summarizes the simulation results, showing robustness to process, voltage and temperature (PVT) variations and Monte Carlo mismatches, and provides a comparison with the literature. Section IV concludes.

2. Analysis of the topology

Inductor-less biquads can be designed either exploiting closed-loop architectures (Tow-Thomas, Sallen-Key) or open-loop structures. The latter include Gm-C and active-C architectures, where the transconductances of active devices and external capacitors determine the poles of the transfer function, and RLC equivalents that make use of active inductors. To maximize resonance frequency and minimize power consumption, open-loop active-C architectures seem to be the most suited, their main limitation consisting in a lower dynamic range, because active-C filters use the transconductance of the active devices in place of passive resistances, so that on one hand they require much lower power consumption, but also have significant linearity limitations.

The class of source-follower-C (SF-C) filters [33] is therefore a good choice to design high-frequency low-power biquads: their simple structure minimizes the number of extra poles and zeros that affect the ideal transfer function of the biquad. Biquads based on simple source followers and on the flipped voltage follower (FVF) have been presented in the literature and exploited for low-frequency low-power biomedical applications; Fig. 1a shows the topology of an FVF-C biquad filter [37]. Its simple structure and short input-output path are well suited for high-frequency applications, and the DC voltage drop between input and output terminals can be easily coped with in a CMOS technology, where the cascadability of biquads to design higher-order filters can be easily achieved by using complementary stages based on NMOS and PMOS devices. The main limitations of the simple FVF stage used in Fig. 1a are the constraints on DC levels due to the closure of the feedback

loop and the consequent reduction in allowable signal swing. These limitations can be overcome by inserting a voltage drop in the feedback path, between the drain of the input transistor M_1 and the gate of the feedback transistor M_2. The typical approach [38] is to use an additional common-gate stage in the feedback loop (CGFVF in the following): this inserts a DC level shift that simplifies biasing and increases the loop gain of the feedback.

The resulting biquad topology is shown in Fig. 1b: as it will be shown in the remaining of this Section, the resonance frequency and quality factor Q are determined by the transconductances of devices M_1 and M_2 and by the values of capacitors C_1, placed between the gate and drain of M_2, and C_2, placed between the output and ground. In high-frequency applications, these capacitances will be affected by device and layout parasitics, which will cause additional poles and zeros, limiting the maximum frequency that can be achieved. In the next subsection, the ideal behavior of the biquad is first examined, and then the effects of parasitic capacitances and of output resistances of the transistors are taken into account. An interesting result of this analysis is that low output resistances of the deep-submicron MOS devices limit the achievable quality factor, requiring cascoding to obtain higher values. From this point of view, the use of the CGFVF is advantageous, since the input transistor and the common-gate device act as a folded cascode configuration.

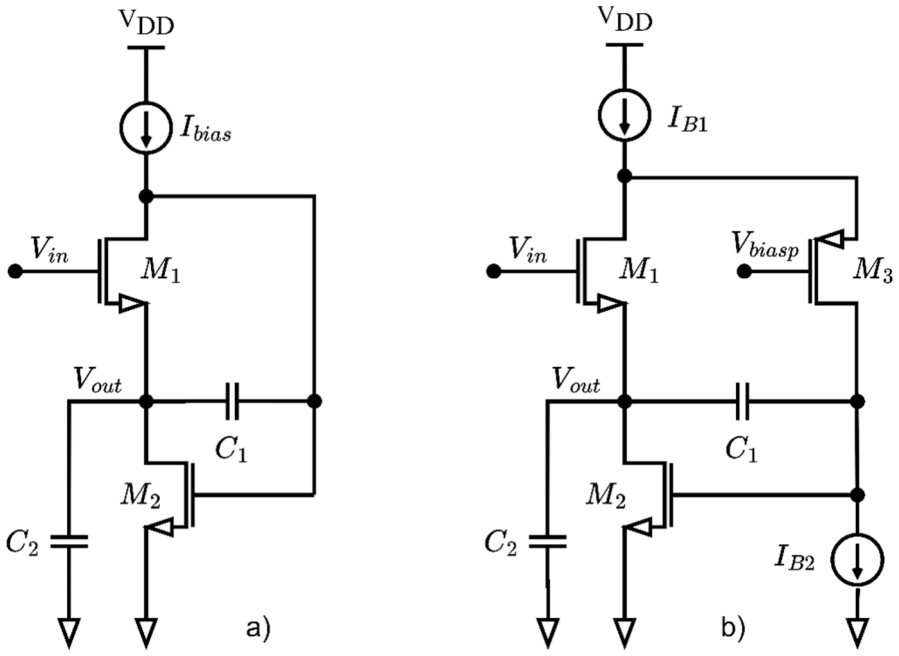

Figure 1. a) FVF-C biquad; b) CGFVF-C biquad.

2.1 Ideal frequency response

Fig. 2 shows the small-signal equivalent circuit of the biquad in Fig. 1b. Initially the parasitic resistances of the transistors g_{ds} and g_G (for the current generators) and the gate-source capacitances of the transistors C_{gs} are neglected to analyze the ideal biquad.

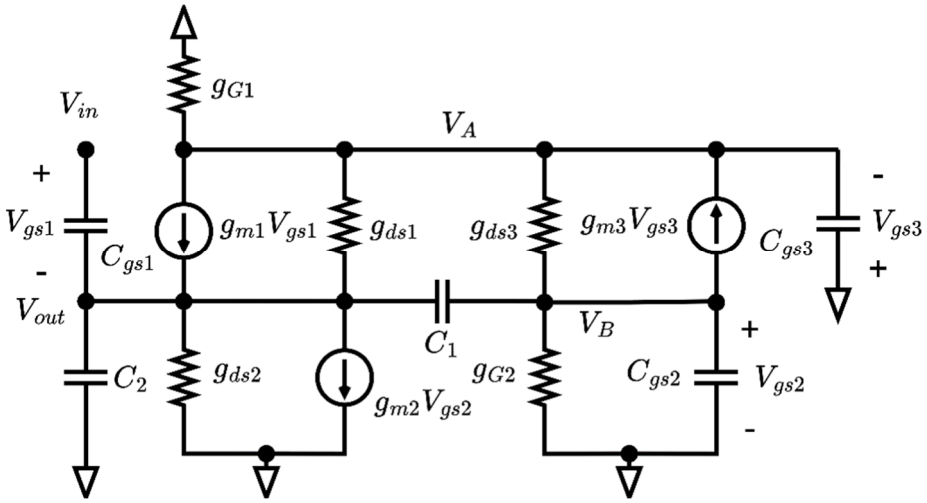

Figure 2. Small-signal equivalent circuit of the CGFVF-C biquad.

The frequency response of the filter in Fig. 1b is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1+s\frac{C_1}{g_{m1}}+s^2\frac{C_1C_2}{g_{m1}g_{m2}}} \tag{1}$$

hence:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{2}$$

$$Q = \sqrt{\frac{C_2g_{m1}}{C_1g_{m2}}} \tag{3}$$

Because the filter is in unity feedback configuration, the low-frequency gain is always close to 0dB at DC and cannot be tuned. The resonance frequency ω_0 can be tuned by changing the bias current I_{B1}, which affects both g_{m1} and g_{m2}. On the other hand, because the current flowing in M_1 and M_2 is the same, the quality factor Q cannot be easily tuned in the ideal case.

2.2 Impact of parasitic capacitances

The main parasitic capacitances in the circuit in Fig. 1b are the gate-source capacitances of the three transistors C_{gsi}, i=1,2,3. Let assume for simplicity that $C_{gs} = g_m/\omega_T$ for all the transistors, with $\omega_T \gg g_{mi}/C_i, i = 1,2$. The frequency response including these capacitances has three poles and three zeros, but the higher frequency pole and zero approximately cancel each other at frequency ω_T, leaving:

$$\frac{V_{out}}{V_{in}} \approx \frac{1+\frac{s}{\omega_T}+\frac{2C_1}{g_{m2}\omega_T}s^2}{1+\frac{C_1}{g_{m1}}s+\frac{C_1C_2}{g_{m1}g_{m2}}\left(1+\frac{C_1g_{m1}+2C_1g_{m2}+C_2g_{m2}}{C_1C_2\omega_T}\right)s^2} \tag{4}$$

The second-order term at the numerator is large with respect to the first-order term, so that the zeroes will be complex conjugated, with a large quality factor, and a negative real part.

$$Q_Z \approx \sqrt{\frac{2\omega_T C_1}{g_{m2}}} \tag{5}$$

$$\omega_{0Z} \approx \sqrt{\frac{g_{m2}\omega_T}{2C_1}} \tag{6}$$

Because the number of zeros is equal to the number of poles, the gain at infinity is finite:

$$F(j\infty) \approx \frac{2g_{m1}}{\omega_T C_2} \tag{7}$$

However, the asymptotic gain is low if $\omega_T \gg g_{m1}/C_2$.

For what concerns the poles, the resonance frequency ω_0 is slightly reduced by the additional capacitances, while the quality factor Q increases slightly:

$$\omega_0 \approx \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \frac{1}{\sqrt{1+\frac{C_1g_{m1}+2C_1g_{m2}+C_2g_{m2}}{C_1C_2\omega_T}}} \tag{8}$$

$$Q \approx \sqrt{\frac{g_{m1}C_2}{g_{m2}C_1}} \sqrt{1+\frac{C_1g_{m1}+2C_1g_{m2}+C_2g_{m2}}{C_1C_2\omega_T}} \tag{9}$$

2.3 Impact of parasitic resistances

In addition to the output conductances of M_1, M_2 and M_3, (g_{dsi}, i=1,2,3 in Fig. 2) also the output conductances of I_{B1} and I_{B2} (g_{G1} and g_{G2} in Fig. 2) must be considered. Let assume for simplicity that all output conductances are proportional to their respective g_m by the reciprocal of an intrinsic device voltage gain $A_V \gg 1$ ($g_{dsi} = g_{m1}/A_V$), and that the output conductances of the two current generators I_{B1} and I_{B2} are proportional to their currents with the same intrinsic gain, so that $g_{G1} = g_{ds1} + g_{ds3}$ and $g_{G2} = g_{ds3}$.Taking these conductances into account, the frequency response is:

$$\frac{V_{out}}{V_{in}} \approx \frac{1+\frac{1}{A_V}\left(1+\frac{g_{m3}}{g_{m2}}\right)+s\frac{C_1}{g_{m2}A_V}\left(1+\frac{g_{m1}}{g_{m3}}\right)}{D} \tag{10}$$

$$D = 1+\frac{1}{A_V}\left(2+\frac{g_{m3}}{g_{m2}}\right)+s\frac{C_1}{g_{m1}}\left[1+\frac{1}{A_V}\left(3+\frac{g_{m1}^2}{g_{m2}g_{m3}}+\frac{g_{m3}}{g_{m2}}+\frac{g_{m1}}{g_{m2}}+\frac{2g_{m1}}{g_{m3}}\right)\right]+s\frac{C_2g_{m3}}{A_Vg_{m1}g_{m2}}+ \\ +s^2\frac{C_1C_2}{g_{m1}g_{m2}}\left[1+\frac{2}{A_V}\left(1+\frac{g_{m1}}{g_{m3}}\right)\right] \tag{11}$$

The parasitic resistances slightly reduce the DC gain, have a negligible effect on the resonance frequency, and reduce the quality factor. An additional zero at high frequency is also created.

From eq. (11) it can be demonstrated that there is a maximum quality factor that can be obtained, that is related to the gain A_V, hence to the parasitic resistances of the transistors. Starting from (11), the resonance frequency and the quality factor can be derived as:

$$\omega_0 \approx \sqrt{\frac{K_G}{K_C}}\omega_1 \tag{12}$$

$$Q = \frac{\sqrt{K_CK_3}\sqrt{K_G(A_V+2)+K_3}\sqrt{K_3(A_V+2)+2}}{1+K_3+K_3^2+2K_G+K_GK_3(A_V+3)+K_CK_3^2} \tag{13}$$

where $K_C = C_2/C_1$ is the ratio of the capacitances, $K_G = g_{m2}/g_{m1}$ is the ratio of the transconductances, $K_3 = g_{m3}/g_{m1}$ and $\omega_1 = g_{m1}/C_1$. Eq. (13), together with the relationship between K_C and K_G imposed by (12) and the technological constraints on ω_1, shows that the maximum quality factor can be enhanced with a higher value of A_V, i.e. a higher resistance of the devices. The demonstration is reported in the Appendix.

2.4 Impact of cascoding

The analysis in the previous subsection shows that the quality factor Q is limited by the intrinsic gain of the transistors, hence it can be increased by exploiting cascoding, in particular of the current generator I_{B2} that sets the bias current of the common-gate device M_3. The conductance of such generator g_{G2} appears in the first-order term depending on C_2 in (11), and the transfer function (10) can be rewritten by setting $g_{G2} \approx g_{ds3}/A_V = g_{m3}/A_V^2$:

$$\frac{V_{out}}{V_{in}} \approx \frac{1+\frac{1}{A_V}+s\frac{C_1}{g_{m2}A_V}\left(1+\frac{g_{m1}}{g_{m3}}\right)}{D} \tag{14}$$

$$D \approx 1+\frac{2}{A_V}+s\frac{C_1}{g_{m1}}\left[1+\frac{1}{A_V}\left(3+\frac{g_{m1}^2}{g_{m2}g_{m3}}+\frac{g_{m1}}{g_{m2}}+\frac{2g_{m1}}{g_{m3}}\right)\right]+s\frac{C_2 g_{m3}}{A_V^2 g_{m1}g_{m2}}+s^2\frac{C_1C_2}{g_{m1}g_{m2}}\left[1+\frac{2}{A_V}\left(1+\frac{g_{m1}}{g_{m3}}\right)\right] \tag{15}$$

Hence, there is a slight reduction in low-frequency gain, there is still a high-frequency zero, and the denominator has resonance frequency and quality factor:

$$\omega_0 \approx \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}\frac{A_V+2}{A_V+2\left(1+\frac{g_{m1}}{g_{m3}}\right)}} \approx \omega_1\sqrt{\frac{K_G}{K_C}} \tag{16}$$

$$Q = \frac{\sqrt{K_C K_G K_3}A_V\sqrt{A_V+2}\sqrt{K_3(A_V+2)+2}}{A_V(1+K_3+2K_G)+K_G K_3 A_V(A_V+3)+K_C K_3^2} \tag{17}$$

Substituting K_C from (16) into (17), the quality factor has a form

$$Q = A\frac{K_G}{BK_G+D} \tag{18}$$

with A, B and D depending on A_V and increases up to

$$Q_{lim} = \frac{A_V}{\Omega}\frac{\sqrt{K_3}\sqrt{A_V+2}\sqrt{K_3(A_V+2)+2}}{2A_V+K_3A_V(A_V+3)+\left(\frac{K_3}{\Omega}\right)^2} \tag{19}$$

where $\Omega = \omega_0/\omega_1$ for K_G going to infinity.

2.5 Noise analysis

The noise behavior of the biquad can be analyzed referring to the small-signal equivalent circuit in Fig. 2, neglecting the parasitic resistances and capacitances of the transistors. Noise sources are related to the three MOS devices M_1, M_2, M_3 and to the devices implementing the current

generators; the former can be represented as current sources I_{ni}, i=1,…3, in parallel with the generators g_{mi}, whereas the latter are represented by current generators I_{nB1} and I_{nB2} from nodes V_A and V_B to ground respectively. Each noise source has a power spectral density

$$S_{ni} = \frac{K_F g_{mi}^2}{f C_{ox} W L} + 4K_B T \gamma g_{mi} \tag{20}$$

where K_B is the Boltzmann constant, T is the absolute temperature, C_{ox} the oxide capacitance per unit area, W and L are the channel width and length, and γ and K_F are process-dependent coefficients. The flicker component can be neglected due to the wide filter bandwidth.

The analysis of the circuit in Fig. 2 shows that noise source I_{n3} has no effect on the output, and the input-referred noise power spectral density can be expressed as:

$$S_{veq} = \frac{1}{g_{m1}^2}\left[I_{n1}^2 + \frac{\omega^2 Q^2 C_1^2}{\omega_0^2 C_2^2} I_{n2}^2 + \left(1 + \frac{\omega^2 Q^2 C_1^2}{\omega_0^2 C_2^2}\right)(I_{nB1}^2 + I_{nB2}^2)\right] \tag{21}$$

Eq. (21) shows that the different noise sources present different frequency behaviors, and the output-referred noise spectrum (given by (21) times the square modulus of (1) for s=jω) can be separated into a lowpass and a bandpass component:

$$S_{no} = \frac{1}{g_{m1}^2} \frac{(I_{n1}^2 + I_{nB1}^2 + I_{nB2}^2) + \frac{\omega^2 Q^2 C_1^2}{\omega_0^2 C_2^2}(I_{n2}^2 + I_{nB1}^2 + I_{nB2}^2)}{\left(1 - \frac{\omega^2}{\omega_0^2}\right)^2 + \frac{\omega^2}{\omega_0^2 Q^2}} \tag{22}$$

Integrating over the whole frequency range provides an output noise power given by

$$P_{no} = \frac{\pi Q \omega_0}{2 g_{m1}^2}\left[I_{n1}^2 + I_{nB1}^2 + I_{nB2}^2 + \frac{Q^2 C_1^2}{C_2^2}(I_{n2}^2 + I_{nB1}^2 + I_{nB2}^2)\right] \tag{23}$$

2.6 Cascadability of complementary stages

The biquad stage has different input and output DC voltages, and can be made cascadable if N-type and P-type devices are cascaded alternately. Let focus on cascadable stages, where the N-type output has the same DC voltage as the P-type input, and vice versa, so that it is possible to obtain a filter with $2N_S$ poles, where N_S is the number of stages. If the input DC voltage of the N-type filter is V_{in}^Q, the output is $V_{in}^Q - V_{GS1n}$, and the following stage will have output $V_{in}^Q - V_{GS1n} + V_{SG1p} \approx V_{in}^Q$.

Figure 3 shows two complementary cascaded stages using two CGFVF-C biquad stages; cascaded current sources are considered. We assume $V_{GS} = V_{SG}$ for all NMOS and PMOS devices, and the same threshold voltage V_T (and hence overdrive voltage V_{ov}). The first biquad sets node Y at $V_i - V_{GS}$; the minimum voltage for such node is V_{ov}, to keep M_{2n} in saturation, and the maximum voltage is $V_{DD} - 3V_{ov}$ to keep M_{1n} in saturation. On the other hand, the second biquad requires voltage at node Y to be lower than $V_{DD} - V_{SG} - V_{ov}$, to keep M2p in saturation, and higher than $3V_{ov} - V_{SG}$ to keep M_{1p} in saturation.

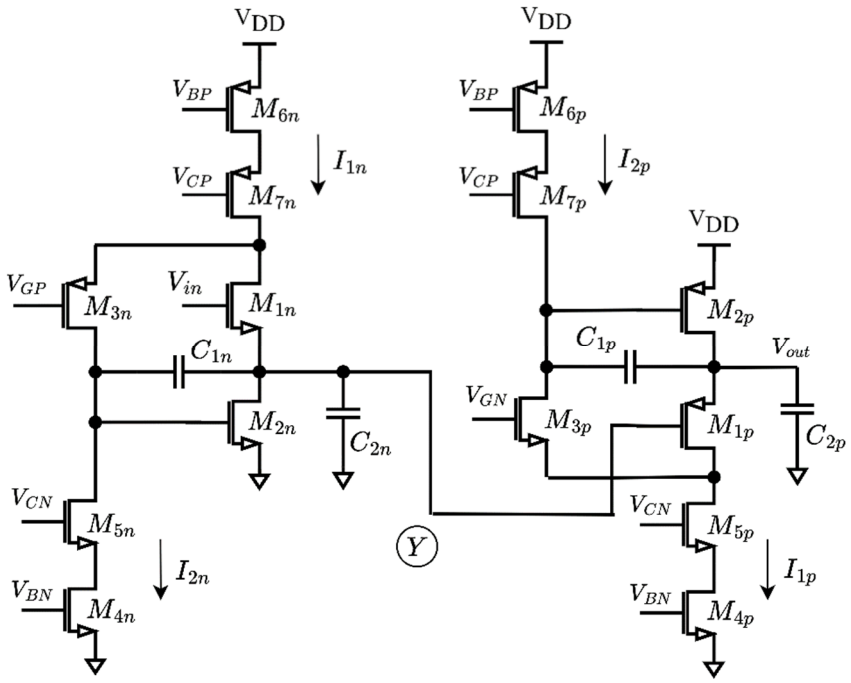

Figure 3. 4-th order filter with two complementary CGFVF-C stages.

The minimum signal swing is obtained for a DC input level $V_i = \frac{V_{DD}}{2} - V_{ov} + V_{GS}$; the resulting maximum output swing is $D_o = V_{DD} - 4V_{ov}$ and it can be achieved for a suitable choice of the gate-source voltage $V_{GS} = V_{SG}$, since the maximum swing at node Y is $D_Y = min(V_{DD} - 3V_{ov}, V_{DD} - V_{ov} - V_{SG}) - max(V_{ov}, 3V_{ov} - V_{SG})$.

3. Simulation results

The filters have been designed in a FD-SOI (fully-depleted silicon-on-insulator) CMOS process with 28-nm devices by STMicroelectronics in the Cadence Virtuoso environment. Both N-type and P-type biquads have been designed with target performance of about 5.7 GHz resonance frequency and a quality factor of 4.5: the resulting device sizes are reported in Table 1, together with the values of capacitors C_1 and C_2. It has to be noted that for such high frequencies small capacitors have to be used, hence parasitic capacitances of the devices and interconnects have a non-negligible effect. Values of C_1 and C_2 reported in the table take this into account and are the physical capacitors that have been implemented.

All the devices have minimum gate length $L = 28$ nm. Forward body biasing has been exploited to reduce the threshold voltage of the devices, and the adopted body voltages are 0.7 V for NMOS transistors and -1.5 V for PMOS transistors (the use of a FD-SOI technology allows using body-source voltages in excess of 0.6 V). This increases the speed of the devices and reduces the leakage currents into the device substrate with respect to the traditional alternatives.

Figure 4 shows the layout of the N-type and P-type biquads, whose areas are 246.23 μm^2 and 193.52 μm^2 respectively. All the following results refer to post-layout simulations. Supply voltage has been set to 1.2 V and the biquads dissipate 1.08 mW and 0.6 mW respectively for the N-type and P-type. DC input levels are 0.8 V for N-type biquad and 0.4 V for P-type biquad.

Table 1. Device sizing

Device	N-type biquad	P-type biquad
M_1	4.4µm	6.4µm
M_2	3.2µm	8µm
M_3	10µm	4.56µm
M_4	1µm	4.5µm
M_5	1µm	4.5µm
M_6	8µm	4µm
M_7	8µm	4µm
I_{B1}	800µA	900µA
I_{B2}	200µA	400µA
C_1	29fF	26fF
C_2	64fF	45fF

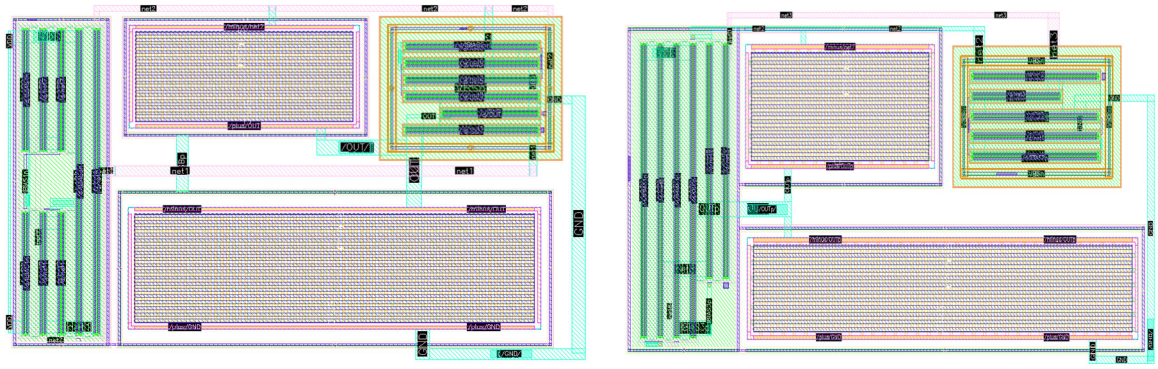

Figure 4. Layout of (a) N-type biquad; (b) P-type biquad.

3.1 Typical post-layout performance

Figure 5 shows the frequency response of the N-type, P-type and cascaded (N + P) filters. The resulting cut-off frequency, resonance frequency and quality factor are 7.57 GHz, 5.89 GHz and 5.19 (14.3 dB) for the N-type biquad, and 7.19 GHz, 5.62 GHz and 5.25 (14.4 dB) for the P-type biquad.

Resonance frequency is quite in line with the designed value, whereas a higher quality factor is achieved, due to the effect of extra poles and zeros and underestimated parasitics.

The gain after cut-off is limited to -30 dB because of the complex zeros caused by the parasitic capacitances, but with two cascaded biquads the remaining gain is less than -50 dB, which is negligible.

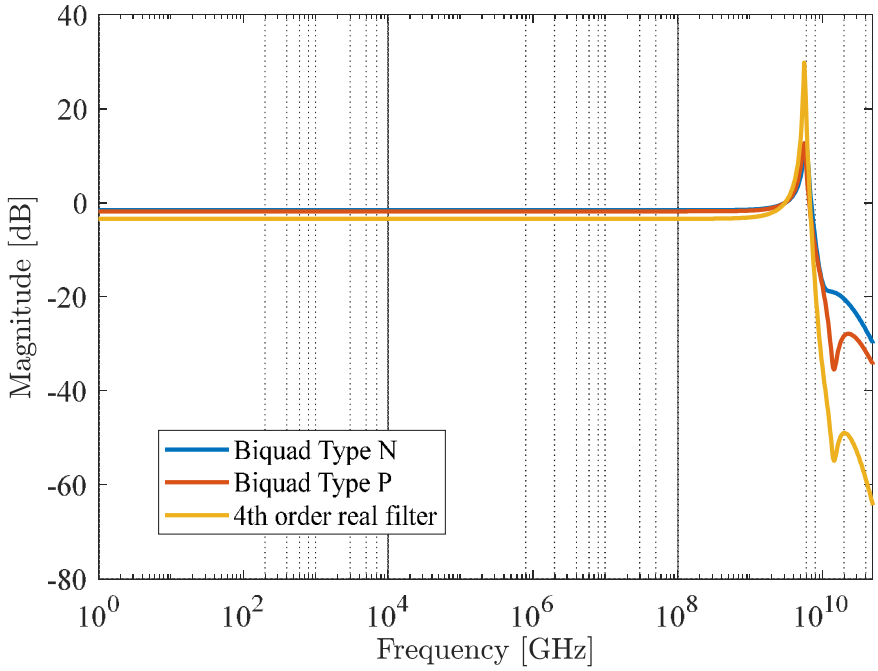

Figure 5. Frequency response of the biquads.

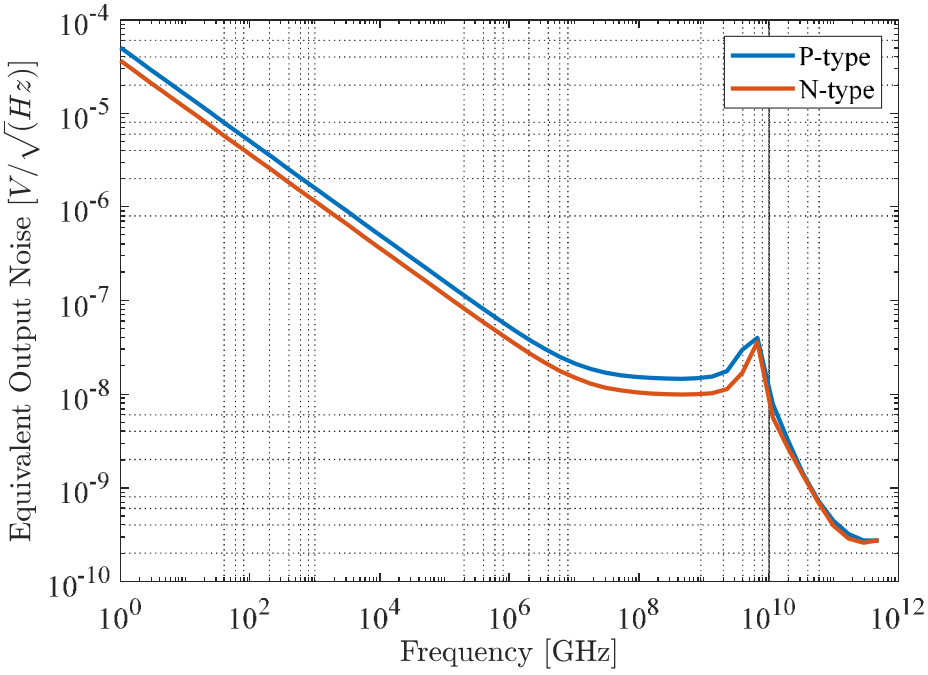

Figure 6. Equivalent output noise spectrum for the N-type and P-type biquads.

Figure 6 shows the output noise spectrum for both biquads. The total in-band integrated output-referred noise is 1.95 mVrms and 2.4 mVrms respectively, for the N-type and P-type biquad stages, and the corresponding input-referred values are 1.49 mVrms and 2.4 mVrms.

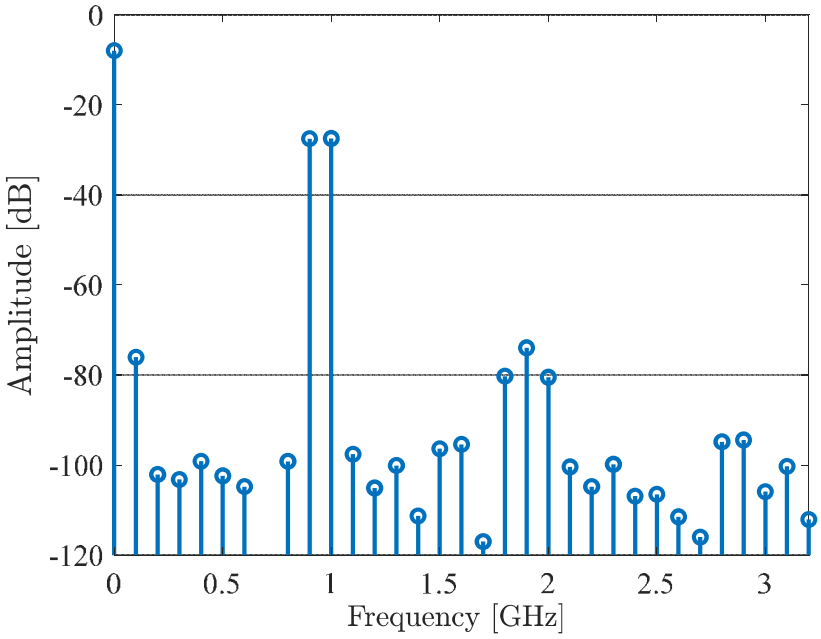

Figure 7. Output spectrum of the N-type biquad for a two-tone test with 200-mVpp sinusoids at 900 MHz and 1 GHz.

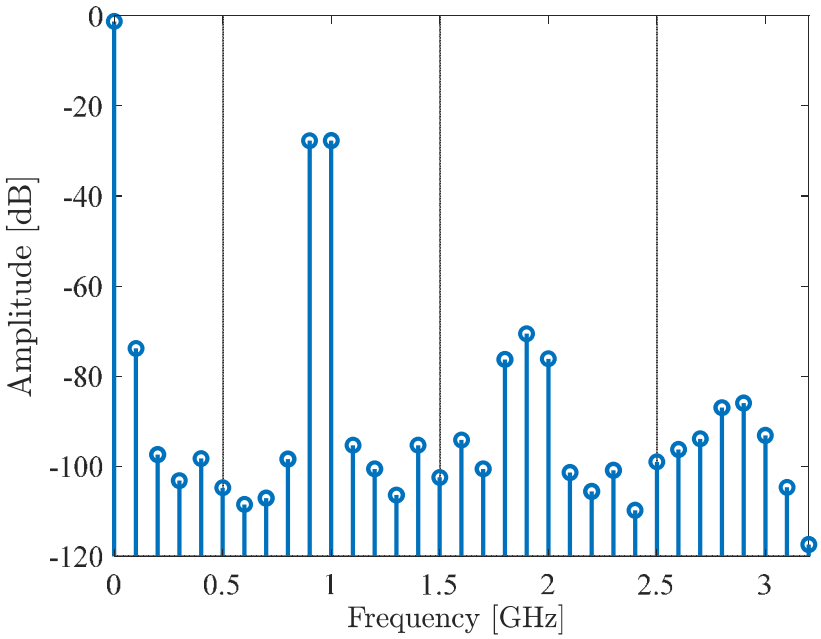

Figure 8. Output spectrum of the P-type biquad for a two-tone test with 200-mVpp sinusoids at 900 MHz and 1 GHz.

To evaluate the linearity of the designed biquads, a two-tone test with 200-mVpp sinusoids at 900 MHz and 1 GHz was performed, and Figs. 7 and 8 report the resulting output spectra for N-type and P-type biquads, showing third-order intermodulation distortion IMD3 of 70.11 dB and 67.65 dB respectively. The spectra also show second- and third-order harmonic distortions, allowing to measure HD2 and HD3 values of -46.86 dB and -64.89 dB (-42.38 dB and -56.20 dB) for N-type (P-type) biquad.

Simulation have also been performed on a single-tone setup to characterize linearity for different input amplitudes and frequencies: amplitudes from 20 to 700 mVpp (at 1 GHz) and frequencies from 1 to 6 GHz (at 200 mVpp) have been considered. Figs. 9 and 10 show the obtained trends for HD2, HD3 and total harmonic distortion (THD) for the N-type biquad, and Figs. 11 and 12 the corresponding curves for the P-type biquad. Figures show that second-order distortions are the dominant term, as expected in a single-ended filter; a net improvement of linearity can be expected if a fully differential approach is adopted. Figs. 9 and 11 also allow to evaluate the allowable input (and output, since gain is 1) of the biquad: to keep THD below 1%, the maximum swing is about 350 mVpp for the N-type biquad and 260 mVpp for the P-type biquad.

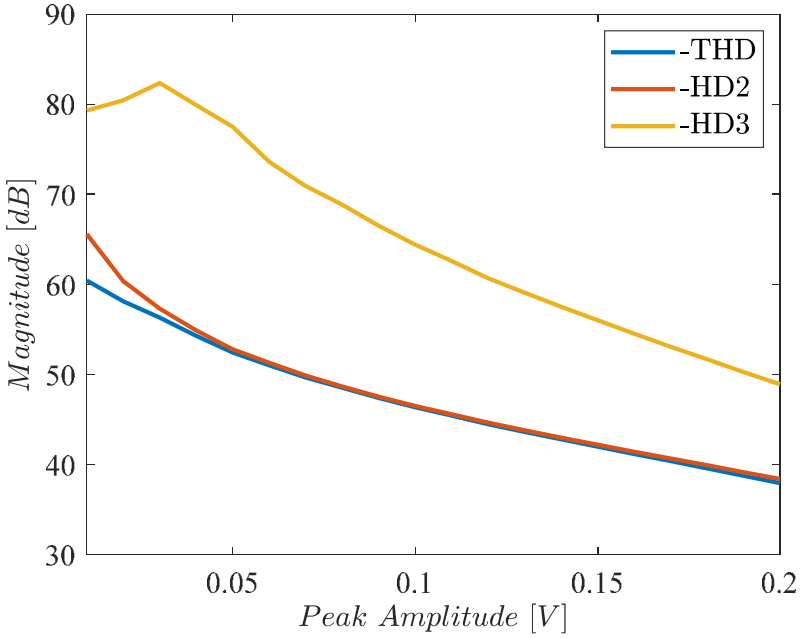

Figure 9: Linearity of the N-type biquad vs input amplitude (f_{in} = 1 GHz).

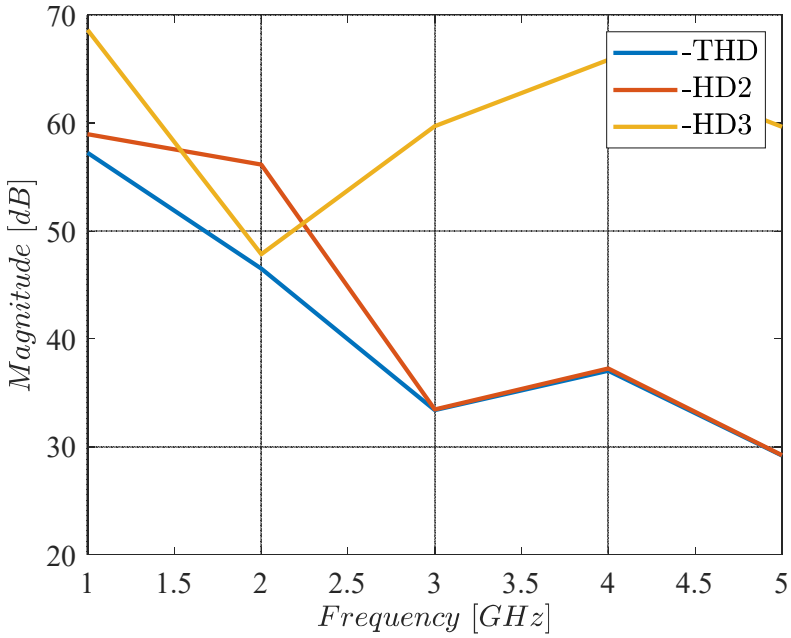

Figure 10: Linearity of the N-type biquad vs input frequency (at 50 mVpp).

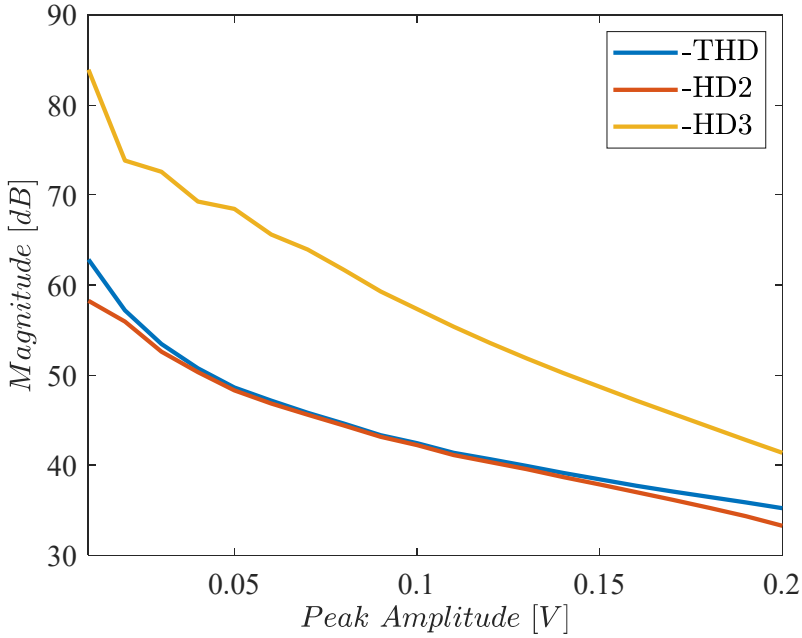

Figure 11: Linearity of the P-type biquad vs input amplitude (f_{in} = 1 GHz).

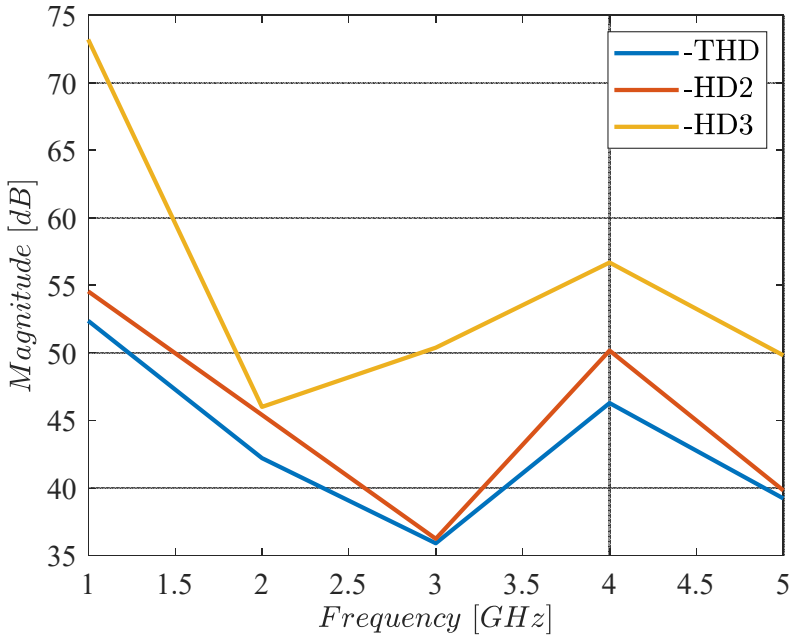

Figure 12: Linearity of the P-type biquad vs input frequency (at 50 mVpp).

3.2 Sensitivity to PVT variations and mismatches

Simulations have been performed to assess the robustness of the designed biquads to supply voltage and temperature variations. Results are synthesized in Tables 2 and 3, that show that gain and bandwidth are rather stable, whereas the quality factor is more variable, but can be adjusted by means of g_{m3}, which depends on the bias current of devices M_{3n} and M_{3p} in Fig. 3.

Table 2. Performance of N-type biquad under PVT variations

Performance	Typ	V_{DD}-5%	V_{DD}+5%	0°C	80°C
Gain [dB]	-1.59	-1.59	-1.59	-1.56	-1.68
f_{3dB} [GHz]	7.57	7.32	7.73	7.82	6.91
f_0 [GHz]	5.88	5.62	6.03	6.16	5.37
Q [dB]	14.3	11.11	15.75	15.11	11.54

Table 3. Performance of P-type biquad under PVT variations

Performance	Typ	V_{DD}-5%	V_{DD}+5%	0°C	80°C
Gain [dB]	-1.81	-1.81	-1.82	-1.79	-1.91
f_{3dB} [GHz]	7.19	6.94	7.36	7.28	6.99
f_0 [GHz]	5.62	5.37	5.62	5.62	5.37
Q [dB]	14.43	12.85	15.03	15.48	12.03

The effect of process variations and device mismatches has also been investigated through Monte Carlo simulations, and results are reported in Table 4, showing the robustness of the frequency response for both filters, especially in terms of resonance frequency and bandwidth. The corresponding histograms are reported in Figs. 13-17.

Table 4. Results of 500 Monte Carlo mismatch simulations

Performance	N-type biquad			P-type biquad		
	Mean (μ)	Std (σ)	σ/μ	Mean (μ)	Std (σ)	σ/μ
f_{3dB} [GHz]	7.49 GHz	203 MHz	0.027	7.16 GHz	216 MHz	0.030
f_0 [GHz]	5.86 GHz	218 MHz	0.037	5.54 GHz	193 MHz	0.035
Q [dB]	13.85 dB	2.27 dB	0.164	14.4 dB	3.16 dB	0.219
Gain [dB]	-1,6 dB	0.11 dB	0.069	-1.82 dB	0.16 dB	0.088
THD (1 GHz 200 mVpp)	-46.16 dB	1.81 dB	0.039	-41.89 dB	1.17 dB	0.028

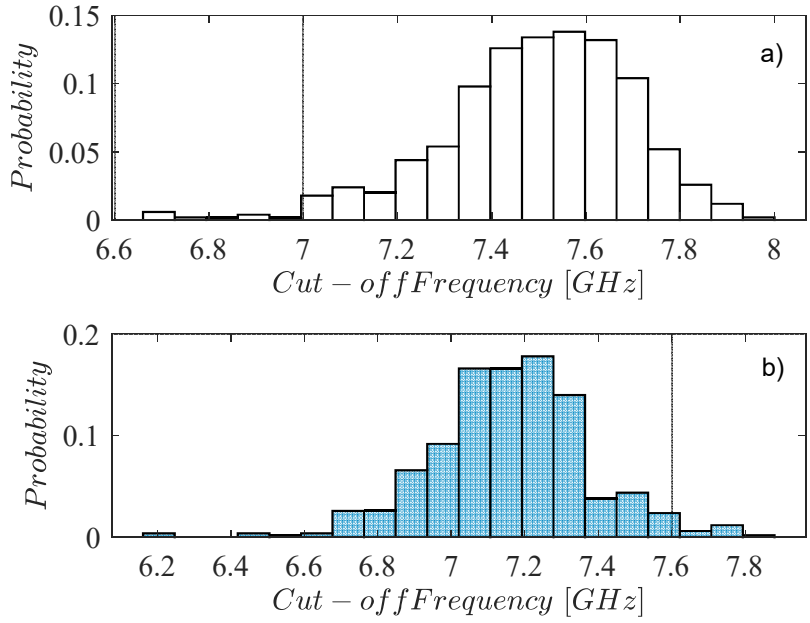

Figure 13. Histogram of the cut-off frequency: a) N-type biquad; b) P-type biquad.

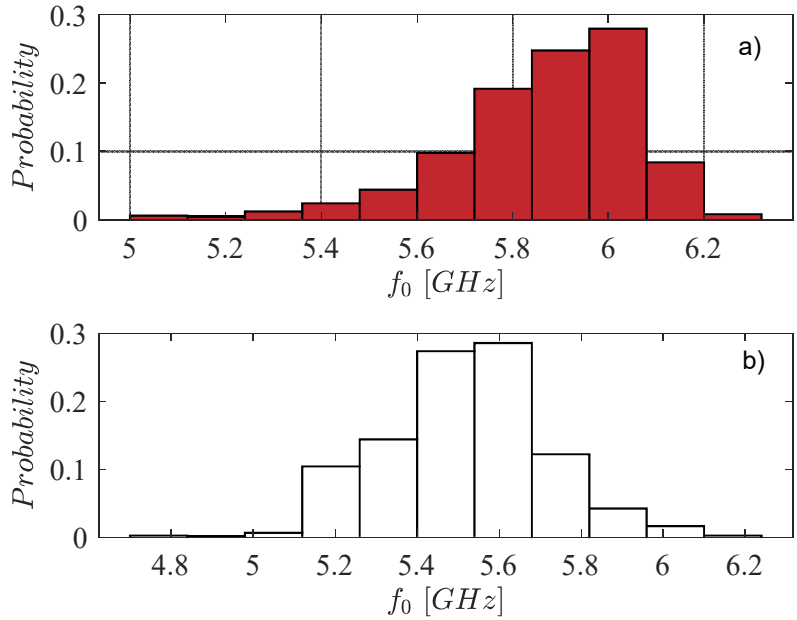

Figure 14. Histogram of the resonance frequency: a) N-type biquad; b) P-type biquad.

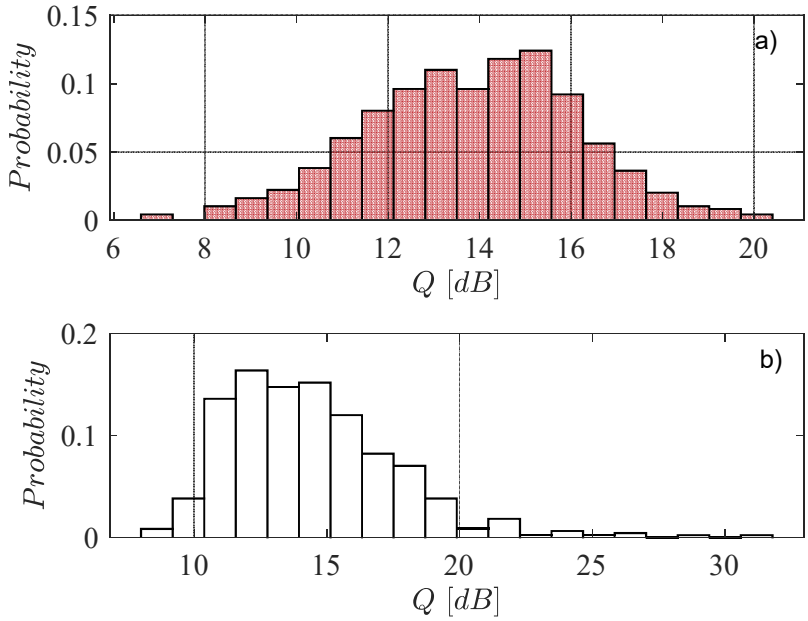

Figure 15. Histogram of the quality factor: a) N-type biquad; b) P-type biquad.

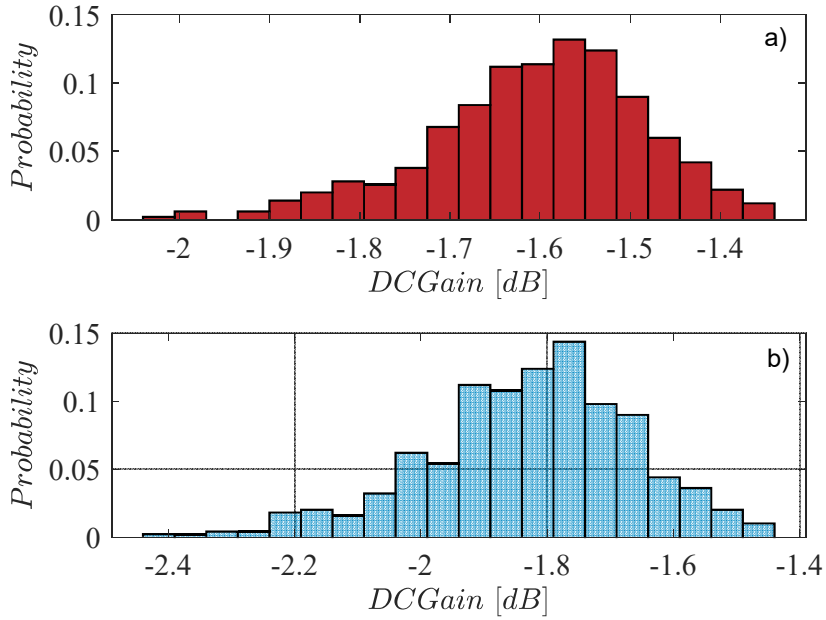

Figure 16. Histogram of the DC gain: a) N-type biquad; b) P-type biquad.

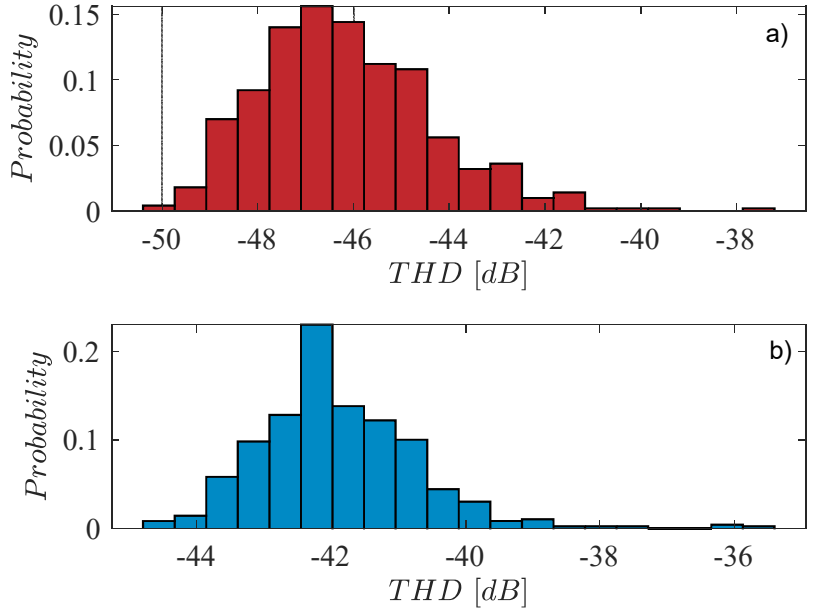

Figure 17. Histogram of THD for a 1-GHz 200-mVpp input: a) N-type biquad; b) P-type biquad.

3.3 Comparison with the literature

Table 5 synthesizes the performances of the biquads and compares them with the state of the art. To allow a fair comparison of different designs, figures of merit are usually defined; in the case of lowpass filters, the following figures of merit are defined and are reported in Table 5:

$$FOM_1 = \frac{P_D}{N_{pole}} \quad (24)$$

$$FOM_2 = \frac{FOM_1}{f_{3dB}} \tag{25}$$

$$FOM_3 = \frac{FOM_2}{D_R^{pow}} \tag{26}$$

FOM_1 is used to compare filters of different order by the point of view of power consumption, by dividing the total power dissipation P_D by the number of poles N_{pole}. FOM_2 also takes into account the bandwidth f_{3dB}, since the higher the frequency, the higher the expected power dissipation. FOM_3 further adds the dynamic range $D_R^{pow} = 10^{D_R^{dB}/10}$, where D_R^{dB} is the linear range in decibel, defined as the difference between the input power corresponding to the maximum signal-to-noise-and-distortion ratio (SNDR) and the input-referred noise power level.

Some of the design in Table 5 are in BiCMOS technology, others use CMOS. CMOS implementations are expected to require lower power, but bandwidth and dynamic range can be limited, so that the two latter FOMs may be challenging. The proposed biquads have the lowest consumption in the literature, and the only CMOS implementation with a larger bandwidth has more than 150 time the power dissipation. The very low power consumption increases the SNR, and thus limits the dynamic range (DR) of the amplifier. Hence, while the proposed biquads have remarkable FOM_1 and FOM_2 performance (consumption per pole and consumption per pole and bandwidth), the FOM_3 (which also includes the dynamic range) is good but two BiCMOS implementations are more efficient because of higher linearity and lower noise. The proposed biquads also have the lowest area occupation in the literature, almost one order of magnitude lower than comparable filters.

4. Conclusion

Two complementary single-ended CMOS high-speed lowpass filters have been developed and extensively simulated, showing remarkable performance and good stability to PVT and Monte Carlo simulations. The two filters have excellent figures of merit, proving that CMOS technologies can be used for filters from DC to beyond 10 GHz of cut-off frequency. CMOS active-C filters allow great performance in terms of power consumption and area occupation, with a slight reduction in dynamic range with respect to BiCMOS alternatives. Furthermore, the low number of internal nodes and active and passive devices in active-C topologies allows increasing the cut-off frequencies while significantly reducing area and power consumption with respect to other CMOS filter topologies, for instance those based on high-gain active devices, e.g. the Tow-Thomas architecture.

The filters exploit the FVF architecture augmented by a common-gate auxiliary stage to maximize the output signal swing, overcoming the biasing limitations of FVF amplifiers: the addition of a common-gate auxiliary stage allows maximizing the output signal, although it is not rail-to-rail owing to the use of a common drain stage. The two filters are complementary, one using a NMOS

Table 5. Comparison with the literature

Performance	This work (N/P-type)		[31]	[32]	[30]	[28]	[18]	[17]	[16]	Units
Technology	CMOS 28		BICMOS	CMOS 22	BICMOS	BICMOS	CMOS 28	CMOS 65	BICMOS	
Measured	NO		NO	YES	YES	NO	YES	YES	YES	
N_{pole}	2	2	2	5	6	2	5	3	5	
V_{DD}	1.2	1.2	2.7	0.8	3	3	1.1	1.4	3.5	V
P_D	1.08	0.6	15.75	19.9	43	18	30	140	100	mW
f_{3dB}	7.57	7.2	17.1	4.9	10.3	9.55	3.3	10	4.1	GHz
A_0	-1.6	-1.8	3.8	0.5	-0.2	-0.5	-1	1.3	-6.8	dB
P_{noise}	-43.5	-39.4	-50.4	-56.8	-45.9	-46.8	-56	-55.6	-40.1	dBm
P_{in}^{Q}	-10	-10	-2.9		-1	-1	-17	-10.6	-18	dBm
SNR @ P_{in}^{Q}	33.5	29.4	47.9	IIP3	44.9	45.8	39	45.4	22.1	dB
THD @ P_{in}^{Q}	-46.8	-42.4	-51.7	0.9 dBm	-42.6	-64	-40	-45	-25	dB
D_R^{dB}	40.2	35.9	47.9	37.3	43.1	50.9	38.4	44	23.2	dB
Area	0.000246	0.000193	0.0025	0.05	0.02	0.0027	0.09	0.01		mm^2
Area/pole	0.000123	0.000096	0.00125	0.01	0.003	0.00135	0.018	0.003		mm^2
FOM_1	0.54	0.3	7.87	3.98	7.2	9	6	46.7	20	mW
FOM_2	0.071	0.042	0.46	0.81	0.69	0.94	1.82	4.67	4.88	pW/Hz
FOM_3	13.65	21.56	11.22	223.26	50.77	11.48	400.62	278.9	34681	aW/Hz

input and the other a PMOS input. In this way, multi-pole filters can be obtained by cascading one NMOS and one PMOS stages, with the biasing voltage decreasing or increasing by a V_{GS} at each stage.

A thorough analysis of the main parasitic effects and their impact on the resonance frequency and the quality factor is carried out, demonstrating the limiting effect on the maximum quality factor that can be achieved. As a consequence, cascoding is exploited to minimize the most important limitations to the quality factor in high-speed advanced CMOS processes affected by limited intrinsic device gain.

Extensive simulations both pre- and post-layout show remarkable stability under process, voltage, temperature variations and device mismatches in parametric and Monte Carlo simulations, highlighting excellent stability.

The filters are designed and simulated in a commercial FD-SOI CMOS 28-nm technology and achieve very good FOMs and record low area occupation by exploiting a simple architecture with two capacitors and no inductors. With respect to comparable CMOS implementations, FOMs are much better because power dissipation is one or two orders of magnitude lower for comparable bandwidth and dynamic range. Some BiCMOS solutions present better FOM3 because of the higher dynamic range, but also much worse consumption for the same bandwidth and number of poles. Furthermore, BiCMOS process are less available and more expensive than CMOS ones.

Appendix

In this appendix, we show that the biquad presents a maximum quality factor and analyze its dependence on the output resistance of the devices (hence on the intrinsic gain). Eq. (12) and (13) give the resonance frequency and the quality factor of the biquad; with the goal of finding the maximum quality factor for a fixed frequency, (12) provides the relationship between K_C and K_G:

$$K_G = K_C \left(\frac{\omega_0}{\omega_1}\right)^2 = K_C \Omega^2 \tag{A.1}$$

where Ω is a normalized resonance frequency. By substituting (A.1) in (13), the quality factor can be written as:

$$Q = \frac{\sqrt{K_G K_3}}{\Omega} \frac{\sqrt{K_G(A_V+2)+K_3}\sqrt{K_3(A_V+2)+2}}{1+K_3+K_3^2+2K_G+K_G K_3(A_V+3)+K_G\left(\frac{K_3}{\Omega}\right)^2} \tag{A.2}$$

Eq. (A.2) shows that the quality factor cannot go to infinity for either K_G or K_3 going to zero or to infinity, hence there exist an optimum value of K_G (K_3) that yields a maximum value of Q. The optimum value of K_G can be found by equating to zero the derivative of (A.2) with respect to K_G, and results:

$$K_{Gopt} = \frac{K_3^2+K_3+1}{\left(\frac{K_3}{\Omega}\right)^2+K_3(A_V+3)-2(A_V+1)} \tag{A.3}$$

The corresponding maximum value of the quality factor is

$$Q_{max} = \frac{K_3\sqrt{K_3}\sqrt{K_3(A_V+2)+2}}{2\Omega\sqrt{1+K_3+K_3^2}\sqrt{\left(\frac{K_3^2}{\Omega^2}+K_3-2\right)-A_V(K_3+1)}} \tag{A.4}$$

that increases with increasing the intrinsic gain A_V.

A similar analysis can be performed for K_3, but does not provide an easy closed-form solution.

References

[1] B. Xu, Y. Zhou, and Y. Chiu, 'A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS,' *IEEE J. Solid-State Circ.*, vol. 52, no. 4, pp. 1091-1100, April 2017.

[2] L. Kull, D. Luu, C. Menolfi, M. Brändli, P.A. Francese, T. Morf, M. Kossel, A. Cevrero, I. Ozkaya, and T. Toifl, 'A 24-72-GS/s 8-b time-interleaved SAR ADC with 2.0-3.3-pJ/conversion and > 30 dB SNDR at Nyquist in 14-nm CMOS FinFET,' *IEEE J. Solid-State Circ.*, vol. 51, no. 12, pp. 3508-3516, Dec. 2018.

[3] J. Luan, X. Zheng, D. Wu, Y. Zhang, L. Wu, L. Zhou, J. Wu, and X. Liu, 'A 56 GS/s 8 bit time-interleaved ADC in 28 nm CMOS,' *MDPI Electronics*, vol. 11, no. 5, paper 688, Mar. 2022.

[4] W. Li, D. Xue, L. Zhou, M. Luo, X. Li, J. Li, F. Jiang, and S. Yu, '32-GS/s 6-bit DAC based on SiGe technology for IM-DD OFDM systems with non-uniform quantization,' *Opt. Express*, vol. 27, pp. 8121-8129, 2019.

[5] J. Lee, J. Weiner, and Y. Chen, 'A 20-GS/s 5-b SiGe ADC for 40-Gb/s coherent optical links,' *IEEE Trans. Circ. Syst. I Regular Papers*, vol. 57, no. 10, pp. 2665-2674, Oct. 2010.

[6] A. Zandieh, P. Schvan, and S. P. Voinigescu, 'Design of a 55-nm SiGe BiCMOS 5-bit time-interleaved flash ADC for 64-Gbd 16-QAM fiber optics applications,' *IEEE J. Solid-State Circ.*, vol. 54, no. 9, pp. 2375-2387, Sep. 2019

[7] D. Knierim, 'Ultra-wide-bandwidth oscilloscope architectures and circuits,' *BCTM 14 IEEE Bipolar/BiCMOS Circ. Technol. Meeting*, Coronado CA, 28 Sep. – 1 Oct. 2014.

[8] P. Monsurrò, A. Trifiletti, L. Angrisani, and M. D'Arco, 'Two novel architectures for 4-channel mixing/filtering/processing digitizers.' *Measurement*, vol. 142, pp. 138-147, Aug. 2019.

[9] F. Centurelli, P. Monsurrò, P. Tommasino, and A. Trifiletti, ‘A novel parallel digitizer with a pulseless mixing-filtering-processing architecture and its implementation in a SiGe HBT technology at 40GS/s,’ *IEEE Access*, vol. 11, pp. 75657-75670, 2023.

[10] P. Monsurrò, S. Pennisi, G. Scotti, and A. Trifiletti, ‘High-tuning-range CMOS band-pass IF filter based on a low-Q cascaded biquad optimization technique,’ *Int. J. Circ. Theory Appl*., vol. 43, no. 11, pp. 1615– 1636, Nov. 2015

[11] M.B. Elamien, B.J. Maundy, A.S. Elwakil, and L. Belostotski, ‘Second-order cascode-based filters,’ *Integration*, vol. 84, pp. 111-121, May 2022.

[12] X. Yin, Z. Zhu, Y. Liu, Q. Lu, X. Liu, and Y. Yang, ‘Ultra.compact TSV-based L-C low-pass filter with stopband up to 40 GHz for microwave application,’ *IEEE Trans. Microwave Theory Techn.*, vol. 67, no, 2, pp. 738-745, Feb. 2019.

[13] J. Zhang, R. Yang, and C. Zhang, ‘High-performance low-pass filter using stepped impedance resonator and defected ground structure,’ *MDPI Electronics*, vol. 8, no. 4, paper 403, Apr. 2019.

[14] M. Abdolmaleki, M. Dousti, and M. B. Tavakoli, ‘Design and simulation of fourth order low-pass Gm-C filter with novel auto-tuning circuit in 90 nm CMOS,’ *Analog. Integr. Circ. Sig. Process.*, vol. 107, no. 3, pp. 451-461, 2021.

[15] N. Ramesh, and J. S. Gaggatur, ‘A 0.6 V, 2nd order low-pass Gm-C filter using CMOS inverter-based tunable OTA with 1.114 GHz cut-off frequency in 90nm CMOS technology,’ *VLSID 21 Int. Conf. VLSI Design*, Guwahati (India), 20-24 Feb. 2021, pp. 305-309.

[16] Y. Lu, R. Krithivasan, W.-M. L. Kuo, X. Li, J. D. Cressler, H. Gustat, and B. Heinemann, ‘A 70 MHz–4.1 GHz 5th-order elliptic gm-C low-pass filter in complementary SiGe technology’ *BCTM 06 IEEE Bipolar/BiCMOS Circ. Technol. Meeting*, Maastricht, 8-10 Oct. 2006.

[17] F. Houfaf, M. Egot, A. Kaiser, A. Cathelin, and B. Nauta, ‘A 65nm CMOS 1-to-10GHz tunable continuous-time low-pass filter for high-data-rate communications,’ *ISSCC 12 IEEE Int. Solid-State Circuits Conf*., pp. 362,363, San Francisco CA, 19-23 Feb. 2012.

[18] N. Sabatino, G. Minoia, M. Roche, D. Baldi, E. Temporiti, and A. Mazzanti, ‘A 5th order gm-C low-pass filter with ±3% cut-off frequency accuracy and 220MHz to 3.3GHz tuning-range in 28nm LP CMOS,*’ESSCIRC 14 IEEE Eur. Solid-State Circuits Conf.*, pp. 351-354, Venezia, 22-26 Sep. 2014.

[19] H. Xiao, and R Schaumann, ‘Very-high-frequency lowpass filter based on a CMOS active inductor,’ *ISCAS 02 IEEE Int. Symp. Circuits Syst.* vol. 2, pp. 1-4, Phoenix AZ, 26-29 May 2002.

[20] Y. Chen, P.-I. Mak, L. Zhang, H. Qian, and Y. Wang, '0.013 mm^2, kHz-to-GHz-bandwidth, third-order all-pole lowpass filter with 0.52-to-1.11 pW/pole/Hz efficiency,' *Electron Lett.*, vol. 43, no. 21, pp. 1340-1342, Oct. 10 2013.

[21] M. A. S. Bhuiyan, M. B. I. Reaz, M. B. Omar, M. T. I. Badal, and N. A. Jahan, 'Advances in active inductor based CMOS band-pass filter,' *Micro and Nanosystems*, vol. 10, pp. 3-10, 2018.

[22] F. Centurelli, P. Monsurrò, and A. Trifiletti, 'A 19 GHz inductorless active SiGe HBT lowpass filter,' *Int. J. RF Microw. Computer-Aided Eng.*, vol. 28, no. 9, paper 21564, Nov. 2018.

[23] S.R. Aghazadeh, H. Martinez, A. Saberkari, and E. Alarcon, 'Tunable active inductor-based second-order all-pass filter as a time delay cell for multi-GHz operation,' *Circ. Syst. Sig. Process.*, vol. 38, no. 8, pp. 3644-3660, Aug. 2019.

[24] X. Wang, W. Zhang, W. Na, D. Jin, H. Xie, Y. Ren, N. Li, W. Gao, and Y. Wu, 'A novel CMOS active inductor with high quality factor, high linearity and mutually independent tuning of inductance and quality factor,' *Microelec. J.*, vol. 141, paper 105984, Nov. 2023.

[25] D. Baranauskas, D. Zelenin, M. Bussmann, S. Elahmadi, J. K. Edwards, and C. A. Gill, 'A 1.6-3.2-GHz sixth-order +13.1-dBm OIP3 linear phase gm-C filter for fiber-optic EDC receivers,' *IEEE Trans Microw Theory Tech.*, vol. 58, no. 5, pp. 1314-1322, May 2010.

[26] P. Wambacq, V. Giannini, K. Scheir, W. Van Thillo, and Y. Rolain, 'A fifth-order 880MHz/1.76GHz active lowpass filter for 60GHz communications in 40nm digital CMOS,' *ESSCIRC 10 Eur. Solid-State Circuits Conf.*, pp. 350-353, Seville, 14-16 Sep. 2010.

[27] M. Pecovsky, M. Sokol, and P. Galajda, 'Integrated low pass filter for M-sequence UWB radars,' *2020 Int. Conf. Radioelektronika*, Bratislava, 15-16 Apr. 2020.

[28] F. Centurelli, P. Monsurrò, G. Scotti, P. Tommasino, and A. Trifiletti, '10-GHz fully-differential Sallen-Key lowpass biquad filter in 55nm SiGe BiCMOS technology,' *MDPI Electronics*, vol. 9, no. 4, paper 563, Apr. 2020.

[29] C.-D. Wu, J.-Y. Hsieh, C.-H. Wu, Y.-S. Cheng, C.-C. Wu, and S.-S. Lu, 'An 1.1 V 0.1–1.6 GHz tunable-bandwidth elliptic filter with 6 dB linearity improvement by precise zero location control in 40 nm CMOS technology for 5G applications,' *ISCAS 17 IEEE Int. Symp. Circuits and Systems*; Baltimore MD, 28-31 May 2017.

[30] F. Centurelli, P. Monsurrò, G. Scotti, P. Tommasino, A. Trifiletti, 'A SiGe HBT 6th-order 10 GHz inductor-less anti-aliasing low-pass filter for high-speed ATI digitizers,' *IEEE Trans. Circ. Syst. I Regular Papers*, vol. 69, no. 1, pp. 100-113, Jan. 2022.

[31] C. Bocciarelli, F. Centurelli, P. Monsurrò, V. Spinogatti, and A. Trifiletti, 'A 17 GHz inductorless low-pass filter based on a quasi-Sallen-Key approach,' *Int. J. Circuit Theory Appl.*, vol. 51, no. 11, pp. 5066-5084, Nov. 2023.

[32] R. Gannedahl, and H. Sjöland, 'Active and passive integrated filters for multi-GHz 6G baseband applications,' *APMC 23 Asia-Pacific Microw. Conf.*, Taipei, 5-8 Dec. 2023, pp. 524-526.

[33] S. D'Amico, M. Conta, and A. Baschirotto, 'A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR,' *IEEE J. Solid-State Circ.*, vol. 41, no. 12, pp. 2713-2719, Dec. 2006.

[34] M. De Matteis, A. Pezzotta, S. D'Amico, and A. Baschirotto, 'A 33 MHz 70 dB-SNR super-source-follower-based low-pass analog filter,' *IEEE J. Solid-State Circ.*, vol. 50, no. 7, pp. 1516-1524, Jul. 2015.

[35] C. Sawigun, and S. Thanapitak, 'A 0.9-nW, 101-Hz, and 46.3-μV_{rms} IRN low-pass filter for ECG acquisition using FVF biquads,' *IEEE Trans. VLSI Systems*, vol. 26, no. 11, pp. 2290-2298, Nov. 2018.

[36] S. Bano, G. B. Narejo, and S. M. Usman Ali, 'Flipped voltage follower based fourth order filter and its application to portable ECG acquisition system,' *Integration the VLSI J.*, vol. 72, pp. 29-38, May 2020.

[37] M. De Matteis, F. Fary, E.A. Vallicelli, and A. Baschirotto, 'A 28 nm CMOS 100 MHz 67 dB-dynamic-range 968 mW flipped-source-follower analog filter,' *MDPI J. Low Power Electron. Appl.*, vol. 11, no. 2, 15, Jun. 2021.

[38] M. De Matteis, N. Galante, F. Fary, E. Vallicelli, and A. Baschirotto, '64 dB dynamic-range 810 mW 90 MHz fully-differential flipped-source-follower analog filter in 28nm-CMOS,' *IEEE Trans. Circ. Syst. II Express Briefs*, vol. 68, no. 9, pp. 3068-3072, Sep. 2021.

[39] D. Thakur, and K. Sharma, 'Ultra-low-power 4^{th}-order cascoded flipped source follower filter for portable biological healthcare systems,' *AEU Int. J. Electron. Commun.*, vol. 169, 154743, Sep. 2023.

[40] A. Cathelin, 'Fully depleted Silicon on insulator devices CMOS: The 28-nm node is the perfect technology for analog, RF, mmW, and mixed-signal System-on-Chip integration,' *IEEE Solid-State Circ. Mag.*, vol. 9, no. 4, pp. 18-26, Fall 2017.