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RESEARCH ARTICLE

A Novel High Performance Standard-Cell Based ULV OTA Exploiting an Improved Basic Amplifier

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ABSTRACT In this paper we introduce an improved standard-cell-based voltage amplifier cell with low output resistance. The proposed amplifier cell exhibits a voltage gain whose value can be accurately set by the number of paralleled inverters, and its output static voltage is well controlled through a replica bias approach. A three-stage fully synthesizable OTA architecture exploiting the improved voltage amplifier is also proposed. The OTA has been designed referring to the standard-cell library of a 180nm CMOS technology with a supply voltage of 0.3V and a nominal power consumption of only 6.63 nW, and exhibits a dc-gain of 73.5 dB with a gain-bandwidth-product of 9.63 kHz. A comparison against the state of the art of ultra-low-voltage OTAs has shown that the proposed amplifier exhibits the best value of the small signal figures of merit.

INDEX TERMS OTA, ULV, ULP, inverter-based, fully-synthesizable.

I. INTRODUCTION

The advent of the Internet-of-Things (IoT) has brought a plethora of advancements in the fields of electronics and communication, prompting researchers to reconsider traditional circuit design methodologies [1], [2]. Recent advancements in compact wireless autonomous devices [3], [4] are poised to facilitate ambulatory and non-invasive health parameter monitoring, leading to enhanced healthcare services [5], [6], [7]. These devices, functioning as wireless sensor nodes (WSN) [8], [9], [10], can be situated on or within the human body, especially in the case of implantable devices [11], [12]. Their primary purpose is to monitor neurological and physiological signals, including electrocardiography (ECG) [13], [14], electroencephalography (EEG) [15], [16], and electro-myography (EMG) [17], [18].

However, before the acceptance of WSN for health monitoring, many challenges including technological challenges and legal challenges must be addressed [19], [20]. These challenges encompass issues like privacy concerns and technology-related aspects such as reliability, security, form factor, low energy consumption, and energy autonomy, particularly for devices relying on harvested energy sources [21]. Among these challenges, minimizing the energy consumption of wireless sensor networks is often deemed one of the most critical issues [22]. This reduction in energy consumption holds the key to improving form factors, reliability, and security, for instance, by employing smaller batteries, extending battery life [23]. Substantial research efforts have been dedicated to this area in recent years. Notably, advancements in integrated circuit (IC) technology and circuit design techniques have led to systems with processing capabilities that can supplement or even entirely replace complex biomedical operations. It's essential to highlight that while ICs offer virtually unlimited processing capabilities, energy resources in biomedical electronics are profoundly limited [24], [25], [26].

Specialized low-power design techniques can enable dedicated solutions to operate with power consumption in the order of μW, ensuring over a decade of functionality with

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the same battery [27]. Furthermore, the demand for portable and wearable devices with stringent requirements has led to a drive for faster design times and reduced area usage to minimize costs [2]. In addition, since many IoT circuits rely on energy harvesting architectures [1], [2], [28], [29], [30], [31], there is an increasing appeal for the development of Ultra-Low-Voltage (ULV) analog building blocks capable of operating with supply voltages as low as 0.3V, such as OTAs [32], [33], [34], [35], [36], [37], [38], [39], comparators [40], [41], [42] and so on.

The Operational Transconductance Amplifier (OTA) is widely used in a plethora of analog applications, and recently, several high-performance ULV OTAs exploiting body-driven [32], [33], [34], [36], [37], [43], [44], [45], [46] and inverter-based [35], [47], [48], [49], [50], [51] architectures have been presented in the literature. All these OTAs require a full custom design approach in which the layout is carried out manually and often the area occupation is large because separate wells are needed for implementing body-driven stages.

Inverter-based OTAs rely on custom-defined inverters to achieve reasonable performance under process, supply voltage and temperature (PVT) variations [52], [53]. Custom inverters offer more degrees of freedom but have a larger area footprint compared to standard-cell inverters. Standard-cell inverters, on the other hand, are difficult to control in terms of bias point and can result in performance sensitivity to PVT variations. In order to reduce the sensitivity to PVT variations of standard-cell-based analog circuits several techniques to properly set internal node voltages have been proposed, resulting in improved robustness [54], [55].

Researchers have recently concentrated on optimizing and improving novel layout strategies in an effort to find a way to automate the design flow of analog blocks. These strategies include the automatic place and route strategies for standard-cell based circuits, which are typically used in the digital design flow to implement fully-synthesizable comparators [42], ADCs [56], DACs [57], LDOs [58], filters [59], and OTAs [60] for both IoT and biomedical applications. The goal is to speed up design time and drastically reduce the area and power consumption of analog building blocks implemented in the design flow of systems on chip (SoCs) for IoT and biomedical applications.

The recent introduction of the digital OTA (DIG-OTA) in [61] offers a new approach to designing OTAs with minimal area and power usage. In [62], a standard-cell implementation of the DIG-OTA is proposed, demonstrating good performance in terms of area consumption and Figures Of Merits (FOMs). However, DIG-OTAs are highly sensitive to PVT and mismatch variations and often require calibration or supply voltage adjustment for proper functionality [62], [63], [64].

A different approach based on the usage of digital standard-cells to mimic the behavior of analog circuits has been recently introduced [65], [66]. This is typically done by utilizing the inverter gate from a standard-cell library as a basic analog amplifier. In [55] a method has been proposed to center the dynamic-range of these inverters, making them more robust against PVT variations. In addition, novel topologies for differential to single-ended converters have been proposed [67] to improve common-mode rejection ratio and input common-mode range of standard-cell-based OTAs.

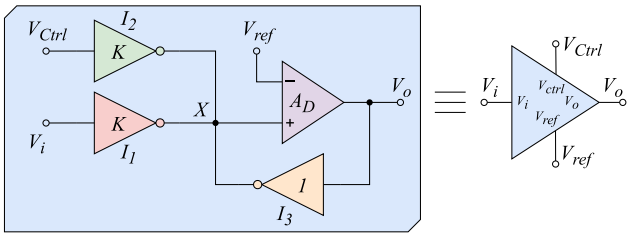


FIGURE 1. Block scheme of the proposed improved K-Amplifier.

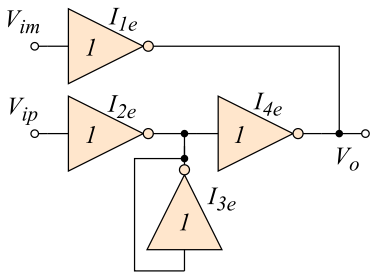


FIGURE 2. Gate level schematic of the error amplifier A_D.

To increase the gain and GBW of inverter-based OTAs, multiple stages need to be cascaded and additional capacitors are required for stability. In [65], the authors have proposed a standard-cell-based analog amplifier that is able to provide voltage gain without introducing high impedance nodes thus allowing the cascading of several amplifier stages. The main limitation of the standard-cell-based voltage amplifier cell proposed in [65] is its limited maximum gain. To overcome this limitation, an improved version of the voltage amplifier cell in [65] is proposed in this work. The proposed improved standard-cell-based voltage amplifier (denoted as K-Amplifier in the following) can attain a voltage gain whose value can be accurately set by the number K of paralleled inverters which results in a transconductance which is K times higher than the transconductance of the loading inverter.

In the following, Section II introduces the proposed standard-cell-based K-Amplifier, Section III discusses the proposed three stage OTA architecture exploiting the K-Amplifier and presents the results of the simulations, and finally conclusions are drawn in Section V.

II. PROPOSED K-AMPLIFIER SCHEME

The block scheme of the proposed improved standard-cell-based voltage amplifier cell (K-Amplifier) is depicted in Fig.1. It is composed by three inverters $I_{1,2,3}$, and a standard-cell-based differential amplifier A_D. The inverters $I_{1,2}$ are

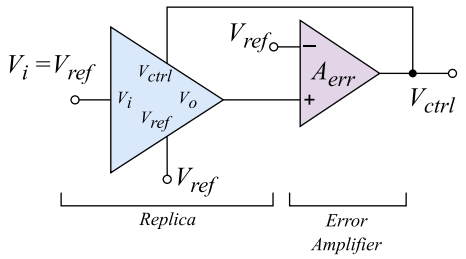


FIGURE 3. Block scheme of the replica biasing approach for the K-Amplifier.

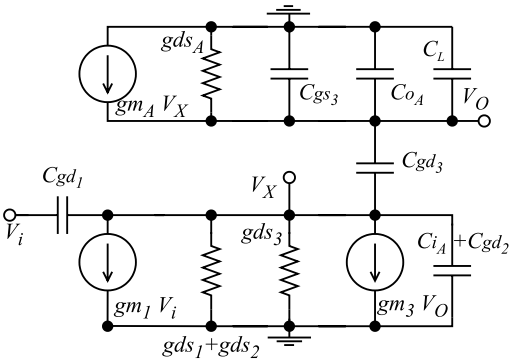


FIGURE 4. Equivalent circuit for small signal analysis.

implemented as the parallel of K instances of a reference inverter [65], whereas the I_3 is a single instance of the reference inverter. The inverters $I_{1,2}$ implement a basic-amplifier [55], in which I_1 is the signal amplifier and I_2 is exploited to properly set the static voltage at node X through a replica bias loop controlling the V_{Ctrl} voltage. The main difference of the circuit in Fig. 1 with respect to the previous implementation in [65] is the introduction of the error amplifier which allows to minimize the effect of the output conductance of $I_{1,2}$ at node X, thus enabling the possibility to achieve a voltage gain accurately set by the factor K for voltage gain values ranging from 0dB to 20dB as will be better shown in the following.

The gate level schematic of the standard-cell-based differential amplifier A_D is reported in Fig. 2. Looking at Fig. 2, it is evident that the differential to single-ended conversion relies on two signal paths. The path connected to V_{ip} consists of three inverters, I_{2e}, I_{3e}, and I_{4e}, the second of which, I_{3e}, has its input and output shorted between each other, while the path connected to V_{im} consists of just one inverter, I_{1e}. Comparing the standard-cell-based differential amplifier A_D against a conventional pseudo-differential pair with current mirror active load, a correlation can be observed between I_{1e}-I_{2e} and the pseudo-differential pair and between I_{3e}-I_{4e} and the current-mirror active load [55].

A. THE REPLICA BIAS APPROACH

The V_{Ctrl} voltage to properly set the static voltage at node X of the K-Amplifier in Fig.1 is generated by the replica bias control loop shown in Fig. 3. A replica bias approach similar to the one adopted in [55] is here exploited by enclosing a replica of the K-Amplifier cell within a negative feedback loop. The input of the replica K-Amplifier is biased with a voltage V_{ref}, typically set to $AGND = V_{DD}/2$, and the output of this replica K-Amplifier is compared with the reference voltage itself through an error amplifier denoted as A_{err} in Fig. 3, which generates the control voltage V_{ctrl}. The error amplifier A_{err} is implemented with the same schematic adopted for the differential amplifier A_D depicted in Fig. 2.

The purpose of the control voltage is to set the output voltage of the replica amplifier close to V_{ref} by compensating both the systematic and the PVT dependent components of the output current offset of the replica amplifier. This control voltage is then applied to the inverter I_2 of every K-Amplifier adopted in the chip for analog design purposes, thus guaranteeing a stable bias point of the amplifiers in all PVT conditions.

It is important to note that the replica bias loop in Fig. 3 does not necessitate any explicit compensation capacitor. This is due to the large parasitic capacitance driven by the error amplifier at node V_{ctrl}, which guarantees the minimum phase margin.

B. CIRCUIT ANALYSIS

The equivalent circuit for small signal analysis of the K-Amplifier is reported in Fig. 4, where the same notation as in [55] has been assumed for small signal parameters of inverters. The differential amplifier A_D in Fig. 1 is modeled in Fig. 4 with its small signal parameters gm_A, gds_A, Co_A and Ci_A, which denote the transconductance, the output conductance, the output capacitance, and the input capacitance respectively. The differential voltage gain A_D of the amplifier is therefore given by $A_D = gm_A/gds_A$. Starting from the circuit in Fig. 4, the transfer function of the K-Amplifier can be easily computed as:

$$\frac{Vo}{Vi} = -\alpha \cdot \frac{gm_1}{gm_3} \cdot \frac{(1 - s\tau_{z1})(1 + s\tau_{z2})}{(1 + s\tau_{p1})(1 + s\tau_{p2})} \tag{1}$$

where:

$$\alpha = \frac{1}{1 + \frac{gds_1 + gds_2 + gds_3}{gm_3 A_D}}, \quad \tau_{z1} = \frac{Cgd_1 + Cgd_2}{gm_1},$$
$$\tau_{z2} = -\frac{Cgd_3}{gm_A}, \quad \tau_{p1} = -\frac{\sum_{i=1}^{3} Cgd_i + Ci_A}{\sum_{i=1}^{3} gds_i}$$
$$\tau_{p2} = -\frac{C_L \sum_{i=1}^{3} gds_i}{gm_3 gm_A} \tag{2}$$

Equation 1 shows that the dc-gain of the K-Amplifier is set by the ratio of the transconductances of I_1 and I_3, with a non-ideality factor α which, considering that $gm_3 = K gm_1$ and $gds_3 = K gds_1$ can be rewritten as:

$$\alpha = \frac{1}{1 + \frac{2K gds_1 + gds_3}{k gm_1 A_D}} \tag{3}$$

According to eq. 3, the non-ideality factor α tends to 1 if the gain A_D of the error amplifier is large. Indeed the

role of the error amplifier introduced in this work with respect to the previous standard-cell-based voltage amplifier block presented in [65], is to minimize the negative impact caused by the output conductance of $I_{1,2}$ at node X, as this significantly restricts the achievable voltage gain of the previous version. However, even if the proposed K-Amplifier outperforms the previous version, a limited value of A_D still results in a constrained maximum achievable gain for the K-Amplifier as will be better pointed out through simulation results in the next Section.

In terms of frequency response, the dominant pole is determined by $p_1 = 1/\tau_{p1}$, and the two high frequency zeros can be neglected. The second pole of the K-Amplifier is determined by its load capacitance C_L, and unless C_L is excessively high, its effect can be disregarded.

Another important feature of the proposed K-Amplifier is its low output resistance. In fact, thanks to the feedback loop closed at node X, the output resistance of the K-Amplifier is lowered with respect to the output resistance of the previous version, and results to be $R_o \approx \frac{1}{g_{m3}A_D}$.

Finally, the equivalent input capacitance C_{in_1} of the proposed K-Amplifier can be easily computed as:

$$C_{in_1} \approx C_{gs_1} + C_{gd_1} \cdot (K+1) \tag{4}$$

where $C_{gd_1} \cdot (K+1)$ is the equivalent Miller capacitance.

C. K-AMPLIFIER DESIGN

The proposed K-Amplifier has been designed in a 180nm CMOS technology utilizing the minimum size standard-cell inverter as the reference inverter [65], and assuming a nominal supply voltage V_{DD} of 0.3V. The error amplifier in Fig. 2 has been also configured with minimum size standard-cell inverters achieving a voltage gain of 21 dB, which, considering also the gain of the inverter I_3, results in a loop gain in excess of 40dB for the feedback loop closed at node X. With such a loop gain the K-amplifier can be sized for large values of K, ideally approaching 100. Fig. 5 reports the gain of the K-Amplifier (Proposed Version) as a function of K, highlighting the accuracy of the voltage gain obtained with the proposed amplifier cell. The voltage gain predicted by eq. 1 (Model of Eq. 1), the voltage gain of the voltage amplifier block proposed in [65] (Previous Version), and the ideal value K (Ideal), are also reported in Fig. 5. As it can be observed, the maximum achievable gain of the previous version is limited to about 4 [V/V], and the accuracy with respect to the value of K is very low. On the other hand, the proposed K-Amplifier can be sized with $K = 10$ achieving a gain of 9.34 [V/V] confirming the high accuracy obtained thanks to the adoption of the error amplifier. Indeed, for $K = 10$, the attained gain is 19.41 dB and just 0.59 dB are lost with respect to the ideal value of 20dB. The maximum achievable gain of the K-Amplifier is in the order of 30 [V/V], but in this extreme condition the accuracy with respect to the value of K is lowered.

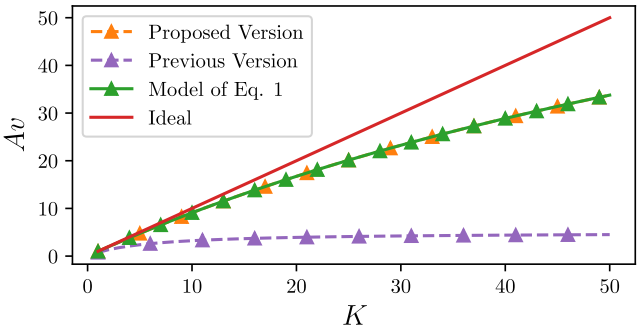


FIGURE 5. Voltage gain of the proposed K-Amplifier as a function of K.

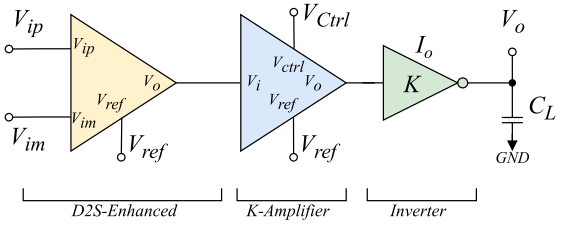


FIGURE 6. Proposed K-Amplifier based OTA.

D. ROBUSTNESS OF THE K-AMPLIFIER TO PVT AND MISMATCH VARIATIONS

In order to test the robustness of the proposed K-Amplifier under PVT and mismatch variations, the amplifier has been sized with $K = 10$, and corner and Monte Carlo simulations have been carried out. The voltage gain A_v of a single K-Amplifier for different process corners, supply voltages and temperatures is reported in Tab. 1. The mean value μ and the standard deviation σ of A_v estimated with 200 mismatch Monte Carlo runs are also reported in Tab. 1. The static output voltage of the K-Amplifier under PVT and mismatch variations has been also reported in Tab. 1. As it can be observed, due to the fact that the overall gain is set by the multiplicity (number of instances) of I_1 with respect to I_3, the proposed amplifier is able to guarantee a very stable voltage gain over the different working conditions, even considering mismatch variations. Results in Tab. 1 also confirm the capability of the replica bias approach to accurately set the static output voltage of the proposed K-Amplifier.

III. PROPOSED STANDARD-CELL-BASED OTA ARCHITECTURE EXPLOITING THE K-AMPLIFIER

The proposed standard-cell-based OTA architecture exploiting the K-Amplifier is reported in Fig. 6. The first stage is a differential to single ended converter (D2S), which has been implemented according to the topology presented in [67] and depicted in Fig. 7. Also the error amplifier A_D in Fig. 7 is implemented with the topology reported in Fig. 2.

The aim of the D2S is to convert the input differential signal into a single ended one, thus rejecting common mode input signals. After the D2S block, a K-Amplifier which sets its static output voltage to V_{ref} due to the replica-bias feedback loop, and whose gain can be set through the multiplicity K

TABLE 1. Voltage gain A_V and static output voltage of the K-Amplifier under PVT and mismatch variations.

	Process Corners					Supply Voltage [V]		Temperature °C		Mismatch	
	TT	FF	SS	FS	SF	270m	330m	0	80	μ	σ
Av [dB]	19.41	19.25	19.59	17.54	19.39	19.35	19.44	19.45	19.31	19.47	1.24
Vo@DC [mV]	149.99	149.93	149.89	144.96	142.59	133.51	166.48	149.99	149.91	150.3	5.12

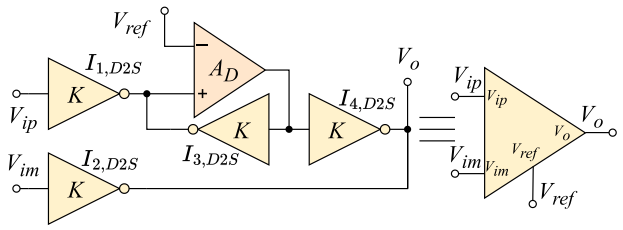


FIGURE 7. Enhanced D2S converter presented in [67].

of I_1 (see Fig. 1) is exploited as the second gain stage of the OTA. The final stage is a conventional standard-cell inverter I_o. This architecture is therefore a three stage OTA whose gain is typically higher than 60dB. In fact the overall dc-gain of the OTA can be expressed as:

$$Av = K \cdot \frac{gm_{4,D2Se}}{2 \cdot gds_{4,D2Se}} \cdot \frac{gm_o}{gds_o} \tag{5}$$

where $gm_{4,D2S}$ and $gds_{4,D2S}$ are the transconductance and the output conductance of $I_{4,D2S}$ in Fig. 7, gds_o is the output conductance of I_o and gm_o is the trunsconductance of I_o in Fig. 6. The common mode rejection ratio (CMRR) is provided only by the D2S, and can be written as [67]:

$$CMRR = A_D \cdot \frac{gm_{3,D2S}}{gds_{1,D2S} + gds_{3,D2S}} \tag{6}$$

where the small signal parameters refer to the inverters $I_{1,D2S}$ and $I_{3,D2S}$ in Fig. 7.

An important feature of the proposed OTA architecture is that, despite it can achieve high dc-gain, it does not require Miller compensation and can be compensated by a single large capacitive load. This is due to the low output resistance of the second stage of the proposed architecture, which results in a phase margin set by the value of the load capacitance C_L and by the sizing of the inverter I_O. In fact, it can be shown that the Gain Bandwidth Product (GBW) of the proposed OTA can be expressed as:

$$GBW = K \cdot \frac{gm_{4,D2S}}{2 \cdot gds_{4,D2S}} \cdot \frac{gm_o}{C_L} \tag{7}$$

Equation 7 confirms that the proposed three stage OTA exhibits just one internal high impedence node, at the output of the D2S, and an high impedance output node at the output of the OTA. The phase margin of the OTA can thus be expressed as:

$$m\varphi = 180 - \arctan\left\{GBW \cdot \frac{C_{in_1}}{gds_1 + gds_4}\right\} + - \arctan\left\{GBW \cdot \frac{C_L}{gds_o}\right\} \tag{8}$$

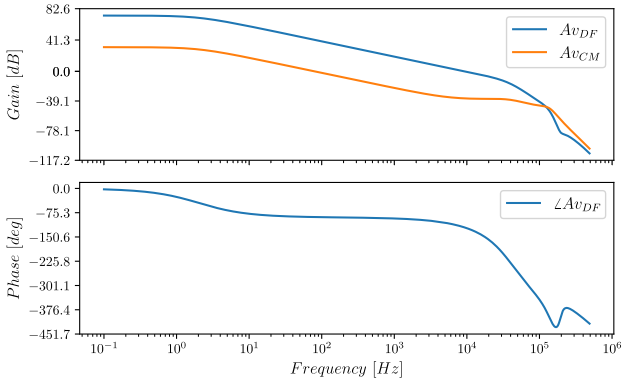


FIGURE 8. Differential and Common Mode gain of the proposed OTA.

where C_{in_1} is the equivalent input capacitance of the K-Amplifier computed in Section II-B. According to Eq. 7 and 8, a minimum load capacitance has to be guaranteed in order to attain the phase margin required to assure the stability of the OTA. The subthreshold current of the NMOS and PMOS transistors of the generic inverter from the standard-cell library can be expressed as:

$$I_{d_{n(p)}} \approx I_{0n(p)} e^{\frac{|Vgs_{n(p)}| - |Vth_{n(p)}|}{nUt}} \tag{9}$$

where $I_{0n(p)}$ can be written as:

$$I_{0n(p)} = \mu_{n(p)} \frac{W_{n(p)}}{L_{n(p)}} \sqrt{\frac{q\epsilon_{si} NDEP}{2\phi_s}} (k_B T/q)^2 \tag{10}$$

where $\mu_{n(p)}$ denotes the mobility of electrons (holes), $W_{n(p)}, L_{n(p)}$ are the widths and lengths of NMOS and PMOS of the inverter, q the electron charge, T denotes the absolute temperature, $NDEP$ is the channel doping concentration, ϵ_{si} is the dielectric constant of the silicon and ϕ_s is the surface potential.

The positive slew and negative slew rate can then be derived as:

$$SR_p = \frac{I_{0p}}{C_L} e^{\frac{V_{DD} - Vth_p}{nUt}}; \quad SR_m = \frac{I_{0n}}{C_L} e^{\frac{V_{DD} - Vth_n}{nUt}} \tag{11}$$

where, defining with $I^*_{0n(p)}$ the subthreshold current of the NMOS (PMOS) of the minimum sized inverter from the standard-cell library, it follows that the output slew rate will be K times the slew rate of the minimum sized standard-cell inverter, being $I_{0n(p)} = KI^*_{0n(p)}$.

IV. SIMULATION RESULTS

A. DESIGN FLOW AND NOMINAL SIMULATIONS

The proposed standard-cell-based OTA architecture exploiting the K-Amplifier whose schematic is reported in Fig. 6 has

TABLE 2. Performance of the OTA with respect to mismatch and process variations.

	TYP	Mismatch		FF	SS	FS	SF	0 deg	80 deg	$V_{DD} = 270mV$	$V_{DD} = 330mV$
		μ	σ								
P_D[nW]	6.63	6.86	0.401	25.23	1.565	12.15	6.16	1.828	47.47	4.396	10.43
Offset [mV]	0.234	0.1	4.71	0.223	0.229	3.40	0.068	0.2183	0.263	0.34	0.29
Av [dB]	73.52	73.48	2.078	69.87	79.57	74.90	69.63	75.07	70.67	72.4	74.34
GBW [kHz]	9.63	9.875	2.48	32.69	2.99	8.45	7.96	3.146	51.61	5.727	15.84
mφ [deg]	58.14	57.12	5.12	64.63	43	54.63	64.93	54.74	63.32	65.55	51.28
CMRR [dB]	42.01	37.11	9.81	39.87	42.57	31.10	43.40	42.24	40.26	37.81	43.75
PSRR [dB]	49.90	44.34	8.87	47.85	51.1	36.50	46.92	51.42	47.31	41.07	53.72
IRN@1kHz [$\mu V/\sqrt{Hz}$]	0.969	0.970	23.38	0.702	0.914	0.963	1.75	1.42	0.715	1.049	0.869
SR_p [V/ms]	0.146	0.146	0.011	0.757	0.022	0.038	0.540	0.050	0.669	0.062	0.112
SR_m [V/ms]	0.429	0.448	0.098	3.25	0.172	0.084	0.351	0.162	1.98	0.229	0.335

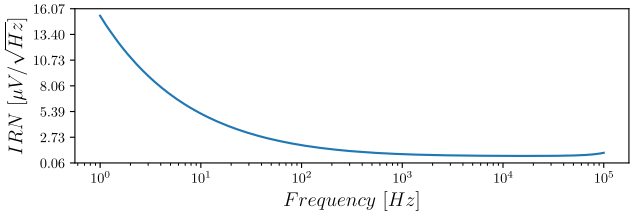


FIGURE 9. Equivalent input referred noise (IRN) in $\mu V/\sqrt{Hz}$.

been designed in a 180nm CMOS technology utilizing the minimum size standard-cell inverter as the reference inverter, and assuming a nominal supply voltage V_{DD} of 0.3V, and $K = 10$ in all the three stages (see Fig. 6).

The circuit in Fig. 6 has been described in structural Verilog language and the Verilog netlist has been used to generate the layout by means of an automatic place and route flow for digital circuits in the Cadence Innovus environment. The layout of the proposed OTA resulting from the automatic place and route flow is reported in Fig. 11, with a layout area of 17.78 μm x 47.46 μm.

The differential-mode gain Av_{DF} and the common-mode gain Av_{CM} of the OTA are reported in Fig. 8. It is worth noting that Av_{DF} exceeds 70 dB, whereas Av_{CM} ensures a minimum CMRR of about 40 dB. The minimum load capacitance, considering 45 [deg] of phase margin is about 175 pF. The equivalent input referred noise (IRN) is depicted in Fig. 9. Its value at the corner frequency (of about 1 KHz) is $969nV/\sqrt{Hz}$.

B. PVT AND MISMATCH PERFORMANCE CHARACTERIZATION

The main performance parameters under PVT and mismatch variations are summarized in Tab. 2. Notably, the voltage gain of the OTA is very stable under PVT and mismatch variations. Power consumption and GBW are dependent on the PVT conditions as in all standard-cell-based OTAs in which the bias current is not controlled.

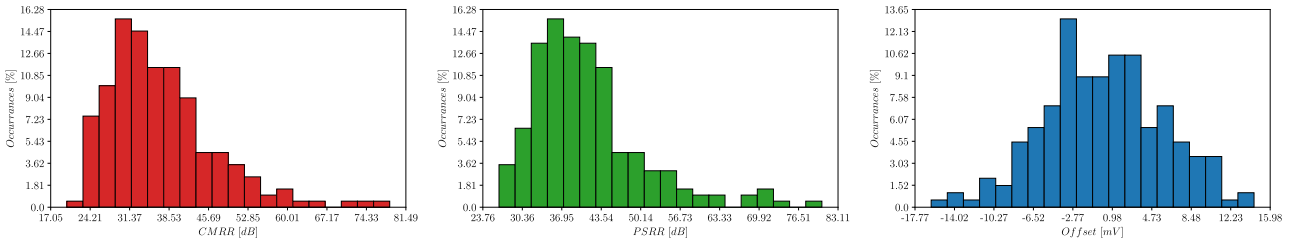
The OTA exhibits excellent offset performance under PVT and mismatch variations, with a standard deviation below 5 mV. This offset stability is primarily attributed to the implementation of a replica bias loop, as described in [55], which precisely sets the static output voltage of the standard-cells to $V_{ref} = V_{DD}/2$. In Fig. 10a it has been depicted the CMRR vs mismatch variations and as it can be observed the mean value of the CMRR is about 37 dB whereas the standard deviation is about 9.78 dB. The worst case CMRR is about 20 dB whereas the best case is about 78.56 dB. For what concerns the power supply rejection ratio (PSRR), it is depicted in Fig. 10b. As it can be observed, the PSRR has a mean value of about 44.34 dB with a standard deviation of about 8.87 dB. The worst case for the PSRR is about 26.46 dB whereas its best case is about 80.41 dB. The offset under mismatch and PVT variations has been reported in Tab. 1 and depicted in Fig. 10c. As it can be observed, the standard deviation of the offset is lower than 4.71 mV. For what concerns the GBW under mismatch variations, values reported in Tab. 1 a mean value of 9.875 kHz whereas the standard deviation is about 2.48 kHz, with a best case and worst case respectively equal to 5.26 kHz and 17.4 kHz.

C. COMPARISON WITH THE LITERATURE

To compare the performance of OTAs, the small-signal and large-signal Figures of Merit (FOM_S and FOM_L) are commonly adopted [33]. However, these metrics do not consider the amplifiers' area footprint, which is an essential aspect for a more comprehensive comparison. To address this limitation, the area-normalized $FOM_{S,A}$ and $FOM_{L,A}$ were proposed in [61]. These normalized FOMs are defined as:

$$FOM_{S,A} = \frac{GBW \cdot C_L}{P_D \cdot Area}; \quad FOM_{L,A} = \frac{SR_{avg} \cdot C_L}{P_D \cdot Area} \tag{12}$$

A comparison between recently published ULV OTAs is reported in Table 3, in which OTAs are classified in the fully synthesizable (Automatic Layout Flow Available) and not fully synthesizable (Automatic Layout Flow Not Available) categories. Notably, the proposed OTA achieves the highest dc-gain and the highest FOM_S and $FOM_{S,A}$ values, with good overall performances. With respect to other works, it can be observed that only [68] reaches an higher gain, but it can be also observed that, with respect to a capacitance of about 8 times lower than the one driven by the proposed OTA, the GBW results about 4 times lower. This is the proof that, the proposed technique, results in an effective GBW enhancement with respect to a minimum load capacitance. Similar considerations follow for other OTAs depicted in Table 3.



(a) (b) (c)

FIGURE 10. CMRR a) PSRR b) and offset c) of the proposed K-Amplifier based OTA under mismatch variations.

TABLE 3. Comparison table.

	Automatic Layout Flow Available				Automatic Layout Flow Not Available				
	This Work†	[65] †	[67]†	[66]†	[69]†	[70]‡	[32]†	[61]‡	[68]‡
Year	2023	2023	2022	2022	2023	2023	2022	2021	2020
Technology [μm]	0.18	0.13	0.13	0.13	0.028	0.13	0.13	0.18	0.18
V_{DD} [V]	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
DC_{gain} [dB]	73.52	50.33	34.97	28.3	66	86.83	52.92	30	64.7
C_L [pF]	250	150	2	1.5	250		50	150	30
GBW [kHz]	9.63	10.40k	12.69k	15.42k	12.3	10.32	35.16	0.25	2.96
$m\varphi$ [deg]	58.14	56.33	62.56	54	68	58.27	52.40	90	52
SR_p [V/ms]	0.146	631.4	4.54k	9.08k	-	2.32	18.61	-	1.9
SR_n [V/ms]	0.429	811.3	6.82k	9.08k	-	5.14	11.51	-	6.4
SR_{avg} [V/ms]	0.288	721.35	5.68k	9.08k	3.2	3.73	15.06	0.085	4.15
$CMRR$ [dB]	42.01	42.88	27.08	41.07	105	57.80	42.11	41	110
P_D [nW]	6.63	12.09k	6.10k	4.41k	44	33.73	21.89	2.4	12.6
$Mode$	STD-CELL	STD-CELL	STD-CELL	STD-CELL	DIGITAL	BD	BD	DIGITAL	BD
FOM_S $[\frac{MHz \cdot pF}{mW}]$	363.12k	128.2k	4.16k	5.25k	69.88k	10.70k	80.29k	15.89k	7.05k
FOM_L $[\frac{V \cdot pF}{\mu s \cdot mW}]$	10.859k	8.949k	1.86k	3.09k	18.18k	3.88k	34.40k	5.40k	9.88k
$Area$ $[\mu m^2]$	844	598	217.85	164	625	2340	5200	982	8500
$FOM_{S,A}$ $[\frac{MHz \cdot pF}{mW \cdot \mu m^2}]$	430.23	214.38	19.10	32.01	111.81	4.57	15.44	16.18	0.83
$FOM_{L,A}$ $[\frac{V \cdot pF}{\mu s \cdot mW \cdot \mu m^2}]$	12.87	14.96	8.54	18.84	29.09	1.66	6.62	5.50	1.16

† Simulated; ‡Measured.

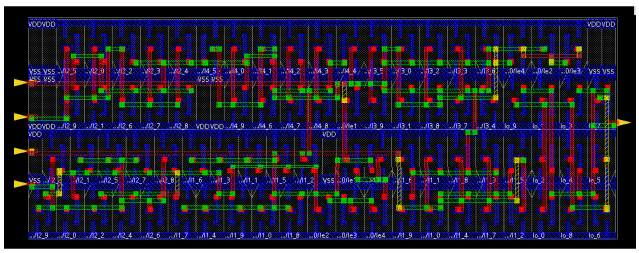


FIGURE 11. Layout of the proposed standard-cell-based OTA resulting from the automatic place and route flow.

V. CONCLUSION

In this work an improved standard-cell-based voltage amplifier with low output resistance has been proposed. The proposed K-Amplifier cell exhibits a voltage gain whose value can be accurately set by the number of paralleled inverters, and its output static voltage is well controlled through a replica bias approach. A three stage fully synthesizable OTA architecture exploiting the improved voltage amplifier has also been presented. Due to the low output impedance of the K-Amplifier, the proposed three stage OTA can be compensated through a single large capacitance at the output of the OTA. Simulation results in a 180nm CMOS process have demonstrated that, compared to previously published ULV OTAs, the proposed architecture achieves the highest Figures of Merit, FOM_S and $FOM_{S,A}$, while maintaining a consumption of merely 6.63 nW and a limited area footprint of 844 μm^2. This underscores the effectiveness of the K-Amplifier, which significantly enhances the OTA's GBW by a factor of K, resulting in a FOM_S approximately 10 times higher than the ones reported by previous ULV OTAs in the literature.

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