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Standard-Cell-Based Comparators for Ultra-Low Voltage Applications: Analysis and Comparisons

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Abstract: This work is focused on the performance of three different standard-cell-based comparator topologies, considering ultra-low-voltage (ULV) operation. The main application scenarios in which standard-cell-based comparators can be exploited are considered, and a set of figures of merit (FoM) to allow an in-depth comparison among the different topologies is introduced. Then, a set of simulation testbenches are defined in order to simulate and compare the considered topologies implemented in both a 130 nm technology and a 28 nm FDSOI CMOS process. Propagation delay, power consumption and power–delay product are evaluated for different values of the input common mode voltage, as a function of input differential amplitude, and in different supply voltage and temperature conditions. Monte Carlo simulations to evaluate the input offset voltage under mismatch variations are also provided. Simulation results show that the performances of the different comparator topologies are strongly dependent on the input common mode voltage, and that the best values for all the performance figures of merit are achieved by the comparator based on three-input NAND gates, with the only limitation being its non-rail-to-rail input common mode range (ICMR). The performances of the considered comparator topologies have also been simulated for different values of the supply voltage, ranging from 0.3 V to 1.2 V, showing that, even if standard-cell-based comparators can be operated at higher supply voltages by scaling their performances accordingly, the best values of the FoMs are achieved for V_{DD} = 0.3 V.

Keywords: standard cell; comparators; ultra-low voltage; ultra-low power; IoT

Citation: Della Sala, R. ; Centurelli, F.; Scotti, G.; Palumbo, G. Standard-Cell-Based Comparators for Ultra-Low Voltage Applications: Analysis and Comparisons. *Chips* **2023**, *2*, 173–194. https://doi.org/10.3390/chips2030011

Academic Editors: Paolo Crippa and Andrea Boni

Received: 18 April 2023
Revised: 13 July 2023
Accepted: 16 August 2023
Published: 18 August 2023

1. Introduction

A latched comparator is a circuit element that interfaces the analog to the digital world: its output is either a low or high logic level, according to the relationship between the input signal, sampled by the latching clock, and a reference threshold. Often, a differential input signal with an implicit zero reference level is used, but fully differential comparators that have explicit differential inputs both for the signal and for the reference are also used [1–6].

The latched comparator is a key building block for many mixed-signal applications, and finds wide diffusion in systems such as analog-to-digital converters (ADCs), wireline receivers, memory bit-line detectors and digital low-dropout regulators (DLDOs) [3,7–11]. The comparator is usually composed of an input preamplifier followed by a latch, often combined in the StrongARM topology [12–14], where a clocked transconductor drives a pair of cross-coupled inverters by their sources or, in the double-tail topology [15–18], where the clocked preamplifier and the latch use separate tail current branches. It is worth noting that, for high frequency applications, Current-Mode Logic (CML) latches are also used [11,19–22].

From a designer's point of view, the comparator is an analog block, and is typically designed according to the standard analog design flow. Indeed, both the schematic and

the layout design phases are carried out manually, iterating each step until specifications are met with a suitable robustness under process, supply voltage and temperature (PVT) variations and mismatches. The overall design effort, however, is highly time-consuming when compared to the typical semi-automatic digital design flow, so that the design of analog blocks requires a large fraction of the overall effort, even if they constitute a small portion of the overall system. There is, therefore, a strong drive to innovate the analog design flow, making it compatible with the automatic place-and-route CAD tools and possibly also allowing automatic sizing of the devices [23–28].

Following the above-described context, research trends are towards designing analog blocks using digital standard cells, either to mimic the behavior of analog building blocks [29–34] or by implementing analog functions in the digital domain [7,9,10,35–49]. A standard-cell-based implementation of analog functions simplifies the portability of designs among different technologies, and the speed vs. supply voltage reconfigurability. In particular, the standard-cell-based approach is well suited to a ultra-low voltage (ULV) context, where stacking of several devices becomes very difficult, thus limiting the use of typical analog design techniques such as cascoding.

The usual approach to design standard-cell-based latched comparators starts from a NAND-based [3,6–8,46] or NOR-based latch [50,51], and several designs have been presented in the literature to optimize different performances for applications in ADCs and LDOs [9,10,49,52–57]. However, such applications typically focus on different performance parameters, hence proposed designs are not always easy to compare. In this work, we analyze the main application scenarios for latched comparators to derive the performance parameters of interest and, hence, some suitably tailored figures of merit to evaluate and compare designs. We then review the main topologies for standard-cell-based latched comparators presented in the literature from these different viewpoints, defining a standardized characterization setup. This allows evaluating the suitability of the different topologies to the different application scenarios, and devising design guidelines for the optimization of comparators.

The paper is structured as follows: performance parameters and application scenarios are presented in Section 2, a review of the main standard-cell-based comparator topologies is reported in Section 3, whereas the simulation testbench and the figures of merit defined in this work to compare the different topologies in the different application scenarios are presented in Section 4. The results of the simulations and a comparative analysis are reported in Sections 5 and 6, respectively. Finally, some conclusions are drawn in Section 7.

2. Latched Comparators: Performance Parameters and Application Scenarios

2.1. Performance Parameters of the Latched Comparator

Several performance parameters can be defined to characterize the latched comparator, and they mostly concern its resolution, speed and energy consumption. The clock-to-output propagation time is defined as the comparator delay [16,58–60]: it measures the time that intercurs from the latching edge of the clock signal to the time when the output voltage can be identified as one of the logic levels (50% of the transition). The comparator delay sets the maximum speed of the comparator.

Other time-related parameters, shown in Figure 1, are the setup and hold times, defined as the time intervals where the input signal has to keep a stable value (or at least remain constantly above or below the reference), before and after the latching clock edge, respectively.

From the power dissipation point of view, the latched comparators do not typically have a static current. Power (P_D) is dissipated during latching and reset phases, i.e., in correspondence with positive and negative clock edges, and is usually measured as energy per conversion. Power consumption is often combined with the comparator delay (i.e., $P_D \cdot Delay$) to define the Power–Delay Product (PDP).

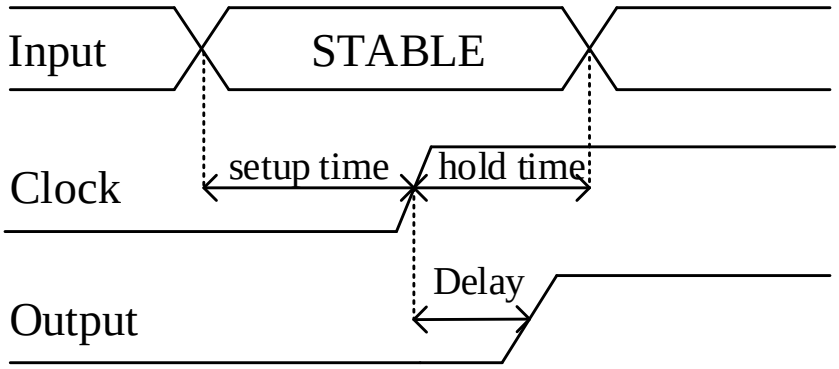


Figure 1. Comparator time-related parameters.

The comparator is used to establish if the input signal is above or below a given threshold, hence important performance parameters are related to its resolution, i.e., the minimum difference between signal and threshold that the comparator is able to resolve [61]. Several phenomena affect the comparator resolution. First of all, the time needed to settle the output to a logic level increases when the difference between the input and the reference gets smaller, tending to infinity when such difference goes to zero. Hence, for a finite available decision time, there is a minimum signal that can be resolved, and it is called the comparator sensitivity. For lower inputs, the comparator enters a metastable state [62–65], i.e., its output is neither a logic 1 nor a logic 0, and is strongly affected by other factors (memory effect, noise, disturbances, etc.).

Comparator resolution is also affected by offset and noise. The comparator offset, due to device mismatches, can be seen as a random signal that adds to the input, altering the comparison with the reference [60,66]. Noise in the comparator is important when the input signal is small and the comparator is near its tripping point, thus resulting in a linear periodically time-varying (LPTV) process [60,67,68].

Further performance parameters refer to the input interface of the comparator. In fact, in applications where the comparator interfaces with a capacitive source, its dynamic input current can alter the value of the charge stored in the capacitors [61,69], and its input capacitance is seen in parallel to the source capacitance, affecting the voltage-to-charge conversion. Moreover, the comparator behavior and performance is generally dependent on its input common-mode voltage, and a parameter of importance in some applications is the comparator input common mode range (ICMR).

2.2. Performance Parameters vs. Latched Comparators Applications

The main application fields of standard-cell-based latched comparators are analog-to-digital converters and digital LDOs. Whereas some performance parameters are important in all those cases, the different application scenarios pose different requirements on the comparator.

Stochastic flash ADCs [3,7,70–72] were one of the first architectures considered for standard-cell-based implementation. Basically, a large number of nominally identical comparators (i.e., with the same reference level) are used, and the statistical distribution of the offset is used to map the input voltage level in the output code. In this case, the standard deviation of the offset of the comparators sets the input voltage range of the ADC, hence a large offset dispersion results in an advantage. On the other hand, other performance parameters are of little importance, including the ICMR, since all the comparators use the same reference level (in a single-ended implementation, the common-mode voltage of the comparator is set by the reference level).

For all the other (non-stochastic) ADC architectures, sensitivity, offset and noise levels are very important specifications, and have to be compatible with the required resolution of the overall ADC. Typically specifications on noise and offset are very stringent, whereas the comparator sensitivity results often much lower than practical values of the quantization

levels; in this case, since sensitivity reduces in lower comparison times, designers can trade sensitivity for speed.

The requirements on ICMR are, instead, heavily dependent on the architectural details. In particular, flash ADCs use several comparators with different reference levels; hence, a large ICMR is required, unless a fully differential implementation is adopted. Focusing on successive-approximation-register (SAR) ADCs, details of the implementation make the difference. In a single-ended implementation, a solution where the input signal is sampled and compared with the DAC output [9] requires a large ICMR, whereas the implementation exploiting a capacitive DAC that is also used to sample the input signal, so that Vin-Vdac is compared with a fixed reference, has no ICMR requirement. The differential implementation generally features a capacitive DAC also used to sample the input signal, and compares the Vin-Vdac difference with an implicit zero reference level. This typically poses no requirement on the ICMR of the comparator, unless the set-and-down algorithm [73] is exploited. In this case, to minimize power consumption, such an algorithm acts on a single side of the differential capacitive DAC, thus also affecting the input common mode of the comparator, which evolves towards the bottom end of the input range as the conversion of each sample proceeds. If a rail-to-rail input range is considered, with an input common mode of $V_{DD}/2$, an ICMR from 0 to $V_{DD}/2$ is required. SAR ADCs with a capacitive DAC are affected by the input capacitance of the comparator, which has to be minimized, and by kickback noise, i.e., the dynamic input current of the comparator in correspondence of clock edges.

Discrete-time sigma-delta ADCs [51,74] are a further architecture where standard-cell-based latched comparators find an application: in this case, a single fixed reference voltage is used in a 1-bit quantizer; thus, requirements on both the comparator resolution and the ICMR are relaxed.

In the case of digital LDOs [10,46–49], a single comparator is used to compare the output voltage with the reference which, however, could be variable, with the aim of generating an adjustable output voltage. Requirements on the comparator resolution, i.e., offset and noise, are set by the acceptable ripple and error on the output voltage, and are typically less stringent than the requirements found for high-resolution ADCs. The need for a variable reference determines the specification for the ICMR.

Other requirements, such as comparator delay, energy per conversion and area footprint, are strongly dependent on the application, but their minimization can be always considered an important design goal.

3. A Review of the Main Topologies to Implement Standard-Cell-Based Dynamic Voltage Comparators

The first standard-cell-based comparator was proposed in [7], and is the one depicted in Figure 2a (denoted as a $NAND_3$-based comparator in the following figure). It is composed of a first stage, made up of two $NAND_3$ cells, and a second-stage NOR latch that samples and holds the output of the first stage. The two input terminals of the comparator are connected to the A input of the two $NAND_3$ gates. The differential input signal results are therefore amplified by the $NAND_3$ and by the following NOT gates.

The NOR_3-based version of the standard-cell-based comparator proposed in [7] is shown in Figure 2b (NOR_3-based comparator in the following figure). In this circuit, the two input terminals of the comparator are connected to the A input of the two NOR_3 gates. The differential input signal results amplified only by the NOR_3 gates, resulting in lower gain than in the $NAND_3$-based comparator. The transistor level schematics of the $NAND_3$ and NOR_3 gates are reported in Figure 3a,b, respectively, showing the connections of the input, the clock and the feedback signals.

As discussed in [55], the ICMR of the comparator in Figure 2a is limited to voltages larger than $V_{DD}/2$, whereas lower voltages cause the comparator to stop operating. In a similar way, a dual issue occurs for the comparator in Figure 2b, in which the ICMR is limited to voltages lower than $V_{DD}/2$.

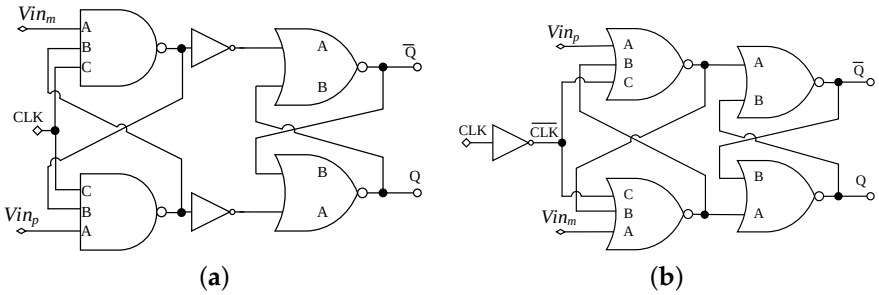


Figure 2. Comparators presented in [7] with $NAND$ logic gates (**a**) and NOR gates (**b**).

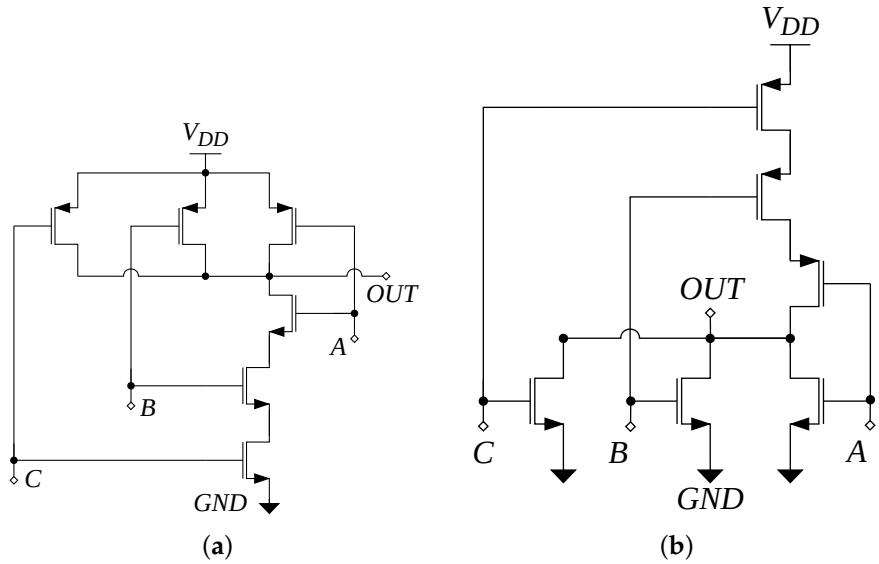


Figure 3. Schematic of logic cells $NAND_3$ (**a**) and NOR_3 (**b**).

The above limitations to the ICMR for the comparators in Figure 2a,b can be overcome by using the rail-to-rail comparator presented in [52,55] and shown in Figure 4 (rail-to-rail comparator in the following figure). The comparator in Figure 4 combines the digital outputs of the $NAND_3$- and NOR_3-based comparators in a complementary way, as in rail-to-rail analog operational amplifiers. It has to be pointed out that this paper focuses on comparators which do not require specific gates, which may have different schematic-level implementations in the different technologies and libraries and, therefore, can be implemented in all the digital standard-cell libraries. In particular, since the comparator proposed in [53] exploits the specific schematic level implementation of the AOI and OAI gates, which is, in general, different in the different standard-cell libraries, we have not included this circuit in the comparisons.

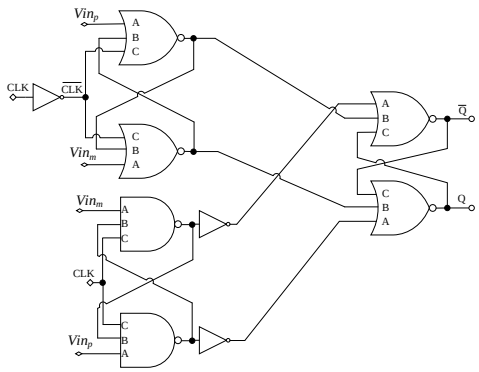


Figure 4. Comparator presented in [52,55].

4. Simulation Testbench and Figures of Merit

In order to test the performance of the comparators reported in [7,52,55] we have carried out simulations referring to the standard-cells library of both a 130 nm bulk-CMOS process and a 28 nm fully depleted silicon on insulator (FDSOI) CMOS technology from STMicroelectronics, in the Cadence Virtuoso environment. More specifically, a high-performance library based on a low threshold voltage and high speed transistors has been adopted for the 130 nm technology, whereas and an high-density library based on standard threshold voltage and low leakage transistors has been chosen for the 28 nm technology. Each comparator output has been loaded by a minimum size inverter taken from the standard-cells library, as is typically performed for measuring the propagation delays of digital gates. To carry out a fair comparison, the minimum size standard-cells have been adopted to implement all the comparator topologies. A supply voltage of 0.3 V has been assumed to compare the different topologies working in a ULV regime, as deduced by literature applications of standard-cell-based comparators. Further, to provide more complete information to the reader, a technology comparison for 0.6 V, 0.9 V and 1.2 V (especially this last two values now not represent ULV operation) has been carried out on the 130 nm CMOS.

4.1. Testbench Description

An ad hoc testbench has been designed to characterize the main performance parameters of the standard-cell comparators. In this section, we explain in detail how the main performance parameters have been evaluated.

4.1.1. Propagation Delay vs. Input Common Mode Voltage

The clock-to-output propagation delay of the different comparators has been evaluated with considering different input common mode voltages in the following test conditions:

- Supply voltage $V_{DD} = 0.3$ V;
- Input common mode varied in the range between 0 and V_{DD};
- Differential input signal amplitude of 10 mV;
- Temperature of 27 °C.

The differential input signal amplitude of 10 mV has been assumed as a trade-off between a very small input signal (i.e., high sensitivity) and speed.

4.1.2. Propagation Delay vs. Input Differential Signal Amplitude

The clock-to-output propagation delay characteristic versus the input differential signal amplitude has been carried out with considering the following parameters:

- $V_{DD} = 0.3$ V;
- Input common mode voltage set at $\frac{V_{DD}}{4}$, $\frac{V_{DD}}{2}$ and $\frac{3V_{DD}}{4}$;
- Temperature set at 27 °C.

The three points, $\frac{V_{DD}}{4}$, $\frac{V_{DD}}{2}$ and $\frac{3V_{DD}}{4}$, have been chosen to sample the ICMR, because they represent the midpoint of the ideal ICMR of the NOR_3, rail-to-rail and $NAND_3$ comparators, respectively.

4.1.3. Power Consumption vs. Input Common Mode Voltage, Supply Voltage and Temperature Variations

The power consumption versus the input common mode voltage has been estimated with considering:

- $V_{DD} = 0.3$ V $\pm$ 10%;
- A differential input signal amplitude of 10 mV;
- A clock frequency set at 10 Hz and at 10 MHz;
- A temperature varying from 0 to 80 °C.

The clock frequency set at 10 Hz is in agreement with previous works dealing with ULV standard-cell-based comparators. Since we have found that for such a low clock frequency, static power is not negligible, to better compare the different topologies, we have also computed power consumption at a frequency of 10 MHz, which has been chosen as a frequency in which power consumption is dominated by dynamic power and at which all comparators can reliably operate. The temperature range has been chosen in agreement with several papers dealing with ULV circuits [75–77], as well as the supply voltage variation.

4.1.4. Input Offset Voltage vs. Supply Voltage, Temperature and Mismatch Variations

The input offset voltage of the comparators has been evaluated in the following conditions:

- V_{DD} = 0.3 V;
- An input signal varying linearly with time in a transient simulation;
- A differential input signal amplitude ranging from −70 mV to +70 mV;
- Monte Carlo simulations using statistical models provided by IC manufacturers are used to account for technology mismatches;
- 1000 Monte Carlo runs have been performed on each topology.

4.2. Figures of Merit Definition

The Power–Delay Product (PDP) is a commonly adopted parameter to quantify how good the trade-off between speed performance and power consumption is, and is also used in the context of comparator design. Even if the PDP is useful to quantify the performance of comparators in almost all ADC and LDO applications, it does not take into account other important aspects that, depending on the specific application, should also be considered as primary parameters of interest. For example, the PDP does not account for the standard deviation of the offset under mismatch variations, which is very important in the context of both ADCs and digital low-dropout regulator (DLDO) designs. Thus, in order to allow a more complete characterization and comparison among different comparator topologies in different application scenarios, we introduce the following figures of merit (FoMs), which are suitable for use in the different application scenarios.

FOM_{off}

In almost all applications of comparators, the input offset voltage is one of the key parameters that has to be taken into account, especially when one has to consider the design strategies to adopt. Though some applications, such as ΣΔ and SAR, require comparators with high performance in terms of PDP and offset voltage near 0 mV, comparators adopted in stochastic flash ADCs require an offset voltage with high variance in order to cover a dynamic range as wide as possible with respect to the supply voltage range. In detail, when mismatch occurs in CMOS technologies, the offset voltage represents a concern, and its standard deviation depends on the comparator topology, CMOS technology node, adopted design strategy, and sizing of the standard cells. Thus, to evaluate the efficiency of a topology, we have to combine both PDP and offset. However, depending on the application, the offset has to be accounted for in two different ways. In particular, the two following FoMs can be introduced:

$$\begin{cases} FOM_{off} = P_D \cdot Delay \cdot \frac{\sqrt{\sigma_{off}^2+\mu_{off}^2}}{V_{DD}} & \text{for SAR, ΣΔ and LDO;} \\ FOM_{off,SF} = \frac{P_D \cdot Delay}{\sqrt{\sigma_{off}^2+\mu_{off}^2}/V_{DD}} & \text{for Stochastic Flash ADCs;} \end{cases} \quad (1)$$

where μ_{off} and σ_{off} denote the mean value and the standard deviation of the offset, and have been normalized to the supply voltage (i.e., the maximum allowed voltage range).

Indeed, for what concerns SAR, ΣΔ and also LDO applications, we consider that, ideally, the standard deviation of the offset should be 0mV; thus, the greater the standard deviation normalized to the supply voltage is, the greater the FOM_{off} would be. For an

ideal comparator with no power consumption, no delay and no offset standard deviation, FoM_{off} tends to 0 and, in general, the lower the FOM_{off} value is, the better the performance of the comparator is. On the other hand, for stochastic flash ADC applications, a larger offset would imply a larger voltage range; thus, a greater normalized standard deviation of the offset should imply a lower $FOM_{off,SF}$ and thus better performance.

4.3. FOM_{cm}

Another important parameter which has to be taken into account in the evaluation of comparators' performance is the ICMR. This is a key parameter which researchers are working on, and several improvements have been proposed in the recent literature [52,53,55]. In this regard, in order to characterize and take into account this performance, FOM_{cm} is introduced:

$$FOM_{cm} = \frac{P_D \cdot Delay}{ICMR/V_{DD}} \tag{2}$$

which is a measure of the PDP multiplied by the ICMR normalized to the supply voltage V_{DD}. Hence, the greater the ICMR is, the lower FOM_{cm} will be, denoting better performance.

4.4. A Universal FoM

With the aim of providing a single FOM which takes into account all the key parameters of comparators, the Universal FoM FOM_{Uni} is here defined as:

$$\begin{cases} FOM_{Uni} = \frac{P_D \cdot Delay \cdot \sqrt{\sigma_{off}^2 + \mu_{off}^2}}{ICMR} & \text{for SAR, } \Sigma\Delta \text{ and LDO;} \\ FOM_{Uni,SF} = \frac{P_D \cdot Delay \cdot V_{DD}^2}{\sqrt{\sigma_{off}^2 + \mu_{off}^2} \cdot ICMR} & \text{for Stochastic Flash ADCs;} \end{cases} \tag{3}$$

obtained by combining the $ICMR$ with FOM_{off}.

In addition, since in these FoMs the silicon area is not taken into account, a further FoM, $FOM_{Uni_{norm}}$, which also allows accounting for the silicon area normalized to F^2 (i.e., according to the minimum feature size of the technology), is introduced as follows:

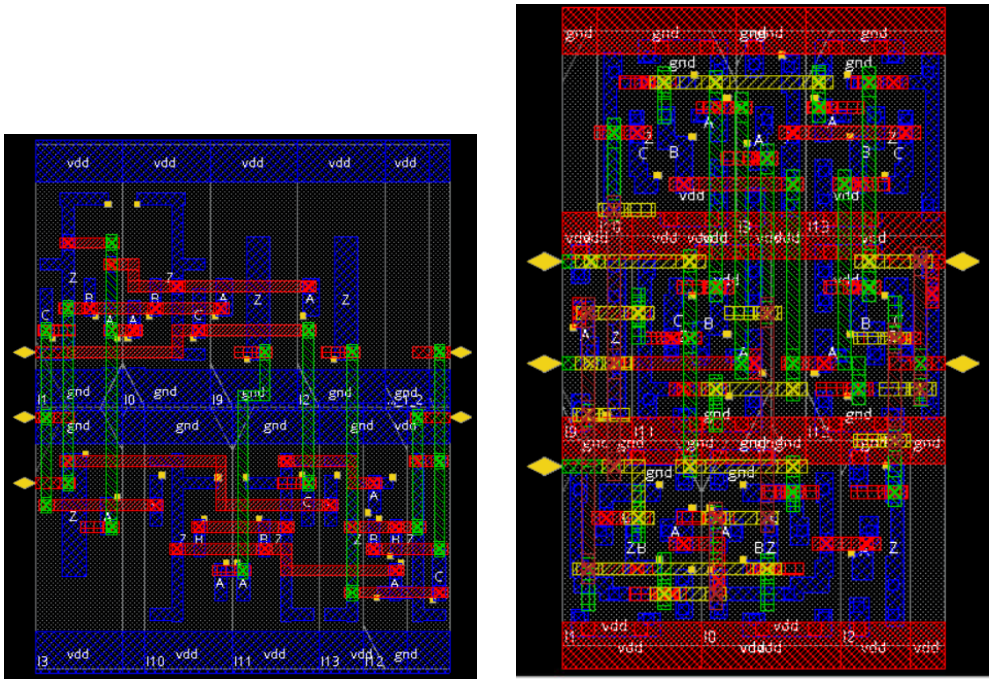
$$\begin{cases} FOM_{Uni_{norm}} = \frac{P_D \cdot Delay \cdot \sqrt{\sigma_{off}^2 + \mu_{off}^2}}{ICMR} \cdot \frac{Area}{Min_{Area}} & \text{for SAR, } \Sigma\Delta \text{ and LDO;} \\ FOM_{Uni_{norm},SF} = \frac{P_D \cdot Delay \cdot V_{DD}^2}{\sqrt{\sigma_{off}^2 + \mu_{off}^2} \cdot ICMR} \cdot \frac{Area}{Min_{Area}} & \text{for Stochastic Flash ADCs;} \end{cases} \tag{4}$$

where $Area$ is the silicon area occupation of the comparator and Min_{Area} denotes a scaling factor equal to square of the minimum feature size of the technology (i.e., (0.13 µm)^2 for a 130 nm technology node). Of course, smaller comparators imply a smaller normalized area, and thus a lower $FOM_{Uni_{norm}}$.

5. Simulation Results

In this section, we compare the different comparator topologies by means of simulations referring both to a well-assessed, commercial 130 nm CMOS, and a more recent, Fully Depleted Silicon on Insulator (FDSOI) 28 nm CMOS. All the simulations have been carried out on post-layout with back-annotated parasitics. The layouts of all the circuits have been generated by an automatic place-and-route flow within the Cadence Innovus tool, and the layout screenshots for the rail-to-rail topology implemented in the 130 nm and 28 nm technologies are reported in Figure 5a,b, respectively. Simulation results evaluating the delay, input offset voltage, power dissipation and Power–Delay Product of the different standard-cell-based comparators are presented, focusing on their performances in ULV conditions. The different topologies are compared for a nominal supply voltage

$V_{DD} = 0.3$ V, according to previous papers dealing with standard-cell-based comparators and ULV circuits [52,55,75–77], and performances are analyzed also under supply voltage and temperature variations. Mismatch variations are assessed through Monte Carlo simulations. The comparison is then also extended, for the 130nm CMOS technology, to higher supply voltages, in order to check if main comparison results are maintained.



(**a**) (**b**)

Figure 5. Layout screenshots for the rail-to-rail topology implemented in the 130 nm technology with an area of 9.84 × 7.79 µm^2 (**a**), and implemented in the 28 nm technology with an area of 2.4 × 1.5 µm^2 (**b**).

5.1. $NAND_3$-Based Comparator

This subsection reports the analysis and characterization of the comparator topology depicted in Figure 2a, proposed in [7] ($NAND_3$-based comparator).

5.1.1. Propagation Delay

The propagation delay of the $NAND_3$-based comparator, measured according to Figure 1 as a function of the input common mode voltage, and considering a clock frequency of 10 Hz and an input differential signal of 10 mV, is reported in Figure 6a. It is evident from Figure 6a that the ICMR is not rail-to-rail; indeed, as expected, the comparator works fine for input common mode voltages V_{CM} higher than $V_{DD}/2 = 150$ mV, whereas for V_{CM} lower than 150 mV the delay starts to highly increase with respect to the nominal value. In fact, when the input common mode voltage is increased, the gate-source voltage of the NMOS transistor connected to the input signal (see Figure 3a) is lowered, and the current driving of the transistor is worsened. The abrupt rise in the propagation delay is due to the gate-source voltage of the NMOS transistor connected to the input signal to approach the threshold voltage of the device, thus drastically limiting its current drive capability.

The propagation delay as a function of the input differential signal amplitude for the $NAND_3$-based comparator is reported in Figure 6b for an input common mode voltage of $\frac{3}{4} \cdot V_{DD}$, which, for this comparator topology, is the mid-point of the ideal ICMR, and is therefore close to the V_{CM}, at which delay is minimum. As can be observed, the propagation delay increases as the signal amplitude decreases, and the worst-case propagation delay occurs when the minimum differential input amplitude (1 mV) is considered.

The delay of the comparator as a function of the supply voltage and as a function of the temperature is reported in Figure 7a,b, respectively, showing the delay dependence on environmental conditions: propagation delay decreases at higher supply voltages and temperatures.

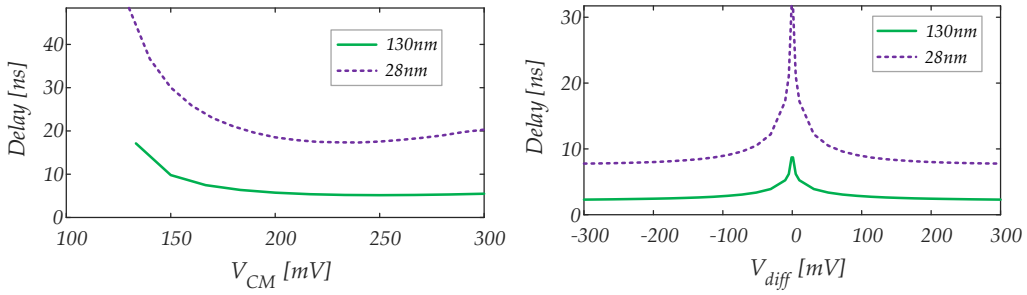


Figure 6. Propagation delay of the $NAND_3$-based comparator as a function of the input common mode voltage (**a**) and input differential signal amplitude (**b**).

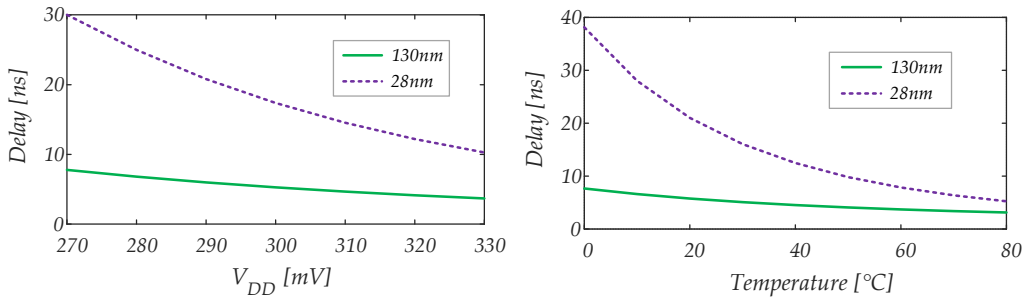


Figure 7. Propagation delay of the $NAND_3$-based comparator with respect to supply voltage variations (**a**) and temperature variations (**b**).

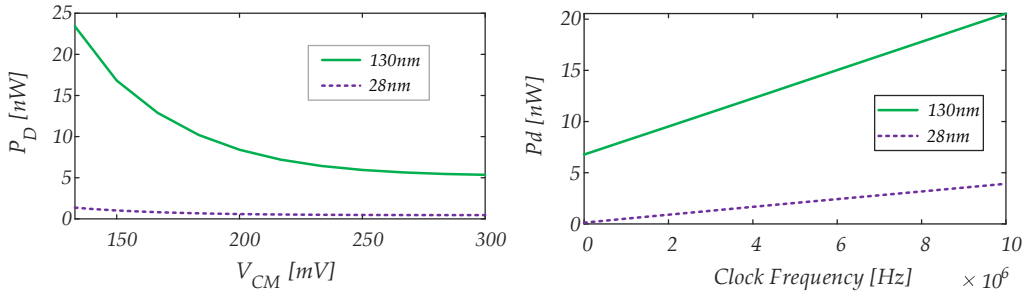
It is interesting to note that the propagation delay of the $NAND_3$-based comparator implemented in the 130 nm technology is faster than the $NAND_3$-based comparator implemented in the 28 nm technology. This is mainly due to the different threshold voltages of MOS devices in the two digital libraries adopted for the design. Considering the supply voltage of only 0.3 V since, for the 130 nm technology, low threshold voltage transistors are used, they are able to drive a higher current with respect to the high threshold voltage transistors adopted for the 28 nm library, resulting in faster operation. Obviously, this leads to higher power consumption of the comparator in 130 nm with respect to the comparator in 28 nm, as will be shown in the next section.

5.1.2. Power Consumption and Power–Delay Product

The power consumption versus the input common mode voltage of the $NAND_3$-based comparator measured at an operating frequency of 10 Hz is reported in Figure 8a, whereas Figure 8b shows the power dissipation of the $NAND_3$-based comparator as a function of the clock frequency for an input common mode voltage of $\frac{3}{4} \cdot V_{DD}$. Power consumption at 10 Hz is dominated by static power (which is particularly high for the 130 nm bulk CMOS technology) whereas, at higher frequencies, the dynamic power is the most relevant. In both figures, it is evident that power consumption in 28 nm is much lower than power consumption in 130 nm. This result was expected and is due to two main reasons:

- The minimum-sized gates in 28 nm exhibit a much lower parasitic capacitance than the minimum-sized gates in 130 nm, thus resulting in much lower dynamic power;
- The transistors of the considered 130 nm technology exhibit a lower threshold voltage compared to the transistors of the considered 28 nm FDSOI technology, and this results

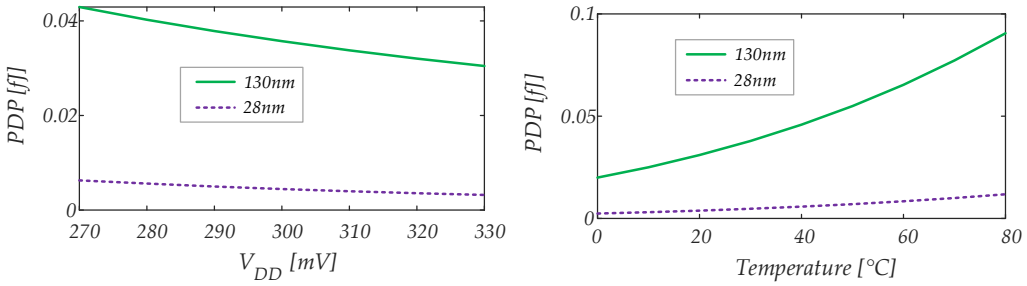
in deeper subthreshold operation for the 28 nm transistors at V_{DD} = 0.3 V, resulting in much lower static power consumption for the 28 nm technology.



(**a**) (**b**)

Figure 8. Power dissipation of the $NAND_3$-based comparator as a function of the input common mode voltage measured @ 10 Hz (**a**), and power dissipation of the $NAND_3$-based comparator as a function of the clock frequency for an input common mode voltage of $\frac{3}{4} \cdot V_{DD}$ (**b**).

The Power–Delay Product (PDP) of the $NAND_3$-based comparator has been simulated under supply voltage and temperature variations, and the results are reported in Figure 9a,b, respectively. Of course, it is evident that the 28 nm technology allows the achieving a much lower PDP.

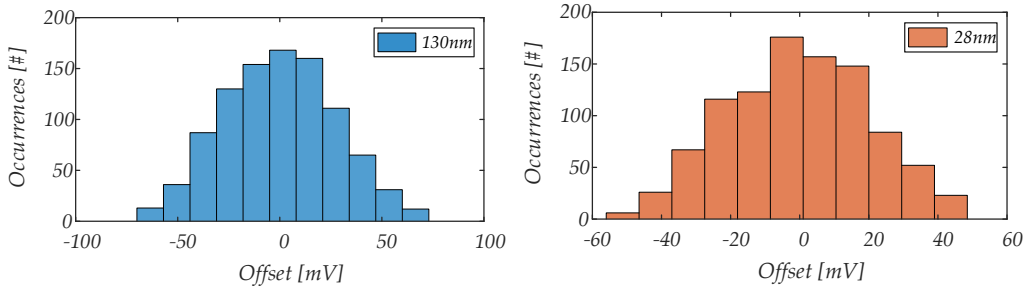


(**a**) (**b**)

Figure 9. Power–Delay Product (PDP) of the $NAND_3$-based comparator with respect to supply voltage variations (**a**) and temperature variations (**b**).

5.1.3. Offset

The input offset voltage of the $NAND_3$-based comparator has been evaluated considering an input common mode voltage equal to $\frac{3}{4} \cdot V_{DD}$. In order to account for the effect of mismatch, 1000 Monte Carlo simulations have been carried out, and results are reported for the 130 nm technology in Figure 10a and for the 28 nm technology in Figure 10b, showing that the input offset voltage can be described with a Gaussian distribution with mean value and standard deviation equal to $\mu \approx -0.27$ mV, $\sigma \approx 27.4$ mV for the 130 nm technology, and $\mu \approx -0.41$ mV, $\sigma \approx 20.2$ mV for the 28 nm technology.



(**a**) (**b**)

Figure 10. Input offset voltage of the $NAND_3$-based comparator evaluated by using 1000 mismatch Monte Carlo simulations for the 130 nm technology (**a**) and for the 28 nm technology (**b**).

5.2. NOR_3-Based Comparator

This section reports the analysis and performance characterization of the comparator topology depicted in Figure 2b, proposed in [7] (NOR_3-based comparator).

5.2.1. Propagation Delay

The propagation delay as a function of the input common mode voltage for the NOR_3-based comparator is reported in Figure 11a. It is evident from Figure 11a that the ICMR is not rail-to-rail; indeed, the NOR_3-based comparator works fine for input common mode voltages V_{CM} lower than $V_{DD}/2 = 150$ mV, as expected, whereas, for V_{CM} approaching 150 mV, the delay results drastically increased with respect to the nominal value. In the case of the 28 nm technology, the ICMR is limited to a range from 0 to 110 mV.

The propagation delay as a function of the input differential signal amplitude for the NOR_3-based comparator is reported in Figure 11b for an input common mode voltage of $V_{DD}/4$. As can be observed, the delay increases when the differential input amplitude is lowered. At this purpose, it has to be pointed out that the NOR_3-based comparator is not able to properly work for input differential signal amplitudes below 2.2 mV, and this is probably due to its lower gain with respect to the $NAND_3$-based comparator, where the input signal is further amplified by a NOT gate, which is not present in the NOR_3-based comparator topology (see Figure 2b).

The delay of the comparator as a function of the supply voltage and as a function of the temperature is reported in Figure 12a,b, respectively, showing the delay dependence on environmental conditions. Furthermore, in this case, it is interesting to note that the propagation delay of the NOR_3-based comparator implemented in the 130 nm technology is smaller than for the $NORr_3$-based comparator implemented in the 28 nm technology. This is mainly due to the different threshold voltages of MOS devices in the two digital libraries adopted for the design.

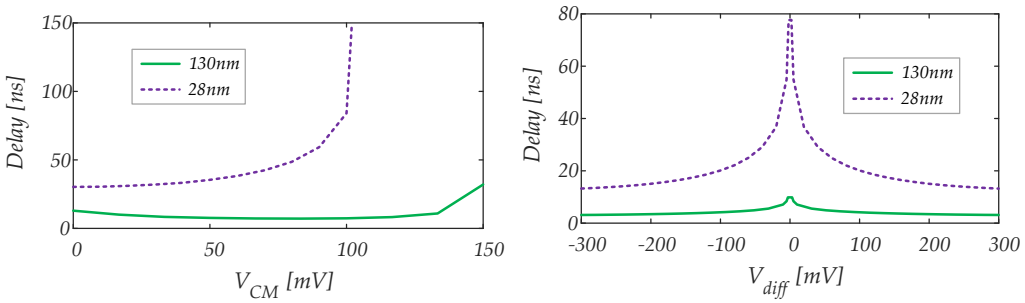


Figure 11. Propagation delay of the NOR_3-based comparator as a function of the input common mode voltage (**a**) and input differential signal amplitude (**b**).

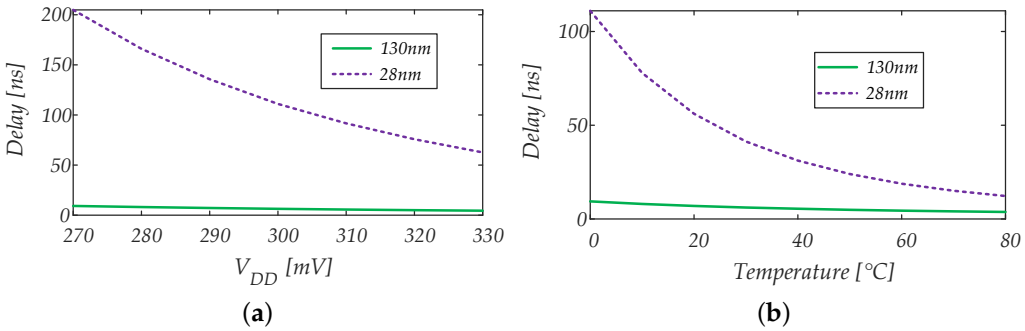
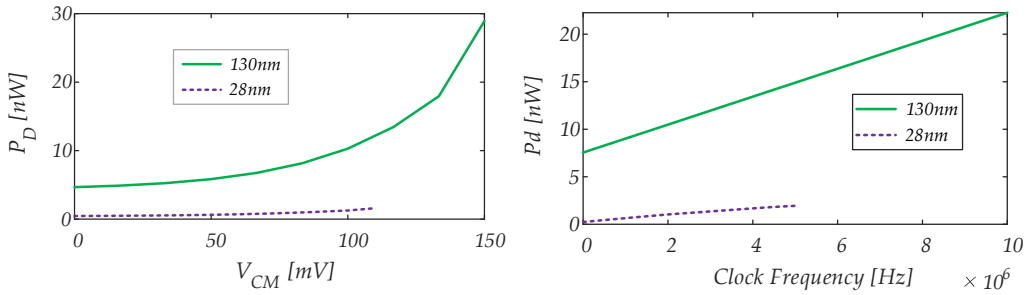


Figure 12. Propagation delay of the NOR_3-based comparator with respect to supply voltage variations (**a**) and temperature variations (**b**).

5.2.2. Power Consumption and Power–Delay Product

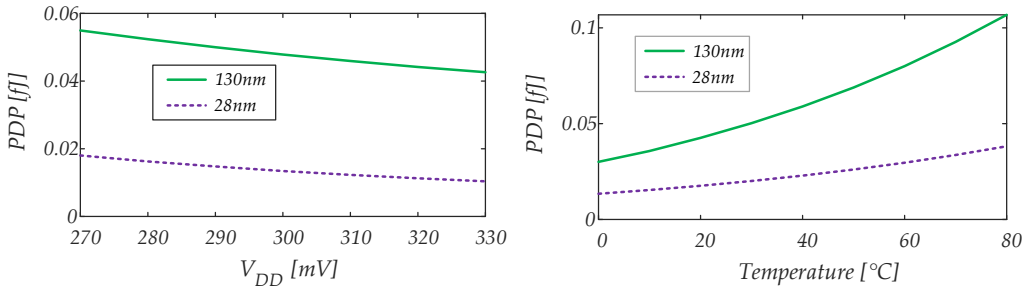
The power consumption versus the input common mode voltage of the NOR_3-based comparator measured at an operating frequency of 10 Hz is reported in Figure 13a, whereas Figure 13b shows the power dissipation of the NOR_3-based comparator as a function of the clock frequency for an input common mode voltage of $V_{DD}/4$. The same considerations for the $NAND_3$-based comparator in terms of static and dynamic power components also apply in this case.



(**a**) (**b**)

Figure 13. Power dissipation of the NOR_3-based comparator as a function of the input common mode voltage measured @ 10 Hz (**a**), and power dissipation of the NOR_3-based comparator as a function of the clock frequency for an input common mode voltage of $V_{DD}/4$ (**b**).

The Power–Delay Product (PDP) of the NOR_3-based comparator has been simulated under supply voltage and temperature variations, and results are reported in Figure 14a,b, respectively.



(**a**) (**b**)

Figure 14. Power–Delay Product (PDP) of the NOR_3-based comparator with respect to supply voltage variations (**a**) and temperature variations (**b**).

5.2.3. Offset

The input offset voltage of the NOR_3-based comparator has been evaluated considering an input common mode voltage equal to $\frac{1}{4} \cdot V_{DD}$. In order to consider the effect of the mismatch, 1000 Monte Carlo simulations have been carried out, and the results are reported for the 130 nm technology in Figure 15a and for the 28 nm technology in Figure 15b, showing that the input offset voltage can be described with a Gaussian distribution with mean value and standard deviation equal to $\mu \approx -1.24$ mV, $\sigma \approx 27.2$ mV for the 130 nm technology, and $\mu \approx -1.3$ mV, $\sigma \approx 22.1$ mV for the 28 nm technology.

5.3. Rail-to-Rail ICMR Standard-Cell Comparator

This section reports the analysis and performance characterization of the comparator topology depicted in Figure 4, proposed in [52,55] (rail-to-rail ICMR standard-cell comparator).

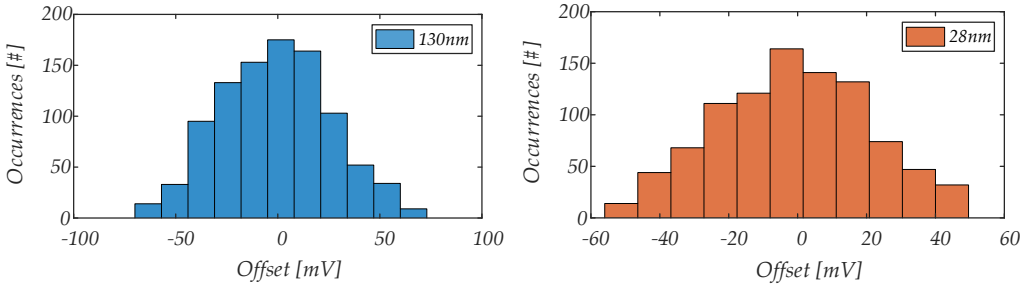


Figure 15. Input offset voltage of the NOR_3-based comparator evaluated by using 1000 mismatch Monte Carlo simulations for the 130 nm technology (**a**) and for the 28 nm technology (**b**).

5.3.1. Propagation Delay

The propagation delay as a function of the input common mode voltage of the rail-to-rail ICMR standard-cell comparator is reported in Figure 16a. As can be observed, the maximum value of the propagation delay is obtained for an input common mode voltage of $V_{DD}/2$, where both the $NAND_3$ and NOR_3 cells are powered on. Indeed, for an input common mode voltage equal to $V_{DD}/2$, both the $NMOS$ and $PMOS$ parts of both the $NAND_3$ and NOR_3 cells (see the transistor level schematics in Figure 3a,b) are active and, thus, it is more difficult to unbalance the input differential cells.

The delay of the rail-to-rail comparator as a function of the input differential signal amplitude is reported in Figure 16b for an input common mode of $V_{DD}/4$, in Figure 16c for an input common mode of $V_{DD}/2$, and in Figure 16d for an input common mode of $3/4 \cdot V_{DD}$. As can be observed, the worst case delay occurs when the minimum differential input voltage is considered.

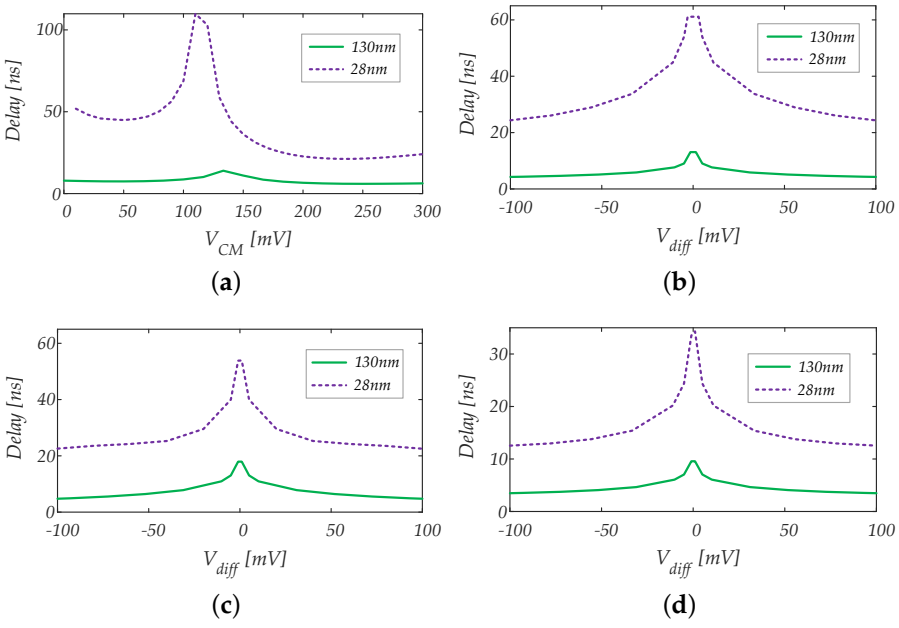


Figure 16. Propagation delay of the rail-to-rail comparator as a function of the input common mode voltage (**a**), input differential signal amplitude for an input common mode of $V_{DD}/4$ (**b**), input differential signal amplitude for an input common mode of $V_{DD}/2$ (**c**) and input differential signal amplitude for an input common mode of $3/4 \cdot V_{DD}$ (**d**).

The propagation delay of the rail-to-rail ICMR comparator as a function of the supply voltage is reported in Figure 17a for an input common mode of $V_{DD}/4$, in Figure 17b for an input common mode of $V_{DD}/2$, and in Figure 17c for an input common mode of $3/4 \cdot V_{DD}$. The propagation delay of the rail-to-rail comparator as a function of the temperature is

reported in Figure 17d for an input common mode of $V_{DD}/4$, in Figure 17e for an input common mode of $V_{DD}/2$, and in Figure 17f for an input common mode of $3/4 \cdot V_{DD}$.

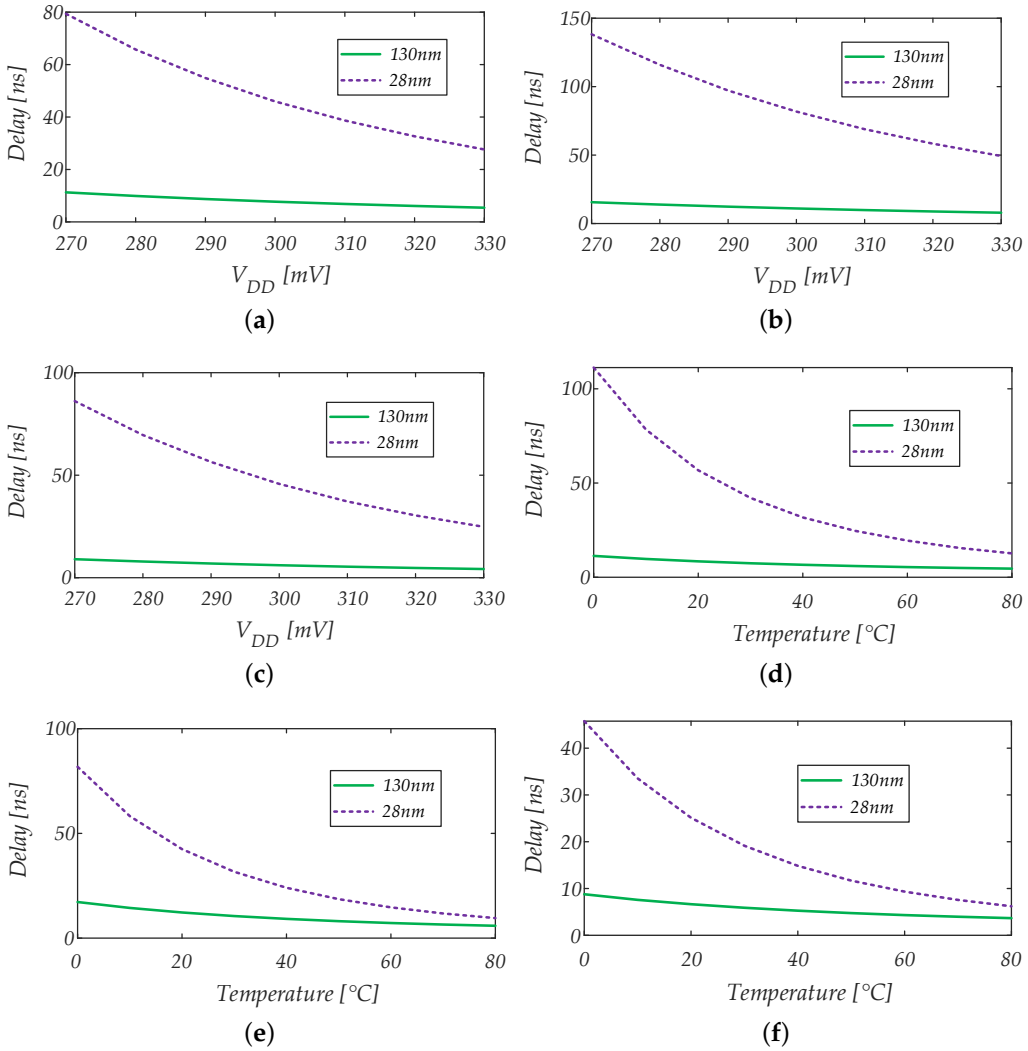


Figure 17. The propagation delay of the rail-to-rail comparator as a function of the supply voltage for an input common mode of $V_{DD}/4$ (**a**), for an input common mode of $V_{DD}/2$ (**b**), for an input common mode of $3/4 \cdot V_{DD}$ (**c**); the propagation delay of the rail-to-rail comparator as a function of the temperature for an input common mode of $V_{DD}/4$ (**d**), for an input common mode of $V_{DD}/2$ (**e**), and for an input common mode of $3/4 \cdot V_{DD}$ (**f**).

5.3.2. Power Consumption and Power–Delay Product

The power consumption versus the input common mode voltage of the rail-to-rail comparator measured at an operating frequency of 10 Hz is reported in Figure 18a, whereas Figure 18b shows the power dissipation of the rail-to-rail comparator as a function of the clock frequency for an input common mode voltage of $V_{DD}/2$. The same considerations for the $NAND_3$ and NOR_3-based comparators in terms of static and dynamic power components apply also in this case. The power dissipation characteristic of the rail-to-rail comparator depicted in Figure 18b shows two "humps", due to the two $NAND_3$ and NOR_3 input cells, which are centered at two different input common mode voltages.

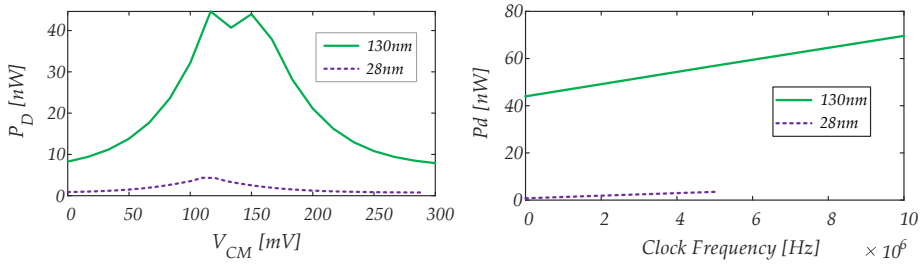


Figure 18. Power dissipation of the rail-to-rail comparator as a function of the input common mode voltage measured @ 10 Hz (**a**), and power dissipation of the rail-to-rail comparator as a function of the clock frequency for an input common mode voltage of $V_{DD}/2$ (**b**).

The Power–Delay Product of the rail-to-rail comparator as a function of the supply voltage is reported for an input common mode of $V_{DD}/4$ in Figure 19a, for an input common mode of $V_{DD}/2$ in Figure 19b, and for an input common mode of $3/4 \cdot V_{DD}$ in Figure 19c, whereas the Power–Delay Product of the rail-to-rail comparator as a function of the temperature for an input common mode of $V_{DD}/4$ is reported in Figure 19d, for an input common mode of $V_{DD}/2$ in Figure 19e, and for an input common mode of $3/4 \cdot V_{DD}$ in Figure 19f. As can be observed, the performance of the comparator is almost constant with respect to supply voltage variations, due to the fact that a higher power consumption corresponds to lower delays and, thus, the product between delay and power consumption is constant. Greater delay variations can be observed for temperature variations.

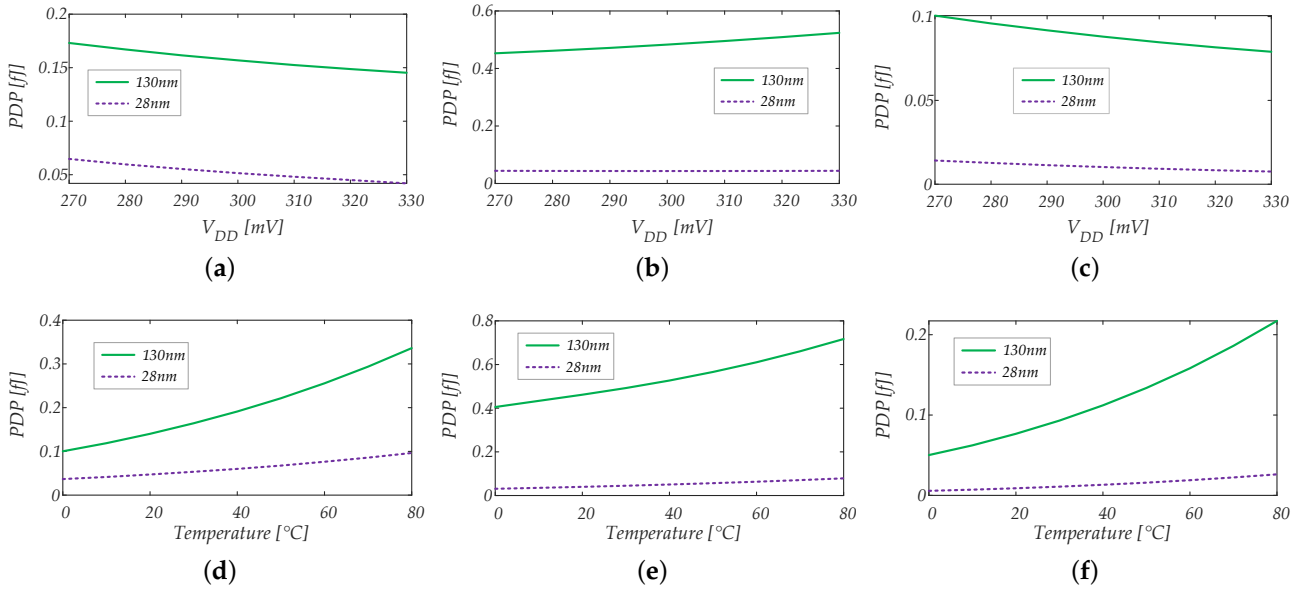
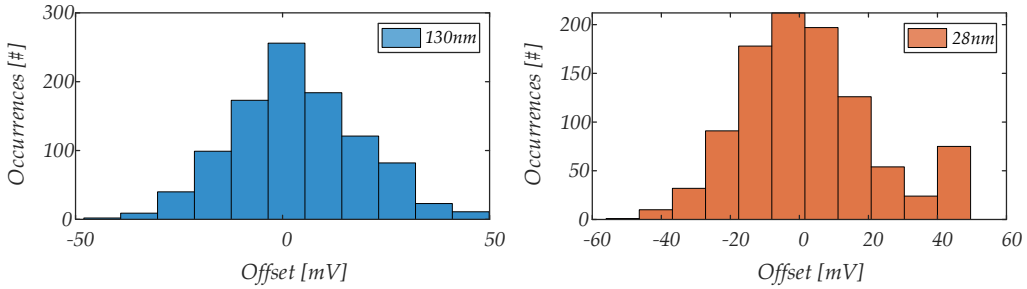


Figure 19. Power–Delay Product of the rail-to-rail comparator as a function of the supply voltage for an input common mode of $V_{DD}/4$ (**a**), for an input common mode of $V_{DD}/2$ (**b**), for an input common mode of $3/4 \cdot V_{DD}$ (**c**); Power–Delay Product of the rail-to-rail comparator as a function of the temperature for an input common mode of $V_{DD}/4$ (**d**), for an input common mode of $V_{DD}/2$ (**e**), and for an input common mode of $3/4 \cdot V_{DD}$ (**f**).

5.3.3. Offset

The input offset voltage of the rail-to-rail comparator has been evaluated considering an input common mode voltage equal to $\frac{1}{2} \cdot V_{DD}$. In order to consider the effect of mismatch, 1000 Monte Carlo simulations have been carried out, and the results are reported for the 130 nm technology in Figure 20a, and for the 28 nm technology in Figure 20b, showing that the input offset voltage can be described with a Gaussian distribution with mean value

and standard deviation equal to $\mu \approx 3.5$ mV $\sigma \approx 15.5$ mV, for the 130 nm technology, and $\mu \approx 2.7$ mV $\sigma \approx 19.9$ mV, for the 28 nm technology.



(**a**) (**b**)

Figure 20. Input offset voltage of the rail-to-rail comparator evaluated by using 1000 mismatch Monte Carlo simulations for the 130 nm technology (**a**) and for the 28 nm technology (**b**).

6. Comparison

In this section, we compare the performances of the standard-cell-based latched comparator topologies described in Section 3 and calculate the figures of merit defined in Section 4.2. This allows us to draw conclusions on relative advantages and disadvantages, also taking into account the possible application scenarios.

6.1. Comparison in ULV Conditions

Comparisons are initially performed for a supply voltage of 0.3 V, since this is the typical context for the application of standard-cell-based analog circuits. Table 1 reports main performance parameters and FoMs both for the case of a high speed standard-cell library in a bulk 130 nm CMOS technology, and for the case of a high density, low leakage, standard-cell library in a 28 nm FDSOI CMOS technology. In the latter case, body bias is not exploited, thus larger delays are achieved due to the higher threshold voltage of the MOS devices. On the other hand, a much lower power consumption is achieved in 28 nm CMOS, due to the reduced speed and to a much lower static current, resulting in an overall better PDP performance.

For what concerns a comparison among the three tested topologies, Table 1 shows that the rail-to-rail topology presents the worst delay and power consumption for an input common mode voltage equal to $V_{DD}/2$, where both the $NAND_3$ and the NOR_3 parts are activated. For an input common mode voltage equal to $V_{DD}/4$ ($\frac{3}{4} \cdot V_{DD}$), the propagation delay is only slightly worse than for the NOR_3 ($NAND_3$) case, and power consumption is higher, especially for the 130 nm technology, where static power consumption is significant. The $NAND_3$ topology performs better than the NOR_3 one, and the difference is very significant in the 28 nm technology. This is due to the fact that the absolute value of the threshold voltage of PMOS devices is higher than the threshold voltage of NMOS devices, and this is particularly evident in the 28 nm technology.

The input referred offset standard deviation is similar for all topologies, and ICMR is limited to half the supply voltage or less for the $NAND_3$ and NOR_3 topologies.

Taking into account the results in Table 1, and the requirements of the different applications, a trade-off results between PDP and ICMR: if a large ICMR is nor required, the $NAND_3$ and NOR_3 topologies are preferable, with the former providing better performance. Obviously, the rail-to-rail topology is required for a large (i.e., larger than $V_{DD}/2$) ICMR. If the application requires an input common mode equal to $V_{DD}/2$, the $NAND_3$ topology can be adopted, since it exhibits better performances than the rail-to-rail one. However, performances vs. the differential input voltage have to be examined, since, depending on technology, $V_{DD}/2$ can be at the edge of acceptable input common mode voltages.

Table 1. Comparison in ULV conditions (i.e., $V_{DD} = 0.3$ V).

Topology	**[7]-NAND**	**[7]-NOR**	**[52,55]**	**[7]-NAND**	**[7]-NOR**	**[52,55]**
Technology node (nm)	130	130	130	28	28	28
Area [μm^2]	36.50	27.74	60.80	3.264	2.62	5.22
Normalized area	2160	1641	3598	4163	3342	6658
V_{DD} [V]	0.3	0.3	0.3	0.3	0.3	0.3
Input Common Mode Range (min-max [mV])	125–300	0–150	0–300	125–300	0–110	0–300
Input offset (μ, σ)[mV]	−1.1, 24.2	−1.4, 23.8	4.4, 15.7	−0.4, 19.4	−2.3, 22.6	2.6, 19.6
Delay @ $V_{CM} = V_{DD}/4$ [ns]	-	6.34	7.71	-	111.0	111.26
Delay @ $V_{CM} = V_{DD}/2$ [ns]	-	-	11.01	-	-	81.80
Delay @ $V_{CM} = 3V_{DD}/4$ [ns]	5.27	-	6.1	38.12	-	45.76
P_D @ $V_{CM} = V_{DD}/4$ [nW]	-	7.55	20.37	-	0.122	0.333
P_D @ $V_{CM} = V_{DD}/2$ [nW]	-	-	43.98	-	-	0.378
P_D @ $V_{CM} = 3V_{DD}/4$ [nW]	6.77	-	14.45	0.063	-	0.124
PDP @ $V_{CM} = V_{DD}/4$ [fJ]	-	0.048	0.156	-	0.0134	0.0367
PDP @ $V_{CM} = V_{DD}/2$ [fJ]	-	-	0.483	-	-	0.0309
PDP @ $V_{CM} = 3V_{DD}/4$ [fJ]	0.035	-	0.087	0.0024	-	0.0056
FOM_{off} @ best V_{CM} [aJ]	2. 82	3.808	4.553	0.155	1.009	0.365
FOM_{cm} @ best V_{CM} [aJ]	20.41	24	87	1.4	4.913	5.6
FOM_{Uni} @ best V_{CM} [aJ]	4.84	7.616	4.553	0.266	2.753	0.365
$FOM_{Uni_{norm}}$ @ best V_{CM} [fJ]	10.45	12.50	16.38	1.107	9.200	2.436

6.2. Comparison at Higher Supply Voltages

A summary of the simulation results for the three considered standard-cell-based comparator topologies for different values of the supply voltage is reported in Table 3. Results in Table 3 confirm the trend observed at 0.3 V: the $NAND_3$ topology is the fastest one, when operated for an input common mode voltage of $\frac{3}{4} \cdot V_{DD}$, but its ICMR is limited to about half the supply voltage. The NOR_3 topology is slightly slower, and exhibits an ICMR which is about half the supply voltage for all the considered values of V_{DD}. The rail-to-rail topology provides a rail-to-rail ICMR, but with higher delay and power consumption at all the considered input common mode voltages, exhibiting the worst case performances at $V_{CM} = V_{DD}/2$.

Results in Table 3 also show that the performances of all the standard-cell-based comparators considered in this work scale with the supply voltage, thus allowing optimization of the trade off between speed and power consumption in different operating conditions through V_{DD} adjusting.

Table 2. Comparison at higher supply voltages.

Topology	**[7]-NAND**	**[7]-NOR**	**[52,55]**	**[7]-NAND**	**[7]-NOR**	**[52,55]**	**[7]-NAND**	**[7]-NOR**	**[52,55]**
V_{DD}		0.6			0.9			1.2	
technology	130	130	130	130	130	130	130	130	130
area [μm^2]	36.50	27.74	60.80	36.50	27.74	60.80	36.50	27.74	60.80
Area normalized	2160	1641 3	598	2160	1641	3598	2160	1641	3598
Input Common Mode Range (min-max [V])	0.26–0.6	0–0.3	0–0.6	0.38–0.9	0–0.430	0–0.6	0.485–1.2	0–0.57	0–1.2

Table 3. Comparison at higher supply voltages.

Topology	[7]-NAND	[7]-NOR	[52,55]	[7]-NAND	[7]-NOR	[52,55]	[7]-NAND	[7]-NOR	[52,55]
input offset (σ)[mV]	9.33	13.15	8.9	19.4	10	15.9	9.8	22.6	19.6
Delay @ $V_{CM} = V_{DD}/4$ [ns]	-	623	731	-	325	350	-	266	276
Delay @ $V_{CM} = V_{DD}/2$ [ns]	-	-	841	-	-	297	-	-	207
Delay @ $V_{CM} = 3V_{DD}/4$ [ns]	468	-	554	205	-	249	148	-	181
P_D @ $V_{CM} = V_{DD}/4$ [nW]	-	76.6	275	-	624	2495	-	3248	14,070
P_D @ $V_{CM} = V_{DD}/2$ [nW]	-	-	1743	-	-	15,830	-	-	55,150
P_D @ $V_{CM} = 3V_{DD}/4$ [nW]	52.8	-	172	417	-	1508	2438	-	8973
PDP @ $V_{CM} = V_{DD}/4$ [aJ]	-	47.6	200	-	200	871	-	861	3675
PDP @ $V_{CM} = V_{DD}/2$ [aJ]	-	-	1461	-	-	4676	-	-	11,350
PDP @ $V_{CM} = 3V_{DD}/4$ [aJ]	24.69	-	94.7	85.4	-	375	360	-	1618
FOM_{off} @ best V_{CM} [aJ]	0.77	2.09	2.81	5.52	6.67	19.88	11.76	64.86	105.71
FOM_{cm} @ best V_{CM} [aJ]	27.98	47.60	189.40	148.03	300.00	1125.00	858.00	1722.00	6472
FOM_{Uni} @ best V_{CM} [aJ]	0.68	2.09	1.40	3.19	4.44	6.63	4.93	32.43	26.43
$FOM_{Uni_{norm}}$ @ best V_{CM} [fJ]	1.46	3.42	5.05	6.88	7.30	23.83	10.66	53.23	95.08

7. Conclusions

In this paper, we have simulated and compared three different standard-cell-based comparator topologies in ULV conditions. In order to better compare comparator performances in different application scenarios, we have introduced a set of FoMs. The simulation testbenches and conditions have been explained in detail, and used to simulate the considered topologies referring to two different technologies: a conventional 130 nm bulk CMOS process and a 28 nm FDSOI CMOS technology. Simulation results have shown that the performances of the different comparators are strongly dependent on the input common voltage. The ICMR of the $NAND_3$-based comparator has been found to be about from $V_{DD}/2$ to V_{DD}, whereas the ICMR of the Nor_3-based comparator has been found to be about from 0 to $V_{DD}/2$; thus, neither of these comparator topologies exhibit a rail-to-rail ICMR. We have also found that the propagation delay of these comparators has its minimum value for an input common mode voltage close to the midpoint of the input ICMR (i.e., $3V_{DD}/4$ for the $NAND_3$ and $V_{DD}/4$ for the NOR_3-based comparator, respectively). The rail-to-rail standard-cell-based comparator considered in this work exhibits two minima for the propagation delay as a function of the input common mode voltage, which are at about $V_{DD}/4$ and $3V_{DD}/4$, whereas for an input common mode voltage equal to $V_{DD}/2$, this comparator exhibits its worst case performance. We have also analyzed how the performances of the considered comparator topologies scale with the supply voltage, and simulation results have shown that, even if standard-cell-based comparators can be used at higher supply voltages, the best values of the FoMs are achieved at ULV conditions.

Author Contributions: Conceptualization, F.C., R.D.S. and G.S.; data curation, R.D.S.; investigation, F.C., R.D.S., G.P. and G.S.; software, R.D.S. and F.C.; validation, G.P.; supervision, G.S. and G.P.; writing—original draft preparation, R.D.S. and G.S.; writing—review and editing, G.S. and G.P.; All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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