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RESEARCH ARTICLE

On the Feasibility of Cascode and Regulated Cascode Amplifier Stages in ULV Circuits Exploiting MOS Transistors in Deep Subthreshold Operation

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ABSTRACT In the last years several ultra-low voltage (ULV) operational transconductance amplifiers (OTAs) with supply voltages below 0.5V have been proposed in the literature. To achieve high gain, multi-stage amplifiers are frequently exploited, in spite of the complexity of design and compensation approaches, whereas cascode and regulated-cascode OTA topologies have rarely been exploited to implement ULV amplifiers. On the other hand, most ULV amplifiers are designed for IoT and biomedical applications in which reducing power consumption is the most important specification, and MOS devices are operated in the subthreshold region. This paper focuses on exploiting the subthreshold operating region to design ULV single-stage OTAs that utilize an output cascoded branch to increase the equivalent output resistance and, consequently, the overall voltage gain. A detailed analytical study of the conditions for triode and saturation regions for MOS devices operating in deep subthreshold region is presented to demonstrate that, for an appropriate choice of the inversion coefficient (IC), a cascode configuration exhibits higher gain than a single transistor, for the same voltage overhead, even in ULV conditions. More specifically, the results presented in this work demonstrate that 4 MOS devices (2 NMOS and 2 PMOS) can be reliably stacked to build a complementary cascode amplifier, even with a supply voltage as low as 0.4V. We also present a novel topology of regulated-cascode amplifier suitable to be operated with a supply voltage of 0.4V and a voltage gain approaching 100dB. Simulation results referring to a 180nm CMOS technology and including PVT and mismatch variations confirm state-of-the-art performances, as well as the good robustness of the proposed regulated-cascode ULV OTA.

INDEX TERMS OTA, ULV, ULP, gain-boosting, body-driven.

I. INTRODUCTION

Internet-of-Things (IoT) and biomedical devices, such as smart dust sensors and implants, have experienced significant advancements due to nanoscale integration in recent years [1], [2], [3], [4]. These compact electronic systems, however, face a challenge in incorporating traditional batteries due to their miniature size, leading to limited energy capacity and quick depletion of stored power. This issue becomes critical in biomedical implants, where frequent battery replacements or invasive procedures for devices like pacemakers pose significant challenges and risks [5], [6], [7].

The reliance on finite battery power underscores the urgent need for alternative energy sources in these devices [8], [9]. The development of energy harvesting technologies intends to cope with this challenge by utilizing natural or excess environmental energy sources such as light, wind, vibrations, or temperature differences to supply power to these embedded systems [10]. The adoption of energy harvesting systems is driven by advancements that increase

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power output from harvesters while decreasing the energy demands of electronic devices [11], [12].

Unlike traditional batteries that require frequent replacement or recharging, energy harvesting offers a promising solution by potentially providing a perpetual energy source, dependent on the availability of suitable energy in the environment. This innovation represents a significant shift away from the dependence on finite energy storage towards a more sustainable and continuous power supply for biomedical devices [13], [14], [15].

Focusing on the power consumption issues discussed above, similar considerations can be done also for IoT devices [16]. Therefore, since the stringent energy constraints dominate architectural and implementation decisions throughout the design of IoT and implanted biomedical systems, ultra-low power (ULP) circuits require specialized design techniques, and their associated trade-offs and limitations are highly specific to these fields of application [17], [18].

In order to reduce the overall power consumption of integrated circuits for IoT and biomedical applications, the design of the analog building blocks is of fundamental importance [19], [20], [21], [22]. Analog building blocks are usually found in the acquisition chain, which is typically made up of frontend amplifiers [23], active filters [24], [25], [26], [27], [28], and analog-to-digital converters (ADCs) [29], [30], [31], [32], [33]. All these blocks are essentially composed of complex architectures which, however, exploit basic analog circuits such as the operational transconductance amplifier (OTA) [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], or the comparator [44].

Since the final performance of amplifiers and filters is strictly related to the characteristics of the OTA, considerable effort is dedicated during the design phase to optimize the OTA's figures of merit under ultra-low power (ULP) and ultra-low voltage (ULV) constraints [45]. For instance, parameters such as power consumption, gain bandwidth product (GBW), DC-gain, phase margin, total harmonic distortion (THD), noise, and slew rate, are critical characteristics that need optimization [46], [47].

Another important parameter for OTAs used in active filters is the output resistance. In fact, the performance of integrators typically adopted in filters is strongly related to the output resistance of the OTAs, which has a strong impact on the maximum achievable quality factor (Q) [48], [49], [50].

In order to achieve high gain from OTAs, especially under stringent supply voltage and power constraints, multiple stages are often cascaded to accumulate the gain of each individual block that forms the amplifier chain [51], [52], [53], [54], [55], [56], [57]. However, this technique raises concerns as the compensation of multi-stage OTAs is a very complex research field [52], [53]. Frequently, multi-stage OTAs require complex compensation networks and various capacitances, significantly impacting the overall silicon area usage [55].

On the other hand, one possible approach is to increase the output resistance of an OTA to achieve high DC voltage gain [58], [59], [60]. However, this is not a straightforward task, especially under strict supply voltage constraints.

Several techniques have been proposed to increase the output resistance of an OTA through feedback strategies, giving rise to a variety of complex architectures that employ cascoded output stages or gain-boosting techniques [61], [62], [63]. Nevertheless, these architectures typically require a minimum supply voltage in the range of 0.6V [64], [65], [66], which is higher than the minimum supply voltage allowed by state-of-the-art ULP OTAs.

A myriad of ULV and ULP OTAs, capable of operating at supply voltages as low as 0.3V, has been proposed in the recent literature. Some of these architectures adopt an inverter-based approach, requiring only a two-drain-source voltage headroom to function properly in the subthreshold region [67], [68], [69], [70], [71]. To increase the input common mode range, most ULV OTAs in the literature exploit body-driven stages [36], [37], [55], [56], [57], [72], [73], [74]. As the body-source voltage of these OTAs is extremely low, the bulk current is negligible and does not significantly affect the overall power consumption and performance of the OTA. Furthermore, the bandwidth limitation of body-driven stages is not a concern, as these OTAs are employed in applications typically operating at frequencies lower than 10 kHz. However, one drawback of these stages is their limited gain, which is low due to the body transconductance of MOS devices.

State-of-the-art ULV OTAs operating with supply voltages in the range of 0.3V typically exhibit a DC-gain between 40 and 60 dB for a two-stage topology. Furthermore, most of these architectures require Miller compensation techniques or a high load capacitance to achieve good phase margin. Multi-stage OTA topologies suitable for ULV operation are currently the preferred option to achieve high DC gain, but they, as discussed above, entail significant area consumption due to the high-value capacitance used for frequency compensation.

Single-stage OTAs which rely on techniques to increase the output resistance (e. g. cascode or regulated cascode) are not popular in the technical literature dealing with such constrained supply voltages, due to the cumbersome biasing of these stages and the difficulties in providing robustness under process, supply voltage and temperature (PVT) variations.

This paper focuses on exploiting the subthreshold operating region to design ULV single-stage OTAs that utilize an output cascoded branch to increase the equivalent output resistance and, consequently, the overall voltage gain. Results presented in this work demonstrate that 4 MOS devices (2 NMOS and 2 PMOS) can be reliably stacked even with a supply voltage as low as 0.4V. However, this feasibility is only achievable if appropriate sizing and biasing strategies are considered. Once cascode stages become viable with a

given supply voltage, several gain-boosting approaches can be applied to achieve very high gain single-stage OTAs with the same ultra-low supply voltage. Consequently, these OTAs do not require complex frequency compensation techniques.

In the following, Section II analyzes the conditions for triode and saturation operation for MOS devices operating in subthreshold, Section III presents a review of low voltage regulated-cascode amplifier topologies, Section IV deals with the implementation of ULV, single-stage, cascode, and regulated cascode OTAs. Simulation results are reported in Section V, a comparison against the state of the art is presented in Section VI, and finally some conclusions are drawn in Section VII.

II. CONDITIONS FOR TRIODE AND SATURATION OPERATION OF MOS DEVICES OPERATING IN SUBTHRESHOLD

According to [75] and [76], a MOS transistor operates in the deep subthreshold region when its inversion coefficient IC is lower than 0.01. A value of IC of 0.01 corresponds to an overdrive voltage $V_{OV} = (V_{gs} - V_{TH})$ equal to -145mV (V_{gs} and V_{TH} denote the gate-source voltage and the threshold voltage of the MOS device, respectively). In such mode of operation the MOS transistor behaves similarly to a bipolar device, and the $V_{ds,sat}$ voltage at which the transistor enters the triode region is nearly independent on the overdrive voltage.

A. DRAIN CURRENT IN SUBTHRESHOLD AND DEFINITION OF $V_{DS,SAT}$

The drain induced barrier lowering (DIBL) effect [77], [78] has a non negligible impact on short channel MOS devices, and affects the value of the threshold voltage V_{TH} of MOS transistors according to the following equation:

$$V_{TH} = V_{TH,int} - \lambda_D V_{ds} \tag{1}$$

where $V_{TH,int}$ is the threshold voltage for $V_{ds} = 0$, and λ_D is the DIBL factor.

Considering also the above short channel effect, the drain current I_D of a MOS transistor operating in the subthreshold region can be expressed as follows:

$$I_D = I_0 S \exp\left[\frac{V_{gs} - V_{TH}}{n \cdot U_T}\right] \cdot \left(1 - \exp\left[\frac{-V_{ds}}{U_T}\right]\right) \cdot \exp\left[\frac{\lambda_D V_{ds}}{n \cdot U_T}\right] \tag{2}$$

where I_0 is the technology current, S is the transistor size aspect ratio, n is the subthreshold slope, U_T is the thermal voltage, V_{ds} is the drain-source voltage and λ_D is the DIBL effect factor defined above, and whose value results higher for MOS devices with shorter channel length.

In the traditional literature dealing with subthreshold MOS transistors, the DIBL effect is often neglected and the value of the voltage $V_{ds,sat}$ at which the MOS transistor enters the triode region is approximated as follows [79]:

$$V_{ds,sat} \approx 3 \cdot U_T \tag{3}$$

This means that if DIBL is not considered $V_{ds,sat}$ depends only on the factor $\left(1 - \exp\left[\frac{-V_{ds}}{U_T}\right]\right)$, which results to be $(1 - \exp[-3] \approx 0.95)$ for V_{ds}=$V_{ds,sat}$. According to this definition, the MOS transistor operating in subthreshold enters the triode region when its drain current exhibits a 5% reduction with respect to the value achieved for an high value of the drain-source voltage V_{ds}:

$$I_D(V_{ds,sat}) \approx 0.95 \cdot I_0 S \exp\left[\frac{V_{gs} - V_{TH}}{n \cdot U_T}\right] \tag{4}$$

Since the practical value of the saturation voltage $V_{ds,sat}$ depends on both the temperature value and on the DIBL effect factor, we have evaluated it for a maximum temperature of 100°C, and for λ_D equal to 0.01 (which is a typical value for CMOS technology nodes below 100nm), obtaining a value of 95mV. According to the above considerations, $V_{ds,sat} = 100mV$ is sufficient to guarantee a reliable operation, even considering temperature variations and the DIBL effect, and therefore a complementary cascode amplifier (made up of two NMOS and two PMOS devices) can reliably be operated with a minimum supply voltage of only 0.4V, if the MOS devices are properly biased in the subthreshold region.

B. INTRINSIC GAIN OF MOS DEVICES OPERATING IN SUBTHRESHOLD

From a circuit design perspective, the triode region is avoided because the output resistance (and therefore the intrinsic voltage gain) is lower than in the saturation region. Therefore it is important to quantify also the reduction of the output resistance and of the intrinsic gain of the device at $V_{ds} = V_{ds,sat}$.

At this purpose, the output conductance g_{ds} of the MOS device in subthreshold can be easily computed starting from eq. 2 as follows:

$$g_{ds} = \frac{\partial I_D}{\partial V_{ds}} = \frac{I_x}{U_T} \cdot \left[\alpha \cdot exp(\alpha\xi) - (\alpha - 1) \cdot exp\left[(\alpha - 1)\xi\right]\right] \tag{5}$$

where

$$I_x = I_0 S \exp\left[\frac{V_{gs} - V_{TH}}{n \cdot U_T}\right] \tag{6}$$

$$\alpha = \frac{\lambda_D}{n} \tag{7}$$

$$\xi = \frac{V_{ds}}{U_T} \tag{8}$$

and therefore the intrinsic gain of the MOS transistor in subthreshold can be expressed as:

$$A_0 = \frac{g_m}{g_{ds}} = \frac{1 - exp(-\xi)}{n \cdot \left[\alpha + (1 - \alpha) \cdot exp(-\xi)\right]} \tag{9}$$

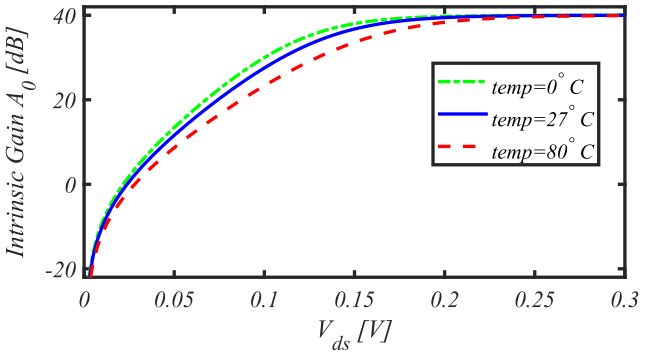

FIGURE 1. Intrinsic Gain A_0 in *dB* of a MOS transistor in subthreshold vs. V_{ds} for $V_{gs} = 0.15V$ and for three different temperatures: 0°C (green), 27°C (blue), 80°C (red).

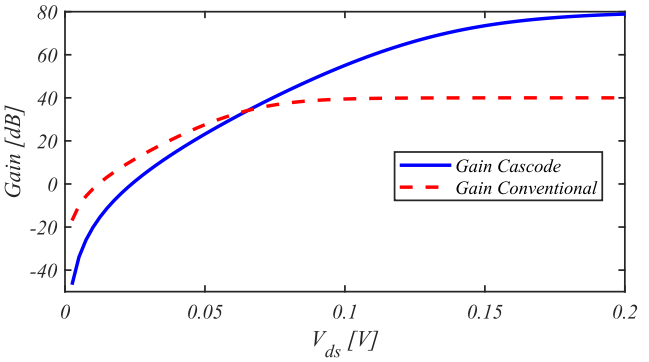

FIGURE 2. Plot of the two terms of inequality (12) in dB.

It is interesting to note that the intrinsic gain A_0 reported in the above equation tends to $\frac{1}{\lambda_D}$ for high values of V_{ds}.

The value of A_0 expressed in *dB* vs. V_{ds} for $V_{gs} = 0.15V$, and assuming λ_D equal to 0.01 is reported in Fig. 1 for three different temperatures: 0°C (green), 27°C (blue), 80°C (red). Considering $V_{ds} = 0.1V$, the intrinsic gain A_0 decreases by about 6dB when the temperature changes from 0°C to 80°C.

C. INTRINSIC GAIN OF CASCODE VS. SINGLE DEVICE FOR THE SAME VOLTAGE HEADROOM

In this section we compute the intrinsic gain of a conventional amplifier made up of a single MOS device in subthreshold, $A_{0,conv}(V_{ds,conv})$, and of a cascode configuration with both MOS devices in subthreshold, $A_{0,cascode}(V_{ds,cascode})$. Since the intrinsic gain of both these amplifiers depend on the V_{ds} voltage across each device, we compare the situation in which a given available voltage headroom $2V_{ds}$ is applied to a single device or to a cascode amplifier in which each device is biased with half the voltage headroom V_{ds}. Then we find the minimum V_{ds} for which the intrinsic gain of the cascode configuration ($A_{0,cascode}(V_{ds})$) is higher than the intrinsic gain of the conventional amplifier ($A_{0,conv}(2V_{ds})$). At this purpose we write the following inequality:

$$A_{0,cascode}(V_{ds}) > A_{0,conv}(2V_{ds}) \tag{10}$$

which, considering the usual approximations for computing the small signal gain of the cascode configuration, can be rewritten as:

$$\Big[A_0(V_{ds})\Big]^2 > A_0(2V_{ds}) \tag{11}$$

from which we obtain:

$$\frac{[1-exp(-\xi)]^2}{n^2\Big[\alpha+(1-\alpha)exp(-\xi)\Big]^2} > \frac{1-exp(-2\xi)}{n\Big[\alpha+(1-\alpha)exp(-2\xi)\Big]} \tag{12}$$

The first term (gain of the cascode configuration) and the second term (gain of the conventional single-stage amplifier) of inequality (12) expressed in dB, are reported in Fig. 2 as a function of V_{ds}, assuming $V_{gs} = 0.15V$, $\lambda_D = 0.01$, and a temperature of 27°C. The plot in Fig. 2 shows that for a drain source voltage V_{ds} of the single device greater than about 62mV the cascode configuration exhibits higher gain than the conventional single-stage amplifier. Fig. 2 also shows that for $V_{ds} = 100mV$ the cascode configuration guarantees a gain enhancement of 16dB with respect to the conventional amplifier, whereas for $V_{ds} = 150mV$ the gain enhancement is as high as 34dB.

All the above considerations confirm that when MOS devices are biased in the deep subthreshold region, the cascode configuration is advantageous even in ULV conditions; in fact, a cascode amplifier made up of 4 MOS stacked devices (2 NMOS and 2 PMOS) with a supply voltage as low as 0.4V can achieve 16dB higher gain with respect to the conventional single-stage amplifier with the same supply voltage.

III. REVIEW OF LOW VOLTAGE REGULATED-CASCODE AMPLIFIER TOPOLOGIES

The most important topologies available in the literature to implement regulated cascode (also known as gain boosted cascode) amplifiers are depicted in Fig. 3. The conventional method (Fig. 3a) makes use of a common source amplifier (or, in a differential setup, a source-coupled pair) to close the gain-boosting feedback loop. This technique offers a sufficient gain without having a substantial negative impact on frequency behavior. The fundamental issue which prevents the possibility of using this conventional topology in low-voltage applications is due to the sequence of two gate-source voltages that results in a minimum supply voltage equal to $2V_{gs} + V_{ds,sat}$ (where V_{gs} and $V_{ds,sat}$ are the gate-source voltage and the drain-source saturation voltage of the generic MOS transistor, respectively). To overcome this issue, a number of strategies have been put out in the literature to lower the minimum supply voltage need.

A popular solution exploits body driving [61], [80] in the auxiliary amplifier M_3, as shown in (Fig. 3b), to lower the minimum supply voltage at a value of $V_{gs}+2V_{ds,sat}$. However, this approach necessitates more power, due to additional

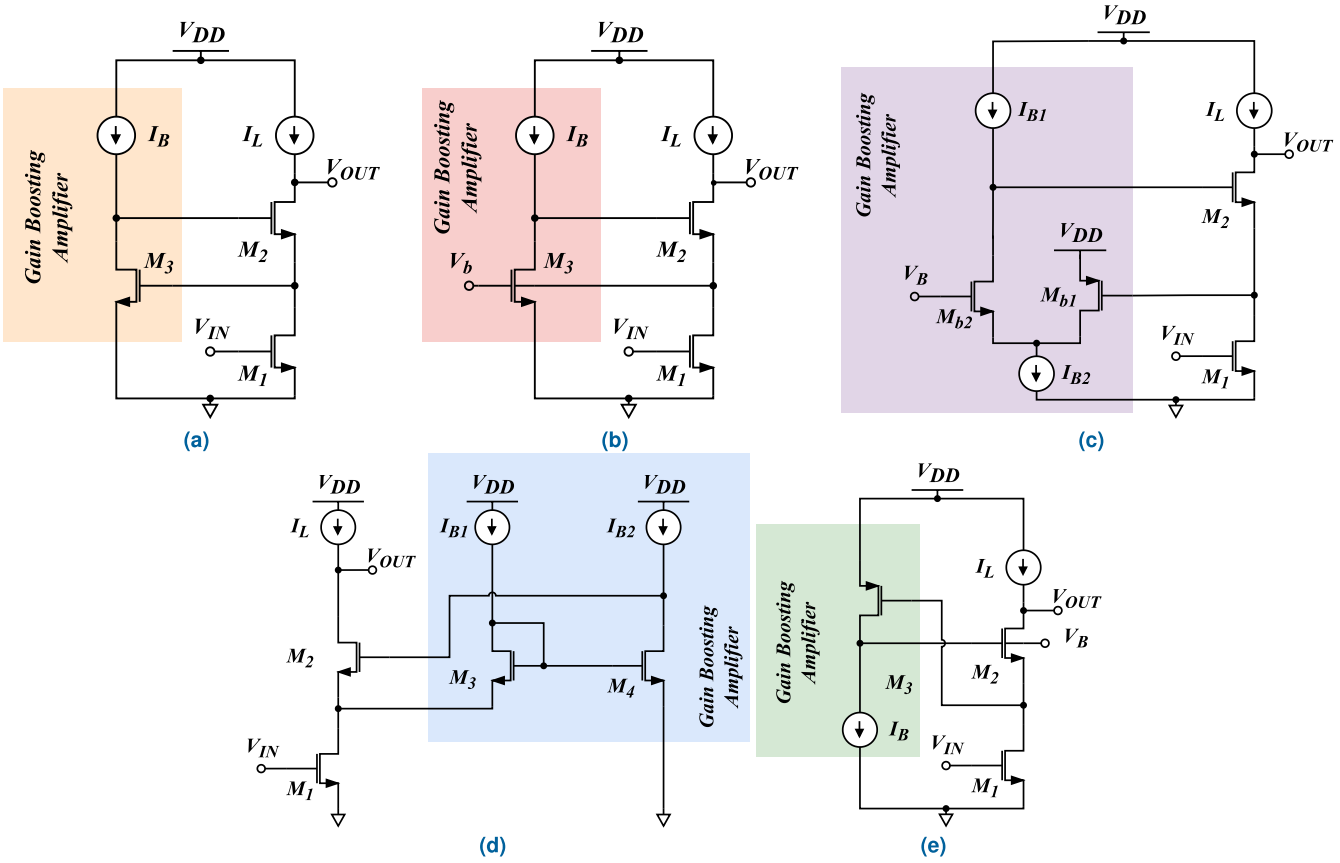

FIGURE 3. Review of low-voltage gain boosting techniques: (a) basic configuration; (b) body-driven cascode; (c) folded cascode; (d) level shifter; (e) complementary gate-driven cascode. Minimum supply is $2V_T + 3V_{ds,sat}$ for (a) and $V_T + 3V_{ds,sat}$ for the other cases.

biasing circuitry, and offers a lower gain for the auxiliary amplifier.

The solution reported in Fig. 3c [81] can ease these issues, thanks to the auxiliary amplifier based on a folded-cascode architecture, which loosens restrictions on its input and output DC levels. The adoption of this topology results in a lowering of the minimum supply voltage, but requires more DC current and introduces an additional high frequency pole. In the circuit shown in Fig. 3d [81], M_3 serves as a level shifter, M_4 serves as an inverting common-source amplifier, with $V_{gs3} < V_{gs4}$ to bias M_1 into the saturation region. The minimum supply voltage can be decreased by shifting the gate of M_4 upward of V_{gs3}, but greater current is once more needed to bias M_3. The analysis of these gain boosting options reveals that the minimal supply voltage can be reduced to $V_{DD,min} = V_{gs} + 2V_{ds,sat}$.

The low-voltage gain boosting topology based on complementary gate-driven devices, which has been recently proposed in [64], is depicted in Fig. 3e. It is based on an auxiliary common-source stage that utilizes a device that is complementary to the main stage, (in this example, a PMOS is utilized as an auxiliary amplifier to boost an NMOS cascode stage). The most important feature of this topology is that it enables to attain the same voltage gain and power consumption as the classic gain boosting strategy of Fig. 3a, but with a much lower supply voltage, which, referring to MOS devices biased in strong inversion, can be determined by inspection to be $|V_{TH3}| + 2V_{ds,sat}$, where V_{TH3} is the threshold voltage of M_3. In fact, by inspection of Fig. 3e, it is evident that, since $V_{sd3} = V_{sg3} - V_{gs2}$, if $V_{sg3} = V_{gs2}$ (i.e. the overdrive and threshold voltages of M_2 and M_3 were the same), V_{sd3} would be equal to zero, resulting in M_3 biased in the triode region. Hence, in order to keep M_3 in saturation, V_{sg3} must be higher than $V_{gs2} + V_{ds,sat}$, and this, referring to MOS devices operating in strong inversion, implies $V_{gs2} < |V_{TH3}|$. Considering low-voltage circuits with MOS biased in strong inversion, the minimum supply voltage of analog circuits is usually computed in terms of a certain number of V_{TH} and V_{ov} voltages [64], [80], and, by following this approach, the minimum supply voltage of the circuits in Fig. 3b, 3c, and 3d can be expressed as $V_{DD,min} = V_{TH} + 3V_{ov}$ [64]. In this paper, with the aim of dealing with ultra-low-voltage circuits, we focus on deep subthreshold operation, in which the inversion coefficient IC is lower than 0.01. A value of IC of 0.01 corresponds to an overdrive voltage $V_{ov} = (V_{gs} - V_{TH})$ equal to -145mV. Therefore in deep subthreshold the overdrive voltage V_{ov} is always a negative quantity whose modulus increases by lowering the IC, and

the minimum supply voltage of a given circuit can be lowered by biasing MOS devices with a lower IC, at the expense of increased area. To better highlight this additional degree of freedom, we introduce here the underdrive voltage V_{ud} defined as follows:

$$V_{ud} = (V_{TH} - V_{gs}) = -V_{ov} \tag{13}$$

which is a positive quantity for MOS devices operating in the deep subthreshold region. Considering the above definitions, the minimum supply voltage of the topologies reported in Fig. 3b, 3c, and 3d, designed with MOS transistors biased in the subthreshold region can be expressed as:

$$V_{DD,min} = V_{TH} - V_{ud} + 2V_{ds,sat} \tag{14}$$

As an example, considering a CMOS technology with $V_{TH} = 0.4$V, and assuming a $V_{ds,sat}$ of about 100mV to account also for the DIBL effect, the underdrive voltage V_{ud} can be designed to be around 0.2V in order to obtain a minimum supply voltage $V_{DD,min}$ in the range of 0.4V which is a remarkably low supply voltage for a gain boosting amplifier, and results equal to the minimum supply voltage of the cascode configuration.

IV. ULV SINGLE-STAGE OTA AND DC POLARIZATION

To validate the theoretical considerations made in the previous sections through simulation results, in this section we compare three different amplifier configurations in ULV conditions (i.e. supply voltage $V_{DD} = 0.4V$). The three amplifier configurations which will be compared in the following are a single-stage conventional ULV OTA, a cascode ULV OTA, and a cascode-gain-boosting OTA whose schematics are reported in Fig. 4a, 4b, and 4c respectively.

All the circuit topologies reported in Fig. 4 exploit the body terminals of both NMOS and PMOS devices as input to maximize the input common mode range of the OTA. As it can be observed, the differential to single ended conversion with common mode cancellation is provided by a gate-driven current mirror.

A. SINGLE-STAGE CONVENTIONAL BODY-DRIVEN ULV OTA

The conventional single-stage ULV OTA is reported in Fig. 4a. The differential to single ended conversion with common mode cancellation is provided by the gate-driven current mirror composed by $Mn_{1,2}$. The gate terminals of transistors $Mp_{1,2}$ are exploited to accurately set the bias current in the two branches (V_{bp1} voltage is set through a biasing current mirror, not shown), thus guaranteeing a stable transconductance gain (set by the body transconductances $gmb_{n,p}$) and therefore a stable gain-bandwidth product (GBW). Transistors dimensions and bias settings are reported in Tab. 1, for a supply voltage $V_{DD} = 0.4V$.

As a design choice, the $|V_{gs}|$, the $|V_{ds}|$ and the $|V_{bs}|$ are set to $V_{DD}/2$.

TABLE 1. DC operating point and sizing of the OTA depicted in Fig. 4a.

Transistor	W	L	$\|V_{gs}\|$	$\|V_{ds}\|$	$\|V_{bs}\|$	$\|V_{th}\|$	I_{DC}
$Mn_{1,2}$	1µm	10µm	200mV	200mV	200mV	390mV	13.2nA
$Mp_{1,2}$	1µm	1.3µm	200mV	200mV	200mV	414m	13.2nA

TABLE 2. DC operating point and sizing of the cascode ULV OTA.

Transistor	W	L	$\|V_{gs}\|$	$\|V_{ds}\|$	$\|V_{bs}\|$	$\|V_{th}\|$	I_{DC}
Mn_1	1.00µm	10.0µm	200mV	100mV	200mV	451mV	10nA
Mp_1	1.00µm	1.30µm	200mV	100mV	200mV	463mV	10nA
Mn_2	1.85µm	1.00µm	200mV	100mV	0V	420mV	10nA
Mp_2	7.80µm	1.00µm	200mV	100mV	0V	485mV	10nA
Mn_3	1.00µm	10.0µm	200mV	100mV	200mV	451mV	10nA
Mp_3	1.00µm	1.30µm	200mV	100mV	200mV	463mV	10nA
Mn_4	1.85µm	1.00µm	200mV	100mV	0V	420mV	10nA
Mp_4	7.80µm	1.00µm	200mV	100mV	0V	485mV	10nA

The differential gain transfer function of this simple circuit can be easily derived as follows:

$$Av \approx \frac{gmb_{n1} + gmb_{p1}}{gds_{n2} + gds_{p2}} \frac{1}{1 + sC_{load}/(gds_{n2} + gds_{p2})} \tag{15}$$

with usual notation for the small signal parameters of MOS devices.

The output conductance of the conventional configuration is given by $gds_{n2} + gds_{p2}$. The phase margin is not a concern for this amplifier configuration. In fact, for a minimum load capacitance C_{load} (which has to be greater than parasitic one seen at the gate of Mn_2), a phase margin close to 90 degree is guaranteed. The GBW of the architecture can be expressed as:

$$GBW = \frac{1}{2\pi} \frac{gmb_{n1} + gmb_{p1}}{C_{load}} \tag{16}$$

whereas the common mode rejection ratio is equal to:

$$CMRR = \frac{gm_{n1}}{gds_{n1} + gds_{p1}} \tag{17}$$

B. SINGLE-STAGE BODY-DRIVEN OTA WITH CASCODE BRANCHES

The cascode ULV body-driven OTA is reported in Fig. 4a. The differential to single ended conversion with common mode cancellation is provided by the high-swing-cascode current mirror composed by $Mn_{1,2,3,4}$. The gate terminals of transistors $Mp_{1,3}$ are exploited to accurately set the bias current in the two branches (V_{bp1} voltage is set through a biasing current mirror, not shown), thus guaranteeing a stable transconductance gain (set by $gmb_{n,p}$) and therefore a stable gain-bandwidth product (GBW). Transistors dimensions and bias settings for the amplifier in Fig. 4b are reported in Tab. 2, for a supply voltage $V_{DD} = 0.4V$.

Also in this case, the $|V_{gs}|$, and the $|V_{bs}|$ are set to $V_{DD}/2$.

The differential gain transfer function of the cascode OTA can be computed as follows:

$$Av_D \approx (gmb_{n1} + gmb_{p1}) \cdot R_{out} \cdot \frac{1}{1 + sC_{load}R_{out}} \tag{18}$$

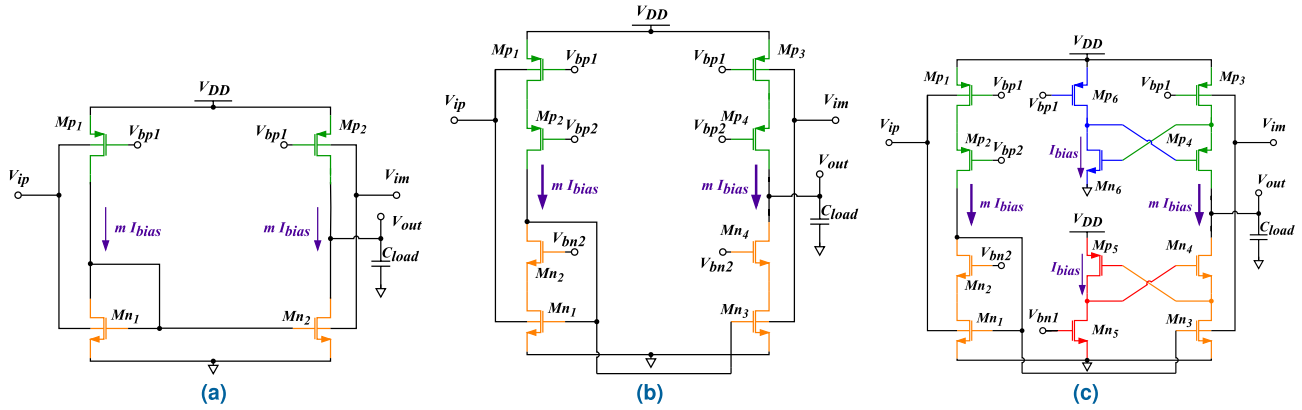

FIGURE 4. Single-stage conventional ULV OTA (a), cascode ULV OTA (b) and cascode-gain-boosting OTA (c).

where R_{out} is the output resistance of the cascode configuration, and can be expressed as:

$$R_{out} \approx \frac{1}{2}\frac{Av_4}{gds_3}\left(1+\frac{1+\alpha}{Av_4}\right) \tag{19}$$

where

$$Av_4 = \frac{gm_4}{gds_4} \tag{20}$$

and

$$\alpha = \frac{gds_3}{gds_4} \tag{21}$$

The common mode rejection ratio of this architecture can be expressed as:

$$CMRR \approx \frac{1}{2}\frac{gm_{n1}\cdot gm_{n2}}{gds_{n1}\cdot gds_{n2}} \tag{22}$$

As it can be observed, with respect to the architecture which doesn't exploit any cascoded branch, also the CMRR is improved, since a cascode current mirror has been introduced.

C. SINGLE-STAGE BODY-DRIVEN OTA WITH GAIN BOOSTING AND CASCODE BRANCHES

The proposed regulated-cascode ULV body-driven OTA is reported in Fig.4c. The differential to single ended conversion with common mode cancellation is provided by the high-swing-cascode current mirror composed by $Mn_{1,2,3,4}$. The gate terminals of transistors $Mp_{1,3}$ are exploited to accurately set the bias current in the two branches (V_{bp1} voltage is set through a biasing current mirror not shown), thus guaranteeing a stable transconductance gain (set by $gmb_{n,p}$) and therefore a stable gain-bandwidth product (GBW). The gain boosting at the output is performed through $Mn(p)_5$ and $Mp(n)_6$, which implement a complementary gate-driven gain boosting configuration. More specifically, by sensing the voltage at the source of $Mn(p)_4$ the output resistance of both the NMOS (PMOS) part of the output branch is boosted by a factor $Av_{gb_{p(n)}}$:

$$Av_{gb_{p(n)}} = \frac{gm_{p5(n6)}}{gds_{n5(p6)}}\frac{1}{1+s\tau_{gb_{p(n)}}} \tag{23}$$

TABLE 3. DC operating point and sizing of the OTA depicted in Fig. 4c.

Transistor	W	L	$\lvert V_{gs}\rvert$	$\lvert V_{ds}\rvert$	$\lvert V_{bs}\rvert$	$\lvert V_{th}\rvert$	I_{DC}
Mn_1	1.00µm	10.0µm	200mV	100mV	200mV	451mV	10nA
Mp_1	1.00µm	1.30µm	200mV	100mV	200mV	463mV	10nA
Mn_2	1.85µm	1.00µm	200mV	100mV	0V	420mV	10nA
Mp_2	7.80µm	1.00µm	200mV	100mV	0V	485mV	10nA
Mn_3	1.00µm	10.0µm	200mV	100mV	200mV	451mV	10nA
Mp_3	1.00µm	1.30µm	200mV	100mV	200mV	463mV	10nA
Mn_4	1.85µm	1.00µm	200mV	100mV	0V	420mV	10nA
Mp_4	7.80µm	1.00µm	200mV	100mV	0V	485mV	10nA
Mn_5	1.75µm	1.00µm	200mV	100mV	200mV	520mV	1nA
Mp_5	1.00µm	3.80µm	200mV	100mV	200mV	463mV	1nA
Mn_6	1.00µm	31.6µm	200mV	100mV	0V	450mV	1nA
Mp_6	7.48µm	1.00µm	200mV	100mV	0V	485mV	1nA

where:

$$\tau_{gb_{p(n)}} \approx \frac{Cgs_{p(n)4}}{gds_{p6(5)}+gds_{n6(5)}} \tag{24}$$

Transistors dimensions and bias settings for the amplifier in Fig.4c are reported in Tab. 3, for a supply voltage $V_{DD} = 0.4V$.

The differential gain transfer function of the cascode-gain-boosting OTA can be derived as follows:

$$Av_D \approx (gmb_{n1}+gmb_{p1})\cdot R_{out}\cdot\frac{1}{1+sC_{load}R_{out}} \tag{25}$$

where R_{out} is the output resistance of the regulated-cascode branch, and can be expressed as:

$$R_{out} \approx \frac{Av_{gb}}{2}\frac{Av_4}{gds_3}\left(1+\frac{1+\alpha}{Av_4}\right) \tag{26}$$

Considering the expression of Av_4 in equation (20) and of Av_{gb} in equation (23), the proposed cascode gain-boosting amplifier is able to achieve a voltage gain Av_D similar to the gain of a three stage OTA, but without the need of complex frequency compensation approaches.

Since the boosted output resistance is seen by both the differential and common-mode signals, the CMRR of this amplifier can be expressed as in equation 22.

V. CIRCUIT SIMULATION AND VALIDATION

The amplifier topologies reported in Fig. 4a, 4b, and 4c have been designed referring to a 180nm CMOS technology

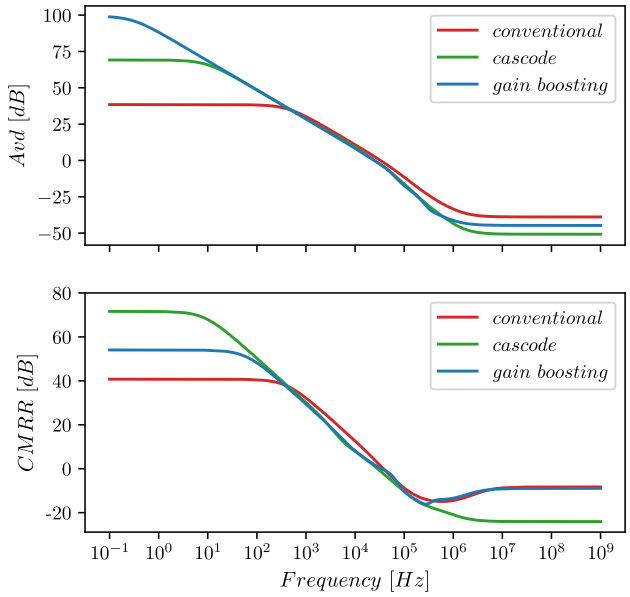

FIGURE 5. Differential gain A_{vd} and CMRR of the conventional single-stage amplifier (red trace), of the cascode amplifier (green trace) and the gain boosted cascode amplifier (blue trace).

and simulation results are provided in this Section. The differential gain A_{vd} and the CMRR of the conventional single-stage amplifier (red trace), of the cascode amplifier (green trace) and the gain boosted cascode amplifier (blue trace) are depicted in Fig. 5. As it can be observed, the conventional single-stage amplifier exhibits a differential gain of about 40dB, the cascode configuration allows to increase the differential gain by about 30dB, attaining a gain of about 70dB, whereas the gain boosted cascode amplifier is able to reach about 100dB of differential gain from a single-stage, body-driven ULV OTA. This can be considered as an outstanding result, especially if considering that this very high gain is attained with a power consumption lower than 9nW. It has also to be pointed out that the proposed ULV gain boosted cascode amplifier does not require any complex compensation technique, and can be easily compensated by a small capacitance at the very high impedance output node. For what concerns the CMRR, the conventional ULV amplifier is able to attain in typical conditions a CMRR of about 40dB, whereas, the cascoded version is able to guarantee a nominal CMRR of about 70dB (which is very high). However, the architecture which exploits the gain boosting at the output branch nominally reaches lower common mode rejection (CMRR is about 55dB) and this is due to the fact that in typical condition the NMOS and PMOS branches in the regulated-cascode are less matched than in the simple cascode OTA (due to the fact that auxiliary amplifiers have been introduced to boost the output conductance).

The performance of the three compared amplifiers has been evaluated also under PVT and mismatch variations. A load capacitance of 1pF has been assumed for the simulations. From the output terminal of the OTA closed in non inverting buffer configuration it has been computed the positive, negative and average slew rate assuming ideal steps with a peak to peak amplitude of 100mV. A summary of the performance of the conventional single-stage amplifier is reported in Tab. 4, confirming the robustness of the proposed OTA to PVT variations. The amplifier is also resilient to mismatch variations, as it can be observed from the values of power consumption Pd, static output voltage $V_{out}@DC$, and gain-bandwidth product GBW, obtained from mismatch Monte Carlo simulations. A summary of the performance under PVT variations is reported in Tab. 5 for the cascode OTA, and in and Tab. 6 for the gain boosted cascode amplifier respectively. As it can be observed from Tab. 6, for the gain boosted cascode amplifier, the differential gain is increased by about 30 dB with respect to the cascode one, and by 60 dB with respect to the conventional single-stage OTA. Even if the DC differential gain is as high as 99dB, it results robust against PVT and mismatch variations. This gain enhancement comes at the cost of a small increment of the dissipated power consumption (about 800pW), which is a reasonable price in terms of power consumption if compared with the increasing of the differential gain.

VI. COMPARISON WITH THE LITERATURE

A figure of merit (FOM), commonly adopted in the technical literature to compare OTAs, is the FOM_S, defined as follows:

$$FOM_S = \frac{GBW \cdot C_L}{Pd} \tag{27}$$

It has to be noted however that the FOM_S doesn't take into account the output resistance of the OTA, which is a critical requirement for some application scenarios, such as integrators, filters and so on, and is not dependent on the achieved differential gain, which is a critical requirement to achieve high accuracy amplifiers to be used in sample and hold and analog to digital converters. Power consumption is one of the most important trade-offs in the design and development of an OTA with high gain and high output resistance. Therefore, since the focus of this work is on amplifiers with high gain and high output resistance, we propose to compare different amplifier topologies also in terms of the following figure of merit:

$$FOM_{GE} = \frac{Av}{Pd} = \frac{Gm_{eq}R_{out}}{Pd} \tag{28}$$

where Gm_{eq} denotes the equivalent transconductance gain of the OTA. The above FOM_{GE} quantify the gain efficiency (GE) in the sense that the best trade-off is achieved when with the lowest power consumption the highest gain is attained. The comparison among different ULV amplifier architectures is reported in Tab. 7. As it can be observed, the proposed architecture outperforms all other amplifiers in terms of FOM_{GE}, attaining the best trade-off among Av and Pd. Furthermore, it can be noted that the proposed regulated cascode amplifier is the only single-stage OTA which achieves a gain of about 100dB, with as supply voltage as low as 0.4 V.

TABLE 4. Performance of the conventional single-stage amplifier under PVT and mismatch variations.

	TYP	Process				Voltage		Temperature		Mismatch	
		FF	SS	SF	FS	-10%	10%	0 deg	80 deg	μ	σ
Pd [nW]	10.56	10.54	10.61	10.46	10.67	9.166	12.04	10.68	10.44	10.6	0.9
$V_{out}@DC$ [mV]	200.1	199.8	200.5	200.4	199.9	180.5	219.9	200.5	199.4	200.2	2.08
$Gain$ [dB]	38.43	37.88	39.01	38.24	38.63	37.85	38.88	38.67	37.75	38.42	0.25
GBW [kHz]	35.16	34.33	36.21	35.08	35.27	33.61	36.77	38.26	30.57	35.27	2.85
$m\varphi$ [deg]	79.29	79.32	79.24	79.46	79.12	79.54	79.05	79.48	78.95	79.29	0.13
Avc [dB]	-1.309	-1.101	-1.51	-1.404	-1.222	-1.552	-1.063	-1.42	-1.113	-5.68	1.98
SR_p [V/ms]	2.446	2.308	2.558	2.456	2.441	2.332	2.487	2.591	2.173	2.446	102m
SR_m [V/ms]	8.338	7.9	8.709	8.445	8.188	7.693	8.692	9.506	6.353	8.31	163m
SR_{avg} [V/ms]	5.392	5.104	5.633	5.451	5.315	5.012	5.59	6.049	4.263	5.378	87m

TABLE 5. Performance of the cascode amplifier under PVT and mismatch variations.

	TYP	Process				Voltage		Temperature		Mismatch	
		FF	SS	SF	FS	-10%	10%	0 deg	80 deg	μ	σ
Pd [nW]	8.029	8.02	8.073	8.014	8.064	7.23	8.828	8.146	8.135	8.044	0.70
$V_{out}@DC$ [mV]	200	200	200	200	200	180	220	200	199.7	200	2.06
$Gain$ [dB]	69.14	64.25	62.81	64.16	67.1	60.86	71.48	61.65	44.4	69.09	0.17
GBW [kHz]	26.69	25.94	27.12	26.61	26.45	25.99	27.04	28.64	21.68	26.77	2.184
$m\varphi$ [deg]	89.94	89.96	89.97	89.96	89.95	89.98	89.94	89.97	90.27	89.94	0.082
Avc [dB]	-2.461	6.958	3.16	4.048	4.494	2.437	2.095	2.941	0.155	-4.18	9.09
SR_p [V/ms]	1.459	1.577	1.299	1.515	1.269	1.411	1.495	1.293	0.803	1.466	102m
SR_m [V/ms]	3.137	6.269	1.278	5.383	1.629	1.658	5.24	1.067	6.009	3.07	0.163
SR_{avg} [V/ms]	2.298	3.923	1.289	3.449	1.449	1.534	3.368	1.18	3.406	2.27	87.42m

TABLE 6. Performance of the gain boosted cascode amplifier under PVT and mismatch variations.

	TYP	Process				Voltage		Temperature		Mismatch	
		FF	SS	SF	FS	-10%	10%	0 deg	80 deg	μ	σ
Pd [nW]	8.834	8.75n	8.907	8.768	8.931	7.98n	9.636	8.933	9.084	8.865	744.2
$V_{out}@DC$ [mV]	200	200.1	199.7	198.6	201.7	179.1	220.1	200.8	199.3	200	1.95
$Gain$ [dB]	99.34	90.21	95.76	88.44	87.57	90.07	97.05	96.56	87.76	99.3	0.387
GBW [kHz]	26.79	25.7	27.39	26.98	26.45	25.35	27	29.31	23.11	26.86	2.16
$m\varphi$ [deg]	89.91	89.92	89.85	89.92	89.86	89.91	89.91	89.63	89.92	89.91	2.26m
Avc [dB]	45.27	40.91	34.24	45.08	48.45	36.35	44.03	54.83	44.72	45.1	1.45
SR_p [V/ms]	1.279	1.47	1.104	1.585	0.893	1.299	1.288	0.836	1.823	1.27	0.074
SR_m [V/ms]	2.913	6.726	0.567	7.883	0.811	1.112	5.722	0.222	6.275	2.93	0.14
SR_{avg} [V/ms]	2.096	4.098	0.836	4.734	0.852	1.205	3.505	0.529	4.049	2.1	46m

TABLE 7. Comparison Table

	This Work		[66]	[82]	[83]	[73]	[74]	[36]	[72]	[37]	[55]
	Gain Boosting	Cascode									
$Tech$ [nm]	180	180	180	180	180	180	180	180	180	180	130
V_{DD} [V]	0.4	0.4	0.5	0.3	0.5	0.6	0.4	0.3	0.6	0.5	0.3
Id [nA]	22.08	20.08	5000	2.5	626	666.67	60	42	43.33	692	112.43
Pd [nW]	8.83	8.03	2500	0.75	313	400	24	12.6	26	346	33.73
$Gain$ [dB]	99.34	69.14	60.05	62.6	95	82	60	64.7	106.3	92	86.83
GBW [kHz]	26.79	26.69	131.28	2.17	12.82	19.1	7	2.96	33	49.2	10.32
C_L [pF]	1	1	30	20	15	15	15	30	15	30	35
$m\varphi$ [deg]	89.91	89.94	72.56	61	55	60	60	52	102.4	54.8	58.27
CMRR [dB]	54.07	71.6	66.46	89	60	130.2	85.4	110	127	65	57.8
PSRR [dB]	50.94	78.14	60.48	58	66	-	76.3	68	104	61	46.59
SR_{avg} [V/ms]	2.1	2.3	128	150	16.25	12	79	4.15	28	570	3.74
THD [%]	0.75	1.25	-	1	0.34	0.16	-	1	0.63	0.49	0.2
$Vpkpk$ [mV]	200	200	-	63	500	520	-	255	600	250	220
FOM_S [kHz· pF/nW]	3.03	3.32	1.58	57.87	0.61	0.72	4.38	7.05	19.04	4.27	10.71
FOM_{GE} [1/nW]	10496.37	356.68	0.4	1798.62	179.66	31.47	41.67	136.34	7943.77	115.06	650.85
	Single-Stage			Two Stage					Three Stage		

VII. CONCLUSION

In this paper we have discussed how to exploit MOS transistors biased in the subthreshold region to design ULV single-stage OTAs with cascode and regulated-cascode output branch to achieve a very high voltage gain. A detailed analytical study of the conditions for triode and saturation regions for MOS devices operating in deep subthreshold region has been presented, illustrating the advantages of the

cascode configuration in ULV conditions with MOS operating in deep subthreshold. Based on the theoretical analysis we have proposed a novel topology of regulated-cascode amplifier suitable to be operated with a supply voltage of only 0.4V, while exhibiting a voltage gain approaching 100dB. A comparison against the state of the art of ULV high gain OTAs has confirmed that the proposed architecture outperforms all other amplifiers in terms of FOM_{GE}, attaining the best trade-off among Av and Pd, and is the only single-stage OTA able to achieve a gain of about 100dB.

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