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Body Biasing Techniques for Dynamic Comparators: A Systematic Survey

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Abstract: Forward body biasing (FBB) has often been exploited in the literature for improving the performance of both analog and digital building blocks. Recent works have explored the application of FBB variants to mixed-signal electronics and in particular to dynamic comparators, where these techniques can help to relax the trade-off between speed and power consumption at medium and low supply voltages. However, the literature lacks a structured analysis of the solutions that have been developed and of the trade-offs that affect them. This work attempts to fill the gap by providing a survey of the application of FBB techniques to dynamic comparators. The analysis focuses on the two most popular dynamic comparator topologies, the Strong Arm latch and Elzakker's comparator. Several FBB variants are examined from a theoretical point of view. Moreover, the benefits and the limitations of the different approaches are assessed in terms of the main figures of merit through a systematic campaign of simulations in a 55 nm CMOS technology.

Keywords: comparators; forward body bias; high speed; latch; IoT

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1. Introduction

Comparators are essential building blocks in data conversion applications, which in turn have become pervasive in the contemporary world due to the dominance of digital signal processing in communication systems. The performance of an analog-to-digital converter (ADC) is in most cases heavily influenced by the figures of merit of its comparator(s) [1,2]. Noise, distortions, and power consumption of popular architectures such as successive approximation register (SAR) [1], pipeline [3] and flash [4] can be improved significantly by optimizing the comparator's parameters.

While several classes of comparators exist, dynamic ones are among the most popular in CMOS integrated design due to their several appealing features, which encompass limited delay, remarkable power efficiency, rail-to-rail output swing, and ease of design/layout [5]. Dynamic latched comparators are also attractive because their performance improves as technological scaling advances, unlike open-loop comparators based on cascading high-gain elements. Thanks to their properties, dynamic comparators are employed in a wide variety of scenarios, ranging from low- and ultra-low voltage systems [6–10] to high-speed applications [11–14].

From a high-level perspective, dynamic comparators usually consist of a block that performs dynamic preamplification and a CMOS latch that regenerates the differential signal to full swing. Based on this principle, several topologies can be developed depending on how the two blocks are implemented and interfaced with each other. Over the years, two topologies have become dominant: the Strong Arm latch [5,15] and the Elzakker comparator [16]. The first one, shown in Figure 1, consists of a clocked differential pair loaded by a CMOS latch. When the clock is high, the differential pair preamplifies the signal by discharging its drain nodes until the devices in the latch turn on. At that point, the latch

takes over and brings its outputs to saturation. Due to the limited number of components, the Strong Arm comparator is suited for energy-efficient operation at high clock speeds. However, its performance declines rapidly when the supply voltage decreases below a certain value. In addition, depending on the targeted application, the Strong Arm latch may produce excessive kickback noise due to the absence of isolation between the input pair and the latch. The Elzakker comparator [16] (Figure 2), which is a variant of the double-tail comparator [17], improves on these limitations because the dynamic preamplifier is decoupled from the latch. The operation is similar to the Strong Arm latch; when the clock signal goes high, the preamplifier discharges its output nodes until devices M_7–M_8 turn on. At that point, a differential voltage starts to build up at the output nodes of the latch and the cross-coupled inverters regenerate the signal.

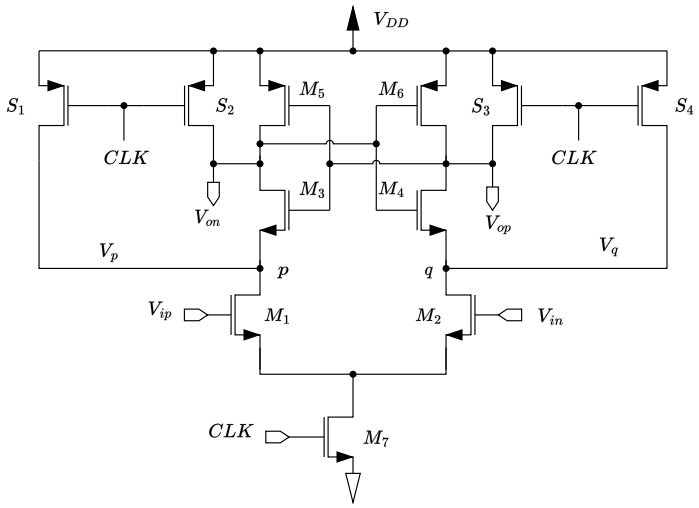

Figure 1. Schematic of the Strong Arm latch [5].

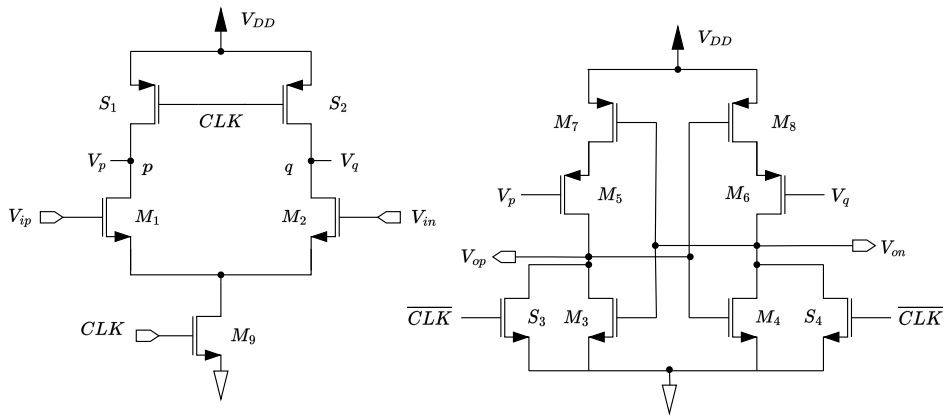

Figure 2. Schematic of Elzakker's comparator [16].

Several modifications have been proposed in the literature in the attempt to relax the trade-off between the delay and power consumption of dynamic comparators, and in particular of the Strong Arm latch and Elzakker comparator. This work focuses on forward body biasing (FBB), a class of techniques that consist in biasing the substrate terminals of MOS devices in such a way that $V_{bs} > 0$ V (when considering N-channel devices) and/or $V_{sb} > 0$ V (when considering P-channel devices) [18]. For the sake of simplicity, when describing a configuration we will refer to NMOS devices unless otherwise specified. FBB techniques are attractive because they allow the performance of a MOS device to be improved with limited overhead in terms of power consumption and can typically be implemented with minimal modifications to the topology. FBB has been exploited in a wide range of applications, including digital cells [19], analog building

blocks such as operational amplifiers, mixers, voltage controlled oscillators (VCO) [20–22], and mixed-signal circuits such as comparators and charge-pump topologies [8,23,24].

This paper explores the application of FBB to dynamic latched comparators by focusing on applications at medium supply voltage, where its implementation can be more challenging, as it often requires generating a limited bias voltage (less than 0.6 V) without compromising the comparator's power efficiency.

Among the simplest variants of FBB is the dynamic threshold MOS (DTMOS) technique, which consists in applying a signal-dependent bias to the substrate of a MOS transistor. In the DTMOS technique [19], which is aimed at digital applications, the gate is connected to the body, meaning that the threshold voltage of the transistor is smaller when the gate voltage V_g is V_{DD} and higher when $V_g = 0$ V. This increases the on-state current of the device while minimizing leakage currents when the transistor is switched off. In logic gates, this reduces the delay without increasing static power consumption. The augmenting device DTMOS configuration [25] improves on DTMOS by adding a device that acts as a voltage follower between the gate and the body of the main device and as a current follower between the body and the drain of the main device. This approach has two advantages: it reuses the substrate current to drive the output, and it limits the bias voltage applied to the substrate thanks to the V_{gs} drop of the augmenting device.

Another simple yet effective approach consists in connecting the body terminals of MOS devices to the supply rails in such a way that the body–source junctions of said devices are forward biased. In this configuration, known in the literature as swapped body biasing (SBB), the substrate terminals of the NMOS (resp. PMOS) devices are connected to V_{DD} (resp. ground) [8,23]. The application of SBB is limited to low-voltage and ultra-low-voltage circuits, as the leakage current can be excessive due to the fact that $|V_{bs}| = V_{DD}$ at all times.

Recently, more elaborate techniques have been introduced in the literature in the attempt to leverage FBB in dynamic comparators that operate at medium–high supply voltages. In [24], a new technique called clocked FBB (CFBB) was proposed for the Strong Arm comparator. CFBB consists in precharging the substrate nodes of the NMOS devices in the regenerative latch (M_3–M_4) and exploiting the capacitive divider effect created by the discharge of the intermediate nodes of the comparator so that $V_{bs3,4} > 0$ V during the evaluation phase. By acting on the sizing of the precharge transistors, it is possible to adjust the settling value of $V_{bs3,4}$ so as to avoid excessive leakage and prevent latch-up.

In [26], it was shown that CFBB can suffer from robustness issues when a large differential voltage is applied to the comparator's inputs. Moreover, CFBB is limited in that it cannot be applied to the PMOS devices of the latch, which limits the advantage associated with FBB. A new technique was proposed called hybrid FBB (HFBB) that improves on both of these aspects by splitting the precharge devices into a pair of separate transistors and adding a stack of diode-connected devices to bias the body terminal of the PMOS transistors.

This work adopts a systematic approach to compare the strengths and drawbacks of the techniques reported in the literature with the aim of creating a comprehensive overview of FBB-based design techniques that a designer may resort to in order to relax the main trade-offs involved in the design of a comparator. In order to provide better insight on each technique, we carried out a simulation campaign in which the main variants of FBB were applied to different comparator topologies, namely, the Strong Arm latch and Elzakker's comparator. In addition to the comparison between the existing topologies, this work provides original contributions by exploring and validating variants of FBB-enhanced comparators for which the literature lacks an exhaustive performance analysis, namely, the DTMOS-enhanced versions of the Strong Arm and Elzakker comparators and the CFBB- and HFBB-enhanced Elzakker comparators. The remainder of this paper is organized as follows: in Section 2, the benefits and the limitations of FBB techniques are discussed from a general standpoint; Section 3 provides an overview of the state of the art concerning dynamic latched comparators; Section 4 describes the results of the simulation campaign; and Section 5 concludes the paper.

2. FBB in Dynamic Comparators

2.1. Delay Analysis and Effect of FBB

The threshold voltage of an MOS device can be expressed as follows:

$$V_{th} = V_{th0} + \gamma(\sqrt{2|\Phi_B| - V_{bs}} - \sqrt{2|\Phi_B|}) \tag{1}$$

where V_{th0} is the threshold voltage at $V_{bs} = 0$, γ is the body effect coefficient, and $2\Phi_B$ is the inversion layer potential. The body coefficient is defined as $\gamma = \sqrt{2qN_a\epsilon_s}/C_{ox}$, where N_a is the doping concentration in the channel, ϵ_s is the Si permittivity, and C_{ox} is the gate oxide capacitance. The zero-bias threshold voltage V_{th0} is provided by

$$V_{th0} = 2|\Phi_B| + V_{FB} + \gamma\sqrt{2|\Phi_B|}. \tag{2}$$

Now, the drain current and the transconductance in weak inversion are provided by

$$\begin{cases} I_d = I_{d_0} e^{\frac{V_{gs} - V_{th}(V_{bs})}{nU_T}} (1 - e^{-\frac{V_{ds}}{U_T}}) \\ g_m = \frac{I_d}{nU_T} \end{cases} \tag{3}$$

where I_{d_0} and n depend on the technology while $U_T = kT/q$ is the thermal voltage. When the transistor is biased in strong inversion and operates in the saturation region, instead, one has

$$\begin{cases} I_d = \beta(V_{gs} - V_{th}(V_{bs}))^2 \\ g_m = 2\beta(V_{gs} - V_{th}(V_{bs})) \end{cases} \tag{4}$$

Finally, in the triode region, the drain current and the transconductance are provided by

$$\begin{cases} I_d = \beta\left[2(V_{gs} - V_{th}(V_{bs}))V_{ds} - V_{ds}^2\right] \\ g_m = 2\beta V_{ds} \end{cases} \tag{5}$$

By increasing V_{bs}, the threshold voltage V_{th} is reduced and the device's drain current for a given V_{gs} increases. This is true both in the weak and strong inversion regions. Moreover, g_m increases both in weak inversion and in saturation.

In order to study how these effects can benefit a dynamic comparator, we can consider the expressions of the delay t_d. For both the Strong Arm latch and Elzakker's comparator, the delay can be expressed in the form

$$t_d = t_d^{pre} + t_d^{latch}, \tag{6}$$

where t_d^{pre} represents the preamplification time, conventionally defined as the time (measured from 50% of the clock rising edge) required for the four latch devices to turn on, and t_d^{latch} is the regeneration time, i.e., the time required for the latch to regenerate the output differential signal to a magnitude equal to $V_{DD}/2$. For the Strong Arm comparator, it can be shown that the delay is provided by

$$t_{d_{SA}} = \frac{2C_{pq}V_{th_{3,4}}}{I_{tail}} + \frac{2(C_{pq} + C_{out})|V_{th_{5,6}}|}{I_{tail}} + \frac{C_{out}}{g_{m_{eff}}} \ln\left(\frac{V_{DD}}{2V_{id}} \frac{I_{tail}}{g_{m_{1,2}}|V_{th_{5,6}}|}\right), \tag{7}$$

where V_{id} is the input differential voltage of the comparator, C_{pq} denotes the parasitic capacitance at each of nodes p and q, C_{out} is the parasitic and explicit load capacitance at each of the output nodes, and $I_{tail} = I_{d7}$ is the tail current, which is assumed to be constant. This is an approximation, as in reality M_7 quickly enters the triode region. The quantity $g_{m_{eff}}$ is defined as the sum of the transconductance of the PMOS and of the NMOS transistors.

For the Elzakker comparator, the expression of the delay is

$$t_{d_{DT}} = \frac{2C_{pq}|V_{th_{5,6}}|}{I_{tail_1}} + \frac{2C_{out}V_{th_{3,4}}}{I_{tail_2}} + \frac{2C_{out}}{g_{m_{eff}}} \ln\left(\frac{V_{DD}}{2V_{id}} \frac{C_{pq}C_{out}}{g_{m_{1,2}}g_{m_{5,6}}t_{d,DT}^{pre}t_d^{pre_2}}\right), \tag{8}$$

where $t_{d,DT}^{pre} \triangleq \frac{2C_{pq}|V_{th_{5,6}}|}{I_{tail_1}} + \frac{2C_{out}V_{th_{3,4}}}{I_{tail_2}}$ and $t_d^{pre_2} \triangleq \frac{2C_{out}V_{th_{3,4}}}{I_{tail_2}}$, while I_{tail_1} and I_{tail_2} are respectively defined as the tail current of the preamplifier and the common mode current flowing in the second stage (i.e., the quantity $(I_{d_7} + I_{d_8})/2$). The reader is referred to the Appendix A for the derivation of the analytical expressions of t_d^{pre} and t_d^{latch} in the Strong Arm and Elzakker topologies.

By inspecting Equations (7) and (8), it is possible to see that FBB can reduce the comparator's delay in two ways:

- The preamplification time improves thanks to the reduction in the devices' threshold voltages.
- The regeneration time improves because of the increase in the devices' transconductance. It should be noted that the regeneration time constant decreases while the logarithm increases due to its argument being inversely proportional to $t_{d,DT}^{pre}$ and t_d^{pre2}. However, the net effect will typically be a reduction of the regeneration time because the logarithm varies weakly as its argument varies.

A properly designed FBB scheme can improve delay while causing a negligible increase in power consumption. Obviously, there are technological limitations which may pose issues related to reliability and resource usage. These aspects are addressed in detail in Section 2.3, while the next section analyzes the effect of FBB on offset and noise.

2.2. Noise and Offset and Effect of FBB

Noise and offset represent key parameters in dynamic comparators. This subsection briefly analyzes the influence that FBB has on these figures of merit by exploiting the results presented in [27]. Commencing with the input-referred offset the impact of mismatches in the latch devices may be deemed negligible when the preamplification gain is large enough. Consequently, the input-referred offset can be approximated as the outcome of the asymmetries influencing the input pair and its associated load capacitors [27]:

$$V_{offset} \approx -\Delta V_{th_{1,2}} + \frac{\Delta\beta}{\beta}\frac{V_{ov_{1,2}}}{2} - \frac{\Delta C_{pq}}{C_{pq}}\frac{V_{ov_{1,2}}}{2}. \tag{9}$$

In the above equation, $\Delta V_{th_{1,2}}$, $\Delta\beta$, and ΔC_{pq} respectively represent the mismatch on the input pair's threshold voltages and the β and load capacitances, while $V_{ov_{1,2}}$ represents the overdrive voltage of M_1–M_2. Because the initial part of the preamplification phase unfolds in the same way in the Strong Arm latch and in the Elzakker comparator, Equation (9) can be used for both topologies. The expression of V_{offset} suggests that FBB has a minor influence on the input-referred offset of both topologies, as none of the parameters that appear in Equation (9) is affected significantly by the latch devices being forward biased. This, of course, only remains true as long as the preamplification provided by the input pair is strong enough to mask offset contributions from the latch devices. It should be noted that the additional transistors that form the FBB circuit can contribute with their own mismatch. As a result, the input-referred offset may increase slightly depending on the FBB topology.

The analysis of noise leads to different expressions for the Strong Arm latch and the Elzakker comparator. According to [27], the mean square input-referred noise of the Strong Arm latch can be expressed as

$$< V_{noise}^2 >= 4kTY\frac{V_{ov_{1,2}}}{V_{th}} \times \begin{cases} \frac{1}{2}\frac{1}{C_{out}+2C_{pq}} & C_{pq} < C_{out}/2 \\ \frac{1}{C_{out}+3C_{pq}} & C_{pq} \approx C_{out} \\ \frac{1}{C_{pq}+V_{ov_{3,4}}/V_{th}} & C_{pq} > 2C_{out} \end{cases} \quad (10)$$

where Y is the noise factor of the FET and $V_{th} = V_{th_{3,4}} \approx V_{th_{5,6}}$. The authors of [27] do not provide an expression for the input-referred noise of the Elzakker comparator; nonetheless, ref. [27] contains useful considerations that can be exploited to derive an expression of the input-referred noise for this topology. First, we observe that in the Elzakker comparator white noise is filtered by a windowed integrator for $t_d^{pre_1} \triangleq 2C_{pq}|V_{th_{5,6}}|/I_{tail_1}$ seconds. Then, a second integrator starts filtering the output of the first integrator for $t_d^{pre_2} = 2C_{out}V_{th_{3,4}}/I_{tail_2}$ seconds, while the first one continues to integrate. According to the analysis developed in [27], this is equivalent to an input-referred noise current that is band-limited to $1/(t_d^{pre_1} + \frac{1}{2}t_d^{pre_2})$. As a consequence, the input-referred noise voltage can be written as

$$< V_{noise}^2 >= \frac{4kTY}{g_{m_{1,2}}} \frac{1}{\frac{2C_{pq}|V_{th_{5,6}}|}{I_{tail_1}} + \frac{1}{2}\frac{2C_{out}V_{th_{3,4}}}{I_{tail_2}}}. \quad (11)$$

It is important to acknowledge that this analysis overlooks the fact that the second integrator is a time-varying system due to the linear increase of $g_{m_{5,6}}$ with $V_{gs_{5,6}}$ (refer to Appendix A). Considering this variation, the term representing $t_d^{pre_2}$ is scaled by a factor different from 1/2 yet still less than one. While Equations (10) and (11) are different, they indicate that both topologies exhibit similar responses to FBB in terms of noise. In both scenarios, $< V_{noise}^2 >$ decreases as a function of $V_{th_{3,4}}$ and $V_{th_{5,6}}$, consequently worsening the input-referred noise due to the reduction in threshold voltages caused by FBB. This effect is evidently undesirable. Nevertheless, the threshold voltage variation induced by FBB is often within limits where the degradation of noise can be accepted, contingent on the specific application.

2.3. Limitations of FBB

2.3.1. Parasitic Currents

As already highlighted, Equation (3) shows that the subthreshold drain current is a function of the threshold voltage. While this can help to improve performance at low supply voltages, it means that FBB can cause an increase in leakage in circuits where the MOS devices should behave as switches and exhibit an on/off behavior. Hence, in applications such as CMOS digital circuits and dynamic comparators, FBB can introduce a penalty associated with static power consumption. Such issues can be avoided by biasing the devices' substrate terminals with signal- or clock-dependent voltages to ensure that the body-source voltage becomes greater than 0 only when required.

Another source of additional power consumption in circuits that make use of FBB is related to the current flowing into the body terminal and through the substrate–source junction. With reference to NMOS devices, a positive V_{bs} causes a current flow through the p-n junction that exists between the p-doped substrate and the n-doped source region, according to the Shockley diode equation:

$$I_b = I_s(e^{\frac{V_{bs}}{nU_T}} - 1) \quad (12)$$

where I_s is a process-dependent constant and n is the ideality factor that accounts for non idealities in the junction. Therefore, the body–source voltage should remain limited at all times in order to avoid excessive power consumption. The typical threshold is around 0.6–0.7 V [19].

In light of the above discussion, when considering the problem of sizing an FBB scheme by using parasitic currents as a criterion, the maximum allowable V_{bs} depends mainly on the maximum acceptable penalty on power consumption.

As a final note, it should be remarked that the body current does not represent an issue in fully-depleted silicon-on-insulator (FDSOI) technologies due to the fact that the substrate of an FDSOI MOSFET is perfectly isolated from the region containing the drain and source diffusions.

2.3.2. Latch-Up, Area Footprint, and Power Consumption

Latch-up in integrated circuits has been a concern since the beginning of CMOS technologies [28,29]. There are a number of phenomena and conditions that can trigger latch-up events, FBB being one of them. Indeed, the substrate current associated with a forward-biased body–source junction gives rise to a voltage drop that may activate the positive feedback loop formed by a parasitic PNPN structure. Hence, the body–source voltage of the devices to which FBB is applied should be limited to ensure that the current flowing through the substrate remains negligible. However, it should be noted that the risk of latch-up events is strongly dependent on the characteristics of the technological process and on the layout. We now attempt to discuss the main tradeoffs associated with reducing the risk of latch-up in FBB circuits. To this end, it should first be recognized that latch-up is a concern only in dual-well and merged triple-well structures; pure triple-well configurations and FDSOI technologies are immune from latch-up, as NMOS devices and PMOS devices are isolated from each other [29]. Because dual-well technologies are essentially obsolete and FDSOI technologies do not pose any design challenges from the point of view of latch-up, we choose to focus on the distinction between triple-well and merged triple-well and the implications for FBB-based circuits. Hereinafter, FDSOI technologies are excluded from the discussion unless explicitly mentioned.

In merged triple-well structures (Figure 3a), the n-well used for PMOS devices is merged with the n-well used to isolate NMOS devices. Consequently, while the area footprint is optimized, latch-up can still occur, although the latch-up response tends to be different from that of a dual-well configuration [29]. In pure triple-well structures, the isolating wells used for NMOS devices are distinct from the n-wells in which PMOS devices are placed (Figure 3b). As already mentioned, latch-up cannot occur because the devices are isolated from each other; however, this comes at the expense of greater occupied area due to the increased spacing between devices.

In general, when triple-well structures are used, a variety of layout choices may be possible depending on the particular topology that is being implemented. These choices are usually subject to a trade-off between area footprint and robustness. If the topology allows for the adoption of merged structures and a pure triple-well process is available, for example, the designer may choose to accept the increased area occupation and keep NMOS and PMOS devices in separate wells to eliminate latch-up.

Another important aspect that should be factored in when implementing FBB in dynamic circuits (e.g., comparators, CMOS logic cells) is that the increase in area may cause a significant penalty in terms of delay and power consumption because of the parasitics associated with routing. In some cases the improvement that is introduced through FBB may be limited; thus, designers should be aware of the potential overhead that arises by modifying the layout of the circuit and take it into account when choosing whether to implement FBB. In addition, it is worth noting that the overhead may be null, as not all FBB topologies require additional isolation wells (e.g., when FBB is applied to PMOS devices only or when isolation wells are already required for all devices).

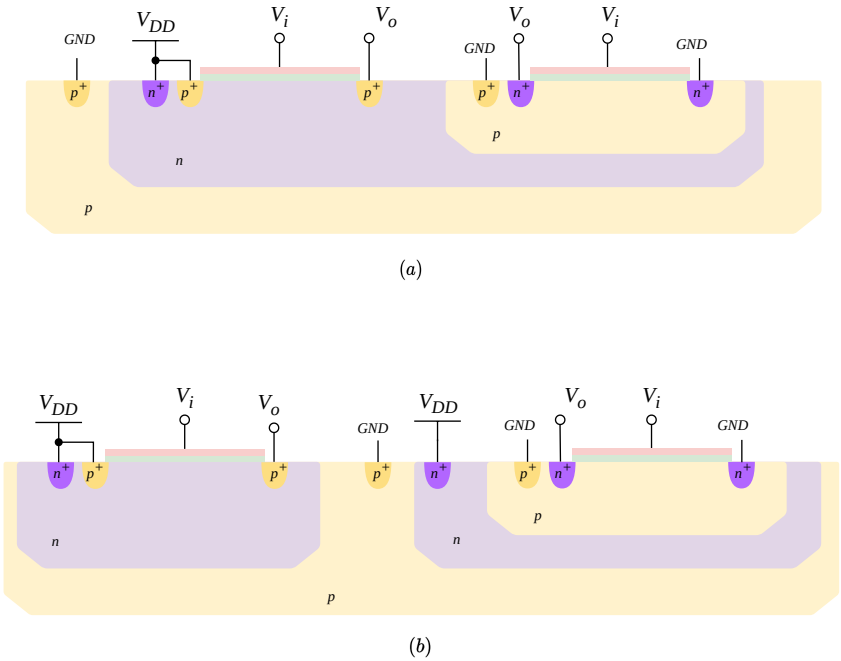

Figure 3. Triple-well structures exemplified in the cross-section of a CMOS inverter: (**a**) merged triple-well and (**b**) pure triple-well.

3. State-of-the-Art of FBB Techniques

3.1. Swapped Body Biasing

Swapped Body Biasing (SBB) is the most straightforward approach to implementing FBB [8,23]. It consists in connecting the substrate terminals of the MOS devices to the supply bars in such a way that the body–source junctions of the relevant devices are forward biased. This means that the substrate of NMOS transistors is connected to V_{DD}, while the substrate of PMOS devices is connected to ground. Clearly, the body bias can be limited to the most critical devices in order to avoid unnecessary leakage.

The main advantage of SBB lies in its ease of implementation; no additional sizing is required because the bias voltages for the body terminals are obtained directly from the supply rails. In other words, FBB can be implemented without the need for additional circuitry, which helps to minimize area overhead and shorten development times. At the same time, the absence of degrees of freedom restricts the scope of application. As a matter of fact, SBB is mostly limited to low-voltage applications. In particular, when this technique is implemented in dynamic comparators V_{bs} is equal to V_{DD} for most of the time due to the large voltage swings that the internal and output nodes are subject to. As already discussed in Section 2.3, body–source voltages larger than a certain threshold cause excessive energy absorption due to leakage and the current sink due to the body terminal. This constrains V_{DD} to less than 0.6 V. Factoring in supply voltage variations and taking into account that parasitic currents are normally already significant at $V_{bs} = 0.6$ V, we can expect SBB to be ineffective, if not detrimental, when the supply voltage exceeds 0.5 V. These considerations are clearly qualitative in nature, as the actual threshold varies with the technology. When the specification on V_{DD} is between 0.4 V and 0.6 V, it may be advisable to perform simulations in order to establish whether SBB represents a viable approach.

3.2. DTMOS

The Dynamic Threshold MOS (DTMOS) configuration was originally proposed for digital applications, and several variants have been developed over time. In its simplest version, DTMOS consists in biasing the substrate of a device by short-circuiting the body to the gate [19]. This creates a signal-dependent body biasing that lowers the threshold voltage of an MOS device when the latter is active and sets $V_{bs} = 0$ V when the transistor should

be turned off to avoid unnecessary leakage. The resulting component has an improved current drive without any penalty in terms of off-state leakage. The most significant DTMOS variants (shown in Figure 4) are discussed below. In the figures contained in the remainder of this paper, the arrow that indicates the source terminal of a forward body biased transistor is colored in white in order to make it more distinguishable.

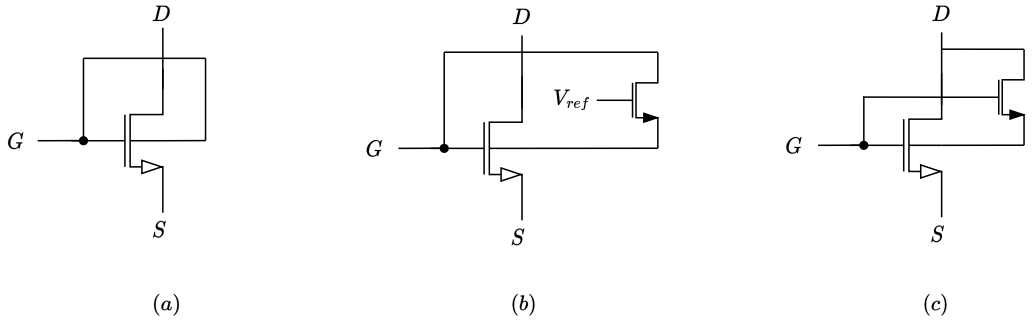

Figure 4. DTMOS configurations: (**a**) basic, (**b**) with limiter device, and (**c**) with augmenting device.

- **Basic DTMOS.** In the basic DTMOS configuration, the body and the gate terminal of the transistor are simply short-circuited together, as shown in Figure 4a [19]. In this way, the transistor's V_{bs} is 0 V when $V_{gs} = 0$ V and increases as V_{gs} grows. This means that the device is identical to a conventional MOSFET when it is in the off state, but $I_D(V_{gs})$ increases at a higher rate when $V_{gs} > 0$ V. The threshold voltage of the DTMOS device can be computed by letting $V_{gs} = V_{bs} = V_{th}$, and is provided by [19]:

$$V_{tf} = 2\Phi_B + |V_{FB}| + \frac{\epsilon_s q N_a}{C_{ox}^2}\left(\sqrt{1 - \frac{2V_{FB}C_{ox}^2}{\epsilon_S q N_a}} - 1\right). \tag{13}$$

  Because the square root in Equation (13) is less than 1, we have $V_{tf} < V_{th0}$ (see Equation (2)). This means that the threshold voltage of a DTMOS device is lower than the threshold of a conventional device when $V_{ov} = 0$ V. In addition, V_{th} continues to decrease as V_{gs} increases above V_{tf}. At $V_{gs} = V_{bs} = 2|\Phi_B|$, V_{th} reaches its minimum value, that is,

$$V_{th,min} = 2|\Phi_B| + V_{FB}. \tag{14}$$

  The gate–body connection causes the gate terminal to sink a non-zero current, which may be interpreted as the device having finite current gain. This is the main limitation of the basic DTMOS configuration; V_{gs} should not exceed 0.5–0.6 V, as higher voltages would cause significant current absorption from the gate. In circuits characterized by rail-to-rail swings, such as digital cells and dynamic comparators, this imposes an upper bound of the same magnitude on the supply voltage.
- **DTMOS with limiter device.** A limiter device, typically implemented as a minimum area MOSFET, can be added to increase the flexibility of the DTMOS configuration and allow operation at $V_{DD} > 0.6$ V [19,25]. An adequate reference voltage V_{ref} is applied to the gate of the limiter transistor to ensure that the body voltage of the DTMOS is clamped at 0.6 V. The drain and source terminals are connected to the gate and substrate of the main device, as shown in Figure 4b. In this way, the maximum body voltage of the transistor is independent of the supply voltage. Thus, a higher range of operating condition is achieved with the limiter device at the expense of increased area and the addition of a reference voltage.
- **DTMOS with augmenting device.** In this configuration, a small transistor (referred to as the augmenting device) is added to synthesize a voltage follower between the gate and the substrate of the main device and a current follower between the body and the drain [25,30]. The gate, drain, and source of the augmenting transistor are connected to the gate, drain, and body, respectively, of the main device, as depicted in Figure 4c. Instead of limiting the substrate voltage, the augmenting device reuses the current sink

due to the body to increase the drain current and discharge the output more quickly. In circuits such as CMOS logic gates and comparators, where power consumption is only dynamic in nature, the augmenting device eliminates the overhead associated with the body current because the latter is being used to drive a purely capacitive load and consequently does not give rise to static consumption.

3.3. Clocked FBB

Clocked FBB (CFBB) techniques typically exploit the clock signal to modulate the bias voltage that is applied to the substrates of one or more devices. In this way, the transistors' V_{bs} can be reduced when they should be in interdiction so as to limit leakage and minimize the power consumption. An obvious requirement of CFBB is the fact that it can be applied only to clocked circuits, as is the case for dynamic comparators. Although CFBB may take several forms, we will focus here on the technique proposed in [24]. The original implementation is shown in Figure 5.

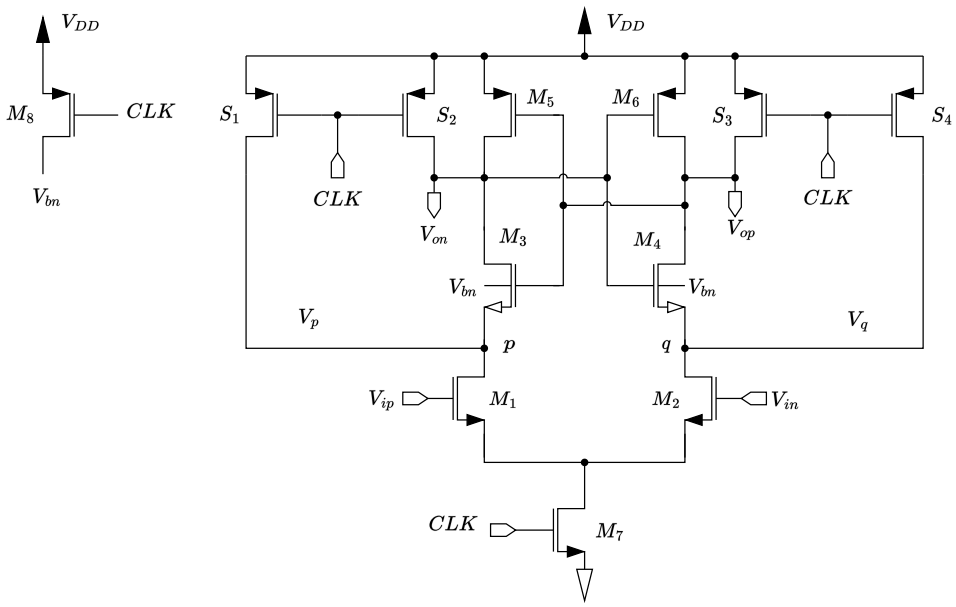

Figure 5. CFBB scheme applied to the Strong Arm latch, as described in [24].

A clocked device (M_8) is added to precharge the substrate of M_3–M_4 during the reset phase. Then, during the evaluation phase, M_8 turns off and the substrate node is left floating. This causes the body voltage V_{bn} to change due to charge redistribution. The charge redistribution phenomenon can be be analyzed by referring to the model shown in Figure 6 [26]. In the circuit, C_8 corresponds to the parallel parasitic capacitance associated with M_8, while C_{bd} and C_{bs} represent the body–drain and body–source parasitic capacitances of M_3–M_4, respectively. The C_{bg}'s, i.e., the body–gate parasitic capacitances, are not indicated because they end up in parallel to those of the C_{bd} due to the fact that the substrates of M_3–M_4 are shorted together. The voltages V_{op}, V_{on}, V_p, and V_q are assumed to be known, while $V_{b_{3,4}}$ is the unknown. The switch that models M_8 is initially closed, and $V_p = V_q = V_{op} = V_{on} = V_{DD}$; then, at a reference instant $t = 0$, the switch opens and the substrate node is left floating. It is not difficult to demonstrate that the following relationship holds for $t > 0$:

$$V_{b_{3,4}} = \frac{C_{bd}(V_{op} + V_{on}) + C_{bs}(V_p + V_q) + C_8 V_{DD}}{2C_{bd} + 2C_{bs} + C_8}. \tag{15}$$

Equation (15) shows that the substrate voltage of M_3–M_4 settles at a level that depends on the output common mode voltage and on the common mode voltage at nodes p and q. Moreover, $V_{b_{3,4}}$ depends on the parasitic capacitances associated with M_3, M_4, and M_8.

Because the sizing of M_3 and M_4 is typically chosen in such a way as to optimize the latch's regeneration time constant, the area of M_8 represents the most important parameter that the designer can act upon to tune $V_{b_{3,4}}$.

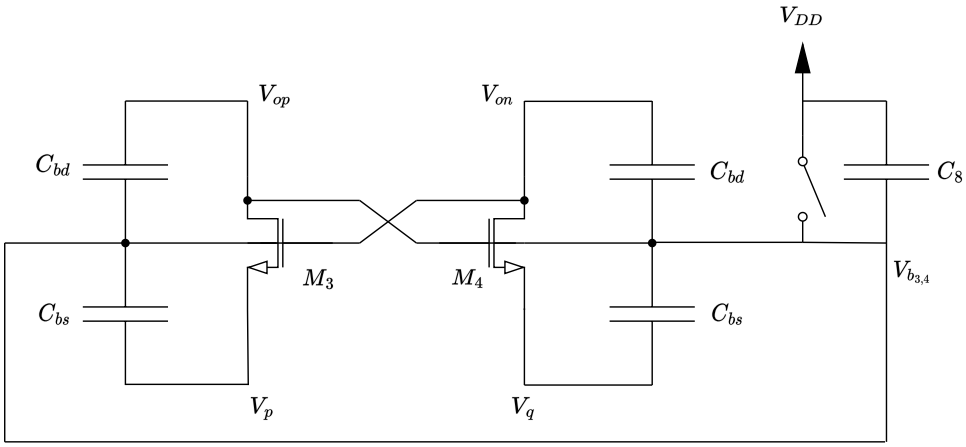

Figure 6. Simplified circuit model for analysis of the CFBB technique.

One of the main limitations of CFBB lies in the fact that $V_{b_{3,4}}$ depends on both V_p and V_q. When the input differential voltage of the comparator is small, V_p and V_q are discharged (almost) completely to ground by the differential pair M_1–M_2. When V_{id} is large, on the other hand, one side of the input pair (i.e., either M_1 or M_2) is partially or completely turned off, causing either V_p or V_q to remain partially charged. In this scenario, $V_p + V_q$ will settle at a higher value compared to the case in which V_{id} is small. This may cause either V_{bs_3} or V_{bs_4} to exceed the 0.6 V threshold when the comparator is processing large signals, thereby increasing the risk of latch-up if a merged triple-well process is being used. In order to avoid latch-up issues, the designer has two alternatives:

- Adopt a pure triple-well configuration (if possible) using distinct n-wells to isolate the PMOS and the NMOS devices. This approach removes the limitation on the substrate voltage, though at the expense of increased area occupation. In this case, the layout should be carefully optimized in order to minimize the overhead on delay and power consumption due to parasitic capacitances. In addition, the increase in V_{bs} that occurs when V_{id} is large results in higher leakage current flowing through either M_3 or M_4 during the evaluation phase, which may have a significant impact on power consumption depending on the technological process and the sizing of the circuit.
- Undersize M_8 in order to reduce the peak V_{bs} of M_3–M_4. This approach is highly inefficient because the substrate bias voltage is low when a small V_{id} is applied to the input, which means that the benefits of FBB are reduced precisely when the comparator operates in the most critical region of its transcharacteristic.

Another limitation of the CFBB scheme proposed in [24] is that the application of FBB is typically limited to M_3–M_4 because the source terminals of M_5–M_6 are connected to V_{DD}. If a clocked PMOS device was added to precharge the substrate terminal of M_5–M_6, then charge redistribution would only depend on the common mode shift at the output nodes. If Equation (15) was rewritten for $V_{b_{5,6}}$, then V_p and V_q would be replaced by V_{DD}; hence, the shift experienced by $V_{b_{5,6}}$ during the evaluation phase would be limited in magnitude and would not lead to a significant advantage in terms of regeneration time.

3.4. Hybrid FBB

In [26], an improved version of CFBB was proposed in an attempt to overcome its limitations. The modified CFBB scheme, which is denominated hybrid FBB (HFBB), is shown in Figure 7.

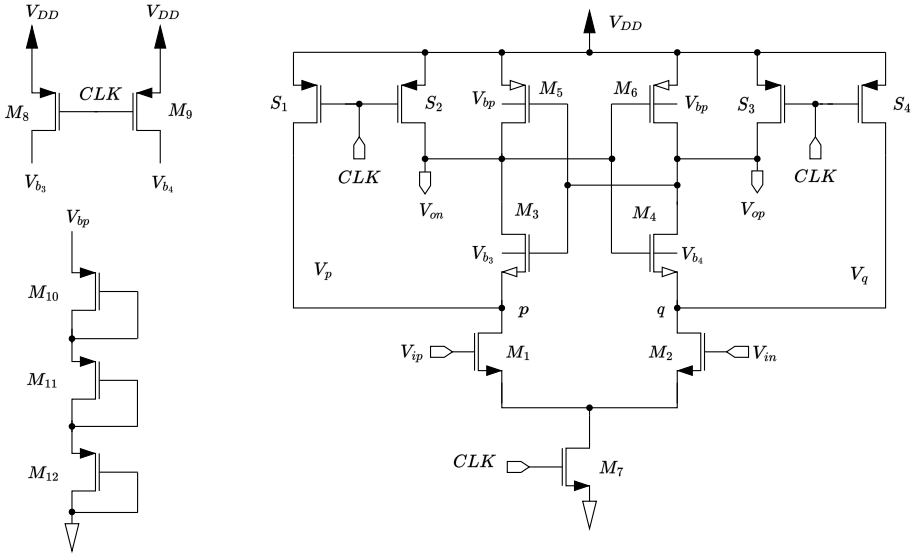

Figure 7. HFBB scheme from [26].

The HFBB scheme addresses the limitations of CFBB in two ways:

- The precharge device (M_8 in Figure 5) is split into a pair of separate transistors to allow for independent charge redistribution at the substrate nodes of M_3 and M_4. This prevents both V_{bs_3} and V_{bs_4} from increasing too much when the input differential voltage of the comparator is large.
- A stack of diode-connected transistors is added to provide a static bias voltage for the body terminals of M_5–M_6. In this way, the substrate voltage of M_5 and M_6 results from the nonlinear resistive divider formed by M_{10}–M_{11}–M_{12} and the body output resistances of M_5–M_6. The term "hybrid" stems from the fact that the circuit uses clocked FBB in combination with a static body biasing circuit.

Similar to the case of CFBB, the behavior of charge redistribution at the substrate nodes of M_3–M_4 can be studied by looking at a simplified equivalent circuit that accounts for the parasitic capacitances of the involved devices (Figure 8).

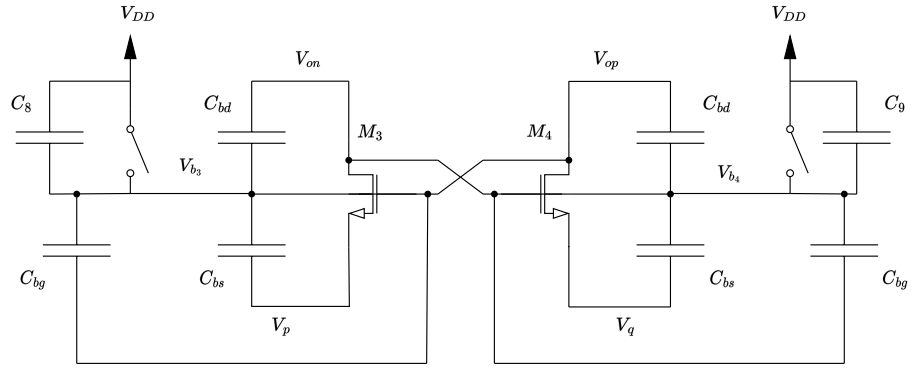

Figure 8. Simplified circuit model for analysis of the HFBB technique.

Note that the equivalent parasitic capacitances between gate and body C_{bg} are explicit, as the substrates of M_3–M_4 are kept separate. To analyze the circuit, we can suppose that $V_p = V_q = V_{op} = V_{on}$ and that switches M_8–M_9 are closed for $t \leq 0$. Then, the switches open at $t = 0$ and the substrate nodes are left floating. The expression of V_{b3} as a function of the other voltages for $t > 0$ is

$$V_{b_3} = \frac{C_{bd}V_{on} + C_{bg}V_{op} + C_{bs}V_p + C_8V_{DD}}{C_{bd} + C_{bg} + C_{bs} + C_8}. \tag{16}$$

Equation (16) shows that V_{b_3} depends on V_p but not on V_q. This ensures that V_{bs_3} remain limited even when V_{id} is large. To illustrate this point, assume that $|V_{id}|$ is large and that $V_{id} < 0$. In such a situation, M_1 will be partially or completely turned off, which means that node p will not be discharged to ground. According to Equation (16), V_{b_3} will settle at a higher value compared to the case in which V_{id} is close to 0. However, this is not an issue, as V_{bs_3} is provided by the difference between V_{b_3} and V_p. On the other hand, V_{b_4} is unaffected by node p not being discharged, as it only depends on V_q. It is worth noting that the same reasoning (including the expression of the substrate voltage for $t > 0$) can be applied to the other half of the circuit by swapping C_8 with C_9, V_p with V_q, V_{on} with V_{op}, and V_{b_3} with V_{b_4}.

As already mentioned, the static body biasing circuit used for M_5–M_6 removes the other limitation of CFBB, i.e., the absence of an adequate bias for the substrates of the PMOS devices. With the configuration shown in Figure 7, the voltage V_{bp} depends on the number of stacked devices and their aspect ratios. It should be noted that the substrate of M_5–M_6 remains biased even when $CK = 0$; however, this does not result in increased leakage, as the PMOS devices are in series with M_3–M_4 and with M_7, and all of their V_{bs} are zero during the reset phase.

The critical aspects concerning HFBB are mainly twofold. The first stems from the fact that the substrate voltages of M_3–M_4 depend asymmetrically on V_{op} and V_{on}. This can cause V_{bs_3} and V_{bs_4} to increase (or decrease) temporarily above (or below) their final settling value (see Section 4). This is not necessarily a limitation, as it can be leveraged to boost the body–source voltage during the most critical part of the evaluation phase; however, it is important for the designer to be aware of this phenomenon so that the sizing of the FBB circuit can be optimized accordingly. The second critical aspect lies in the fact that the applicability of the static biasing technique used to generate V_{bp} may depend on the properties of the technology and/or on the supply voltage. This is because M_5–M_6–M_{10}–M_{11}–M_{12} form a nonlinear resistive divider. Specifically, the value of V_{bp} depends on how the nonlinear transcharacteristics of the body–source diodes of M_5–M_6 intersect with the transcharacteristic of the biasing stack formed by M_{10}–M_{11}–M_{12}. Therefore, the designer should verify that V_{bp} remains stable by means of extensive PVT and Monte Carlo simulations.

As a final note, it should be remarked that the CFBB and HFBB techniques both require triple-well technology, as the bulk terminals of the NMOS devices must be isolated from the substrate.

4. Simulations

4.1. Methodology

We applied the FBB techniques described in the previous section to dynamic comparators implemented in 55 nm CMOS technology by STMicroelectronics (Geneva, Switzerland) at 1 V supply and simulated in Cadence Virtuoso. A clock frequency $f_{ck} = 2$ GHz was used in all the simulations. Each comparator was loaded by a pair of 1 fF capacitors. In order to ensure a fair comparison, a systematic approach was adopted for sizing and simulating the circuits. The first step consisted in sizing the basic versions of both the Strong Arm latch and the Elzakker comparator. The DTMOS, CFBB, and HFBB schemes were then implemented and optimized separately for the two comparators. A number of the FBB configurations that were obtained in this way are not documented in the literature, namely, the DTMOS-enhanced Elzakker comparator, the DTMOS-enhanced Strong Arm latch, and the CFBB- and HFBB-enhanced Elzakker comparators. When the same FBB scheme had several possible versions, we simulated the different variants and compared their performance. To improve the readability of the results, we report only the variant with the lowest power-delay product (PDP) for each FBB scheme.

4.2. Topologies and Sizing Choices

As already specified in the previous subsection, the Strong Arm latch and the Elzakker comparator were simulated in their basic, DTMOS-enhanced, CFBB-enhanced, and HFBB-

enhanced versions, for a total of eight topologies. The sizings of the Strong Arm and Elzakker cores were kept identical in all the simulations, and are reported in the Appendix B (Tables A1 and A2) together with the sizings of the FBB circuits. We now provide a brief overview of the six FBB-enhanced comparators and discuss the sizing choices adopted for each of them.

4.2.1. DTMOS-Enhanced Strong Arm

The DTMOS-enhanced Strong Arm latch is shown in Figure 9a. The special transistor symbols represent the DTMOS devices, as depicted in Figure 10. We employed augmenting device DTMOS because this technique does not lower the gate impedance of the MOS transistor and does not require a reference voltage, as is the case for limiter device DTMOS. FBB was applied to the cross-coupled inverters (M_3 through M_6) to speed up regeneration and improve the delay of the comparator. The simulations showed that the best performance was obtained when the four augmenting devices were implemented as minimum size transistors ($W = 0.135$ µm, $L = 0.06$ µm). It was found that a set of reset switches must be added in order for DTMOS to work properly when applied to dynamic comparators. Each decision of the comparator creates a memory effect on the substrate nets of the forward body biased transistors, and the augmenting devices are not able to suppress it during the reset phase; for this reason, S_5–S_6 and S_7–S_8 were added to cancel the differential voltage that builds up at the substrate nets of M_5–M_6 and M_3–M_4, respectively. All the reset switches had the minimum channel width and length.

4.2.2. CFBB-Enhanced Strong Arm

The CFBB-enhanced Strong Arm comparator is presented in Section 3, while its topology is shown in Figure 5. The precharge device M_8 was sized in such a way as to provide an adequate bias voltage for M_3–M_4. As indicated by Equation (15), the settling level of $V_{b_{3,4}}$ increases with the parasitic capacitance associated with M_8. Having this in mind, the precharge transistor was sized with $W = 2$ µm and minimum length. With these choices, $V_{b_{3,4}}$ settles close to 0.5 V but not above it.

4.2.3. HFBB-Enhanced Strong Arm

The HFBB-enhanced Strong Arm comparator is presented in Section 3, while its topology is shown in Figure 7. The precharge devices M_8-M_9 were sized using Equation (16) as a guideline. Similar to the case of CFBB, the settling levels of V_{b_3} and V_{b_4} increased with the parasitic capacitances associated with M_8 and M_9, respectively. Having this in mind, the precharge transistors were sized with $W = 0.4$ µm and minimum length. With these choices, V_{b_3} and V_{b_4} settled close to 0.5 V but not above it. The transistors that form the stack of diodes (that is, M_{10} through M_{12}) had the minimum channel length and width.

4.2.4. DTMOS-Enhanced Elzakker

The circuit of the DTMOS-enhanced Elzakker is depicted in Figure 9b. In this case, the augmenting devices were added to M_3 through M_6. As concerns the PMOS devices, our simulations showed that the performance improvement was maximized by applying FBB to M_5–M_6, the reason being that V_P and V_Q are discharged rapidly to 0 V at the very beginning of the regeneration phase. Moreover, in this configuration the drain terminals of the augmenting devices are connected directly to the outputs, which means that the device that is supposed to act as a pull-up will charge the output faster thanks to the drain current of the augmenting device. However, it should be noted that the current flowing through the augmenting devices is quite small compared to the drain current of the main devices. As in the DTMOS-enhanced Strong Arm latch, a set of switches S_3–S_4–S_5–S_6 was added to equalize the substrate nodes and suppress the memory effect; S_3 and S_4 were NMOS devices, as the substrates of M_3 and M_4 must be reset to ground (their sources are tied to GND). All the augmenting devices and the reset switches were minimum area devices. Finally, it should be noted that DTMOS was not applied to M_7–M_8, as the simulations showed that this caused only a negligible improvement in PDP.

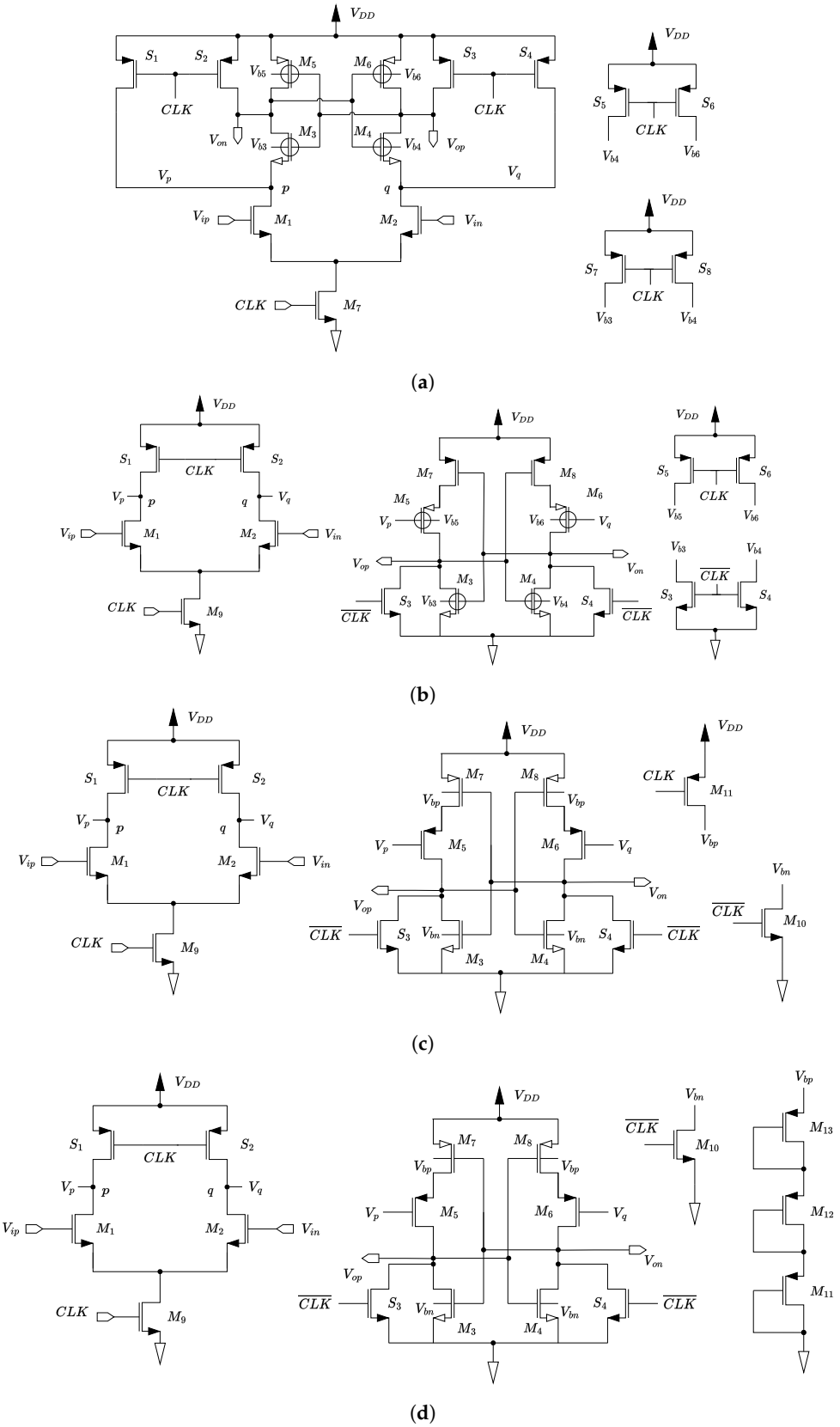

Figure 9. FBB -enhanced comparator topologies: (**a**) DTMOS-enhanced Strong Arm, (**b**) DTMOS-enhanced Elzakker, (**c**) CFBB-enhanced Elzakker, and (**d**) HFBB-enhanced Elzakker. The CFBB- and HFBB-enhanced Strong Arm are described in Section 3.

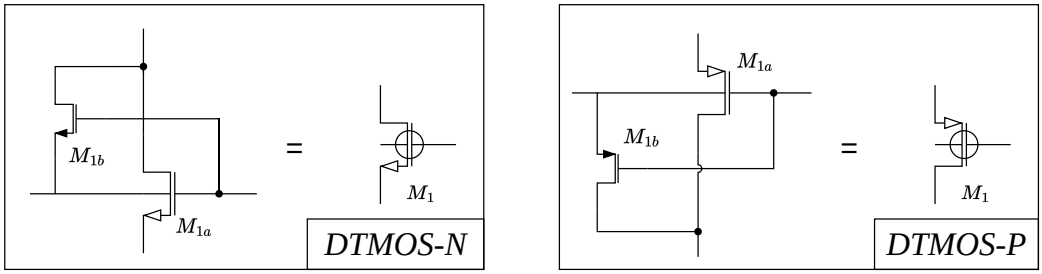

Figure 10. Equivalent symbol for the augmenting DTMOS.

4.2.5. CFBB-Enhanced Elzakker

The CFBB-enhanced Elzakker comparator is shown in Figure 9c. An interesting property of Elzakker's comparator is that CFBB can be applied both to the PMOS and the NMOS devices thanks to the topology of the regeneration circuit. Specifically, the common mode voltage at the source nodes of M_5–M_6 experiences a downward shift at the beginning of the evaluation phase, while the common mode voltage at the drain nodes of the same devices experiences an upward shift. These shifts are exploited to generate the bias voltages for M_3–M_4 and for M_7–M_8. A downside of this configuration is that the clocked device M_{10} requires an inverted clock. However, it should be remarked that the inverted clock is already available, as it is also required by the Elzakker topology. The clocked devices M_{10}–M_{11} were both sized with minimum channel length and $W = 0.2$ µm.

4.2.6. HFBB-Enhanced Elzakker

Figure 9d shows the schematic of the HFBB-enhanced Elzakker comparator. Similar to the HFBB-enhanced Strong Arm, the PMOS devices M_7–M_8 were biased through a stack of diode-connected devices (M_{11} through M_{13}), while the NMOS transistors M_3–M_4 were biased by the clocked transistor M_{10}. The clocked device was not split into two separate transistors, as the substrate voltages experience smaller variations compared to the CFBB-enhanced Strong Arm latch. In particular, $V_{bs_{3,4}}$ remained below 0.3 V even when $|V_{id}| = V_{DD}$. As in the previous case, M_{10} requires an inverted clock. As concerns the sizing, M_{11} through M_{13} are minimum area devices, while M_{10} has the minimum channel length and $W = 0.2$ µm.

4.3. Results

The topologies described in the previous subsection were characterized in terms of their body–source voltages, average power consumption, delay, PDP, noise, and offset. It is worth pointing out that the energy–delay product (EDP), defined as the PDP normalized by the clock frequency, was not used because all the comparators were simulated at the same f_{ck}, making it sufficient to compare their performance in terms of PDP. Simulations were run by applying an input differential voltage V_{id} such that $|V_{id}| = 1$ mV. The sign of the input differential voltage was toggled every two clock cycles during the reset phase. The delay was measured after a toggle event.

The characterization of the topologies in terms of delay, power consumption, and PDP is shown in Tables 1–3. First, let us focus our attention on the results obtained in the typical corner at $T = 27$ °C and nominal supply voltage (Table 1). The best performance in terms of PDP is achieved by the HFBB technique, both for the Strong Arm latch (where it provides a ≈13% improvement with respect to the conventional topology) and for the Elzakker comparator (where the improvement amounts to ≈11%). The enhancement of PDP brought about by CFBB is significant (around 5% for both topologies), though smaller compared to HFBB. DTMOS is always the least effective approach; in the case of the Strong Arm comparator, the PDP is even higher than that of the reference circuit. Next, let us consider delay and power consumption.

Table 1. Performance of different FBB techniques in the typical corner at $T = 27$ °C.

	Strong Arm				**Elzakker**			
	Conv.	CFBB	DTMOS	HFBB	Conv.	CFBB	DTMOS	HFBB
P_{avg} [µW]	72.23	72.33	72.98	73.33	106.5	106.9	109.1	111.9
Delay [ps]	57.49	53.34	57.63	49.27	89.01	84.25	82.68	75.8
PDP [W·fs]	4.153	3.817	4.205	3.613	9.48	9.009	9.024	8.479

When looking at the performance of HFBB and CFBB, similar considerations can be made for the Strong Arm comparator and the Elzakker comparator. It is apparent that while HFBB always causes a large improvement in terms of delay, its power consumption is the highest among the topologies reported here. While CFBB has a lower penalty on power consumption, it produces a moderate improvement in delay. DTMOS requires separate considerations for each comparator topology. In the Strong Arm latch, DTMOS is detrimental for performance, as delay and power consumption are worse than those of the conventional version. In the Elzakker comparator, DTMOS instead causes an appreciable improvement in terms of delay; however, power consumption increases significantly. An interpretation for the different performance of the two DTMOS-based topologies could be that in the Elzakker comparator the gates of M_5–M_6 are discharged rapidly by the input pair. This causes the substrate of M_5–M_6 to be forward biased from the very beginning of the evaluation phase. As a result, regeneration is sped up despite the fact that the $|V_{bs}|$ are smaller in magnitude (see Figure 11b below). In the Strong Arm latch, on the other hand, FBB intervenes at a later stage, as none of the forward body biased devices has their gate connected directly to the outputs of M_1–M_2.

Let us now consider the performance of the eight topologies under PVT variations. First, it is worth noting that the three FBB techniques exhibit good robustness under all the corners for both the Strong Arm latch and the Elzakker comparator. Moreover, Tables 2 and 3 show that the trends outlined in the typical corner remain consistent in the other corners. For the Strong Arm latch, HFBB always leads to the smallest delay, followed by CFBB and DTMOS. It is worth remarking that the advantage associated with HFBB increases in the most critical corners, namely, SS and $V_{DD} = 0.9$ V. This suggesting that HFBB may be suitable for high-speed low-voltage applications. For the Elzakker comparator, HFBB is again the most beneficial technique in terms of delay, while DTMOS and CFBB exhibit similar performance. As concerns power consumption, the comparison yields similar results for both the Strong Arm and the Elzakker topologies: CFBB is the best option in terms of energy efficiency across all corners, while HFBB always leads to the highest dissipation.

When characterizing an FBB-enhanced circuit, it is advisable to analyze the transient behavior of the body–source (for NMOS devices) and/or the source–body (for PMOS devices) voltages. This step is fundamental when using merged triple-well configurations, as it allows the designer to assess whether the topology is robust with respect to latch-up. In addition, verifying the behavior of V_{bs} and V_{sb} can help the designer to size the FBB circuit. Figure 11 shows the body–source (resp. source–body) voltages for the NMOS (resp. PMOS) devices in the six FBB-enhanced comparators. The dashed lines correspond to the V_{bs} of the NMOS transistors, while the continuous lines represent the V_{sb} of the PMOS transistors. Because the topologies are symmetric, the transient behavior of V_{bs} and V_{sb} is only shown for one side of the circuit over a duration of two clock periods. This provides an exhaustive characterization, as the time window includes the instant at which the sign of V_{id} toggles. The figure shows that V_{bs} and V_{sb} always remain below ≈500 mV in the FBB-enhanced Elzakker topologies. In the FBB-enhanced Strong Arm topologies, instead, the V_{bs} of the NMOS devices exhibit a spike after the end of the evaluation phase. This phenomenon is caused by the fact that the charge transient that occurs when the clock goes low is faster for the substrate nodes than it is for the source nodes of M_3–M_4. The spike can be attenuated or even removed by increasing the aspect ratio of precharge devices S_1 through S_4 so that the sources of M_3–M_4 are charged faster. It is important to remark that

these spikes cannot cause latch-up, as the source nodes remain floating when $CK = 0$ V, which in turn implies that the emitter of the NPN transistor in the parasitic PNPN structure is floating as well. In this condition, the positive feedback loop is broken.

Finally, it is worth noting that in the HFBB-enhanced Strong Arm the body–source voltage of M_3–M_4 settles to different values depending on the sign of the output. This is a consequence of the fact that the bulk terminals of M_3 and M_4 are kept separate, and as such are coupled differently with each output. This asymmetry is observable in the curves of the DTMOS-enhanced comparators, in which the forward body biased transistors have independent bulk terminals.

Table 2. Simulation results for delay vs. PVT. The delay is expressed in ps.

		FF	**SS**	**FS**	**SF**	**0.9V_{DD}**	**1.1V_{DD}**	**0°**	**80°**
SA	Conv.	50.44	66.38	55.25	60.55	74.49	47.35	57.67	57.85
	CFBB	46.91	61.1	51.04	56.33	67.88	44.82	53.07	54.46
	DTMOS	50.97	66.65	55.49	60.78	73.44	48.27	57.44	58.69
	HFBB	44.25	55.37	47.01	52.23	60.89	42.11	48.62	51.31
Elzakker	Conv.	77.5	103.1	91.44	87.4	116.2	73.39	89.68	89.17
	CFBB	74.22	96.27	87.05	82.22	108.6	70.26	84.37	85.23
	DTMOS	73.13	94.15	84.06	81.90	106.7	68.89	82.99	83.34
	HFBB	68.29	84.34	78.06	74.19	93.51	65.04	74.56	79.15

Table 3. Simulation results for average power consumption vs. PVT. Power consumption is expressed in µW.

		FF	**SS**	**FS**	**SF**	**0.9V_{DD}**	**1.1V_{DD}**	**0°**	**80°**
SA	Conv.	75.29	71.7	72.33	73.32	56.66	90.28	69.61	78.12
	CFBB	75.97	70.24	71.9	72.64	55.69	90.35	68.81	77.85
	DTMOS	76.86	71.67	73.65	73.60	56.65	92.26	70.13	79.43
	HFBB	77.41	72.13	73.71	74.3	56.83	92.73	70.36	79.6
Elzakker	Conv.	107.5	105.9	107.5	106.1	83.65	132.9	103.2	114
	CFBB	107.9	106.3	108	106.4	83.86	133.6	103.5	114.6
	DTMOS	110.4	108.4	110.1	109.0	85.77	136.4	105.8	117.0
	HFBB	112.4	111.6	113.1	111.1	87.36	140.2	108.2	119.5

Figure 12 shows the behavior of the source–body and body–source voltages (for NMOS and PMOS devices, respectively) when $|Vid| = 900$ mV. Clearly, the DTMOS-enhanced and HFBB-enhanced topologies do not suffer from robustness issues when V_{id} increases in magnitude, as V_{bs} and V_{sb} always stay well below 0.6 V. The CFBB-enhanced Elzakker exhibits good robustness as well. Indeed, the substrate nodes of M_3 through M_8 are not coupled directly to the drain nodes of the input differential pair in Elzakker's comparator thanks to the two-stage architecture. Hence, the partial discharge of these nodes has a smaller impact on the bias voltages that are applied to the bulk terminals. The CFBB-enhanced Strong Arm, on the other hand, is prone to latch-up and/or increased power consumption caused by the bulk current. As shown in Figure 12c, V_{bs} of M_3–M_4 exceeds 0.7 V and then settles around 0.6 V during the evaluation phase. As already explained, this follows from the fact that the common mode voltage at the drain nodes of the input pair does not reach ground during the evaluation phase, because either M_1 or M_2 remains switched off (depending on the sign of V_{id}). Obviously, latch-up may be avoided by adopting a pure triple-well configuration at the expense of increased area and routing parasitics.

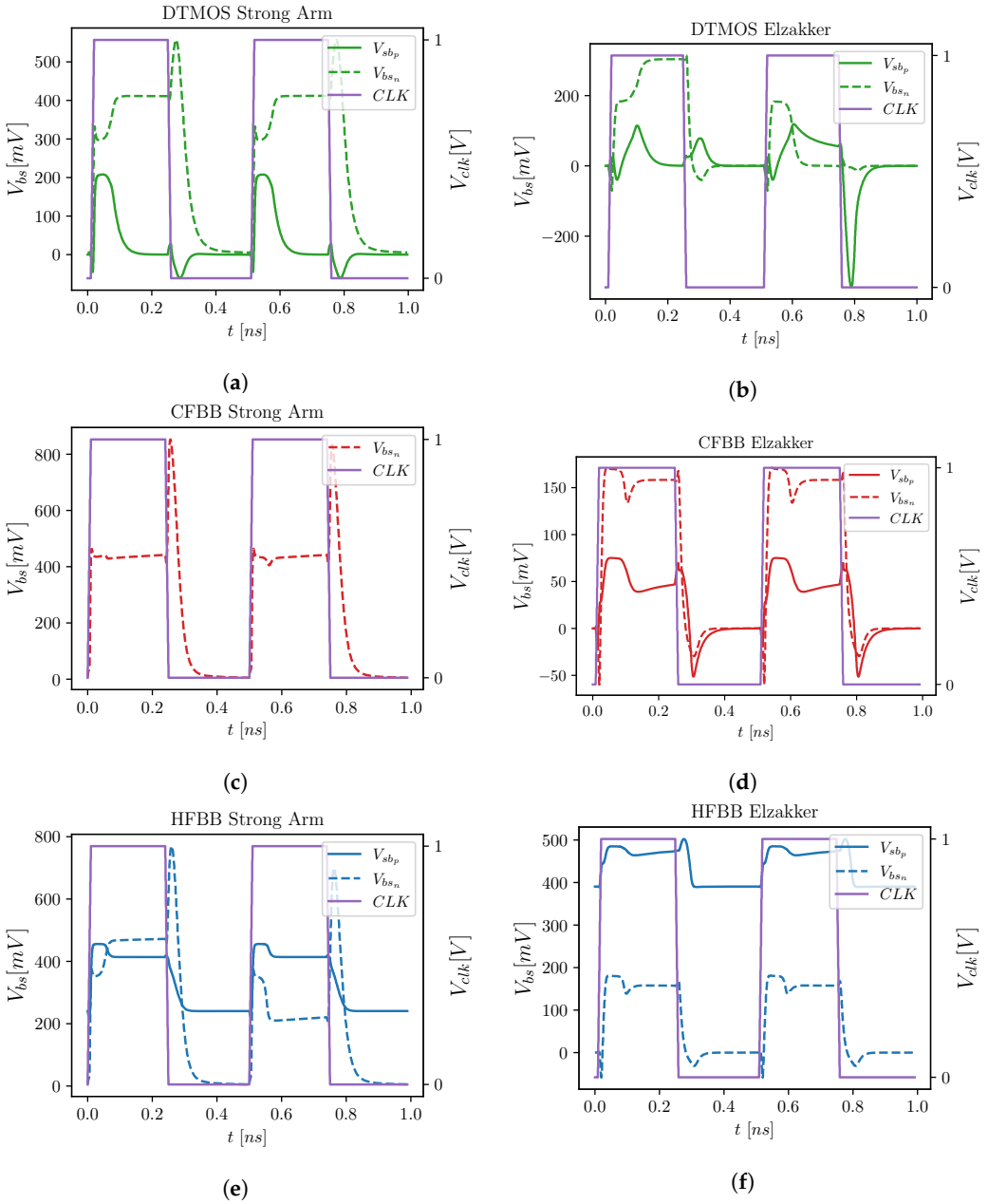

Figure 11. Transient behavior of body–source (resp. source–body) voltages of NMOS (resp. PMOS) for the FBB-enhanced topologies at $|V_{id}| = 1mV$: (**a**) DTMOS-enhanced Strong Arm, (**b**) DTMOS-enhanced Elzakker, (**c**) CFBB-enhanced Strong Arm, (**d**) CFBB-enhanced Elzakker, (**e**) HFBB-enhanced Strong Arm, and (**f**) HFBB-enhanced Elzakker. The dashed lines represent the V_{bs} of the NMOS devices, while the continuous lines represent the V_{sb} of the PMOS devices.

Table 4 compares the performance of the conventional and FBB-enhanced topologies in terms of input-referred noise and input-referred offset. The FBB-enhanced Strong Arm topologies exhibit worse noise performance compared to the conventional comparator. This is in accordance with theory, because in the Strong Arm latch the main noise contributions are inversely proportional to the threshold voltage of the latch devices [31] and FBB causes a reduction of said threshold voltages. Moreover, CFBB has better noise performance because only the threshold voltage of M_3–M_4 is lowered.

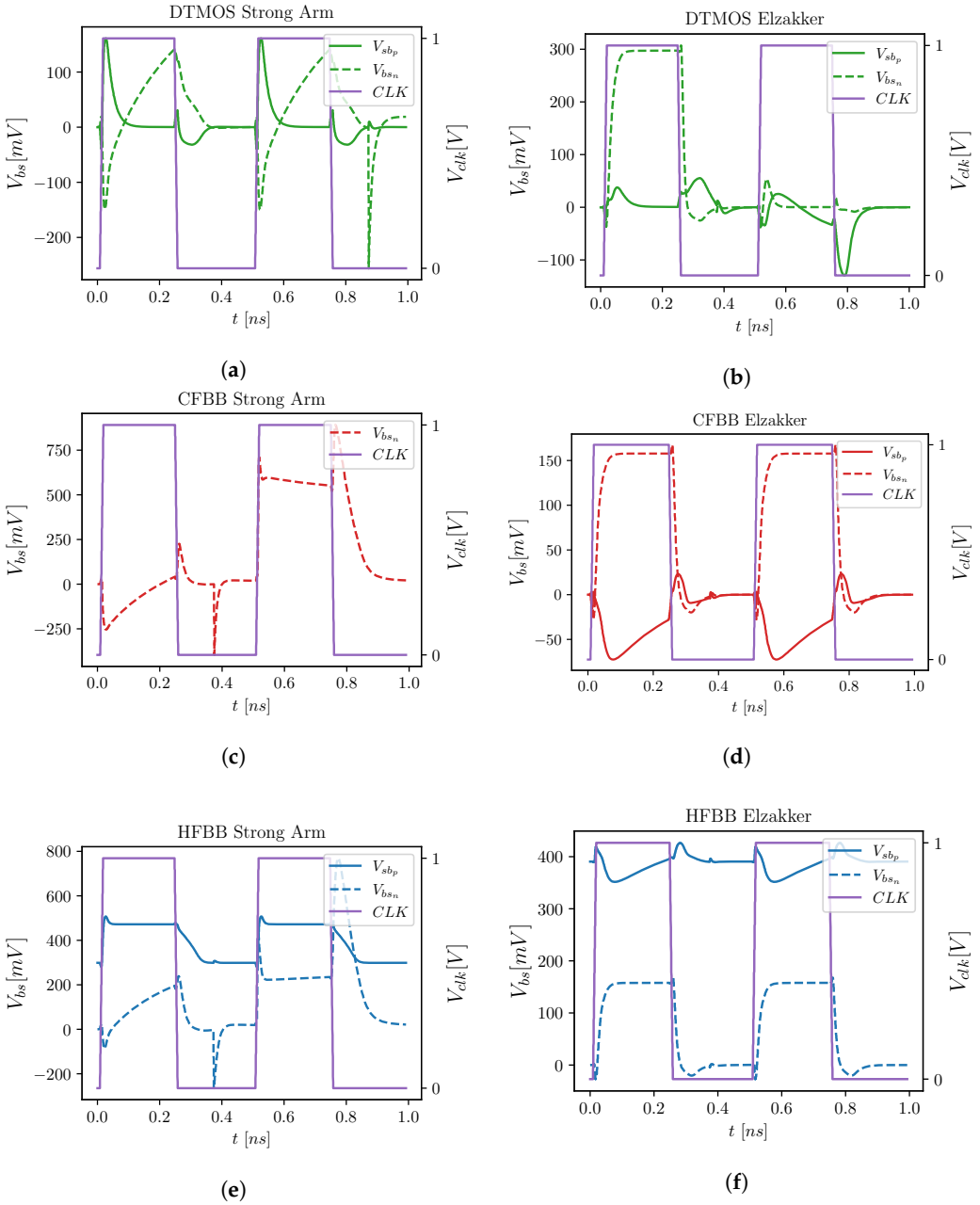

Figure 12. Transient behavior of body–source (resp. source–body) voltages of NMOS (resp. PMOS) for the FBB-enhanced topologies at $|V_{id}| = 900$ mV: (**a**) DTMOS-enhanced Strong Arm, (**b**) DTMOS-enhanced Elzakker, (**c**) CFBB-enhanced Strong Arm, (**d**) CFBB-enhanced Elzakker, (**e**) HFBB-enhanced Strong Arm, and (**f**) HFBB-enhanced Elzakker. The dashed lines represent the V_{bs} of the NMOS devices, while the continuous lines represent the V_{sb} of the PMOS devices.

The behavior of the Elzakker topologies in terms of noise is slightly counterintuitive and more difficult to interpret. The noise performance does not change significantly despite the decrease in the threshold voltages caused by FBB. The DTMOS-enhanced Elzakker topology even experiences a significant improvement. The fact that noise performance is not worsened by FBB may be (at least in part) related to the fact that V_{bs} and the V_{sb} are generally smaller compared to the Strong Arm-based topologies, especially in the case of DTMOS, where $V_{sb_{5,6}}$ has negative spikes at the beginning of the evaluation phase. This detail may explain the improvement brought about by DTMOS; the body terminals of M_5 and M_6 are initially reverse biased, which temporarily increases the preamplification gain, then become forward biased as the comparator enters regeneration. Additionally,

DTMOS may be influencing the way the two cascaded integrators interact in the Elzakker comparator. As pointed out in [27], in a two-stage regenerative comparator there exists a race condition between the two integrators: if the input pair enters triode before the second stage reaches regeneration, the differential voltage at nodes p and q is erased too early and preamplification is less effective. In the DTMOS-enhanced Elzakker comparator, the additional parasitics introduced by the augmenting devices may help to slow down the attenuation of V_{pq}, while the augmenting devices of M_5–M_6 help charge the output nodes. This interpretation is supported by the fact that DTMOS is the only FBB circuit that has a direct effect on the parasitic capacitance at nodes p and q (recall that the gate terminals of the augmenting devices are connected to the gate terminals of the main transistors).

Offset performance was evaluated by running 200 Monte Carlo mismatch iterations for each comparator. The input-referred offsets of the FBB-enhanced topologies are similar to those of their conventional counterparts for both the Strong Arm latch and the Elzakker comparator. The only exception is the DTMOS-enhanced Elzakker, which has a smaller input-referred offset compared to the conventional topology. This is likely due to the same phenomenon that causes the input-referred noise to improve, namely, a significant boost of the preamplification gain due to the presence of the augmenting devices. In the Strong Arm latch, the DTMOS and HFBB configuration cause a slight deterioration in offset because the FBB circuits require separate precharge devices which contribute with their mismatch. Finally, it should be highlighted that the mean value of the offset is always negative. This is simply a simulation artifact caused by the fact that the offset is estimated by applying a ramp to the comparator inputs (linear search). Because of this, the mean value is slightly influenced by the residual memory effect at the intermediate and output nodes of the comparator.

Table 4. Simulation results for input-referred noise and offset of the topologies under examination. The offset was estimated with 200 Monte Carlo mismatch iterations.

		V_{noise}^{rms} [mV]	μ_{offset} [mV]	σ_{offset} [mV]
SA	Conv.	1.29	−0.358	7.73
	CFBB	1.34	−0.493	7.32
	DTMOS	1.56	−0.410	8.84
	HFBB	1.47	−0.335	8.70
Elzakker	Conv.	3.05	−0.472	15.2
	CFBB	3.07	−0.629	15.1
	DTMOS	2.73	−0.005	12.7
	HFBB	2.96	−0.892	16.0

5. Conclusions

This work has presented a survey on the application of FBB techniques to dynamic comparators in the context of high-speed systems with medium to low supply voltage (around 1 V). In particular, three body biasing techniques were examined and compared: CFBB, HFBB, and DTMOS. After establishing criteria for evaluating the points of strength and the limitations of FBB techniques, the three approaches were analyzed from both a practical and a theoretical standpoint, then the different FBB schemes were implemented and simulated by focusing on two popular topologies: the Strong Arm latch and Elzakker's comparator. In total, eight circuits were simulated and their performances were compared in terms of delay, power consumption, and PDP. In addition to the comparison between different FBB approaches, the results presented in this paper contain two new contributions: the adaptation of the CFBB and HFBB schemes to the Elzakker comparator, and the application of augmenting device DTMOS to the Strong Arm and Elzakker topologies. To the best of our knowledge, the application of DTMOS (especially augmenting device DTMOS) is poorly documented in the literature, while both the CFBB- and HFBB-enhanced Elzakker comparators are novel topologies. Our simulations show that HFBB is the most effective technique from the point of view of both delay and PDP. At the same time, HFBB has a

non-negligible overhead in terms of power consumption, noise, and offset. While CFBB tends to be more power efficient, it causes a moderate improvement in the delay. DTMOS proves to be the least beneficial technique in terms of delay and power consumption, especially when applied to the Strong Arm comparator. In the case of the Elzakker topology, however, DTMOS is able to improve noise and offset while leading to a small improvement in PDP. The positive impact of DTMOS on noise and offset is counter-intuitive when considering the operating principles of FBB and dynamic comparators. For this reason, it may be interesting to investigate its effects in future works using a more rigorous theoretical framework.

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Appendix A. Analytical Derivation of the Delay

As already mentioned in Section 2, for the Strong Arm latch and Elzakker's comparator the analytical expression of the delay has the form

$$t_d = t_d^{pre} + t_d^{latch}, \tag{A1}$$

where t_d^{pre} is the preamplification time and t_d^{latch} is the regeneration time. In the Strong Arm latch, preamplification consists of two sub-phases, namely, sampling and propagation [27]. During sampling, which lasts until M_3 and M_4 turn on, the differential current of the input pair is integrated at the drain nodes of M_1 and M_2. Propagation is the time between the end of sampling and the moment at which M_5–M_6 turn on. During this phase, M_3 and M_4 start to discharge the output nodes asymmetrically before the latch takes over. The total preamplification time can be written as [27]

$$t_{d,SA}^{pre} = \frac{2C_{pq}V_{th_{3,4}}}{I_{tail}} + \frac{2(C_{pq}+C_{out})|V_{th_{5,6}}|}{I_{tail}}, \tag{A2}$$

where C_{pq} denotes the single-ended parasitic capacitance at each of the input pair's drain nodes (that is, p and q), C_{out} denotes the single-ended parasitic capacitance at each of the output nodes, and $I_{tail} = I_{d7}$ denotes the tail current. It should be noted that I_{tail} is assumed to be constant; this is an approximation, because in reality M_7 enters the triode region very quickly. The first term accounts for the time it takes for M_3–M_4 to turn on, while the second term corresponds to the time required for M_5–M_6 to turn on.

In the Elzakker topology, the input signal is preamplified by two integrators connected in cascade. As in the previous case, preamplification can be split into two sub-phases. During the first, the input pair discharges nodes p and q until M_5–M_6 turn on. Then, the output nodes are charged until the NMOS devices M_3–M_4 turn on, which marks the end of preamplification. Therefore, the preamplification time can be expressed as

$$t_{d,DT}^{pre} = \frac{2C_{pq}|V_{th_{5,6}}|}{I_{tail_1}} + \frac{2C_{out}V_{th_{3,4}}}{I_{tail_2}}, \tag{A3}$$

where I_{tail_1} is the preamplifier's tail current and $I_{tail_2} = (I_{d7} + I_{d8})/2$ is the common mode current flowing in the two branches of the second stage. Both currents are approximated as constant. Note the second term on the right side of Equation (A3).

If we neglect the series resistance of M_5–M_6 in the Elzakker comparator, the regeneration time can be computed starting from the same expression for both topologies:

$$t_d^{latch} = \frac{C_{out}}{g_{m_{eff}}} \ln\left(\frac{V_{DD}}{2V_{od}^o(V_{id})}\right). \tag{A4}$$

Equation (A4) is the well known expression of the regeneration time of a latch consisting of two cross-coupled inverters [32,33], and is obtained by linearizing the circuit, which means that the g_ms of the devices are approximated as constant. The quantity $g_{m_{eff}}$ is the sum of the transconductance of the PMOS and the transconductance of the NMOS devices in the latch, while $V_{od}^o(V_{id})$ represents the differential voltage at the output nodes at the beginning of the regeneration phase. The expression of $V_{od}^o(V_{id})$ depends on the topology. For the Strong Arm latch, we consider the phase in which M_3–M_4 are on and M_5–M_6 are still off. If we neglect the positive feedback formed by M_3–M_4, we have $I_{d3} = I_{d_1}$ and $I_{d_4} = I_{d_2}$, which means that the input difference is integrated on the output nodes for a time duration $\Delta t = \frac{2C_{out}|V_{th_{5,6}}|}{I_{tail}}$. It follows that

$$V_{od}^o(V_{id}) = \frac{g_{m_{1,2}}V_{id}}{C_{out}}\Delta t = \frac{2g_{m_{1,2}}|V_{th_{5,6}}|}{I_{tail}}V_{id}. \tag{A5}$$

This analysis, which follows the one presented in [32], neglects the initial preamplification that occurs at the drain nodes of M_1 and M_2. Consequently, while the expression of $V_{od}^o(V_{id})$ is lacking in accuracy, it is more compact and usable. The reader is referred to [27] for a more detailed discussion of Strong Arm latch behavior during dynamic preamplification. It is interesting to observe that, according to the analysis developed in [27], Equation (A5) is accurate when $C_c << C_{out}$. For the Elzakker comparator, the analysis is more involved because the differential signal is first integrated by the preamplifier and then by devices M_5–M_6. Moreover, the common mode voltage at nodes p and q decreases during the second integration phase, causing the transconductance of M_5–M_6 to increase. In order to limit the complexity of the calculation, we neglect this effect and assume that $g_{m_{5,6}}$ remains constant. With this assumption, we can write

$$V_{od}^o(V_{id}) = \frac{g_{m_{1,2}}g_{m_{5,6}}t_{d,DT}^{pre_1}t_d^{pre_2}}{C_{pq}C_{out}}V_{id}, \tag{A6}$$

where $t_d^{pre_2} \triangleq 2C_{out}V_{th_{3,4}}/I_{tail_2}$. Again, it is worth remarking that Equations (A6) and (A5) have been obtained by adopting several simplifying hypotheses, and as such they can be expected to be inaccurate when used to make predictions of the delay. However, this is not an issue because these analytical derivations are only being used to make qualitative considerations about the impact of FBB.

Appendix B. Sizing of Survey Topologies

Table A1. Sizing of the Strong Arm latch core. The channel length is set to the minimum value ($L = 0.06$ µm) for all transistors.

Devices	Width [µm]
M_7	16
M_1–M_2	8
M_3–M_6	2
S_1–S_4	0.5

Table A2. Sizing of the Elzakker comparator core. The channel length is set to the minimum value ($L = 0.06$ µm) for all transistors.

Devices	Width [µm]
M_9	20
M_1–M_2	10
M_3–M_8	2
S_1–S_2	1
S_3–S_4	0.5

Table A3. Sizing of the FBB circuits for the Strong Arm comparator. The channel length is set to the minimum value ($L = 0.06$ µm) for all transistors.

Devices	Width [µm]		
	CFBB	HFBB	DTMOS
M_8	2	0.4	-
M_9	-	0.4	-
M_{10}–M_{12}	-	0.135	-
M_{3b}–M_{6b}	-	-	0.135
S_5–S_8	-	-	0.135

Table A4. Sizing of the FBB circuits for the Elzakker comparator. The channel length is set to the minimum value ($L = 0.06$ µm) for all transistors.

Devices	Width [µm]		
	CFBB	HFBB	DTMOS
M_{10}	0.2	0.2	-
M_{11}	0.2	0.135	-
M_{12}	-	0.135	-
M_{13}	-	0.135	-
M_{3b}–M_{6b}	-	-	0.135
S_3–S_6	-	-	0.135

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