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A High Performance 0.3 V Standard-Cell-Based OTA Suitable for Automatic Layout Flow

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Abstract: In this paper, we propose a novel standard-cell-based OTA architecture based on an improved version of the differential to single-ended converter, previously proposed by the authors, on a novel standard-cell-based basic voltage amplifier block. Due to a replica-bias approach, the basic voltage amplifier exhibits a well-defined output static voltage to allow easy cascadability. Another feature of the basic voltage amplifier is to provide a low output impedance to allow dominant pole compensation at the output of the cascade of several stages. An ultra-low voltage (ULV) standard-cell-based OTA based on the proposed architecture and building blocks has been designed referring to the standard-cell library of a 130-nm CMOS process with a supply voltage of 0.3 V. The layout of the OTA has been implemented by following an automatic layout flow within a commercial tool for the place-and-route of digital circuits. Simulation results have shown a differential gain of 50 dB with a gain–bandwidth product of 10 MHz when driving a 150 pF load capacitance. Good robustness is achieved under PVT variations, in particular for voltage gain, offset voltage, and phase margin. State-of-the-art small signal figures of merit and limited area footprint are key characteristics of the proposed amplifier.

Keywords: standard-cell; OTA; fully synthesizable; inverter-based; ultra-low voltage; ultra-low power; IoT

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1. Introduction

The growing diffusion of the Internet of Things (IoT) [1,2] involves the embedding of integrated circuits (ICs) into objects to acquire, process, and exchange useful information. This requires the development of mixed-signal ICs that typically integrate a sensor, analog front-end, analog-to-digital converter (ADC), digital processing, and a simple wireless transceiver [3–6]. Together with area minimization and reconfigurability, one of the strongest constraints is on power consumption: these systems often have to operate for years from tiny batteries or by harvesting energy from the environment; thus, an extremely low power consumption is required. Since in many applications IoT sensor nodes have to be energy autonomous, they have to scavenge energy from the environment by means of photovoltaic cells, thermoelectric generators, and vibration sensors. Operating with this kind of energy harvesting system requires the minimization of the supply voltage, and circuits operating with supply voltages as low as 0.3 V are suitable to properly operate with such harvesting sources [7–9].

The operational transconductance amplifier (OTA) is a fundamental building block to design analog front-ends, allowing for the implementation of amplification and filtering functions needed in IoT and biomedical applications. In this regard, several OTAs have been proposed in recent work, which allow for the attainment of good performance working with supply voltages as low as 0.3 V [10–19]. These solutions are almost all based on body-driven (BD) input stages which, at such low supply voltage, allow them to reach rail-to-rail input common mode range (ICMR) and exploit gate-biased techniques in order

to assure well-defined dc bias point and good robustness against process, supply voltage, and temperature (PVT) variations. In addition, due to the aggressive supply voltage scaling and due to the effectiveness of the deep sub-threshold region in which the most of these architectures work, the performance of recent ultra-low voltage (ULV) OTAs can be considered state-of-the-art in terms of gain bandwidth product and slew rate normalized to the power consumption.

However, such OTA topologies rely on a full custom design approach and, even if the analog part is often only a small fraction of the whole system, it requires a large design effort, with a negative impact on design times and costs, which are very important aspects in the context of IoT nodes development. This is because both the schematic and the layout design phases are typically carried out manually, iterating each step repeatedly until specifications are met with good robustness under PVT variations and mismatches. To overcome this problem and reduce both costs and time-to-market, a design methodology for analog circuits defined as synthesizable analog design has been introduced in [20]. In this design approach, all circuit building blocks are implemented through standard-cells taken from the digital library and coded in a hardware description language, which can then be synthesized from commercial standard-cell libraries and automatically placed and routed using electronic design automation (EDA) tools. Compared to conventional analog implementations, standard-cell-based analog implementations significantly shorten the design time and cost [20–32].

In the context of the design of standard-cell-based amplifiers, researchers have recently focused on automatic place-and-route strategies for standard-cell-based circuits, typically adopted in the digital design flow, to implement fully-synthesizable analog circuits and drastically reduce the area usage of analog building blocks [33]. Research studies are investigating both the use of a digital approach to implement analog functions [20,34] and the design of analog blocks exploiting digital standard-cells [22,25,35,36]. In the latter case, digital gates are used as basic blocks to design analog functions, with the goal of exploiting both the automatic place-and-route steps of the digital design flow and, in particular, a fully automatic synthesis flow of the analog part together with the digital one.

On the one hand, different approaches to mimic the behavior of the OTA through digital-based architectures have been proposed, such as the VCO-based OTA [37,38] and the fully-digital OTA (DIGOTA) [39–41] approaches. On the other hand, several inverter-based OTA architectures [42–44] have been proposed in the literature to allow operation at low supply voltages [15–17,22,45–50]. The design of standard-cell based OTAs [29,33,40,51,52] is the direct evolution of this approach, with some added constraints due to the fact that optimization at the transistor level is not allowed. Differently from custom-designed inverters, the standard-cell inverter is typically optimized for digital operation, e.g., to achieve symmetrical slew rate, and this results in a systematic offset in the dc transfer function [52,53]; moreover, as pointed out in several papers, the performance and even the operation of standard-cell-based analog circuits are severely impaired by PVT and mismatch variations, resulting in incorrect bias, large offsets, and significant performance variations [46,47,53–57].

To cope with these issues, approaches that exploit body biasing of the standard-cells, together with a custom-designed body bias generator, have been proposed in the literature [45,58,59]. However, these solutions require the availability of the body terminals: this is common in modern technologies, where body biasing is exploited to compensate for PVT variations in digital circuits [60,61], but it is not compatible with older technologies often used for analog designs. Moreover, the limited gain of the body input could require control voltages beyond the supply rails to cope with large bias point variations. A different solution has been proposed in [52], which presents a basic amplifier cell where an auxiliary inverter or one input of a two-input logic gate is driven by a fully-standard-cell replica bias loop to stabilize the bias point.

In this work, we present improvements to two analog building blocks that have been previously presented in [33,52]. More specifically, we propose a novel standard-cell-based

basic voltage amplifier cell that exploits the same biasing strategy as in [52], based on a replica loop to control the output dc voltage, but exhibits a gain approximately equal to an integer factor k (i.e., the number of inverters in parallel) and a low output impedance. We also present a modified version of the D2S introduced in [33], in which a novel error amplifier topology is adopted in the feedback loop. A further contribution of the present paper is the OTA architecture, which combines all of these building blocks into a multi-stage fully synthesizable amplifier.

The paper is structured as follows: Sections 2–4 present the proposed improved standard-cell-based analog building blocks, while the OTA architecture and design guidelines are reported in Sections 5 and 6, respectively. Simulation results are presented in Section 7, a comparison against other ULV OTAs taken from the literature is presented in Section 8, and finally some conclusions are reported in Section 9.

2. Replica Bias Approach to Control the Static Output Voltage of Inverters

This section briefly reviews the standard-cell-based replica-bias control loop presented in [52] to accurately set the output static voltage of the inverter gates exploited as basic amplifier (BA) cells [52].

The replica-bias control loop is depicted in Figure 1 and is composed of an instance (I_0) of a reference inverter taken from the standard-cell library of the target technology. The input of the inverter I_0 is biased at a voltage equal to the analog ground $AGND$ (i.e., $V_{DD}/2$). The output static voltage of I_0 is compared with a reference voltage V_{ref} (usually equal to $V_{DD}/2$) through the standard-cell-based error amplifier composed of the inverters $I_{2,3,4,5}$ (depicted in green in Figure 1). The generated output voltage, namely $Ctrl$, is used to close the negative feedback loop through another instance I_1 of the reference inverter. Referring to the approach presented in [52], the BA cell is implemented by the inverters I_0 and I_1 (depicted in pink in Figure 1). The control voltage $Ctrl$ is then applied to all the BA cells exploited for analog design in order to guarantee a well-defined output static voltage of the BA cells in spite of PVT variations [52]. The reference inverter can be thought to be the minimum-sized inverter taken from the standard-cell library. However, since in the context of analog design, minimum-sized inverters exhibit very high mismatch (resulting in unacceptable offset for most analog applications), the reference inverter is here defined as an inverter gate taken from the standard-cell library whose area is the minimum one that allows it to achieve an acceptable matching performance for the specific analog design. For example, referring to a 130-nm CMOS technology, the area of the reference inverter to be used to design standard-cell-based OTAs is typically 10 times larger than the area of the minimum-sized one (e.g., $\times 20$ instead of $\times 2$).

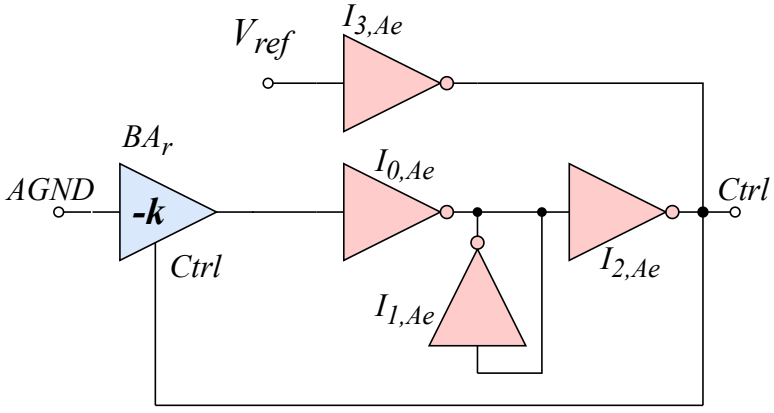

Figure 1. Control loop to generate the control voltage.

3. A Standard-Cell-Based Amplifier Cell with Stable Voltage Gain and Well-Defined DC Output Voltage

In this section, we introduce a novel standard-cell-based analog building block that can be easily designed to exhibit a voltage gain, approximately equal to an integer number

k, which remains stable over PVT variations. Additional requirements of this basic voltage amplifier are to exhibit a well-defined output static voltage to allow easy cascadability and to provide a low output impedance.

The schematic of the proposed standard-cell-based basic voltage amplifier is depicted in Figure 2 and is made up of three inverters, $I_{0,1,2}$, implemented by a certain number of reference inverters. Symbols '1' and 'k' in the left part of Figure 2 indicate the number of instances of the reference standard-cell inverter connected in parallel. In particular, the gain is set by inverter I_0, composed of k reference inverters in parallel, and the diode-connected inverter I_1, which is a single instance, whereas inverter I_2 (also a single instance) is exploited to set the static output voltage through the replica-bias loop of Figure 1. The overall voltage gain V_{om}/V_{ip} of the cell is thus approximately $-k$, hence we adopt for it the symbol in the right part of Figure 2, where the label $-k$ indicates the voltage gain and where the pin *Ctrl* is the bias control input. We would like to point out that one important feature of the proposed standard-cell-based basic voltage amplifier is that its gain is set (at least as a first order approximation) by the number of reference inverters in parallel used to implement the inverter I_0 in Figure 2, and it is therefore technology independent.

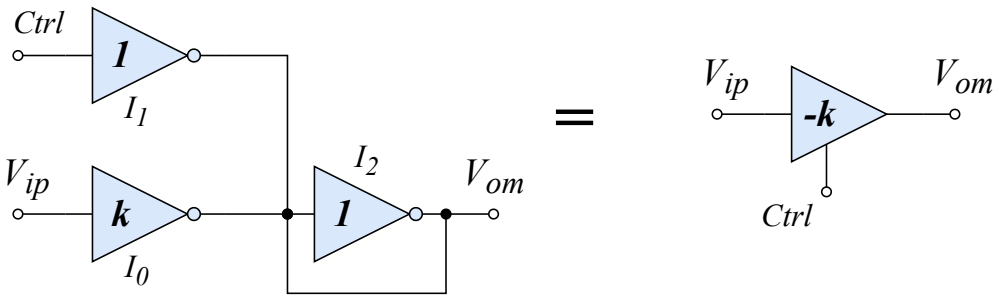

Figure 2. Standard-cell-based basic voltage amplifier with stable gain and well-defined static output voltage.

The proposed basic voltage amplifier can be analyzed by referring to the small-signal equivalent circuit reported in Figure 3, where:

$$Gm_i = gm_0; \tag{1}$$

$$Ro_i = \frac{1}{gm_2 + gds_2 + gds_0 + gds_1}; \tag{2}$$

$$Ci_i = C_{gs_0} + C_{gd_0} \cdot \frac{gm_0}{gm_2}; \tag{3}$$

$$Co_i = C_{gd_0} + C_{gd_1} + C_{gd_2} \tag{4}$$

are the transconductance, the output resistance, the input capacitance, and the output capacitance of the amplifier, respectively. Small-signal parameters $gm_{0,1,2}$, $gds_{0,1,2}$, $C_{gd_{0,1,2}}$, and $C_{gs_{0,1,2}}$ of the inverter gates are expressed as in [52].

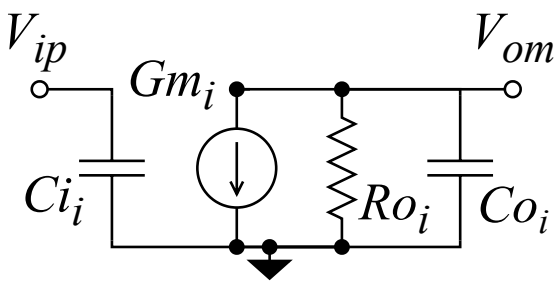

Figure 3. Small-signal equivalent circuit of the proposed standard-cell-based basic voltage amplifier.

Remembering that I_0 is implemented as k instances in parallel in the reference inverter and I_1 is a single instance of the reference inverter, we can write:

$$gm_0 = k \cdot gm_1 \ = k \cdot gm \tag{5}$$

$$gds_0 = k \cdot gds_1 = k \cdot gds; \tag{6}$$

$$C_{gs_0} = k \cdot C_{gs_1} = k \cdot C_{gs}; \tag{7}$$

$$C_{gd_0} = k \cdot C_{gd_1} = k \cdot C_{gd}; \tag{8}$$

where gm, gds, C_{gs}, and C_{gd} denote the transconductance, the output conductance, the gate–source capacitance, and the gate–drain capacitance of the reference inverter, respectively. Now, considering the small-signal equivalent circuit in Figure 3 and assuming a generic load capacitance C_{L_i} at the output of the amplifier, the transfer function of the proposed basic amplifier can be expressed as:

$$Av(s) = -\frac{Gm_i \ Ro_i}{1 + s \ [Co_i + C_{L_i}] \ Ro_i}. \tag{9}$$

It has to be remarked that the proposed amplifier shows a low output impedance Ro_i whose value is approximately determined by Gm_2. The voltage gain of the amplifier is given by $Av(0) = Gm_i \ Ro_i$ and can be written as:

$$Av(0) = Gm_i \ Ro_i \ = \frac{gm_0}{gm_2 + gds_2 + gds_0 + gds_1}. \tag{10}$$

Assuming $gm_2 \gg gds_2 + gds_0 + gds_1$, $|Av(0)|$ can be expressed as:

$$|Av(0)| = Gm_i \ Ro_i \ \approx \frac{gm_0}{gm_2} \approx \frac{kgm}{gm} = k. \tag{11}$$

This condition can be considered true until k is not high enough to compromise the assumption $gm_2 \gg gds_2 + gds_0 + gds_1$. For larger values of k, the following expression has to be considered:

$$Av = \frac{k \ gm}{(k+2)gds + gm} = \frac{k}{1 + (k+2)gds/gm} \tag{12}$$

which, denoting with $Av_{inv} = gm/gds$ the intrinsic voltage gain of the reference inverter, can be rewritten as:

$$Av = \frac{k}{1 + (k+2)/Av_{inv}}. \tag{13}$$

It is evident from the above equation that the voltage gain of the proposed basic amplifier approaches k only if $(k+2)/Av_{inv} \ll 1$. Hence, the limit of the approach is related to the intrinsic gain of the reference inverter, which is technology-dependent and tends to become lower and lower for short-channel CMOS technologies. In order to account for this issue, in the following we consider values of k that satisfy the relation:

$$Av_{inv} \gg k + 2. \tag{14}$$

Since Av_{inv} is typically on the order of 10 V/V in modern CMOS technologies, Equation (14) is not appropriate even for low values of k, and the more accurate Equation (12) should be preferred.

Another important feature of the amplifier in Figure 2 is that, due to its low output resistance, it can be cascaded several times to achieve high voltage gain without requiring

frequency compensation, as will be better shown in the following. Indeed, the dominant pole of the proposed amplifier is given by:

$$p_i = -\frac{1}{\tau_{p_i}} = -\frac{1}{[Co_i + C_{L_i}]\, Ro_i} \tag{15}$$

and is a high-frequency pole since Co_i, Ro_i, and C_{L_i} are low (C_{L_i} coincides with Ci_i when several basic amplifiers are cascaded). As a consequence, if the value of k is appropriately chosen (i.e., to have parasitic poles far from the gain–bandwidth product of the amplifier), the cascade of several instances of the proposed basic voltage amplifier can be compensated through the output load capacitance, without requiring complex frequency compensation approaches needed in conventional multi-stage amplifiers.

4. The Proposed Inverter-Based D2S Converter with Enhanced Common Mode Rejection

Inverter-based OTAs require a differential-to-single-ended (D2S) converter that determines the overall common mode rejection ratio (CMRR) and input common mode range (ICMR) of the amplifier. In the context of inverter-based OTAs, the conventional approach to implement the D2S converter exploits an inverter that drives another inverter whose input and output terminals are connected to each other, thus obtaining a voltage gain approximately equal to -1 [59]. However, due to the poor matching and the low intrinsic gain of the inverters, this approach results in poor CMRR performance and high sensitivity to PVT variations if the bias point is not properly stabilized. Recently, a novel topology of an inverter-based D2S converter, exploiting an auxiliary, standard-cell-based, error amplifier, and a local feedback loop, was presented by the authors in [33]. The D2S in [33] exhibits higher CMRR, improved ICMR, and better robustness with respect to PVT variations than the conventional inverter-based D2S.

In this paper, to further improve the CMRR and robustness to PVT variations, we propose an enhanced version ($D2S_E$) of the D2S in [33], whose schematic is depicted in Figure 4. In particular, the proposed $D2S_E$ exploits the two-stage standard-cell-based error amplifier reported in Figure 5 to boost the gain of the feedback loop with respect to the previous version. As further modifications, we have also added the inverters I_7 and I_8 to accurately set the output static voltage of the $D2S_E$ and to provide a low-output impedance as discussed in Sections 2 and 3. The factor h in the inverters $I_{3,4,5,6}$ in Figure 4 denotes the number of reference inverters in parallel used to implement each one of the inverters $I_{3,4,5,6}$, whereas, referring to Figure 5, the factor g in the inverters $I_{e0,e1,e2,e3,e5}$ denotes the number of reference inverters in parallel used to implement each one of the inverters $I_{e0,e1,e2,e3,e5}$.

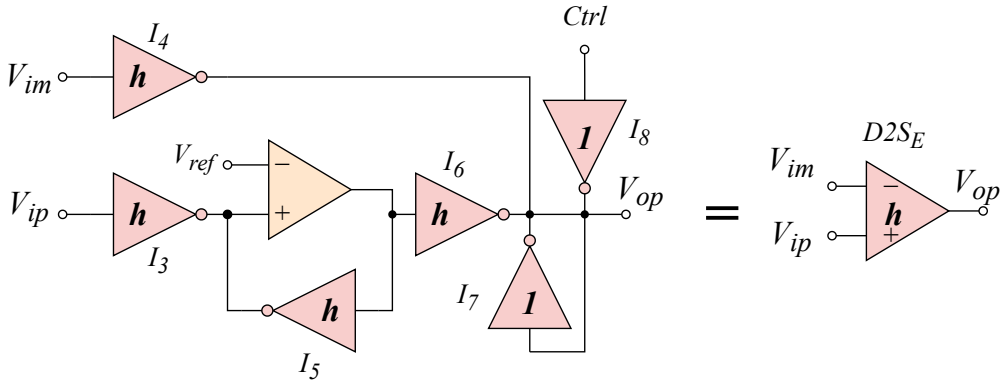

Figure 4. Standard-cell D2S converter with enhanced common mode rejection.

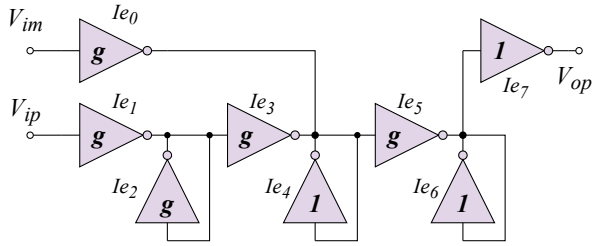

Figure 5. Standard-cell inverter-based error amplifier with improved gain.

The gain of the proposed improved error amplifier can be computed as:

$$Av_{err}(s) \approx \frac{gm_{e_0}}{gds_{e_0}+gds_{e_3}+gds_{e_4}+gm_{e_4}} \cdot \frac{gm_{e_5}}{gds_{e_5}+gds_{e_6}+gm_{e_6}} \cdot \frac{gm_{e_7}}{gds_{e_7}} \cdot \\ \cdot 1 \Big/ \left(1+s\frac{Cgs_{e_4}+Cgd_{e_0}+Cgd_{e_3}}{gm_{e_4}}\right) \cdot 1 \Big/ \left(1+s\frac{Cgs_{e_6}+Cgd_{e_5}+Av_{e_7}Cgd_{e_7}}{gm_{e_6}}\right) \\ \cdot 1 \Big/ \left(1+s\frac{C_L+Cgd_{e_7}}{gds_{e_7}}\right) \quad (16)$$

and, considering the definition of g, it can be rewritten as:

$$Av_{err}(0) = \left(\frac{g}{1+(2+g)/Av_{inv}}\right)^2 Av_{inv}. \quad (17)$$

It has to be remarked that the proposed two-stage error amplifier does not require any internal compensation if its load capacitance (i.e., the sum of the input capacitances of I_5 and I_6 in Figure 4) is high enough to guarantee a good phase-margin in the range of operation of the OTA.

The frequency response of the proposed $D2S_E$ converter can be derived as follows:

$$Av(s) = \frac{gm_4}{gm_7+gds_7+gds_4+gds_8+dsg_6} \cdot \frac{1}{1+s\frac{Cgs_7+Cgd_6+Cgd_8+C_L}{gm_7+gds_7+gds_4+gds_8+gds_6}} \quad (18)$$

and, remembering the definition of the factor h, the dc differential gain can be simplified as:

$$Av(0) = h \cdot \frac{gm}{gm+(3+h)gds} = \frac{h}{1+(3+h)/Av_{inv}}. \quad (19)$$

By following the same aprroach reported in [33], the CMRR of the proposed $D2S_E$ can be derived as:

$$CMRR = \left(\frac{g}{1+(2+g)/Av_{inv}}\right)^2 \cdot \frac{Av_{inv}^2}{2}. \quad (20)$$

5. Proposed Standard-Cell-Based ULV OTA Architecture

The proposed standard-cell-based OTA architecture is depicted in Figure 6 and is composed of the $D2S_E$ reported in Figure 4 and by a multi-stage transconductor ($-Gm_B$) that exploits the cascade of two basic voltage amplifiers as shown in Figure 7. A very important feature of the proposed OTA architecture is to have a single high-impedance node that allows for dominant pole compensation through the load capacitance C_L, as explained in detail in [52,62]. To achieve this feature, the transconductor $-Gm_B$ is made up of the cascade of two basic voltage amplifiers, exploited to boost the voltage gain without introducing high impedance nodes (see Figure 7), followed by the conventional inverter I_9. The transconductance gain of the block $-Gm_B$ depends on the factor k of the basic voltage amplifiers and on the sizing of the inverter I_9 in Figure 7.

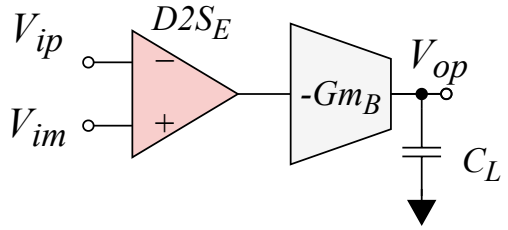

Figure 6. Architecture of the proposed standard-cell-based ULV OTA.

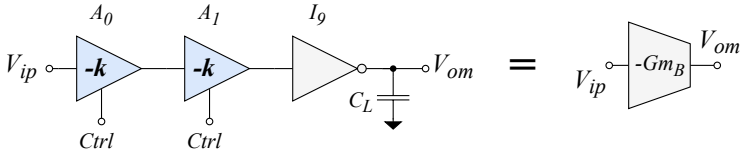

Figure 7. Implementation of the transconductor $-Gm_B$ in Figure 6.

5.1. Analytical Model and Design Guidelines

The transfer function of the $-Gm_B$ block can be derived as follows:

$$Gm_B = \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot gm_9 \cdot \left(\frac{1}{1+s\frac{(k+1)\cdot(Cgd+Cgs)}{gm+(k+2)\cdot gds}}\right)^2. \tag{21}$$

Thus , also considering Equation (18) and the definition of k, h, and g, it can be derived that:

$$Av(s) = \frac{h}{1+(3+h)/Av_{inv}} \cdot \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot Av_{inv} \cdot \\ \cdot \frac{1}{\left(1+s\frac{(k+1)\cdot(Cgd+Cgs)}{gm+(k+2)\cdot gds}\right)^2} \cdot \frac{1}{\left(1+s\,\frac{Cgs(1+k)+Cgd(1+h)}{gm+2\cdot gds(1+h)}\right)} \cdot \frac{1}{\left(1+s\frac{C_L}{gds}\right)}, \tag{22}$$

which results in a dc voltage gain expressed by the following equation:

$$Av(0) = \frac{h}{1+(3+h)/Av_{inv}} \cdot \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot Av_{inv}, \tag{23}$$

where gm, gds, C_{gs}, and C_{gd} are the small-signal parameters of the reference inverter as discussed in Section 3. Thus, it is clear that, given the four poles of the architecture, the one set by the load capacitance and the output impedance of inverter I_9 is the dominant one, and the gain–bandwidth product (GBW) of the OTA can be expressed as:

$$GBW = \frac{1}{2\pi} \cdot \frac{h}{1+(3+h)/Av_{inv}} \cdot \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot M \cdot \frac{gm}{C_L} \tag{24}$$

where M denotes the ratio gm_9/gm.

The phase margin of the OTA can be computed as:

$$m\varphi = 180 - \arctan\left\{\frac{h}{1+(3+h)/Av_{inv}} \cdot \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot M \cdot Av_{inv}\right\} + \\ - 2 \cdot \arctan\left\{\frac{h}{1+(3+h)/Av_{inv}} \cdot \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot \frac{(k+1)\cdot(Cgd+Cgs)}{1+(k+2)/Av_{inv}} \cdot \frac{M}{C_L}\right\} + \\ - \arctan\left\{\frac{h}{1+(3+h)/Av_{inv}} \cdot \left(\frac{k}{1+(k+2)/Av_{inv}}\right)^2 \cdot \frac{Cgs(1+k)+Cgd(1+h)}{1+2\cdot gds(1+h)/Av_{inv}} \cdot \frac{M}{C_L}\right\}. \tag{25}$$

Since Equations (22)–(25) form a system of three equations in the three variables h, k, and M, starting from specific constraints in terms of voltage gain, gain–bandwidth product, and phase margin, it is possible to determine the values of h, k, and M for a given load capacitance C_L. In other words, once the value of the load capacitor C_L is set, design parameters can be chosen to address the trade-off between small-signal and large-signal performances of the OTA in terms of the well-known figures of merit FOM_S and FOM_L [33,39,52,63] by exploiting Equations (22)–(25).

6. Design of the Standard-Cell-Based ULV OTA

In order to validate the analytical models and illustrate the application of the design guidelines outlined in the previous section, we present the design of a ULV standard-cell-based OTA according to the architecture reported in Figure 6, referring to the standard-cell library of a 130-nm CMOS technology provided by STMicroelectronics.

6.1. Simulation of the Standard-Cell-Based Basic Voltage Amplifier in ULV Conditions

As a first step, we have carried out some preliminary simulations on the proposed standard-cell-based basic voltage amplifier depicted in Figure 2, assuming a supply voltage V_{DD} of 0.3 V and considering different values of the factor k ranging from 1 to 13. The voltage gain of the voltage amplifier as a function of k is reported in Figure 8, where the ideal values obtained assuming $gds = 0$ (Equation (11)) are reported in green, the values obtained from Equation (13) are reported in blue, and the values obtained from simulations are depicted in red. Results in Figure 2 both highlight the effect of gds, which limits the intrinsic gain of the inverter in short-channel CMOS technologies, and confirm the accuracy of Equation (13).

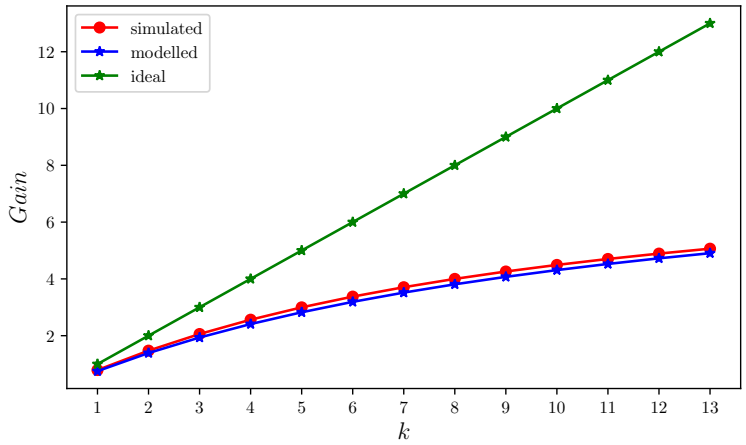

Figure 8. Voltage gain of the proposed standard-cell-based basic voltage amplifier as a function of k. Ideal values obtained assuming $gds = 0$ (Equation (11)) are reported in green, the values obtained from Equation (13) are reported in blue, and the values obtained from simulations are depicted in red.

6.2. Design Flow

The OTA of Figure 6 has been designed and simulated in the Cadence environment considering the 130-nm CMOS standard-cell library from STMicroelectronics. The reference inverter assumed to implement the control loop of Figure 1 and the circuits in Figures 2, 4, and 7 is the $\times 20$ of the standard-cell library (i.e., 10 times larger than the minimum-sized inverter of the standard-cell library), whereas the reference inverter assumed to implement the error amplifier in Figure 5 is the $\times 2$ (i.e., the minimum-sized inverter of the standard-cell library).

To illustrate the design of the proposed standard-cell-based OTA, we exploited Equations (22)–(25) assuming a load capacitance C_L = 150 pF and considering $m\varphi \approx 52$ deg in order to guarantee stability. As further design constraints, we have assumed a GBW of

10 MHz and a gain of 50 dB. From these constraints, the values of g, h, k, and M have been found according to the guidelines given in Section 5.1, and they are reported in Table 1.

Table 1. Design parameters of the proposed standard-cell-based ULV OTA.

	g	h	k	M
Reference inverter	×2	×20	×20	×20
Value	6	6	6	11

6.3. Automatic Layout Flow within the Cadence Innovus Tool

The schematic of the OTA in Figure 6, made up of several ×2 and ×20 inverter gates taken from the standard-cell library, has been coded in structural Verilog. The Verilog netlist has then been imported in the Cadence Innovus tool, together with the technology files needed for the automatic place-and-route flow. A simplified non-timing-driven place-and-route flow consisting of the design import, floorplanning, placement, and routing steps performed automatically through *tcl* scripts was then carried out to generate the layout shown in Figure 9. The area of the OTA is about 598 μm^2 (width = 30.34 μm, length = 19.68 μm). To improve the matching of standard-cells implementing the input stage, the input pins have been placed close to each other at floorplan stage, thus driving the place-and-route tool to place the standard cells of the input stage close to each other.

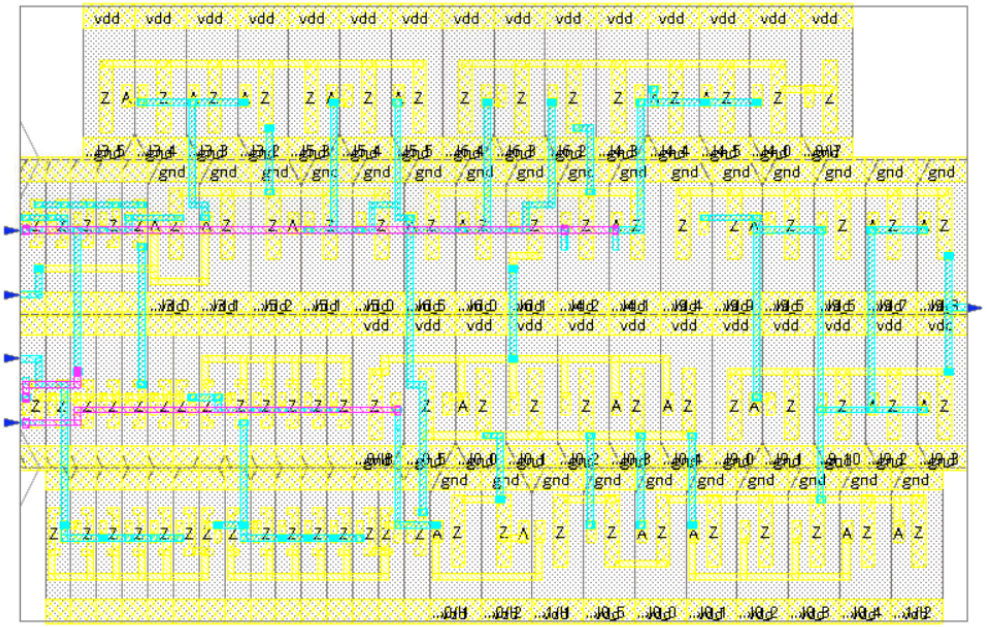

Figure 9. Layout of the OTA generated automatically with the Cadence Innovus place-and-route tool.

7. Simulations of the Proposed Standard-Cell-Based ULV OTA

Figure 10 shows the frequency response of the proposed OTA in different working conditions: the open-loop differential gain is depicted in blue and, as can be observed, its dc value is about 50 dB, whereas the phase margin is about 55 deg. Concerning the common mode voltage gain, it is depicted in green, and its dc value is about 7.4 dB, thus showing a CMRR at dc around 43 dB. The frequency response of the OTA in closed-loop unity-gain configuration is reported in orange in Figure 10.

Figure 11 shows the transient response to a rail-to-rail input pulse in unity–gain configuration, where the input is depicted in orange while the output voltage is in blue. As it can be observed, the slew rate (SR) is quite symmetric and amounts to about 631.4 and 811.3 V/ms, respectively, for positive and negative slew rates (SR_p, SR_n).

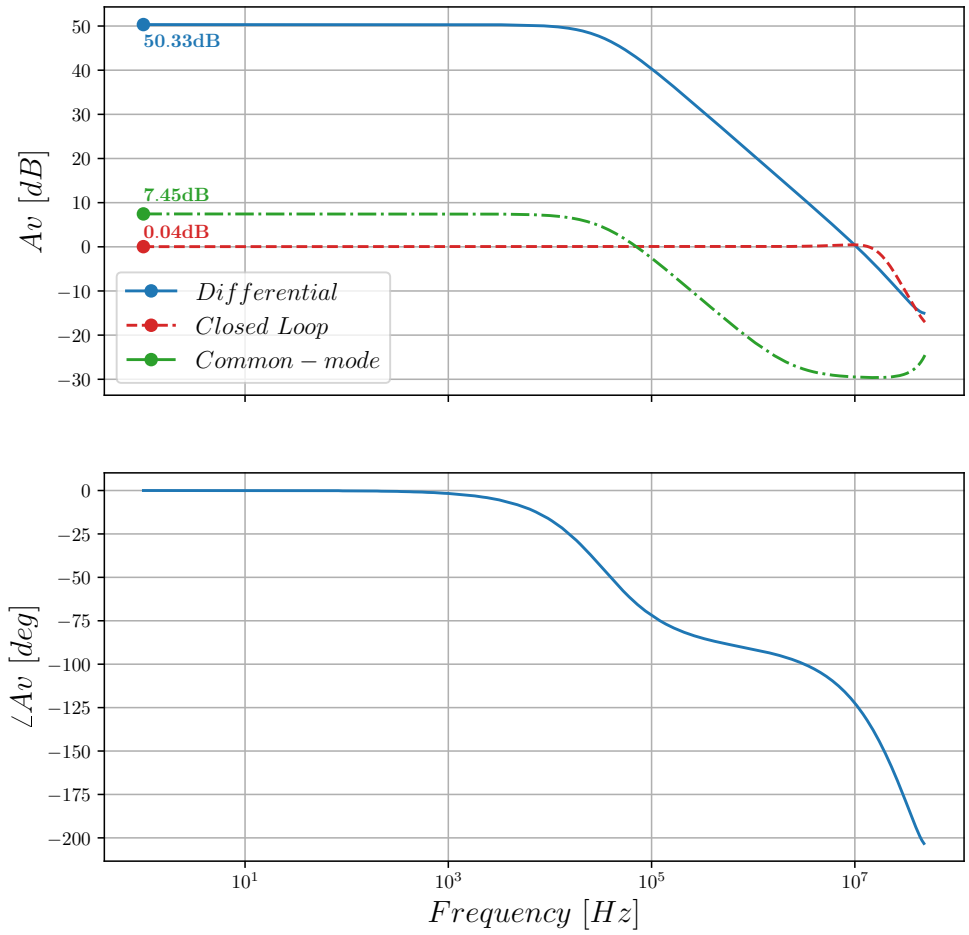

Figure 10. Frequency response of the proposed OTA: open-loop differential gain in blue, open-loop common mode gain in green, and closed-loop gain in unity–gain configuration in orange.

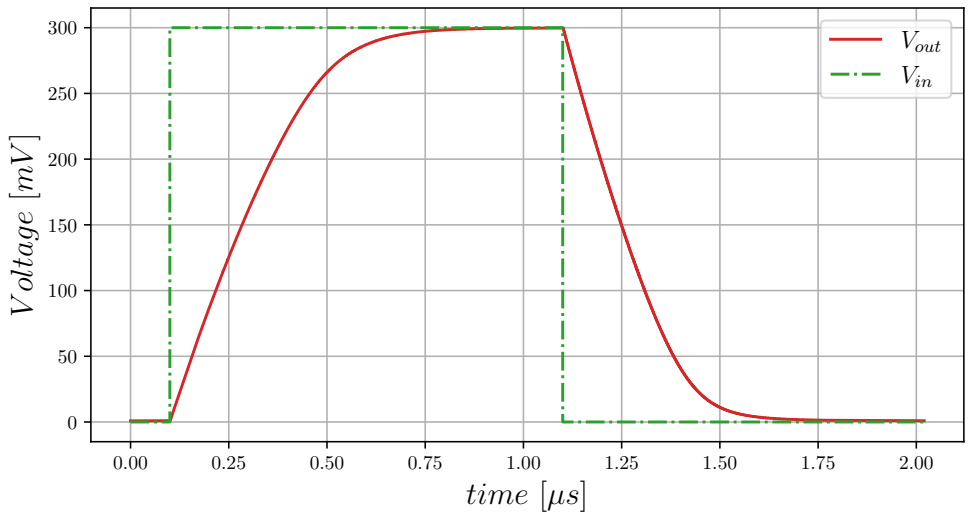

Figure 11. Transient response to a rail-to-rail input pulse in unity–gain configuration: output voltage in blue and input voltage in orange.

Simulations in the Different PVT Conditions

The main performance parameters of the proposed ULV standard-cell-based OTA have been simulated in the different process corners, and results are summarized in Table 2. The total harmonic distorsion (THD) has been evaluated by using transient simulations

and exploiting the "THD" function in the Cadence Virtuoso environment for a sinusoidal input with a frequency of 100 Hz and an amplitude of 240 mV (i.e., 80% of the rail-to-rail input swing).

Table 2. Performance of the proposed OTA in the different process corners.

Parameter	TT	FF	SS	FS	SF
A_{V_D} [dB]	50.33	46.38	53.72	50.58	49.4
A_{V_C} [dB]	7.45	8.27	8.36	25.51	13.11
GBW [MHz]	10.4	16.45	6.84	10.65	9.73
$m\varphi$ [deg]	56.33	63.6	49.46	56.38	59.39
P_D [µW]	12.09	26.21	6.23	13.44	12.41
$Offset$ [mV]	−2.2	−3.7	−1.93	−10.72	6.32
SR_p [V/ms]	631.4	1.044 k	396.5	425.6	863.7
SR_m [V/ms]	811.3	1.407 k	504.2	1.008 k	569.6
THD [%]	0.24	0.28	0.26	0.99	0.95

As it can be observed, both the differential and the common mode gains, as well as the offset and the phase margin, are stable with respect to the different corners. The worst case common mode gain degradation is in the cross corner FS and is probably due to variations in the dc operating points not completely compensated by the replica–bias loop in the FS corner. Since bias currents are not accurately set (current sources are not available in a standard-cell flow), the power consumption varies in accordance with threshold voltage variations of PMOS and NMOS devices of the inverter, resulting in not very stable GBW, SR, and power dissipation P_D, which all are strongly dependent on the bias current of the inverters. The OTA has also been tested under voltage and temperature variations, and results are reported in Table 3. Similar considerations as for Table 2 can be made in this case as well. Indeed, PVT variations have an impact on the GBW, the P_D, and the $SR_{p,m}$.

Table 3. Performance of the proposed OTA in the different supply voltage and temperature conditions.

Parameter	Voltage Variations		Temperature Variations	
T [°C]	27	27	0	80
V_{DD} [mV]	270	330	300	300
A_{V_D} [dB]	49.2	51.19	51.38	48.14
A_{V_C} [dB]	6.32	8.32	11.69	1.061
GBW [MHz]	6.73	15.57	6.59	19.68
$m\varphi$ [deg]	54.13	54.13	54.31	60.32
P_D [µW]	19.6	19.6	6.59	30.45
$Offset$ [mV]	−2.3	−2.32	−2.54	−1.65
SR_p [V/ms]	367.2	1.04 k	488.8	1.006 k
SR_m [V/ms]	464.5	1.33 k	614	1.178 k
THD [%]	0.27	0.20	0.33	0.07

At this point, we want to remark that one intrinsic limit of the standard-cell approach is that, as discussed in the literature [33,52], it does not allow us to accurately set dc currents without additional custom circuitry (see [59]) operating at a higher supply voltage. Thus, performance parameters that depend on the bias current vary in accordance with threshold voltage variations over PVT fluctuations. However, we want to remark that, despite variations with respect to nominal conditions, the proposed OTA can work over all PVT corners, guaranteeing a gain always greater than 48 dB, a reasonable offset voltage, and also a good phase margin.

These results confirm the limits of standard-cell-based OTAs [33,51,52] which, even if allowed to aggressively scale the supply voltage [34,64,65], to strongly reduce the silicon area footprint, and to allow an automatic layout flow (thus shortening the time-to-market), end up somewhat sensitive to PVT variations, especially if compared with ULV full-custom-designed amplifiers [10,11] which, on the other hand, exhibit a larger area, longer design

time, and high effort for the layout step.

Robustness of the proposed ULV standard-cell-based OTA to mismatch variations has been tested by means of Monte Carlo simulations, and results are summarized in Table 4. Results in Table 4 show that the proposed OTA is very robust to mismatch variations. Indeed, the differential gain is always good and close to the nominal one, as well as the GBW, the phase margin, the P_D, and also slew rate performance. However, the common mode gain ends up being quite different from the nominal one. This is due to the fact that, in nominal conditions, the gm_i of the inverters in the $D2S_E$ block are well-matched and thus current cancellation is very accurate, whereas under mismatch variations the accuracy of the current cancellation in the D2S converter is degraded.

Table 4. Performance of the proposed OTA under mismatch variations.

Parameter	Typical	Mean	Std
A_{V_D} [dB]	50.33	50.24	1.12
A_{V_C} [dB]	7.45	16	9.12
GBW [MHz]	10.4	10.56	1.23
$m\varphi$ [deg]	56.33	55.92	3.54
P_D [µW]	12.09	12.47	0.2
$Offset$ [mV]	−2.2	−2.12	3.94
SR_p [V/µs]	631.4	634	21.97
SR_m [V/µs]	811.3	824.4	42.91
THD [%]	0.24	0.27	0.05

8. Comparison

The small-signal and large-signal Figures of Merit (FOM_S and FOM_L) are very popular metrics for comparing OTAs. However, these metrics do not take into account the area footprint of the amplifiers. Therefore the area-normalized $FOM_{S,A}$ and $FOM_{L,A}$ have been proposed in [39] to allow for a more comprehensive comparison. These FOMs are defined as:

$$FOM_{S,A} = \frac{GBW \cdot C_L}{P_D \cdot Area}; \quad FOM_{L,A} = \frac{SR_{avg} \cdot C_L}{P_D \cdot Area}. \tag{26}$$

The proposed OTA has been compared against several ULV (i.e., operating with a supply voltage as low as 0.3 V) OTAs from the literature, and the results of this comparison are reported in Table 5. The proposed amplifier results in the highest FOM_S and $FOM_{S,A}$ outperforming all the other ULV OTAs. In addition, it exhibits the highest dc gain among the standard-cell-based OTAs. Large-signal performance is in line with the state of the art. Indeed, the FOM_L and $FOM_{L_{wc}}$ of the proposed OTA are higher than the ones in [33,51], whereas they are comparable with those shown by [11,12,66]. Power consumption of the proposed OTA is relatively high, and this is mainly due to two main reasons: (1) the usage of non-minimum-sized standard cells to minimize the offset standard deviation under mismatch variations; (2) the adoption of a standard-cell library built with the low threshold voltage transistors of the technology (which allow us to achieve the best GBW). If higher offset and lower GBW are acceptable for the application, wherein the minimization of power consumption is the most important design goal, the following strategies can be combined: (1) reduce the size of the reference standard-cell; (2) choose the standard-cell library built with the high-threshold voltage transistors (recent CMOS technologies typically offer two or three threshold voltage options); (3) further reduce the supply voltage.

Table 5. Comparison table.

	Automatic Layout Flow Available			**Automatic Layout Flow Not Available**			
	This Work †	[33] †	[51] †	[39] ‡*	[11] †	[12] ‡*	[66] ‡*
Year	2023	2022	2022	2021	2022	2020	2018
Technology [µm]	0.13	0.13	0.13	0.18	0.13	0.18	0.18
V_{DD} [V]	0.3	0.3	0.3	0.3	0.3	0.3	0.3
DC_{gain} [dB]	50.33	34.97	28.3	30	52.92	64.7	65.8
C_L [pF]	150	2	1.5	150	50	30	20
GBW [kHz]	10.40 k	12.69 k	15.42 k	0.25	35.16	2.96	2.96
$m\varphi$ [deg]	56.33	62.56	54	90	52.40	52	61
SR_p [V/ms]	631.4	4.54 k	9.08 k	-	18.61	1.9	6.44
SR_n [V/ms]	811.3	6.82 k	9.08 k	-	11.51	6.4	7.8
SR_{avg} [V/ms]	721.35	5.68 k	9.08 k	0.085	15.06	4.15	7.12
THD [%]	0.24	3.38	3	2	0.67	1	1
% of input swing	80	90	80	90	90	85	93.33
$CMRR$ [dB]	42.88	27.08	41.07	41	42.11	110	72
P_D [nW]	12.09 k	6.10 k	4.41 k	2.4	21.89	12.6	15.4
Mode	STD-CELL	STD-CELL	STD-CELL	DIGITAL	BD	BD	BD
FOM_S $[\frac{\text{MHz}\cdot\text{pF}}{\text{mW}}]$	**128.2 k**	4.16 k	5.25 k	15.89 k	80.29 k	7.05 k	3.61 k
FOM_L $[\frac{\text{V}\cdot\text{pF}}{\mu\text{s}\cdot\text{mW}}]$	8.949 k	1.86 k	3.09 k	5.40 k	**34.40 k**	9.88 k	9.25 k
$FOM_{L_{WC}}$ $[\frac{\text{V}\cdot\text{pF}}{\mu\text{s}\cdot\text{mW}}]$	7.833 k	1.49 k	3.09 k	-	**26.30 k**	4.52 k	8.36 k
$Area$ $[\mu\text{m}^2]$	598	217.85	**164**	982	5200	8500	8200
$FOM_{S,A}$ $[\frac{\text{MHz}\cdot\text{pF}}{\text{mW}\cdot\mu\text{m}^2}]$	**214.38**	19.10	32.01	16.18	15.44	0.83	0.4
$FOM_{L,A}$ $[\frac{\text{V}\cdot\text{pF}}{\mu\text{s}\cdot\text{mW}\cdot\mu\text{m}^2}]$	14.96	8.54	**18.84**	5.50	6.62	1.16	1.13
$FOM_{L_{wc},A}$ $[\frac{\text{V}\cdot\text{pF}}{\mu\text{s}\cdot\text{mW}\cdot\mu\text{m}^2}]$	13.10	6.84	**18.84**	-	5.06	0.53	1.02

† Simulated; ‡ Measured; * The automatic layout flow of [39] is not allowed on all the standard-cell libraries.

9. Conclusions

In this paper, we have presented an improved standard-cell-based differential-to-single-ended converter and a novel standard-cell-based basic voltage amplifier. These building blocks have been exploited to implement a standard-cell-based ULV OTA with state-of-the-art performances. The layout of the OTA has been implemented by using a fully automated place-and-route flow by using the Cadence Innovus tool and starting from the Verilog netlist of the circuit. Simulation results have shown a dc gain of 50 dB with a gain–bandwidth product of 10 MHz with a 150 pF load capacitance. The THD, simulated at a frequency of 100 Hz and with an amplitude equal to 80% of the rail-to-rail input swing, has ended up as low as 0.24%, showing very good linearity performance for a ULV standard-cell-based OTA. Compared to other ULV OTAs from the literature, the proposed OTA exhibits FOMs of about 128,000 $\frac{\text{MHz}\cdot\text{pF}}{\text{mW}}$, with an area footprint of only 598 μm^2, resulting in the best values for both FOM_S and $FOM_{S,A}$.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-Digital Converter
BA	Basic Amplifier
BD	Body-Driven
D2S	Differential-to-Single-Ended
DIGOTA	Fully-Digital Operational Transconductance Amplifier
CMRR	Common Mode Rejection Ratio
EDA	Electronic Design Automation
FOM	Figure Of Merit
GBW	Gain-Bandwidth Product
IC	Integrated Circuit
ICMR	Input Common Mode Range
IoT	Internet-of-Things
OTA	Operational Transconductance Amplifier
PVT	Process, Supply Voltage and Temperature
THD	Total Harmonic Distortion
SR	Slew Rate
ULV	Ultra-Low Voltage

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