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A Differential-to-Single-Ended Converter Based on Enhanced Body-Driven Current Mirrors Targeting Ultra-Low-Voltage OTAs

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Abstract: In this work, an ultra-low-voltage (ULV) technique to improve body-driven current mirrors is proposed. The proposed technique is employed to improve the performance of conventional differential-to-single-ended (D2S) converters which at these low voltages suffer from a low common-mode rejection ratio (CMRR). In addition, the technique aims to improve the performance of the conventional D2S also under a large signal swing and with respect to the process, voltage and temperature (PVT) variations, resulting in a very low distortion, high current mirror accuracy and robust performance. An enhanced body-driven current mirror was designed in a 130 nm CMOS technology from STMicroelectronics and an exhaustive campaign of simulations was conducted to confirm the effectiveness of the strategy and the robustness of the results. The enhanced D2S was also employed to design a ULV operational transconductance amplifier (OTA) and a comparison with an OTA based on a conventional D2S was provided. The simulation results have shown that the proposed enhanced D2S allows achieving the ULV OTAs with a CMRR and a PSRR which are 18 and 9 dB higher than the ones obtained with the conventional D2S topology, respectively. Moreover, the linearity performance is also improved as shown by the THD, whose value is decreased of about 5 dB.

Keywords: operational transconductance amplifier; ultra-low voltage; ultra-low power; body driven; current mirrors; differential to single ended

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1. Introduction

Recent years have seen a growing diffusion of electronic systems for portable biomedical applications [1–5], smart sensors [6–9] and, in general, for applications in the field of the Internet of Things (IoT) [10–12]. These systems are usually powered by batteries or by energy harvested from the environment: this requires minimizing not only the power dissipation, to extend the battery life, but also the supply voltage, because energy harvesting systems are able to provide voltages in the hundreds of mV range [13]. As a consequence, the research in the field of ultra-low-voltage (ULV) and ultra-low-power (ULP) electronics has received a strong boost [14–17].

The operational transconductance amplifier (OTA) is a key functional block for analog applications and is one of the most challenging blocks to design in a ULV/ULP context. The extremely reduced supply voltage prevents the use of the tail generator in the differential pairs [18] and requires to exploit to the full extent the limited available voltage swing. The main problems to cope with are therefore to provide a well-controlled bias point [19,20]; to provide a robust performance against the process, supply voltage and temperature (PVT) variations and mismatches [21,22]; and to maximize the input common-mode range (ICMR) [23–25] and the common-mode rejection ratio (CMRR) [26]. The absence of the tail generator in fact affects not only the bias point but also the CMRR that therefore relies exclusively on topological choices.

An approach where the OTA behavior is emulated in the digital domain (DIGOTA) was proposed in the literature [27–29]. More common and conventional approaches exploit inverter-based stages [30–37], floating-gate devices [38–40] or the use of body contacts as input terminals (body driving) [19,23–25,41–55] to design OTAs with a rail-to-rail ICMR. Body-biasing techniques [15], where the body terminals are exploited to set the bias point, were proposed in substitution of the tail generator, but in a ULV context, the extremely low voltage swing does not allow to counteract the effect of the PVT variations, due also to the limited body transconductance [50]. On the other hand, for very low supply voltages, below the turn-on voltage of bipolar junctions, a rail-to-rail swing can be applied to the body terminals used as inputs so that the gate terminals remain available to set a robust bias point.

In the absence of a tail generator, the CMRR is provided by the use of common-mode feedback (CMFB) loops, for fully differential stages [19,32,36,44,54,56], or by the differential-to-single-ended (D2S) converter [37], usually designed loading a (pseudo)differential pair with a current mirror. Ideally, the current mirror provides unity gain, yielding an infinite CMRR; in practice, the CMRR is inversely proportional to the gain error of the current mirror. A standard current mirror, with a diode-connected device (the drain is connected to the gate) on the input side, provides a CMRR that is proportional to the intrinsic gain $g_m r_{ds}$ of the devices, around 20 dB in modern deep submicron technologies. Modern CMOS technologies are usually triple-well or FDSOI (fully depleted Silicon on insulator), thus making available body contacts both for NMOS and PMOS devices. A body-driven current mirror (BD-CM) [57], with the drain of the input device connected to the body terminal, allows exploiting the gate terminals for biasing but provides a very low CMRR, because the body transconductance is lower than the gate transconductance.

A body-driven current mirror, whose performance is enhanced exploiting an auxiliary amplifier to lower the input impedance and to accurately match the drain-source voltages of the two transistors of the current mirror, is presented in this paper. When the enhanced body-driven current mirror is used to design a D2S stage, these features result in an improved CMRR, which becomes one order of magnitude higher than the one provided by a conventional body-driven current mirror. Furthermore, the proposed topology improves the linearity performance of the D2S under a large signal swing and increases the robustness with respect to the PVT variations. A simple two-stage OTA, composed of a D2S exploiting the proposed mirror and a body-driven inverter, is designed and simulated in a commercial 130 nm CMOS technology to highlight the advantages of the novel topology over the conventional one.

The paper is structured as follows: Section 2 presents the enhanced body-driven current mirror topology, and Section 3 uses it to design a high-CMRR D2S circuit. The D2S is exploited to design a two-stage OTA in Section 4, whose simulated results are presented in Section 5 and compared with the state of the art. Some conclusions are drawn in Section 6.

2. Proposed Topology of Enhanced Body-Driven Current Mirror

The conventional body-driven current mirror (BD-CM) shown in Figure 1a is made up of two $NMOS$ transistors $M_{n_{1,2}}$ which are gate biased through a bias voltage, namely V_{bias_n}. M_{n_1} has its drain terminal connected to its body to implement a body-diode connection which allows to mirror the input current to the output through the body terminal of M_{n_2}.

The conceptual schematic of proposed enhanced BD-CM is reported in Figure 1b. With respect to the conventional BD-CM, an error amplifier is introduced in the body-diode connection with the aim of lowering the input impedance and improve the mirroring accuracy.

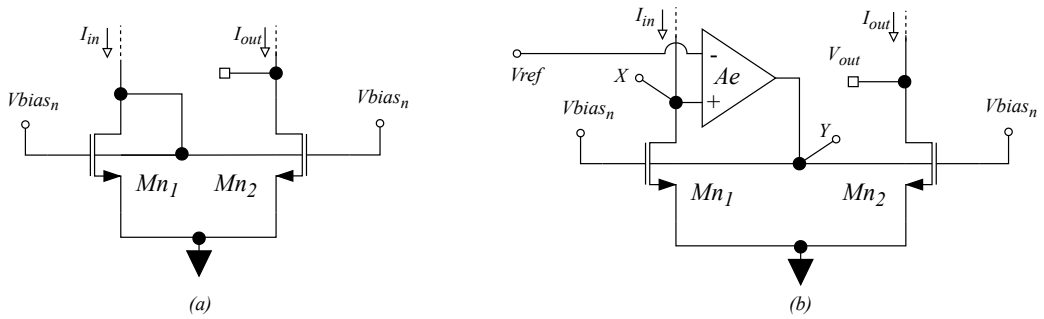

Figure 1. Conventional body-driven current mirror (**a**) and enhanced body-driven current mirror (**b**).

2.1. Comparison between the Conventional Body-Driven Current Mirror and the Proposed Improved One

In this subsection, the conventional BD-CM (Figure 1a) and the proposed enhanced BD-CM (Figure 1b) are compared in terms of input impedance and accuracy of the current gain. For this purpose, referring to the topology of the conventional BD-CM, depicted in Figure 1a, the expression of the input impedance can be easily derived by small-signal analysis as follows:

$$Z_{in_{conv}} = \frac{1}{g_{mb_n}1(1+\frac{g_{ds_{n1}}}{g_{mb_{n1}}})} \frac{1}{1+s\frac{C_{bs_{n1}}+C_{bs_{n2}}+C_{gd_{n1}}+C_{bd_{n2}}\frac{g_{mb_{n2}}}{g_{ds_{n2}}}}{g_{mb_n1}+g_{ds_{n1}}}} \quad (1)$$

where g_{mb}, g_{ds}, C_{bs}, C_{gs} and C_{bd} denote the body transconductance, the output conductance and the body-source, gate-source and body-drain parasitic capacitances of the generic MOS device as usual. Equation (1) clearly shows that, as a first approximation, the input impedance of the conventional BD-CM is about $\frac{1}{g_{mb_{n1}}}$.

The output current I_{out} can then be easily expressed as a function of the input current I_{in} through the following relation:

$$I_{out} = I_{in}\ Z_{in_{conv}}\ g_{mb_{n2}} \quad (2)$$

and thus the current gain A_I of the conventional BD-CM can be derived as follows:

$$A_I = \frac{I_{out}}{I_{in}} = \frac{g_{mb_{n2}}}{g_{mb_{n1}}} \frac{1}{1+\epsilon_{conv}} \frac{1}{1+s\frac{C_{bs_{n1}}+C_{bs_{n2}}+C_{gd_{n1}}+C_{bd_{n2}}\frac{g_{mb_{n2}}}{g_{ds_{n2}}}}{g_{mb_n1}+g_{ds_{n1}}}} \quad (3)$$

where the error term ϵ_{conv} is defined as:

$$\epsilon_{conv} = \frac{g_{ds_{n1}}}{g_{mb_{n1}}} \quad (4)$$

By looking at the above expression of A_I, it is evident that the accuracy of the conventional BD-CM depends mainly on two factors:

1. The value of ϵ_{conv}, which can be minimized if $g_{ds_{n1}}$ is much lower than $g_{mb_{n1}}$;
2. The matching between $g_{mb_{n1}}$ and $g_{mb_{n2}}$.

Then, the input impedance for the proposed enhanced BD-CM can be derived by following a similar approach, as follows:

$$Z_{in_{enh}} = \frac{1}{Ae\ g_{mb_{n1}}(1+\frac{g_{ds_{n1}}}{Ae\ g_{mb_{n1}}})} \frac{1}{1+s\frac{C_{in_{Ae}}+C_{db_{n1}}(1-A_e)+C_{gd_{n1}}}{Ae\ g_{mb_{n1}}+g_{ds_{n1}}}} \tag{5}$$

where Ae is the voltage gain of the error amplifier reported in Figure 1b and $C_{in_{Ae}}$ is the error amplifier input capacitance. Now, considering the following relation at the Y node of the circuit in Figure 1b:

$$I_{out} = I_{in}\ Z_{in_{enh}}\ g_{mb_{n2}}\ Ae \tag{6}$$

and it follows that the output–input current ratio for the enhanced body-driven current mirror can be written as:

$$\frac{I_{out}}{I_{in}} = \frac{g_{mb_{n2}}}{g_{mb_{n1}}} \frac{1}{1+\epsilon_{enh}} \frac{1}{1+s\frac{C_{in_{Ae}}+C_{db_{n1}}(1-A_e)+C_{gd_{n1}}}{Ae\ g_{mb_{n1}}+g_{ds_{n1}}}} \tag{7}$$

where the error term ϵ_{enh} is defined as:

$$\epsilon_{enh} = \frac{g_{ds_{n1}}}{Ae\ g_{mb_{n1}}} \tag{8}$$

From the above equations, it is evident that the accuracy of the enhanced BD-CM depends again on two factors:

1. The value of ϵ_{enh}, which can be minimized by increasing Ae for a given value of $g_{ds_{n1}}$ and $g_{mb_{n1}}$;
2. The matching between $g_{mb_{n1}}$ and $g_{mb_{n2}}$.

For what concerns the value of ϵ_{enh}, the proposed circuit improves the performance through the gain of the error amplifier. Focusing on the matching between $g_{mb_{n1}}$ and $g_{mb_{n2}}$, it has to be noted that, thanks to the feedback loop in Figure 1b, the static voltage at the drain terminal of M_{n_1} is forced at $V_{ref} = V_{DD}/2$ in spite of input current variations; assuming that the static voltage at the output of the current mirror is $V_{DD}/2$, transistors M_{n_1} and M_{n_2} exhibit the same drain-source voltage, thus improving the matching between $g_{mb_{n1}}$ and $g_{mb_{n2}}$ with respect to the conventional BD-CM.

2.2. The Error Amplifier

The schematic of the error amplifier Ae exploited in the proposed enhanced BD-CM is reported in Figure 2. It is made up of transistors $M_{n_{3(4)}}$ which accurately set the DC operating point through the V_{bias_n} voltage. The body terminals of $PMOS$ transistors $M_{p_{3(4)}}$ are used as input terminals to achieve a differential gain which can be expressed as follows:

$$A_e = \frac{g_{mb_{p3(4)}}}{g_{ds_{n_4}} + g_{ds_{n4}}} \tag{9}$$

The common-mode rejection of the error amplifier is improved by common-mode current cancellation at the output (i.e., the current generated through the body transconductance of M_{p_3} is mirrored to the output node by M_{p_4} and subtracted to the current generated through the body transconductance of M_{p_4}).

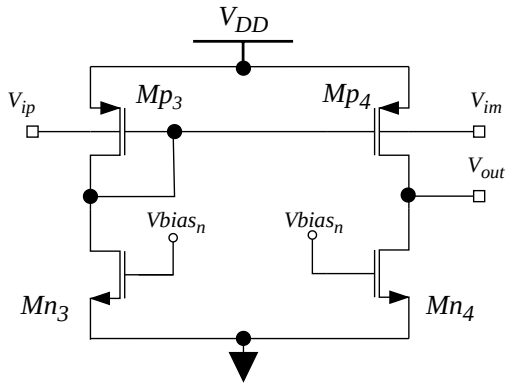

Figure 2. Proposed schematic of the error amplifier.

3. Conventional and Enhanced D2S Circuits

The performance of the D2S converter implemented both through the conventional and the enhanced BD-CM is discussed in the context of the ULV OTA design in this section.

3.1. Conventional D2S Converter Based on Body-Driven Current Mirrors

The D2S converter conventionally used in ULV and ULP circuits, which typically do not have a tail device which biases the differential pair, is the one depicted in Figure 3. The architecture is composed of two gate-biased devices $M_{p_{1,2}}$ which are body driven to attain a rail-to-rail input common-mode range. The current of these devices is set through the gate terminals which mirror a reference current, namely I_{bias}, through a simple gate-driven current mirror. Moreover, the two $NMOS$, respectively, $M_{n_{1,2}}$ are gate biased through a bias voltage, namely V_{bias_n} (i.e., the symmetrical one of V_{bias_p}). In addition, the M_{n_1} shows a body-diode connection which allows to mirror through body terminal of M_{n_2} the current generated by the body transconductance $gm_{b_{p1}}$ of M_{p_1} through the output of the stage. The two currents related to V_{i_p} and to V_{i_m} are added in phase to attain a differential gain which is given by the following equation:

$$A_{v_{D1}} = \frac{g_{mb_{p1(2)}}}{g_{ds_{n2}} + g_{ds_{p2}}} \frac{1 + s\tau_{z1}}{1 + s\tau_{p1}} \frac{1}{1 + s\tau_{o1}} \tag{10}$$

where

$$\begin{aligned} \tau_{p1} = 2 \cdot \tau_{z1} &\approx \frac{C_{bd_{p1}} + C_{gd_{p1}} + C_{bs_{n1}} + C_{bs_{n2}} + C_{gd_{n1}} + C_{bd_{n2}}}{g_{mb_{n1}} + g_{ds_{n1}} + g_{ds_{p1}}} \\ \tau_{o1} &= \frac{C_{in_2} + C_{gd_{n2}} + C_{gd_{p2}} + C_{bd_{n2}} + C_{bd_{p2}}}{g_{ds_{n2}} + g_{ds_{p2}}} \end{aligned} \tag{11}$$

C_{gd} and C_{bs} denote the parasitic capacitances of MOS devices and C_{in_2} denotes the input parasitic capacitance of the second stage. The pole–zero doublet can be neglected due to the fact that the pole and zero are one octave distant from each other; thus, the overall expression can be simplified as:

$$A_{v_{D1}} = \frac{g_{mb_{p1(2)}}}{g_{ds_{n2}} + g_{ds_{p2}}} \frac{1}{1 + s\tau_{o1}} \tag{12}$$

Thus, the architecture as a first approximation shows one pole at the output node.

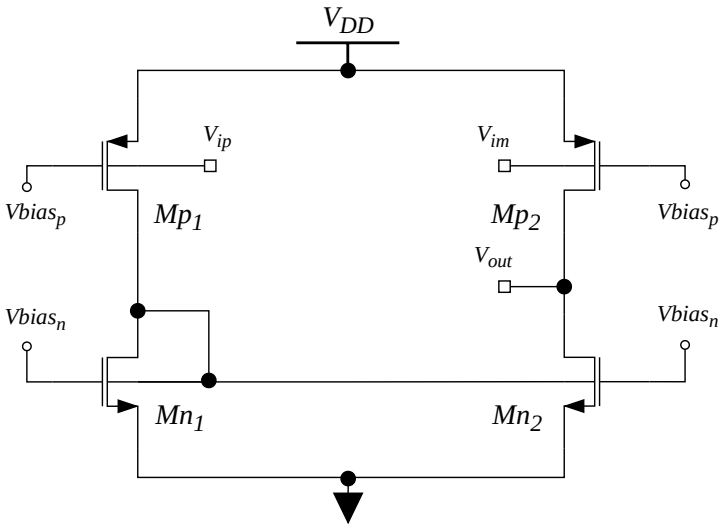

Figure 3. Conventional D2S converter: a standard body-driven current mirror is employed.

The proposed topology results to be very robust with respect to the PVT variations due to the fact that all the transistors are gate biased and thus the power consumption of each branch is well defined over the whole PVT range. However, it has to be noted that, as in the case of other ULV stages [45,46,50,51], it lacks a tail generator; thus, the D2S converter attains a $CMRR$ of about:

$$CMRR_{D2S} = \frac{g_{mb_{n1}}}{g_{ds_{n2}} + g_{ds_{p2}}} \tag{13}$$

which results to be very small if compared with typical low-voltage circuits (i.e., circuits which operate with supply voltages greater than about 0.5 V and which have a tail generator).

As a matter of fact, this architecture seems to be a valid topology for a D2S converter but lacks a good CMRR and thus cannot be used as a good D2S converter. Moreover, the DC voltages at the body terminals of the $NMOS$ devices are not well defined and are selected by the sizing of the devices.

3.2. D2S Converter Based on Enhanced BD-CM

The D2S converter based on the proposed enhanced BD-CM is depicted in Figure 4. The circuit is composed of transistors $M_{n,p_{1,2}}$ which are all gate biased through the V_{bias_n} voltage for the $NMOS$ and V_{bias_p} for the $PMOS$, respectively. Thus, the overall power consumption of the D2S is set accurately and also with respect to the PVT variations (as will be better outlined in the following sections). With respect to the architecture of Figure 3, the D2S exploiting the enhanced BD-CM exhibits a better common-mode rejection and improved stability under the PVT and mismatch variations, as will be better shown in the following.

To explain the operating principle of the proposed enhanced D2S, the block scheme depicted in Figure 5 can be used. Starting from the positive input voltage V_{ip}, the body transconductance gain of M_{p_1} is denoted as $g_{mb_{p1}}$. Then, the generated current is added with the one generated by the body transconductance gain of M_{n_1} and is then converted in voltage at the X node, thanks to the output conductance of M_{n_1} and M_{p_1}. Then, the generated V_X voltage is compared with a reference voltage V_{ref} and the difference is amplified through the error amplifier whose gain is modeled as Ae. Then, the generated V_Y voltage is used to close the negative feedback through the body transconductance gain of M_{p_1}. The V_Y voltage is used to sum in phase the current generated by M_{p_1} with the one generated by M_{p_2}; the two transconductance gains (i.e., the one by V_{ip} and the one by V_{im}) are added in phase for the differential input signal and are subtracted from the common-mode input signal. Thus, the loop enhances the precision of the current mirror,

defines a node voltage at the X node and also improves the CMRR of the architecture. Indeed, given the block scheme of Figure 5, the Y voltage can be expressed as:

$$V_Y = V_{ip}(-g_{mb_{p1}}) \frac{\frac{Ae}{g_{ds_{n1}}+g_{ds_{p1}}}}{1 + g_{mb_{n1}} \frac{Ae}{g_{ds_{n1}}+g_{ds_{p1}}}} \approx -V_{ip} \frac{g_{mb_{p1}}}{g_{mb_{n1}}} \tag{14}$$

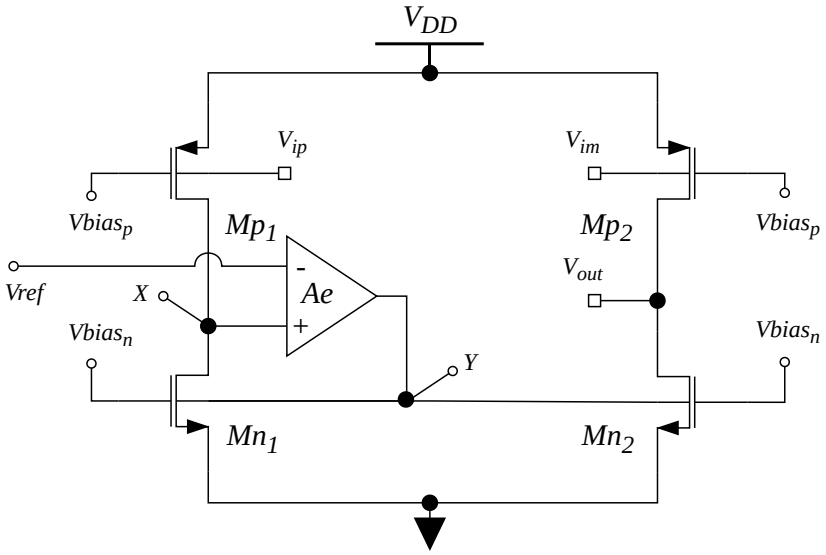

Figure 4. Conventional D2S converter: an enhanced BD-CM is employed.

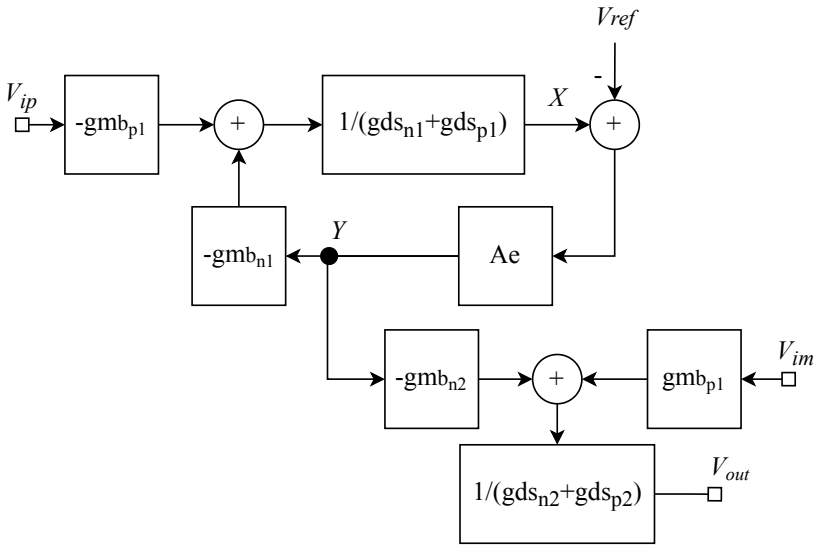

Figure 5. Feedback scheme of the proposed enhanced body-driven D2S.

Thus, for the differential input signal, considering that $g_{mb_{n1}} = g_{mb_{n2}}$, the differential gain can be written as:

$$Av_D \approx \frac{g_{mb_{p1(2)}}}{g_{ds_{n2}} + g_{ds_{p2}}} \tag{15}$$

On the other hand, the overall common-mode gain can be derived as

$$Av_C = \frac{\frac{g_{mb_{p1(2)}}}{g_{ds_{n2}}+g_{ds_{p2}}}}{\frac{g_{mb_{n1}}}{g_{ds_{n1}}+g_{ds_{p1}}} \cdot Ae} \tag{16}$$

Thus, the role of the error amplifier for the small signal is to lower the common-mode gain and thus improve the CMRR of the circuit, which can be easily derived as:

$$CMRR_{D2S_{enh}} = \frac{g_{mb_{n1}}}{g_{ds_{n1}} + g_{ds_{p1}}} \cdot Ae \tag{17}$$

Thus, it can be concluded that the greater the Ae is, the larger the CMRR will be.

4. Two-Stage OTA Based on the Proposed Enhanced D2S

As an application of the proposed enhanced D2S, a ULV OTA, whose architecture is reported in Figure 6, is presented in this section. The OTA is composed of two stages: the enhanced D2S and an inverting output stage. The frequency compensation is achieved through a large load capacitance as in [23,45,46,58–60].

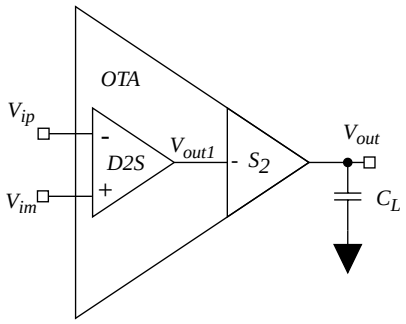

Figure 6. Architecture of the proposed ULV OTA based on enhanced D2S.

4.1. Output Stage

The topology of the output stage of the OTA is depicted in Figure 7. It is composed of two body-driven gate-biased transistors $Mp_5 - Mn_5$. This stage results to be very robust to the PVT and mismatch variations due to the fact that the biasing currents are accurately set through the gate terminals of both the $PMOS$ and $NMOS$ devices which are connected to $Vbias_p$ and $Vbias_n$, respectively. Moreover, the body-driven technique allows to attain a symmetric slew rate due to the fact that the body terminals of the $PMOS$ and $NMOS$ devices behave in a similar way.

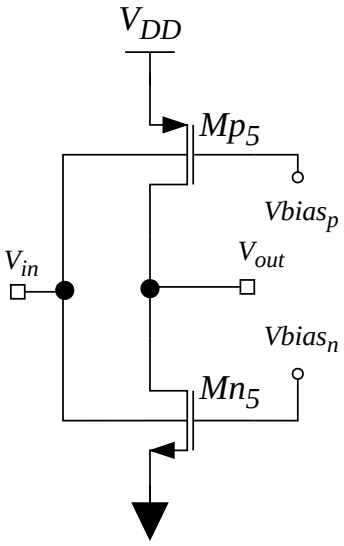

Figure 7. Output stage of the proposed ULV OTA: a body-driven gate-biased inverter.

The voltage gain of the output stage can be easily computed as:

$$A_{v_{buf}} = \frac{g_{mb_{n5}} + g_{mb_{p5}}}{g_{ds_{n5}} + g_{ds_{p5}}} \cdot \frac{1}{1 + s\tau_L} \tag{18}$$

where τ_L is the time constant given by the output load capacitance C_L and by the output conductance $g_{ds_{n5}} + g_{ds_{p5}}$ (the parasitic capacitances at the output node is neglected with respect to C_L), and thus:

$$\tau_L = \frac{C_L}{g_{ds_{n5}} + g_{ds_{p5}}} \tag{19}$$

4.2. Analysis of the Proposed ULV OTA

By following the above approach, the frequency response of the differential gain of the OTA can be easily computed as:

$$Av_{tot} = Av_{D2S} \cdot Av_{S2} = \frac{g_{mb_{p1(2)}}}{g_{ds_{n(2)}} + g_{ds_{p(2)}}} \cdot \frac{g_{mb_{p5}} + g_{mb_{n5}}}{g_{ds_{p5}} + g_{ds_{n5}}} \cdot \frac{1}{1 + s\tau_{o1}} \cdot \frac{1}{1 + s\tau_L} \tag{20}$$

whereas it can be shown that the CMRR is set by the D2S converter, and its expression is reported in Equation (13).

The gain-bandwidth product (GBW) of the OTA can be derived as:

$$GBW = \frac{1}{2\pi} \cdot \frac{g_{mb_{p1(2)}}}{g_{ds_{n(2)}} + g_{ds_{p(2)}}} \cdot \frac{g_{mb_{p5}} + g_{mb_{n5}}}{C_L} \tag{21}$$

whereas the phase margin can be computed according to the following equation:

$$m\varphi = \pi - \arctan\left(2\pi \cdot GBW \cdot \tau_{o1}\right) - \arctan\left(2\pi \cdot GBW \cdot \tau_L\right) \tag{22}$$

Therefore, the phase margin is determined by the current of the first and second stage and by the load capacitance. In this respect, a large load capacitance of $250pF$ is assumed, and the first and second stages of the OTA are designed to meet an $m\varphi \geq 52^\circ$.

5. Simulation Results

OTA Performance and Characterization

The proposed ULV OTA is designed referring to a 130 nm CMOS technology by STMicroelectronics. The devices' sizing is reported in Table 1. The error amplifier topology shown in Figure 2 is chosen to guarantee a CMRR greater than 30 dB and a rail-to-rail ICMR. The power consumption of the OTA is about 120 nW for a supply voltage of 0.3 V. The MOS devices is sized to guarantee good stability and enough of a phase margin in all the PVT conditions for a load capacitance of 250 pF. The layout of the proposed OTA is reported in Figure 8, showing that the occupied area amounts to 74.84 × 31.41 µm.

Table 1. Transistors sizing and DC biasing currents of the proposed OTA.

	W (µm)	**L (µm)**	**I_{BIAS} (nA)**
$Mn_{1,2}$	4.5	1.3	60
$Mp_{1,2}$	48.33	1.3	60
$Mn_{3,4}$	1.5	1.3	20
$Mp_{3,4}$	16.11	1.3	20
Mn_5	18.00	1.3	240
Mp_5	193.32	1.3	240

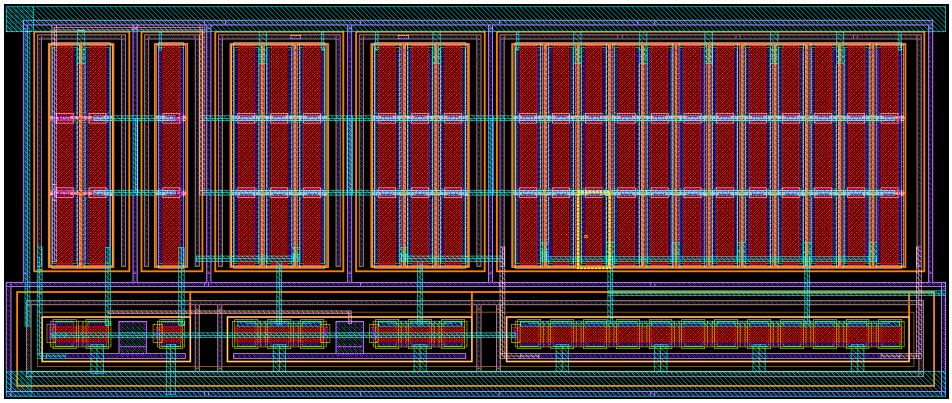

Figure 8. Layout of the proposed OTA: dimensions are 74.84 × 31.41 µm.

The simulations were carried out in the Cadence Virtuoso environment. Figure 9 reports the frequency response of the differential gain of the OTA, showing a dc gain of about 41.28 dB, a 7.95 kHz unity-gain frequency and a phase margin around 52°.

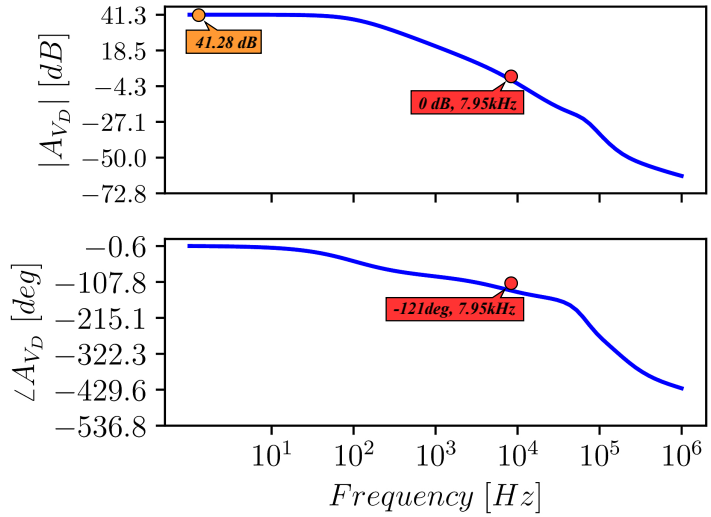

Figure 9. Frequency response of the differential gain (magnitude and phase).

The dc common-mode gain is around 6 dB, resulting in a CMRR of about 35 dB; Figure 10 shows the frequency response of the CMRR. Figure 11 reports the input-referred noise spectral density, which shows a white noise level of 1.4 µV/$\sqrt{\text{Hz}}$ and a noise corner frequency of about 10 kHz.

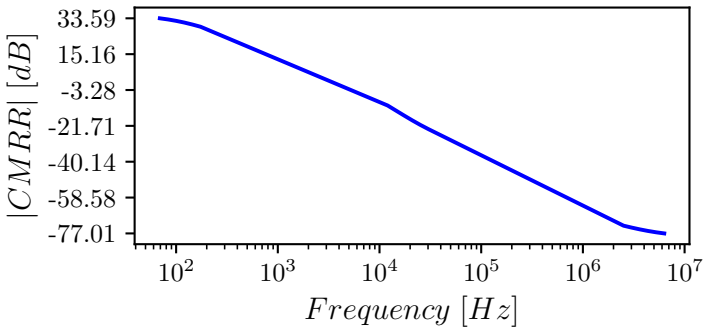

Figure 10. Frequency response of CMRR (magnitude).

The OTA was tested in a unity-gain closed-loop configuration: Figure 12 shows the closed-loop transfer function and Figure 13 the transient response to a 15–285 mV step. The latter allows calculating the slew rate, which results as 1.25 V/ms (SR+) and 1.25 V/ms (SR-), highlighting the symmetry provided by the topology. Figure 14 reports the total harmonic distortion (THD) vs. input amplitude for a 200 Hz sinusoidal input.

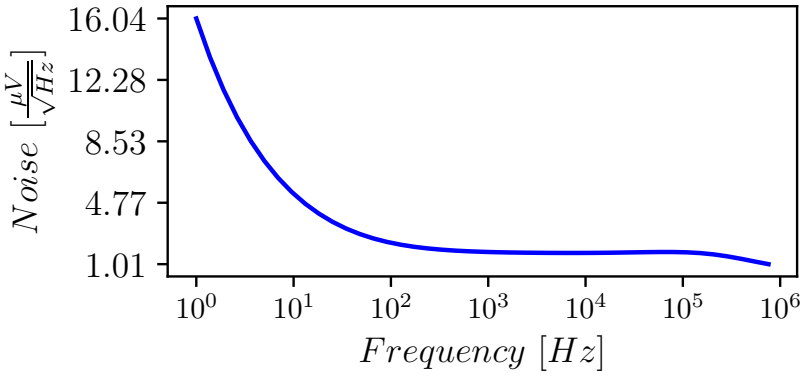

Figure 11. Input-referred spectral noise density.

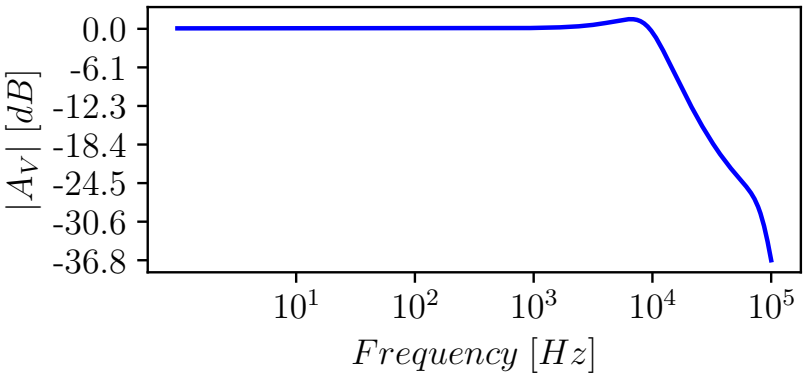

Figure 12. Frequency response of the OTA in unity-gain configuration.

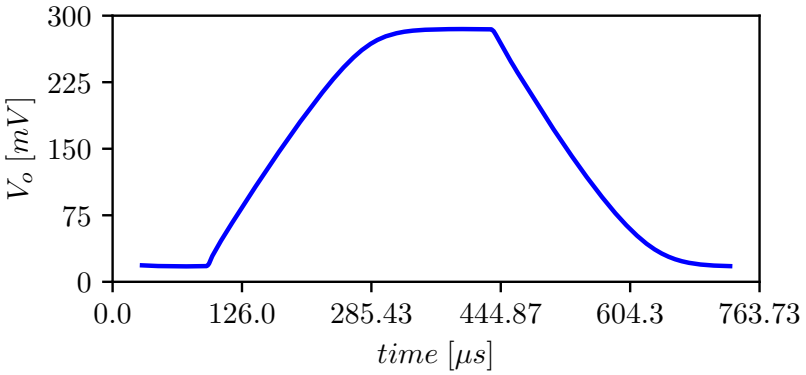

Figure 13. Transient response to a 15–285 mV input step.

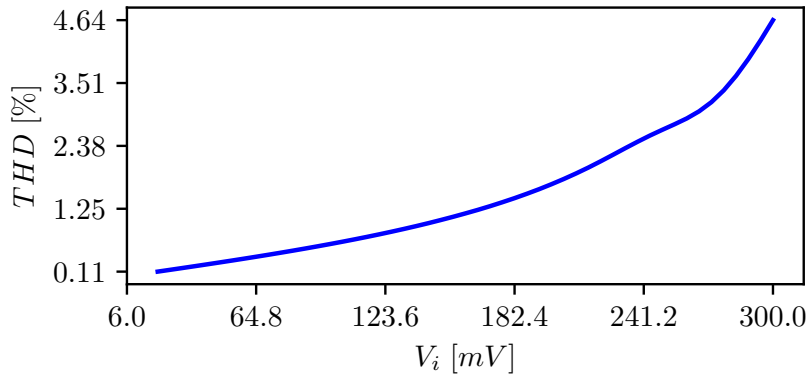

Figure 14. Total harmonic distortion vs. input amplitude for a 200 Hz sinusoidal input in unity-gain configuration.

The OTA's open-loop and closed-loop performances are summarized in Table 2, which also reports the effect of the supply voltage and temperature variations. Together with the effect of the process corners variation, reported in Table 3, this shows the robustness of the proposed topology.

Table 2. OTA performance vs. supply voltage and temperature.

VDD (mV)	**300**	**270**	**330**	**300**	**300**
Temp. (° C)	**27**	**27**	**27**	**0**	**75**
Ad (dB)	41.28	38.03	43.78	41.81	39.52
GBW (kHz)	7.95	7.48	8.21	7.12	8.37
Phase Margin (deg)	51	56.69	47.16	49.66	53.48
Ac (dB)	6	6.1	5.87	6.21	5.93
CMRR (dB)	35.28	31.93	37.91	35.60	33.59
PSRR (dB)	74.41	85.02	82.31	73.49	72.37
Offset (µV)	2.012	391.3	182.9	404.7	962.4
Pd (nW)	120	107.3	132.7	119.1	123
SR+ (V/ms)	1.25	1.08	1.41	1.32	1.13
SR- (V/ms)	1.25	1.11	1.38	1.32	1.12
THD (%) *	3.15	3.23	4.76	2.85	3.59

* = at 90% of full scale.

Table 3. OTA performance vs. process corners.

Corner	**TYP**	**FF**	**SS**	**SF**	**FS**
Ad (dB)	41.28	40.34	42.17	40.82	41.69
GBW (kHz)	7.95	7.71	8.17	7.82	8.08
Phase Margin (deg)	51	53.22	48.13	52.39	50.12
Ac (dB)	6	5.84	6.17	5.23	6.79
CMRR (dB)	35.28	34.50	36.00	35.59	34.90
PSRR (dB)	74.41	77.34	74.97	78.08	74.95
Offset (µV)	2.012	239.8	213.7	524	214
Pd (nW)	120	120.7	119.4	120	120.2
SR+ (V/ms)	1.25	1.21	1.28	1.24	1.24
SR- (V/ms)	1.25	1.20	1.30	1.21	1.29
THD (%)	3.15	3.23	3.02	2.34	2.65

The sensitivity to device mismatches was tested through 200 Monte Carlo mismatch simulations, and the results are reported in Table 4, showing the good robustness of the proposed OTA with a limited input-referred offset.

Table 4. OTA performance in Monte Carlo mismatch simulations.

	Conventional		**Enhanced**	
	μ	σ	μ	σ
Ad (dB)	40.15	0.61	41.18	0.61
GBW (kHz)	6.94	0.18	7.93	0.61
Phase Margin (deg)	51.12	1.03	51	0.8
CMRR (dB)	17.46	1.1	35.17	7.25
PSRR (dB)	63.79	9.81	72.32	6.89
Offset (mV)	0.57	11.22	0.5	9.84
Pd (nW)	108	2.7	120	3.48
SR+ (V/ms)	1.25	0.11	1.25	0.11
SR- (V/ms)	1.26	0.04	1.25	0.05

In Table 4, a comparison between the OTAs exploiting the conventional and the enhanced D2S topology was reported. As it can be observed, the conventional D2S converter results in a lower CMRR (of about 20 dB) and lower PSRR (of about 10 dB) than the enhanced D2S converter.

To further highlight the advantages of the enhanced D2S OTA over the conventional one, the CMRR of both circuits under the mismatch variations were compared. Figure 15 shows a comparison between the histogram of the CMRR for the two circuits obtained from 200 mismatch Monte Carlo simulations. It can be observed that the CMRR of the conventional D2S exhibits a mean value μ of about 17 dB with a very low σ (about 1.1. dB). The histogram of the enhanced D2S shows a mean value μ of 35.17 dB with some Monte Carlo iterations at 80 dB. In addition, it can be observed that the worst-case CMRR associated to the enhanced D2S OTA is determined by the worst-case CMRR of the conventional D2S, enhanced by the gain of the error amplifier of about 18 dB. For what concerns the higher values of the CMRR in the Monte Carlo iterations of the enhanced D2S, they are due to the improved biasing accuracy of the transistors of the body-driven current mirror, which results in better matching between the body transconductances. Finally, it can be concluded that the enhanced D2S converter does not only enhance the worst-case CMRR but also produces occurrences of high CMRR cases thanks to the effect of the proposed approach on biasing accuracy and transconductances matching.

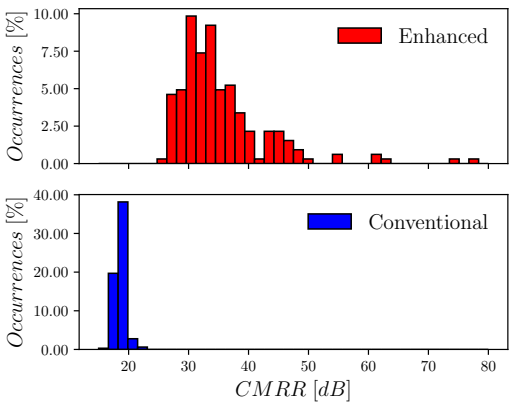

Figure 15. CMRR comparison between the two D2S-based OTA solutions: red color, the enhanced one; blue color, the conventional one.

6. Comparison

The performances of the proposed OTA are compared in Table 5 to recent results for 0.3 V OTAs from the literature. The commonly used figures of merit for a small-signal and large-signal OTA performance, defined in [45,46], are used to allow a comparison. To take into account a more realistic situation, the large-signal FOM was also calculated with reference to the worst-case slew rate:

$$FOM_{Lwc} = \frac{SR_{wc}C_L}{Pd} \tag{23}$$

where $SR_{wc} = \min(SR_+, SR_-)$.

The comparison shows that the proposed circuit exhibits a very good small-signal performance, which is outperformed only by [19], and an adequate large-signal performance. However, the OTA in [19] exhibits a higher sensitivity to process variations and mismatches and results in being less robust than the proposed design.

Table 5. Comparison with the literature.

	This Work *	[19] *	[55] *	[59]	[51] *	[50] *	[47]	[33] *	[46]	[45]	[31]	[43]
Year	2022	2022	2022	2021	2021	2021	2020	2020	2020	2020	2019	2018
Tech (nm)	130	130	130	180	130	130	65	180	180	180	130	180
V_{DD} (V)	0.3	0.3	0.3	0.3	0.3	0.3	0.25	0.3	0.3	0.3	0.3	0.3
V_{DD}/V_{TH}	0.86	0.86	0.86	0.6	0.86	0.86	-	0.6	0.6	0.6	0.86	0.6
A_d (dB)	41.28	52.92	38.07	30	40.80	64.6	70	39	98.1	64.7	49.8	65.8
C_L (pF)	250	50	50	150	40	50	15	10	30	30	2	20
GBW (kHz)	7.95	35.16	24.14	0.25	18.65	3.58	9.5	0.9	3.1	2.96	9100	2.78
mφ (°)	51	52.40	60.15	90	51.93	53.76	89.9	90	54	52	76	61
SR+ (V/ms)	1.25	18.61	20.02	-	10.83	1.7	2	-	14	1.9	-	6.44
SR- (V/ms)	1.25	11.51	8.44	-	32.37	0.15	2	-	4.2	6.4	-	7.8
SRavg (V/ms)	1.25	15.06	14.23	0.085	21.60	0.93	2	-	9.1	4.15	3.8	7.12
THD (%)	3.15	0.673	1.635	2	1.4	0.84	-	1	0.49	1	-	1
% input swing	90	90	80	90	80	100	-	23	83.33	85	-	93.33
CMRR (dB)	35.28	42.11	54.88	41	67.49	61	62.5	30	60	110	-	72
PSRR (dB)	74.41	56.13	51.05	30	45	26/28	38	33	61	56	-	62
IRN ($\mu V/\sqrt{Hz}$)	1.4	1.60	3.156	-	2.12	2.69	-	0.81	1.8	1.6	0.035	1.85
@freq (Hz)	10 k	1 k	1 k	-	1 k	100	-	1 k	-	-	100 k	36
Pd (nW)	120	21.89	59.88	2.4	73	11.4	26	0.6	13	12.6	1800	15.4
Mode	BD	BD	BD	DIG	BD	BD	BD	GD	BD	BD	GD	BD
FOM_S (MHz pF/mW)	16.56 k	80.29 k	20.16 k	15.89 k	10.20 k	15.72 k	5.48 k	15.00 k	7.15 k	7.05 k	10.11 k	3.61 k
FOM_L (V pF/μW)	2.5 k	34.40 k	11.88 k	5.40 k	11.82 k	4.08 k	1.15 k	-	21.00 k	9.88k	4.67k	9.25k
$FOM_{L_{wc}}$ (V pF/μW)	2.5 k	26.30 k	7.04 k	-	5.93 k	4.52 k	1.15k	-	6.30 k	4.52 k	-	8.36 k
Area (μm^2)	2350	5200	2700	982	3600	3600	2000	470	9800	8500	-	8200

* simulated; BD = body driven; GD = gate driven; DIG = digital.

7. Conclusions

In this paper, an enhanced body-driven current mirror was proposed and exploited to build a novel ultra-low-voltage OTA topology that combines several design techniques to achieve a reasonable CMRR under ULV conditions, an interesting performance and robust biasing. The bias currents in all the branches are set by current sources, resulting in a robust bias point and a stable performance under PVT variations.

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Abbreviations

The following abbreviations are used in this manuscript:

ULV	Ultra-Low Voltage
ULP	Ultra-Low Power
D2S	Differential to Single Ended
PSRR	Power Supply Rejection Ratio
CMRR	Common-Mode Rejection Ratio
OTA	Operational Transconductance Amplifier
IoT	Internet of Things
FOM	Figure of Merit
FDSOI	Fully Depleted Silicon on Insulator
BD	Body Driven
BD-CM	Body-Driven Current Mirror
GD	Gate Driven
PVT	Process Voltage and Temperature
DIG	Digital
IRN	Input-Referred Noise
THD	Total Harmonic Distortion
Pd	Power Dissipation
SR	Slew Rate

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