INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2016; **44**:1468–1477
Published online 11 November 2015 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.2172

LETTER

CMOS Non-tailed differential pair

Giuseppe Di Cataldo[1], Alfio Dario Grasso[1], Salvatore Pennisi[1,*,†], Giuseppe Scotti[2] and Alessandro Trifiletti[2]

[1]*DIEEI, University of Catania, Catania, Italy*
[2]*DIE, University of Rome "Sapienza", Rome, Italy*

SUMMARY

A continuous-time complementary metal–oxide–semiconductor differential pair that does not require the traditional tail current source as a way to control the direct current and common-mode current is presented. Compared with a *p*-channel long-tailed pair, the proposed non-tailed solution operates under a higher maximum input common-mode voltage that includes $(V_{DD}+V_{SS})/2$ even under low supply voltages. Experimental measurements on a prototype fabricated in a 0.35-μm technology (with metal–oxide–semiconductor thresholds greater than 0.6 V) confirm this behavior for supply voltages as low as 1.2 V, whereas the long-tailed pair with the same technology offers the same capability only for supplies higher than 1.6 V. Copyright © 2015 John Wiley & Sons, Ltd.

Received 29 July 2015; Revised 27 September 2015; Accepted 8 October 2015

KEY WORDS: body effect; long-tailed pair; low voltage amplifiers; transconductance amplifiers; fully differential amplifiers

1. INTRODUCTION

The long-tailed differential pair (LTP) is one of the most versatile configurations useful for the realization of many analog and digital basic circuits, the most popular of which is the differential amplifier [1–10]. Figure 1 shows a conventional implementation of a complementary metal–oxide–semiconductor (CMOS) single-stage fully differential amplifier based on a *p*-channel pair (transistors M_{1a} and M_{1b}) whose quiescent and common-mode current, $(i_{D1a}+i_{D1b})/2$, is set by the tail current source (I_B). The circuit includes also two transistors acting as an active load (M_{2a} and M_{2b}), with resistors $R_{1a,b}$ controlling the output common-mode voltage, being equal to $V_{SS}+V_{GS2}$.

It is well-known that the *single-ended* differential and common-mode gain of this circuit are respectively given by $\frac{v_{out-}}{v_d}=-\frac{1}{2}g_{m1}R_1$ and $\frac{v_{out-}}{v_{cm}}=-\frac{1}{2g_{m2}r_B}$, where $v_d=v_{in+}-v_{in-}$ and $v_{cm}=(v_{in+}+v_{in-})/2$, r_B is the output resistance of the current generator I_B, and g_m is the (gate) transconductance, respectively.

This circuit has served excellently as long as the supply voltage, $V_{DD}-V_{SS}$, has been substantially higher than 1 V. Unfortunately, the supply reduction together with a non-corresponding decrease of the MOS threshold voltages makes the use of the standard source-coupled pair difficult. One of the most relevant problems is the decrease of the common-mode input voltage range (*CMR*) and, perhaps more importantly, the fact that the analog ground cannot be set to the medium value between V_{DD} and V_{SS}, $(V_{DD}+V_{SS})/2$. In fact, considering the circuit in Figure 1 and taking into account that a change in v_{cm} is followed by a similar change at the source potential of $M_{1a,b}$, the

*Correspondence to: Salvatore Pennisi, DIEEI, University of Catania, Catania, Italy.
†E-mail: spennisi@dieei.unict.it

Copyright © 2015 John Wiley & Sons, Ltd.

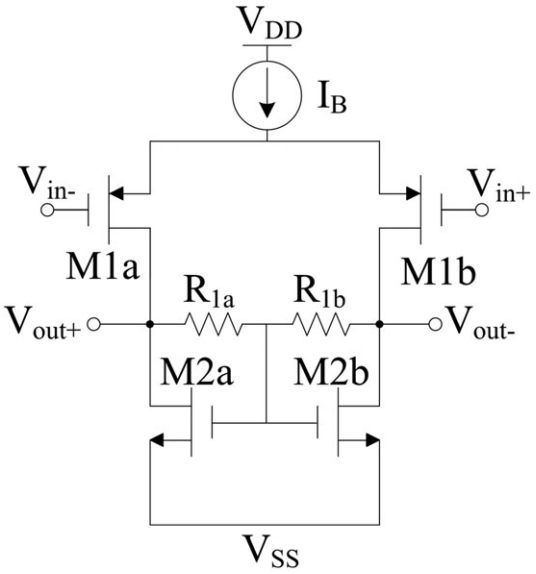

Figure 1. Schematic diagram of a single-stage differential amplifier based on the conventional long-tailed pair.

maximum allowed value of v_{cm} is set by the minimum operating voltage drop tolerated by the current source I_B. If, in the best case, I_B is implemented through a single transistor of a current mirror, the minimum operating voltage across I_B is then one MOS saturation voltage $|V_{DS,SAT\_IB}|$ so that we acquire the following:

$$v_{cm\_\max} = V_{DD} - \left|V_{DS,SAT\_IB}\right| - |V_{GS1}| \approx V_{DD} - 2\left|V_{DS,SAT}\right| - |V_{T1}| \tag{1}$$

where $|V_{DS,SAT}| = |V_{GS1}| - |V_{T1}|$ and $|V_{DS,SAT\_IB}| \approx |V_{DS,SAT1}| = |V_{DS,SAT}|$ have been used in the approximation.

On the other hand, the minimum value of v_{cm} is set by the permanence of $M_{1a,b}$ in saturation, avoiding the triode region. Because the drain voltage of $M_{1a,b}$ is constant and equal to $V_{SS} + V_{GS2}$, and being $|V_{DS,SAT1}| = |V_{GS1}| - |V_{T1}|$ we acquire the following:

$$v_{cm\_\min} = V_{SS} + V_{GS2} - |V_{T1}| = V_{SS} + \left|V_{DS,SAT}\right| + V_{T2} - |V_{T1}|. \tag{2}$$

CMR is hence given by the following:

$$\begin{aligned} CMR &= v_{cm_{\max}} - v_{cm_{\min}} \\ &= V_{DD} - V_{SS} - V_{GS2} - \left|V_{DS,SAT_1B}\right| - \left|V_{DS1,SAT}\right| \approx V_{DD} - V_{SS} - 3\left|V_{DS,SAT}\right| - |V_{T2}|. \end{aligned} \tag{3}$$

Besides, the input terminals can be biased to $(V_{DD} + V_{SS})/2$ only if the following condition is satisfied:

$$v_{cm\_\min} < \frac{V_{DD} + V_{SS}}{2} < v_{cm\_\max}. \tag{4}$$

We plot in Figure 2 relations (1) and (2) versus V_{DD} (assuming for simplicity $V_{SS} = 0$). It is apparent that *CMR* (indicated by the gray area) reduces for decreasing values of V_{DD} and nullifies for $V_{DD} = V_1$. In addition, for $V_{DD} < V_2$, the analog ground (represented by the line $V_{DD}/2$) is outside the allowed *CMR*, and the pair must be biased below $V_{DD}/2$. Voltages V_1 and V_2 are easily found analytically by equating (3) to zero and (1) to $V_{DD}/2$, respectively, and solving for V_{DD} as follows:

$$V_1 = \left|V_{DS,SAT\_IB}\right| + \left|V_{DS1,SAT}\right| + V_{GS2} = 3V_{DS,SAT} + V_{T2}, \tag{5a}$$

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

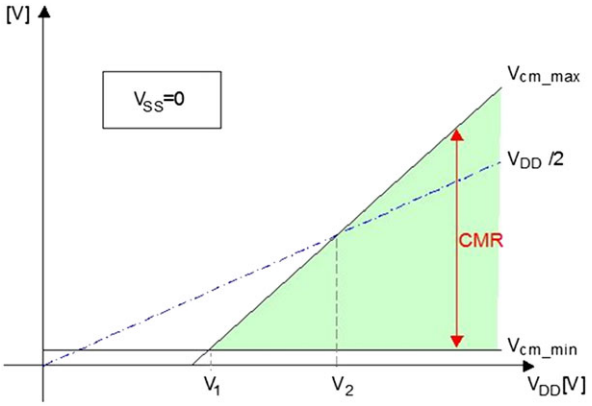

Figure 2. LTP common-mode maximum and minimum voltages versus V_{DD}. The shaded area represents the common-mode range for a given V_{DD}.

$$V_2 = 2\left|V_{DS,SAT\_IB}\right| + 2|V_{GS1}| = 4V_{DS,SAT} + 2|V_{T1}|. \tag{5b}$$

For instance, assuming transistors' threshold and saturation voltages around 0.6 and 0.1 V, respectively, we obtain from (5b) $V_2 = 1.6$ V. This means that for $V_{DD} < 1.6$ V, it is not possible to set the analog ground to $V_{DD}/2$. In the previously simplified analysis, we considered an abrupt MOS transition from saturation to the triode region. However, the real scenario is even worsened because, due to channel length modulation, current I_B starts to decrease well before v_{cm} equals v_{cm_max}, and consequently, small-signal parameters of the pair begin to change well before v_{cm} equals v_{cm_min}.

To face this problem, several techniques have been proposed [11], including level-shifting [12], floating-gate [13], and threshold voltage lowering [14]. In this paper, we shall describe a design approach that allows implementing a gate-driven differential pair that does not require the tail current source, while keeping the full control of the standby and common-mode current through an auxiliary feedback section. Compared to a previously solution by the same authors [15–17], the proposed one operates in a continuous-time mode, by avoiding the use of a switched-capacitor auxiliary amplifier. In this manner, design is simplified and area of application widened. The non-tailed pair is described in Section 2. Circuit topology and design issues of the proposed implementation are discussed in Section 3. Experimental measurements, closely matching the expected behavior, are reported in Section 4. Conclusions are summarized in Section 5.

2. PROPOSED SOLUTION

A. Generalities

Figure 3a shows the main differential amplifier obtained from Figure 1 after removing the tail current source. The body terminals of the pair are now used to provide biasing and common-mode current control through an auxiliary feedback circuit, as illustrated in Figure 3a and b. Figure 3b shows also the simplified circuit generating the feedback voltage V_b to be applied to the body of the input pair M_{1a} and M_{1b}. Body biasing is a technique utilized in digital circuits [18], but seldom applied to analog implementations [19–21]. Actually, by eliminating the tail current, we would lose the control of the direct current (DC) and common-mode current of the main pair. This means that the same current would depend on supply, common-mode input voltage, process tolerances, and temperature. Therefore, fundamental parameters like power dissipation and small-signal transconductance of the pair would be hill defined. To avoid this problem, circuit in Figure 3b sets the common-mode current of M_{1a} and M_{1b} in a robust way. Indeed, transistors M_{1ar} and M_{1br} form a replica of the main Non-Tailed Pair (NTP) and negative feedback provided by the error amplifier, A, sets the sum of drain currents of transistors M_{1ar} and M_{1br} to I_{Br}, while forcing the drain of M_{1ar} and M_{1br} to

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

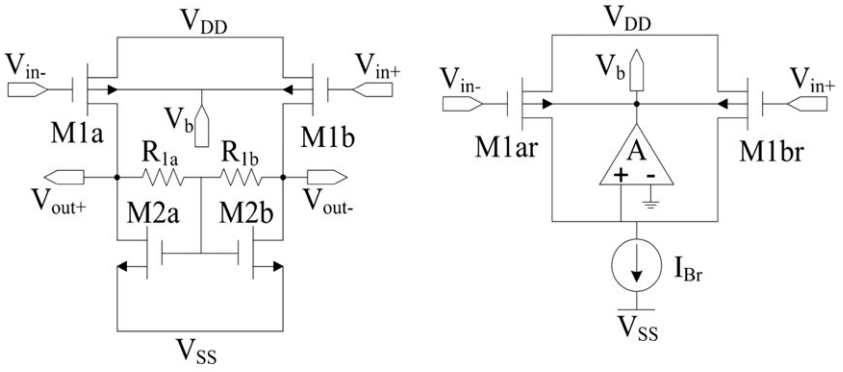

Figure 3. Schematic diagram of: (a) differential amplifier based on a non-tailed source-coupled pair, (b) common-mode current control circuit generating voltage V_b to be applied to the non-tailed differential amplifier in Figure 3a.

ground, by modifying the bulk voltage V_B, irrespectively of the values of common-mode voltage, supply, and temperature. Consequently, because M_{1a} and M_{1b} have the same V_{GS} and V_{BS} as M_{1ar} and M_{1br}, the current in the original pair will be forced to be a mirrored replica of I_{Br}, depending on the relative width of M_1 to M_{1r}.

It should be noted that the feedback loop provided by the error amplifier sets the current in the pair irrespectively of any variation in V_{DD}. Therefore, power supply rejection ratio is expected to be improved with respect to the LTP.

Small-signal analysis of circuit in Figure 3 yields the differential and common-mode gain. Because the auxiliary circuit in Figure 3b does not respond to differential signals, the single-ended differential gain is the same as in the LTP, whereas the single-ended common mode gain is as follows:

$$\frac{v_{out-}}{v_{cm}} = \frac{g_{m1}}{(1+2Ag_{mb1r}r_{br})g_{m2}} - \frac{g_{m1}g_{mb1r} - g_{1r}g_{mb1}}{g_{mb1r}g_{m2}} \tag{6}$$

where A is the gain of the auxiliary error amplifier, g_{mb} is the MOS bulk transcondctance, and r_{Br} is the output resistance of the current generator I_{Br}. Under perfect matching $g_{m1r}g_{mb1} = g_{m1}g_{mb1r}$, A_{cm} is reduced with respect to LTP by about $Ag_{mb1}r_{Br}/g_{m1}r_B \cong Ag_{mb1}/g_{m1}$. As far as the common-mode voltage is concerned, compared with the LTP, the NTP offers a higher maximum common-mode input value, for two reasons. First, as can be seen by comparing (1) and (7), the saturation voltage of the current generator is no more required.

$$v_{cm\_\max} = V_{DD} - |V_{GS1}| = V_{DD} - |V_{DS,SAT1}| + |V_{T1}| \tag{7}$$

Second, the source-gate voltage of $M_{1a,b}$ is a function of v_{cm} and, in particular, decreases with v_{cm}. Indeed, if v_{cm} increases by Δv, the source-gate voltage of M_{1ar} and M_{1br} in Figure 3b decreases by the same Δv, but because the drain current must remain constant (because of the local feedback action of A), the threshold voltage of M_{1ar} and M_{1br} must decrease exactly by Δv in order to keep $|V_{GS1r}|-|V_{T1r}|$ constant. This threshold reduction is mirrored onto the main couple $M_{1a,b}$ through V_b. In summary, an increase in the common-mode voltage causes an identical decrease in the threshold voltage V_{T1}. This mechanism could in principle lead to the ideal condition $v_{cm\_\max} = V_{DD}$, but in practice, $v_{cm\_\max}$ is determined by the finite output swing of the error amplifier A. Indeed, if voltage V_b saturates, then the common-mode current is no longer controlled, and the current in the pair starts to decrease (for $v_{cm} > v_{cm\_\max}$) or increase (for $v_{cm} < v_{cm\_min}$). At this purpose, the error amplifier was originally implemented using the switched-capacitor approach [7, 8], so that V_b was not limited within the supply rails. However, true continuous-time operation was not allowed, and output spurs were introduced by the clock switching.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

In the following, we will use a continuous-time common-mode current feedback circuit,with the main objective of maximizing $v_{cm\_\max}$ and, in turn, the implementation of a fully differential CMOS amplifier whose common-mode input voltage can be set to the analog ground $(V_{DD}+V_{SS})/2$, even under low supply voltages, unlike what can be achieved by a conventional LTP.

B. Topology and design

The proposed implementation of the auxiliary common-mode current control circuit, which is exploited to drive the bulks of the main pair in Figure 3a, is shown in Figure 4. All the transistors operate in saturation. Like in Figure 3b, M_{1ar} and M_{1br} form a replica of the main pair M_{1a} and M_{1b}. Bias current of the pair provided by M_3 can be scaled compared with the current in the main pair, in order to reduce the additional power consumption. The (noninverting) error amplifier (A in Figure 3b) is implemented through common-source transistor M8, current mirror M_9 and M_{10}, and bias current generator M_7. Note that the quiescent drain voltage of M_{1ar}-M_{1br} is V_{DD} minus the source-gate voltage of M_8 and can be adjusted through *W*/*L* ratios.

$$V_{D1,r} = V_{DD} - |V_{T8}| - \sqrt{\frac{I_{D7}}{K_P}\frac{(W/L)_9}{(W/L)_8(W/L)_{10}}}. \tag{8}$$

To nullify the channel modulation effect and accurately replicate the common-mode current, this voltage should equal the drain voltage of the main pair in Figure 3a, that is, $V_{SS}+V_{GS2}$. However, if a systematic error in the current of the main pair is tolerable, this restriction can be avoided, and the supply voltage demand can be reduced. Thanks to the simplicity of the output section (M_7 and M_{10}), the output swing is maximized. It is limited by one saturation voltage towards both supply rails. The gain of the error amplifier is $A = g_{m8}\,(g_{m10}/g_{m9})\,r_{d7}//r_{d10}$.

The non-tailed fully differential amplifier was designed using the BCD6 technology, provided by STMicroelectronics (Catania site, Italy), whose CMOS transistors have a minimum length of 0.35 μm with a nominal threshold voltage of 0.65 and −0.61 V for nMOS and pMOS, respectively. Adopted transistors and resistor dimensions, supply voltage, and bias current are summarized in Table I from which it is deduced that I_{Br} in Figure 3b is equal to $I_{DM3} = 2\,\mu A$, and that the nominal bias current of the main pair $I_{DM1a,b}$ is 6 μA.

Preliminary computer simulations showed that the main amplifier provides a DC gain of 12d B, unity-gain frequency of 89 kHz, and phase margin of 105°, with load capacitance of 40 pF. The auxiliary amplifier exhibits a DC gain of 35 dB with a bandwidth much greater than the main amplifier unity gain frequency because of the small capacitances involved in the feedback loop.

To have an idea of the different *CMR* exhibited by the NTP-based and the LTP-based amplifiers, under similar dimensions and supply, we simulated the common-mode current of the pairs as a function of the input common-mode voltage. The result is illustrated in Figure 5 for V_{DD} equal to

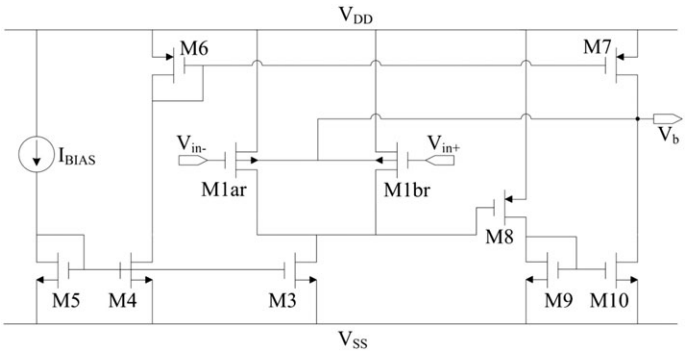

Figure 4. Continuous-time common-mode current control circuit (proposed implementation of circuit in Figure 3b) generating the output voltage V_b to be applied to the non-tailed differential amplifier in Figure 3a.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Table I. Bias settings and transistor dimensions of circuits in Figures 3 and 4.

Parameter	Value
V_{DD}–V_{SS}	1.5 V
I_{BIAS}	1 μA
M_{1a}, M_{1b}	3 × (0.5/0.35)
M_{2a}, M_{2b}	4 × (0.5/0.35)
M_{1ar}, M_{1br}	(0.5/0.35)
M_3	2 × (0.5/0.35)
M_4, M_5, M_6, M_7, M_8, M_9, M_{10}	0.5/0.35
R_{1a}, R_{1b}	200 kΩ

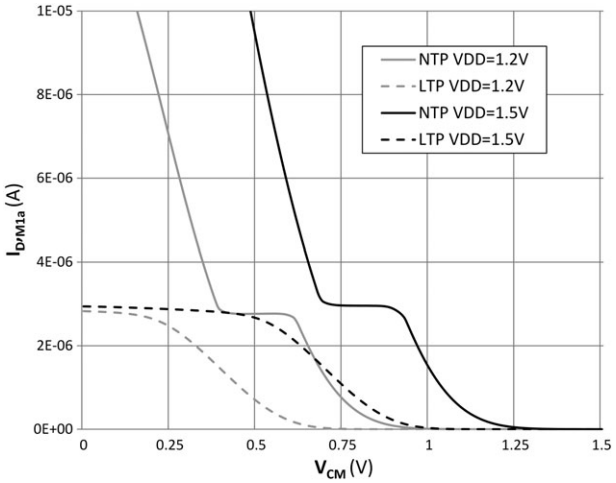

Figure 5. Current flowing in one transistor of the pair for the non-tailed and long-tailed solution and for two supply voltages V_{DD} = 1.5 V and V_{DD} = 1.2 V.

1.5 and 1.2 V. The voltage range for which the common-mode current remains constant indicates the *CMR*. It is confirmed that the LTP exhibits an unrivaled ability to work very closely to V_{SS} (for *p*-channel pairs). Note however that with this kind of simulation, we cannot see the pair entering the triode region according to (3), because the common-mode current obeys to the Kirchhoff current law (and hence is equal to the tail current) even if the pair works in triode. Unfortunately, as discussed in Section I, the LTP common-mode voltage cannot be set to $V_{DD}/2$ because this value is not included in the LTP *CMR*. In contrast, the *CMR* of the proposed NTP,includes 0.75 V for V_{DD} = 1.5 V and, as a limit, even 0.6 V for V_{DD} = 1.2 V.

3. MEASUREMENTS

The amplifier in Figure 3a with the control section in Figure 4 was fabricated using the technology, aspect ratios, and the other component values described in the previous section. The chip microphotograph is illustrated in Figure 6; the area occupied is 87 × 136 μm, and the main part of which is devoted to the implementation of the two resistors $R_{1a,b}$. DC power consumption is 17 μW under 1.5-V supply. Compared with the LTP, the increase in power consumption and area occupation is about 80% and 17%, respectively. As an indirect proof that the common-mode current was effectively set in the main pair, we measured the output voltage (V_{SS} + V_{GS1}), while setting v_{in_cm} = 0.75 V. The difference between the measured and expected (simulated) value is about 7 mV.

The large-signal transfer characteristics of the amplifier under differential input is illustrated in Figure 7. The single-ended output voltage swing is about ±580 mV. The output voltage versus the common-mode input voltage is shown in Figure 8. The *CMR* defined as the input voltage range for

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

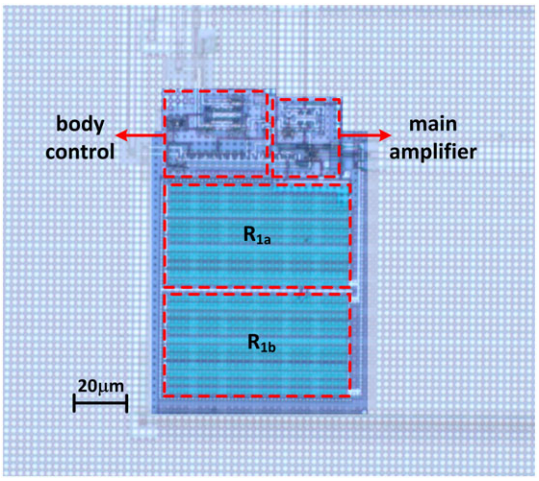

Figure 6. Chip microphotograph. The area occupied is 87 × 136 μm

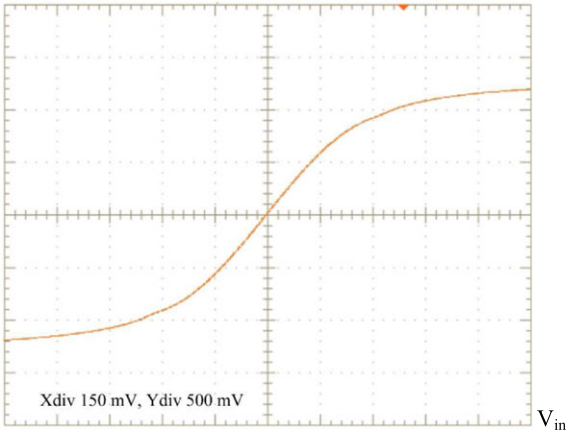

Figure 7. Measured large-signal differential output versus differential input

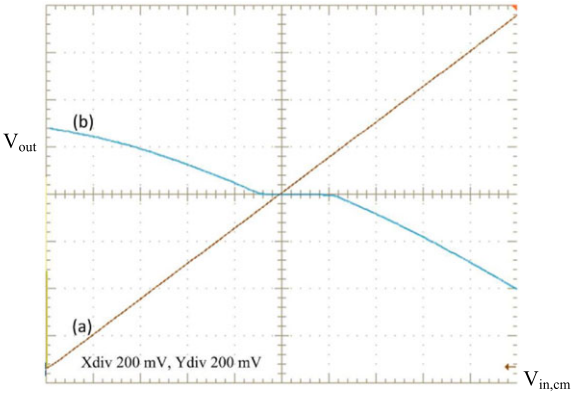

Figure 8. Measured common-mode input range. (a) input common-mode voltage sweep and (b) single-ended output voltage under 1.5-V supply. The common-mode input voltage range so that the output voltage (and hence the common-mode current) remains constant is about 300 mV.

which the output voltage (and hence the common-mode current) remains constant is about equal to 300 mV. It is seen that it includes $V_{DD}/2 = 0.75$ V and that there is room for a further V_{DD} reduction of 200 mV with a small increase of the common-mode current.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

A comparison between the measured Bode plots (solid line) and simulated ones (dotted line) of the magnitude and phase of the differential gain is depicted in Figure 9. The DC gain is 12 dB, and the unity gain frequency is 92 kHz for an estimated C_L of 40 pF. The common-mode gain (single-ended)

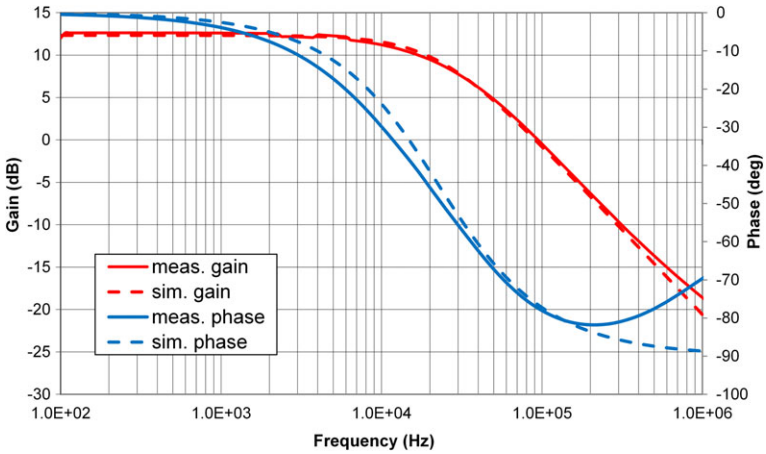

Figure 9. Bode plots of the differential gain $\left(v_{\text{out}}^{+} - v_{\text{out}}^{-}\right)/v_d$ magnitude and phase (CL = 40 pF): measured (solid lines) and simulated (dotted lines).

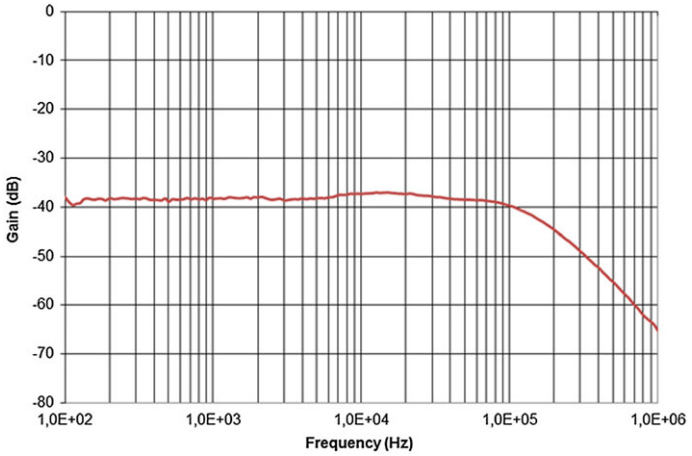

Figure 10. Measured Bode plot of the common-mode gain $\left(v_{\text{out}}^{+} - v_{\text{out}}^{-}\right)/v_{cm}$, ($CL$ = 40 pF).

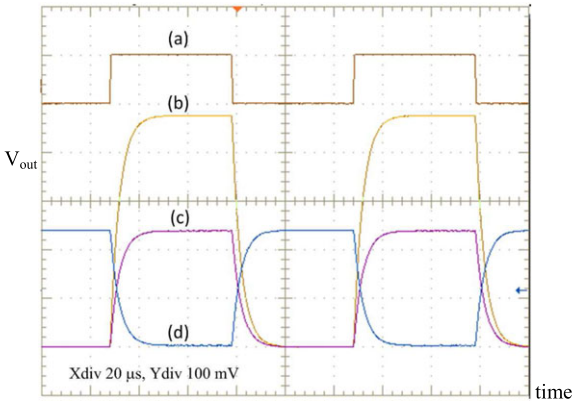

Figure 11. Measured transient response to a 100-mVpp input step: (a) input step, (b) differential output, (c), and (d) single-ended outputs (CL = 40 pF).

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

is illustrated in Figure 10; the DC value is -38 dB. The open-loop single-ended and differential output transient response to a 100-mVpp differential input step is plotted in Figure 11 for an estimated load C_L of 40 pF; 1% settling time is about 20 μs.

4. CONCLUSIONS

We designed and experimentally tested a CMOS *non-tailed differential pair*. The NTP acts as a conventional gate-driven long-tailed source-coupled pair in which the tail current generator is effectively removed thanks to a feedback circuit controlling the common-mode current from the bulk terminals. The adopted solution reduces the supply demand of a conventional LTP differential pair, and the results obtained show promise for practical applications. Main drawbacks are an increase in power dissipation (80% in our design, because of the additional feedback section that has 1/3 standby current of the main pair), a moderate increase in the area occupation (17%), and a decrease of the *CMR* (because of the continuous-time approach followed). The first and second limitations have reduced importance if the solution is used as the first stage of a multistage amplifier (where the output stage usually employs the largest DC current and the widest transistors), whereas the second limitation is not a concern for feedback amplifiers to be operated in inverting configuration, as the input terminals remain virtually shorted to the analog ground because of the high feedback gain. In this last case, on the contrary, an important requisite is the possibility of setting the analog ground to $(V_{DD}+V_{SS})/2$. This is achieved by the proposed NTP under supply voltage as low as 1.2 V. The same behavior cannot be achieved by the conventional LTP adopting the chosen 0.35-μm technology (with thresholds around -0.61 V for *p*-channel devices).

Future work will be devoted to extend the *CMR* of the NTP towards V_{SS}, trying to share the best performance of the LTP and NTP topologies.

ACKNOWLEDGEMENT

This work was partially supported by the Project PON02_00355_3391233 "ENERGETIC" funded by the MIUR (Italian Ministry of Education, University and Scientific Research). The authors thank Eng. Antonio Imbruglia and Eng. Francesco Pulvirenti at STMicroelectronics for their help in the realization of the chip.

REFERENCES

1. Sedra AS, Smith KC. *Microelectronic Circuits* (6th edn). Oxford University Press, 2010.
2. Willingham SD, Martin K. Integrated Video-frequency Continuous-time Filters: High-performance Realizations in BiCMOS, Kluwer 1995.
3. Rodríguez-Vázquez R, Navas M, Delgado-Restituto M, Vidal F. A modular programmable CMOS analog fuzzy controller chip. *IEEE Transactions on Circuits and Systems II* 1999; **46**:251–265.
4. Delgado-Restituto M, Rodríguez-Vázquez A. Design considerations for Integrated continuous-time chaotic oscillators. *IEEE Transactions on Circuits and Systems I* 1998; **45**:481–495 IEEE.
5. Kimura K. A CMOS logarithmic IF amplifier with unbalanced source-coupled pairs. *IEEE Journal of Solid-State Circuits* 1993; **SC-28**:78–83.
6. Kimura K. A unified analysis of adaptively biased emitter- and source-coupled pairs for linear transconductance elements. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences* 1995; **78-A**:485–497.
7. Liu S, Chang C. CMOS subthreshold four quadrant multiplier based on unbalanced source-coupled pairs. *International Journal of Electronics* 1995; **78**:327–332.
8. Tajalli A, Brauer EJ, Leblebici Y, Vittoz E. Sub-threshold source-coupled logic circuits for ultra-low power applications. *IEEE Journal of Solid-State Circuits* 2008; **43**:1699–1710.
9. Chen C, Li Z. A low-power CMOS analog multiplier. *IEEE Transactions on Circuits and Systems II: Express Briefs* 2006; **53**:100–104.
10. Wu R, Lidgey FJ, Hayatleh K, Hart BL. Differential amplifier with improved gain accuracy and linearity. *Solid-State and Integrated Circuit Technology, 2006* 2010; **38**:829–844.
11. Fayomi CJB, Sawan M, Roberts GW. Reliable circuit techniques for low-voltage analog design in deep submicron standard CMOS: a tutorial. *Analog Integrated Circuits and Signal Processing* 2004; **39**:21–38.
12. Carrillo JM, Duque-Carrillo JF, Torelli G, Ausin JL. Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries. *IEEE Journal of Solid-State Circuits* 2003; **38**:8.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

13. Ramirez-Angulo J, Choi SC, Gonzalez-Altamirano G. Low voltage circuits building blocks using multiple-input floating-gate transistors. *IEEE Transactions on Circuits and Systems I Fundamental Theory and Applications* 1995; **42**(11):971–974.
14. Lehmann T, Cassia M. 1-V power supply CMOS cascode amplifier. *IEEE Journal of Solid-State Circuits* 2001; **36**:1082–1086.
15. Monsurrò P, Scotti G, Trifiletti A, Pennisi S. Biasing technique via bulk terminal for minimum supply CMOS amplifiers. *IEEE Journal of Solid-State Circuits* 2005; **41**:779–780.
16. Grasso AD, Monsurrò P, Pennisi S, Scotti G, Trifilietti A. Analysis and implementation of a minimum-supply body-biased CMOS differential amplifier. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 2009; **17**:172–180.
17. Monsurrò P, Pennisi S, Scotti G, Trifiletti A. Exploiting the body of MOS devices for high performance analog design. *IEEE Circuits and Systems Magazine* 2011; **11**:8–23.
18. Corsonello P, Lanuzza M, Perri S. Gate-level body-biasing technique for high-speed sub-threshold CMOS logic gates. *IEEE Journal of Solid-State Circuits* 2014; **42**:65–70.
19. Killat D. Sub-1-V CMOS Bandgap using Forward Body Bias of the PMOS Differential Pair for Reduction of the Threshold Voltages, in *Proc. IEEE Int. Conf. Solid-State and Integr. Circ. Techn* 2006. ICSICT **06**: 1692–1694.
20. Monsurrò P, Pennisi S, Scotti G, Trifiletti A. Linearization technique for source-degenerated CMOS differential transconductors. *IEEE Transactions on Circuits and Systems II* 2007; **54**(10):848–852.
21. Monsurrò P, Pennisi S, Scotti G, Trifiletti A. 0.9-V CMOS cascode amplifier with body-driven gain boosting. *IEEE Transactions on Circuits and Systems II* 2009; **37**:193–202.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta