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High-speed low-voltage and ultra low-voltage SAR ADC

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Dedico questa tesi ai miei amici del dottorato, che si sono dimostrati sempre persone leali, competenti ed altruiste. In particolare Matteo, Lorenzo, Riccardo e Valerio, con il quale ho condiviso ogni passo in questi 8 anni di università. La dedico altresì all'Italia, spesso trascurata, relegata ad essere mero contesto civico o addirittura considerata zavorra, in virtù di un senso di inferiorità che offusca l'eccellenza e le genialità che offre tuttavia al mondo intero

Glossary

ADC Analog-to-Digital Converter

ATI Asynchronous Time-Interleaved

CDAC Capacitive Digital-to-Analog Converter

CPB Charge Pump-Based

DAC Digital-to-Analog Converter

DNL Differential nonlinearity

DSP Digital Signal Processing

EDP Energy-Delay Product

ENOB Effective Number Of Bits

FOM Figure Of Merit

FVF Flipped Voltage Follower

HS High-Speed

ICMR Input Common Mode Range

INL Integral Non-Linearity

IoT Internet of Things

LP Low-Power

LPF Low-Pass Filter

LSB Least Significant Bit

LV Low-Voltage

MQMS Modified Quasi-Monotonic Switching

MS Monotonic Switching

MSB Most Significant Bit

PDP Power-Delay Product

QMS Quasi-Monotonic Switching

RF Radio Frequency

RMS Root-Mean Square

SAR Successive Approximation Register

SFDR Spurious Free Dynamic Range

SHIFT Sustainable tecHnologies enablng Future Telecom applications

SNDR Signal to Noise and Distortion Ratio

SNR Signal-to-Noise Ratio

T&H Track and Hold

THD Total Harmonic Distortion

TI Time-Interleaved

ULV Ultra-Low-Voltage

Abstract

In this thesis work several techniques to optimize SAR (Successive Approximation Register) ADC (Analog-to-Digital Converter) performances have been investigated. The thesis work has been focused on two vertical topics: high speed SAR ADC and LV (Low-Voltage) and ULV (Ultra-Low-Voltage) ADC. The structure of the work is based on the research activity carried out in the three years of the PhD. The first activity that was carried out is the design of an HS (High-Speed) SAR ADC that has been realized in foundry. Subsequently, much of the activity has been focused on the development of innovative techniques and topologies aimed at the optimization of LV and ULV dynamic comparators, then a complete ULV ADC has been realized with one of this comparator, finally a wide band LPF (Low-Pass Filter) for analog front-end of HS ADC has been realized. The document is structured as follows:

The first chapter introduces the work describing the context and the state of the art of the ADC in general and of the SAR ADC in particular. The chapter reports the aims of this thesis and describes the content of all the chapters.

The second chapter contains a theoretical introduction to the ADC in general, reporting the working principles, applications, main characteristics and definitions. The chapter deepens the analysis of the SAR ADC, describing the building blocks and in particular the dynamic comparators.

In the third chapter of the thesis, a 166 MS/s 10 bit $V_{DD} = 1\text{ V}$ fully differential SAR ADC has been designed and tested. The design has been sent to the foundry to be realized within an integrated circuit. The ADC shows good performance in terms of accuracy despite its FOM (Figure Of Merit) is not competitive. The design of this SAR ADC allowed to validate an innovative switching algorithm used to optimize conventional Strongarm comparator performances.

The fourth chapter presents a 6.67 MS/s 8 bit $V_{DD} = 0.4\text{ V}$ fully differential ULV SAR ADC. The chapter describes the ADC architectures and every building block, with particular emphasis on the dynamic comparator that is the most innovative element of the ADC. Finally reports the post-layout simulation results both for the comparator and the ADC, highlighting the competitive performances in terms of speed at a supply voltage as low as 0.4 V.

The fifth chapter is dedicated to a survey of LV and ULV comparators. A series of innovative topologies and techniques to optimize the speed-consumption trade-off at Low and Ultra low supply voltage are presented in this chapter. Detailed theoretical models on the delay behavior of the Strongarm based ULV comparator are presented in this chapter. Particular attention was dedicated to the study of the comparator transistors operating in sub-threshold region and to the study of the CPB (Charge Pump-Based) dynamic biasing. All the presented comparators have been simulated (almost all with post-layout simulations) and the performances that have been evaluated are competitive with the state of the art.

In the sixth chapter of the thesis a 17 GHz inductor-less LPF has been designed and tested, the LPF is an innovative topology based on a modification of conventional Sallen-key topology. This topology involves the internal poles of the amplifier in order to enlarge the bandwidth of the filter. The filter shows very competitive performance in terms of band, noise and linearity.

Ringraziamenti

Un ringraziamento sentito va a tutti i miei professori, che mi hanno trasmesso le conoscenze e la dedizione per scegliere ed affrontare il PhD, in particolare il mio advisor Francesco.

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Chapter 1

Introduction

1.1 Successive Approximation Registers Analog-to-Digital converters literature context and state of the art

1.1.1 The potentiality of SAR ADC

ADC conversion is ubiquitous in today's world. Due to the widespread of digital devices the need for the conversion from analog signal to digital has become pervasive. The ADC links the physical world to the digital domain, making possible complex data acquisition and analysis through digital devices. [104] In recent years, the wide diffusion of electronic devices such as laptops, tablets, and smartphones has significantly enhanced everyday tasks, including banking, booking, traveling, and remote work.

Figure 1.1 shows typical average performances range for the specific applications and figure 1.2 shows the typical performances of the main ADC topologies. No single ADC architecture dominates across all applications and performances; instead, the selection of a particular architecture depends on the specific performance requirements. ADCs generally fall into four main categories. Noise-shaping ADCs are ideal for high-resolution, low-bandwidth applications, while SAR ADCs excel in medium-resolution and low-to-medium sampling speed scenarios. For higher sampling speeds and resolutions, pipelined ADCs are preferred. Flash ADCs, meanwhile, are best suited for very HS but low-resolution tasks [39].

This thesis focuses on the SAR ADC, which is widely used in medium-to-high resolution and medium-to-high speed applications [133].

Contrary to some earlier predictions, the performance and energy efficiency of SAR ADCs have steadily improved over the past two decades. Although the SAR ADC architecture was invented over 40 years ago [84], it initially garnered little attention due to its speed limitations and its relatively high gate count, which was a concern for energy consumption at the time. However, its predominantly digital architecture has made it particularly well-suited to benefit from technology scaling, more so than other ADC architectures. This has led to a resurgence of interest in SAR ADCs since around 20 years ago, coinciding with the advent of 65nm CMOS technology [105]. As can be found in [97] an analysis about the recent literature reveals that SAR ADCs have dominated in the past decade.

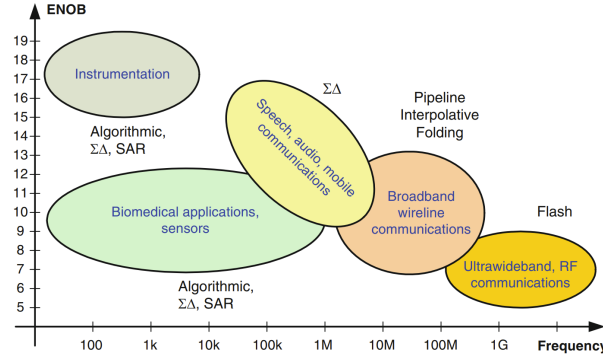


Figure 1.1. Application distribution over performances plot [113]

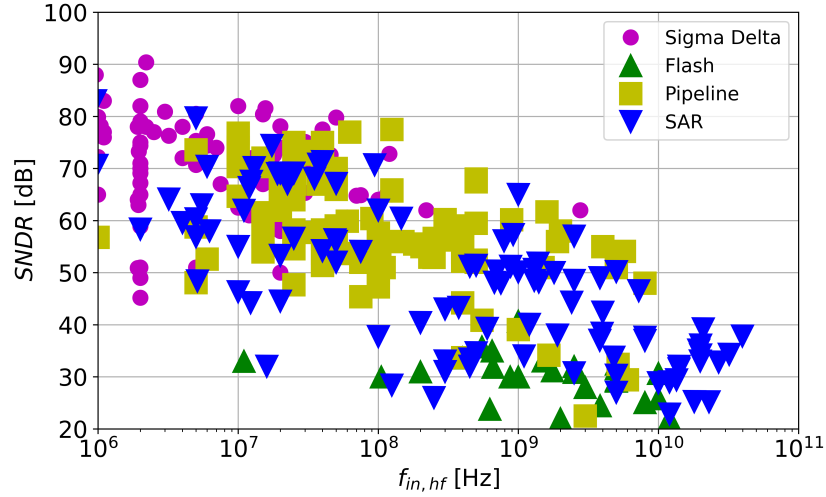


Figure 1.2. ADC topologies performances distribution from ADC survey data available in [97]

Thanks to technology scaling, ADCs have seen a dramatic improvement in energy efficiency. A commonly used metric to evaluate this efficiency is the Walden FOM, defined in the theory section of this thesis (see paragraph 2.1.4). The most power-efficient ADCs in recent years are predominantly SAR ADCs, which explains their widespread adoption in applications such as the IoT (Internet of Things), industrial systems, healthcare, and scientific instrument, especially where high energy efficiency is critical. [133]

Despite technology scaling has played a pivotal role in driving these energy efficiency improvements, it is not the sole factor. An important contribution in optimizing SAR ADC performances has come from innovative engineering and design techniques at both the architectural and circuit levels. Researchers have introduced numerous critical innovations that have enabled this substantial energy reduction while maintaining or enhancing the performances.

1.1.2 Wide band TI ADCs and filters

Higher frequency SAR ADCs are extensively utilized in various electronic systems, including instrumentation, disk read channels, HS serial links, optical communications, and wide-band radios. The ADC plays also a crucial role in the analog front end of wireless and wired transmission systems, often requiring high performance, with bandwidths extending into the hundreds of MHz [64] [21].

Top-end digital storage oscilloscopes (DSOs), HS optical data-links, and wide-band spectrum monitoring instruments utilize advanced digitizers capable of delivering real-time ultra-wide bandwidths of up to 100 GHz and sampling rates exceeding 200 GS/s. The technologies that meet these demanding requirements and drive the pursuit of higher performance include TI (Time-Interleaved), digital bandwidth interleaving (DBI), ATI (Asynchronous Time-Interleaved). These methods enable the development of digitizers with complex architectures and multiple channels, where the digital data from each channel are efficiently combined to generate a digital representation of the analog input [20].

TI converters require LPFs with cut-off frequencies in the GHz range, serving as anti-aliasing filters in ADCs [77] [93].

Wide band filters for these applications must provide sufficient SNDR (Signal to Noise and Distortion Ratio), matching the specifications of the ADCs and DACs to prevent degradation of the system's noise and linearity performance. Integration demands a small area footprint, avoiding large integrated inductors to minimize parasitic effects and enable lumped-element analyses in multi-GHz circuits. Additionally, filter designs should rely on low-Q stages to mitigate the impact of parasitic elements and process variations [89].

ATI architectures [57,90,91] also require LPFs with cut-off frequencies in the tens of GHz range. The primary performance criteria for these filters include out-of-band suppression, necessitating the use of high-order filters, and maintaining sufficient linearity to avoid degrading the performance of the ADCs or DAC (Digital-to-Analog Converter)s. Additionally, power and area efficiency are crucial considerations, particularly when integrating the filters alongside the converters.

1.1.3 LV and ULV ADCs and comparators

Most of the IoT, wearable and biomedical devices are battery-powered or reliant on energy harvesting from the environment and so necessitate careful power optimization by reducing both current levels and supply voltages [29,30,65,139]. A critical factor for such devices is their autonomy, i.e., the duration for which they can operate without requiring a recharge. This aspect plays a crucial role in user decision-making when selecting a device and greatly affects its usability and convenience in diverse scenarios. Ensuring sustained and reliable performance over extended periods is fundamental for both device functionality and user satisfaction.

In scenarios such as IoT devices, wireless sensor networks, and System-on-a-Chip (SoC) systems, achieving high sampling rates while reducing the power consumption in the supply voltage remains crucial to support accurate, real-time data acquisition [73,123,151].

In the biomedical domain, there is growing interest in smart devices designed to

facilitate the study and diagnosis of neurological disorders [28, 33, 43, 50, 100, 131, 153]. Recent research has increasingly focused on implantable electronic systems capable of monitoring and diagnosing conditions such as Parkinson's, Alzheimer's, epilepsy, and others [72, 119]. These complex systems, typically implanted beneath the scalp and directly on neural tissue, must prioritize minimizing power dissipation to prevent overheating, which could cause irreversible damage to neural tissues [80, 127]. Consequently, biomedical signal acquisition systems should operate at supply voltages as low as 0.3V, with current consumption on the order of nanoamperes (nA) to ensure extended autonomy and safe temperature levels.

Among the essential components in both biomedical signal acquisition systems and smart devices in general are ADCs. Due to the limited capacity of batteries, power efficiency is paramount, making the SAR ADC a preferred architecture for its energy efficiency. Thus, the challenge of designing a SAR ADC that achieves both HS and high accuracy is increasingly pressing [64].

A SAR ADC core consists of three primary circuit blocks: a comparator, a capacitive DAC, and SAR logic. In an optimized LP (Low-Power) SAR ADC, the power consumption is evenly distributed across these blocks. Therefore, to achieve significant power reductions, the power consumption of each building block must be minimized. [133]

The performance of an ADC is, in most cases, closely linked to the characteristics of its comparator(s); hence, enhancing the figures of merit of these key components is crucial. The primary challenges in designing LV, LP comparators are associated with achieving high operating frequencies and ensuring a wide ICMR (Input Common Mode Range).

A dynamic comparator processes input signals through charge and discharge transients at its internal nodes, making transistors optimized for digital applications ideal for enhanced performance. Furthermore, dynamic comparators typically feature highly compact topologies that are quick to optimize and implement in layout, such as the Strongarm latch [58, 111] and the Elzaker comparator [136].

Several latched comparators capable of operating at supply voltages as low as 0.5V or lower have been proposed in the literature [15, 48, 51, 75, 85, 103]. These designs are often based on the Strongarm architecture [41, 46, 54, 55, 67, 74, 81, 107, 138, 145].

When the supply voltage is reduced, optimizing the delay becomes particularly challenging due to the reduced overdrive voltages, which limit the available supply headroom. Furthermore, when powered on, devices may enter the triode region because their drain-source voltages are insufficient. To mitigate these issues, circuit topologies have been explored that reduce the number of stacked devices compared to conventional designs [13] [34]. This approach increases the voltage headroom for each device, thereby improving peak current and reducing delay.

To achieve both rail-to-rail ICMR and LV operation, body-driven configurations have emerged as a promising technique [13] [34]. However, a significant drawback of body-driven comparators is the increased input-referred offset, which arises from the fact that the transconductance of the substrate terminals is much lower than that of the gate terminals. To address this issue, various offset calibration techniques can be employed.

A significant portion of recent literature on dynamic comparators focuses on the technique known as dynamic biasing, or energy biasing. This approach was first

introduced in comparators by Bindra et al. in [10] and was applied to the Elzakker comparator to alleviate the trade-off between power consumption and input-referred noise. The technique works by employing purely capacitive degeneration in the input differential pair, reducing the overdrive voltage (V_{ov}) of the input transistors during the dynamic preamplification phase. The underlying principle is that the gain of a dynamic amplifier is proportional to the g_m/I_D ratio of the input transistors, which increases as V_{ov} decreases [144].

While conventional dynamic biasing improves noise performance, it typically comes at the cost of increased delay, making it suitable for applications where speed is not the primary concern [10, 132]. Several studies have explored its application in HS systems to enhance accuracy without compromising delay [11, 13, 83]. For instance, Bindra et al. [11] propose a charge pump configuration applied to the tail capacitor of a two-stage dynamic biasing comparator. This configuration allows for a greater amount of charge to be sunk by the capacitor, which shortens the preamplification time and improves the maximum clock frequency of the circuit.

1.2 Aim of this work

1.2.1 topics covered by this thesis

In this thesis, scientific contributions are proposed aimed at the development and optimization of SAR ADCs which are divided into two main verticals:

- **High speed SAR ADC:** For this purpose two activities were carried out:
 - the design of a medium resolution HS ADC. It involves state of the art functional block topologies and innovative techniques. This research activity characterized the beginning of the doctoral path and was aimed at the creation of a complete ADC design with the final aim of realization in the foundry in the context of the SHIFT (Sustainable technologies enabllIng Future Telecom applications) project [1];
 - the design of a Wide band LPF. LPFs are widely used in HS ADCs as Anti-aliasing filter in the analog front-end of single-channel ADC and TI ADC. Nevertheless LPF are needed in ATIADC to suppress signal spectrum replica in the shifted band of each channel of the ATI;
- **Low voltage and Ultra LV SAR ADC:** The research activity of LV and ULV SAR ADC has been mainly focused on the development of novel techniques and topologies of LV and ULV comparator, that is one of the most important building block of the SAR ADCs. Nevertheless, a novel complete 0.4 V 8-bit 5 MS/s ULV ADC has been designed and tested in post-layout simulation.

1.2.2 Objectives definition

The thesis is composed of multiple sub-topics, all of them relating to the development of HS and ULV ADCs. This section aims to identify the sub-themes, placing them in the relevant vertical of reference and to define the main objectives for each sub-theme.

Complete development of HS SAR ADC design Aims of the activity

- progressive acquisition of the necessary skills in all phases of an integrated circuit SAR ADC design up to realization of the integrated circuit in the foundry;
- highlighting the major critical issues in the HS topologies and structures present in the literature in order to consequently concentrate research activities for the development of techniques and topologies capable of limiting these critical issues and optimizing performances;
- introduction of an innovative switching algorithm to optimize the performance of a conventional Strongarm comparator

Development of innovative topologies and techniques for LV and ULV comparators Aims of the activity

- design of novel comparator topologies able to overcome the operating frequency limits present in the literature for low and ultra-low supply voltages;
- design of novel comparator topologies optimized in terms of the speed-consumption trade-off, taking into account the main FOMs defined in literature (PDP (Power-Delay Product) and EDP (Energy-Delay Product)) ;
- development and validation of theoretical model of the novel techniques and of the techniques adopted in literature;
- validation of the theoretical models and of the topologies performances through post-layout simulations;

Complete development of ULV SAR ADC design Aims of the activity

- validation of a novel ULV comparator topology functionality within a complete SAR ADC system;
- combination of multiple ULV functional blocks and techniques in order to realize a competitive ULV ADC;
- validation of the comparator and ADC system performances through post-layout simulations;

Design of a novel wide band LPF Aims of the activity

- development of an innovative topology aimed at exploiting the internal poles of a Sallen-key amplifier;
- theoretical analysis of the novel quasi Sallen key topology;
- validation of the theoretical model and of the topology performances through post-layout simulations;

1.3 Thesis structure description

This thesis work is organized as follow:

- **Chapter 2** introduces ADC general theoretical principles and describes context, definitions and ADC applications. SAR ADC are described in details, with a section dedicated to the building blocks in particular to the comparators. Moreover there is an in-depth analysis on the context and definitions of HS and LV SAR ADCs;
- **Chapter 3** describes the design and the simulations results of the HS SAR ADC with a particular focus on the innovative switching algorithm. The ADC is a 10-bit fully differential charge redistribution SAR realized in CMOS STMicroelectronics 55 nm technology and optimized to work with $V_{DD} = 1\text{ V}$ and $f_S = 166\text{ MS/s}$;
- **Chapter 4** is a survey of LV and ULV comparator topologies and techniques. Every section describes the topology or the technique and reports the simulation results and the theoretical model and its validation;
- **Chapter 5** describes the design and the simulations results of the ULV SAR ADC with a particular focus on the innovative ULV comparator that as been developed and used in the block scheme. The ADC is a b-bit fully differential charge redistribution SAR realized in CMOS STMicroelectronics 55 nm technology and optimized to work with $V_{DD} = 0.4\text{ V}$ and $f_S = 5\text{ MS/s}$;
- **Chapter 6** describes the design and the simulations results of the wide band LPF. It is a 17 GHz inductor less LPF based on a modification of the Sallen Key topology.
- **Chapter 7** concludes the thesis, summarizing the results;

Chapter 2

ADC context, definitions and theoretical principles

2.1 What an ADC is

Definition of ADC An ADC is a device that makes possible the translation of analog signals to digital ones [135] [104] [45]. It is a fundamental element in every electronic system which involves any kind of digital elaboration, (an example of mixed-signals¹ system in figure 2.1).

In other words, an ADC is able to convert an analog signal, belonging to the continuous time and continuous voltage domain to a series of quantized voltage samples belonging to the discrete time and discrete voltage domain. With reference to figure 2.2, the analog domain is placed in the upper left quadrant whereas the digital domain is placed in the lower right one.

2.1.1 ADC definition and specification

ADC may be characterized based on several parameters, the main ones are defined below [135] [104] [45].

Resolution Resolution of an ADC indicates the number of bits of the digital output code, obviously an higher Resolution value means higher precision, at the cost of conversion speed and/or power consumption.

¹Mixed-signal is the field of electronics that concerns devices operating with combined digital and analog signals

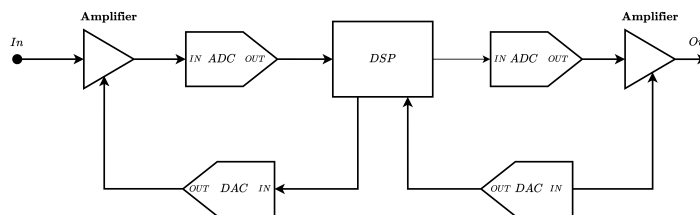


Figure 2.1. An example block scheme of mixed-signal system

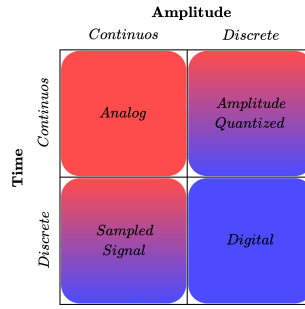


Figure 2.2. Continuous and discrete domains intersections plot

Sample frequency Sample frequency defines the ratio between number of samples and the time to convert them, higher is the sample frequency, higher are the input signal frequency the ADC is able to convert, according to Nyquist criterion.

Input Range The input range defines the minimum and maximum voltage levels that the ADC can convert into a digital value accurately. Matching the input range to the amplitude of the input signal is crucial to avoid clipping or under-utilizing the ADC's resolution.

SNR (Signal-to-Noise Ratio) SNR measures the ratio of the desired signal level to the background noise level, typically it is expressed in decibels (dB). A higher SNR signifies a clearer and more accurate representation of the analog signal. High SNR is essential for applications requiring precise measurements, such as audio processing and instrumentation.

THD (Total Harmonic Distortion) THD quantifies the distortion in the output signal due to harmonics of the input signal's fundamental frequency, expressed as a percentage or in decibels (dB). Lower THD values indicate better signal fidelity, which is critical for high-precision applications.

SFDR (Spurious Free Dynamic Range) SFDR is defined as the ratio, between the amplitude of the fundamental signal and the amplitude of the largest spurious component (harmonic or other distortion product) within the ADC output spectrum. SFDR is commonly expressed in decibels (dB) and provides an indication of the purity of the signal produced by the ADC, free from distortion.

Latency Latency refers to the time delay between sampling the analog input and the availability of the digital output. Low latency is crucial in real-time applications where timely data processing is vital, such as in digital communications and control systems.

DNL (Differential nonlinearity) DNL measures the deviation of the actual step size from the ideal step size. A DNL of zero represents perfect linearity. High DNL can result in non-monotonic behavior, where an increase in the input does not

correspond to an increase in the digital output, which is undesirable in precision applications.

INL (Integral Non-Linearity) INL evaluates the overall deviation of the ADC's transfer function from a straight line. It indicates the overall accuracy of the ADC across its entire input range. Lower INL values imply more precise conversions, which are essential for applications needing high accuracy over a wide input range. DNL and INL will be analyzed, more in detail, in the next subsection.

Power Consumption Power consumption refers to the amount of power the ADC uses during its operation. This is a critical factor in battery-operated and portable devices, where energy efficiency is paramount. Lower power consumption extends battery life and reduces heat generation.

Area Occupation Area occupation indicates the physical space the ADC occupies on an integrated circuit (IC). This characteristic is crucial in applications with limited space, such as mobile devices and compact electronics. Minimizing area occupation helps in integrating more functionality into smaller form factors.

Clock Frequency Clock frequency is the rate at which the ADC's internal clock operates, distinct from the sampling frequency. It impacts the ADC's processing speed and overall performance. Higher clock frequencies can enable faster data processing, but they may also increase power consumption and heat dissipation.

2.1.2 ADC characteristic

ADC samples analog signal at a frequency defined sampling frequency (f_s [S/s]) and associates corresponding digital sequence to each sample, based on the ADC characteristic. ADC resolution is the most important parameter of an ADC, it is the number of bits used to encode a sample, other specifications of the ADC structure will be analyzed in detail in the next sections. Figures 2.3 show a typical characteristic of a 3-bit ADC [135] [104] [45]

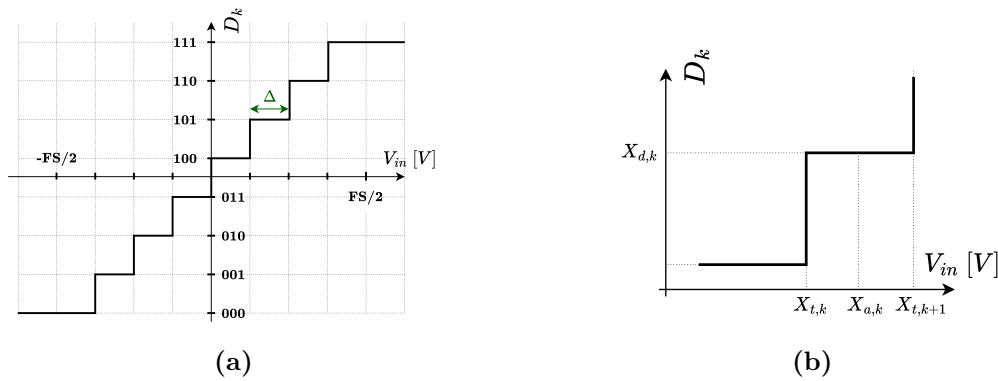


Figure 2.3. ADC characteristic definition.

Δ is the quantization step, it represents the amplitude of the analog voltage interval corresponding to each digital code, as in 2.3a,

$$\Delta = \frac{FS}{2^N} \quad (2.1)$$

with N number of bits of the ADC and FS full-scale² of the ADC. On the y-axis we have the corresponding digital codes $[D_k]$ for each analog interval:

$$D_k = \sum_{i=0}^{N-1} b_i \quad (2.2)$$

where b_j is the j^{th} bit.

The larger the number of bits the higher the resolution and so an ADC with more bits, at the same conditions, is more precise than one with fewer bits. With reference to figure 2.3b, considering a sample k , we have for any interval $X_{t,k}/X_{t,k+1}$ that

$$\Delta = X_{t,k+1} - X_{t,k} \quad (2.3)$$

Every analog sample belonging to this interval (that is: any $V_a \mid X_{t,k} < V_a < X_{t,k+1}$), is encoded with the same digital value D_k , but a single analog value is associated to D_k , that, in the ideal case, is the mean value of the interval and corresponds to the quantization step of the ADC Δ multiplied by the respective digital value:

$$X_{a,k} = \frac{X_{t,k+1} + X_{t,k}}{2} = \Delta D_k \quad (2.4)$$

2.1.3 ADC quantization error

As described in the previous chapter, since each analog interval is represented with a single digital value, to which a single voltage value is associated, it is obvious that, digitizing an analog sample leads to an error. This error is defined *quantization error* and its value corresponds to the difference between original analog voltage sample value and the analog voltage value associated to the digital value corresponding to the sample [135] [104] [45].

With reference to figure 2.4a, assuming $V_{in} \in [X_{a,k} - \Delta/2, X_{a,k} + \Delta/2)$, that means V_{in} belong to the interval $X_{t,k}/X_{t,k+1}$ and is digitized with the code D_k , the quantization error is $\epsilon_q = V_{in} - X_{a,k}$. the further V_{in} is from the center of the interval, the larger is the quantization error. In the absence of elements that can influence sampling of the signal, it can be assumed that quantization error has a uniform probability distribution centered in zero³ and with an amplitude of Δ . It is possible to calculate the ideal SNDR of an ADC, assuming the quantization error is the only source of distortion $SNDR = \frac{P_S}{P_D}$ with, P_S power of the signal and P_D power of distortion. Considering a sinusoidal signal, with a peak voltage equal to the ADC FS the result is:

$$SNDR = \frac{P_S}{P_D} = \frac{V_{pk}^2/2}{E[\epsilon_q^2]} = \frac{FS^2/2}{\Delta/12} = \frac{(\Delta * 2^N)^2/2}{\Delta/12} = 3 * 2^{2N-1} \quad (2.5)$$

²Full-scale of an ADC is the amplitude of the maximum voltage range ADC is able to convert

³This is the demonstration that, selecting the center of the interval as the representative value of the digital code is the best choice, in fact, in this way, quantization error has mean value equal to zero and its absolute value is minimized and is always smaller than $\Delta/2$

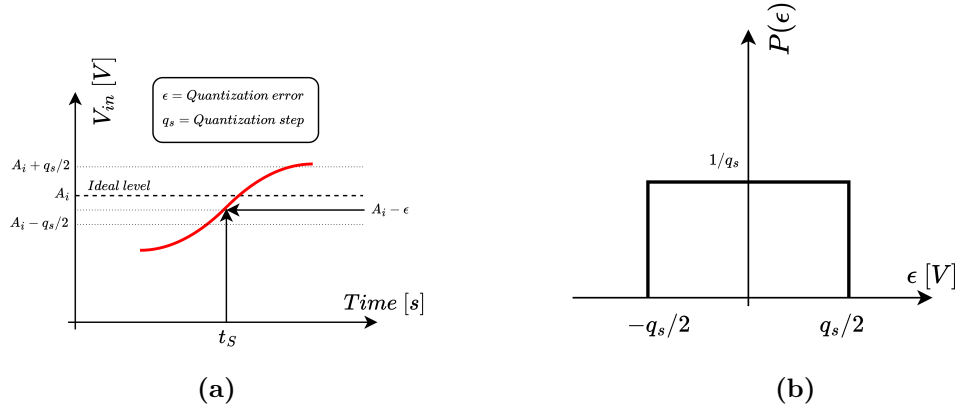


Figure 2.4. ADC quantization error a) trend of the quantization error, b) probability distribution of the quantization error

$$SNDR_{dB} \approx 6.02N + 1.76 \quad (2.6)$$

2.1.4 ADC non-ideal effects

Static characterization Static non-ideal effects of an ADC are based on static, linear and non-linear non-ideal effects on the characteristic. Figure 2.5 reports the non-ideal effects on ADC characteristic. Offset error simply shifts horizontally the characteristic (2.5a), gain error alters the slope of the characteristic (2.5b) [135] [45].

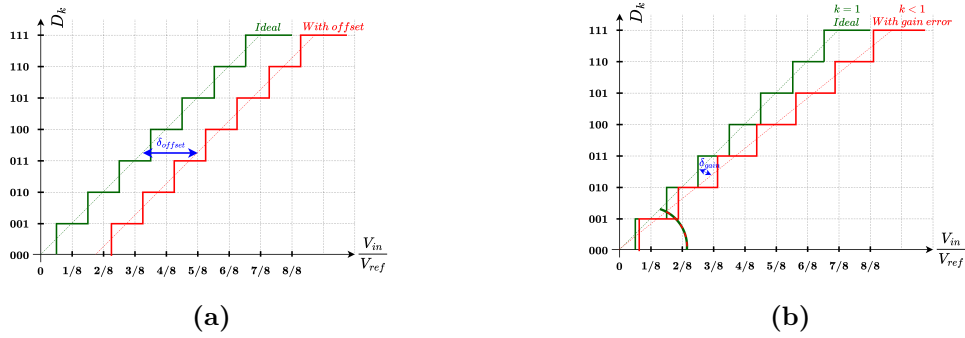


Figure 2.5. Offset (a) and gain (b) error on ADC

Figure 2.6 shows non-linear static non-idealities, thresholds are irregularly spaced, so there is no linearity in the error. Non linearity of the ADC characteristic can be evaluated by means of 2 indicators: DNL and INL. With reference to figure 2.6:

$$DNL[k] = \frac{X_{t,k+1} - X_{t,k} - \Delta}{\Delta} \quad (2.7)$$

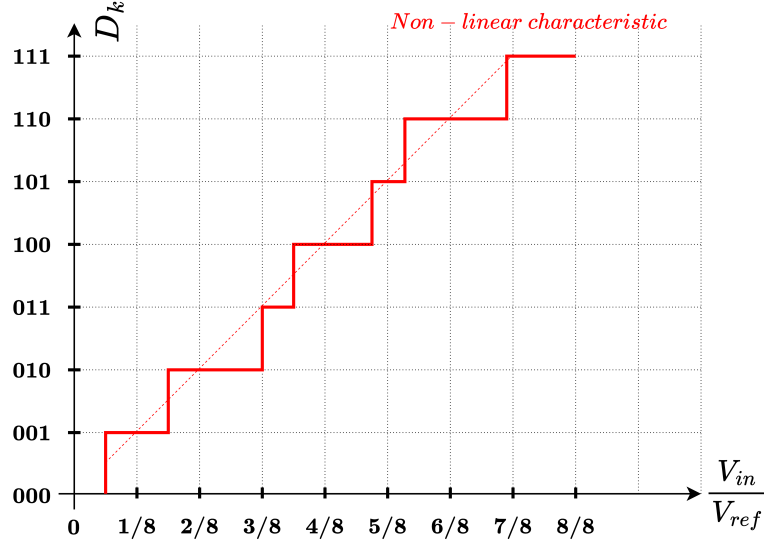


Figure 2.6. Offset and gain error on ADC

for the k^{th} step and with Δ ideal quantization step

$$INL[k] = \frac{X_{t,k} - \overline{X_{t,k}} - \Delta}{\Delta} \quad (2.8)$$

with $\overline{X_{t,k}}$ ideal characteristic threshold of k^{th} step

DNL and INL are linked by:

$$INL[k] = \sum_{i=1}^k DNL[i] \quad (2.9)$$

The sufficient condition for monotonicity (no missing or duplicate code) is:

$$|INL[k]| < \frac{\Delta}{2} \quad |DNL[k]| < \Delta \quad (2.10)$$

Dynamic characterization Dynamic non-ideal effects are inherent to noise and distortion in the ADC [135] [104] [45]. Between input signal of ADC and the analog signal associated to the digital output⁴ there is an error composed by quantization error ϵ_q , noise n and distortion ν : $V_{in} = V[D_{out}] + \epsilon_q + n + \nu$. To characterize noise effect the SNR is used

$$SNR = \frac{P_s}{P_n} \quad (2.11)$$

that is the ratio between signal and noise power. THD is used to characterize the effect of the harmonic distortion on the input signal. The distortion is caused by

⁴The analog signal associated with the digital output is the one that may be generated by an ideal DAC

the quantization error and by the distortion caused by the analog components of the ADC.

THD quantifies the non-linearity of the ADC as a ratio between the total amount of the distortion (evaluate as root-sum-square of all harmonic components), introduced by harmonics relative to the fundamental input signal, and the amplitude of the fundamental input signal.

$$THD = \frac{\sqrt{\sum_{i=2}^{\infty} V_i^2}}{V_1} \quad (2.12)$$

It is typically expressed in dB

$$THD = 20 \log_{10} \left(\frac{\sqrt{\sum_{i=2}^{\infty} V_i^2}}{V_1} \right) [dB] \quad (2.13)$$

SNDR is used to measure the quality of the signal after the conversion, It quantifies the total amount of error in the digitization process in terms of noise and distortion. SNDR is calculated as the ratio between fundamental input signal power and the combined power of all noise and distortion components

$$SNDR = \frac{P_s}{P_n + P_d} \quad (2.14)$$

It is typically expressed in dB. Considering 2.6, it is possible to define the ENOB (Effective Number Of Bits), assuming noise and distortion contribute to quantization error, this is the value equivalent of ADC resolution

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (2.15)$$

ADCs main FOM A lot of FOMs may be defined based on ADC characteristics [135] [104] [45], in the literature, the most used FOMs are Walden FOM (FOM_W) and Schreier FOM (FOM_S) defined as follows: These FOMs have the aim of sublimating the main characteristics of the ADC into a single parameter. The aim is to be able to carry out an immediate comparison between different ADCs on various specific parameters but with a holistic approach.

Walden FOM is defined as:

$$FOM_W = \frac{P_d}{2^{ENOB} f_s} \quad (2.16)$$

it takes into account ADC sampling frequency, ENOB and power consumption. The smaller Walden FOM the better the performance of the ADC.

With a similar approach Schreier FOM is defined as:

$$FOM_S = SNDR_{dB}(f_{nyq}) + 10 \log_{10} \left(\frac{f_s}{2P_d} \right) \quad (2.17)$$

it takes into account ADC sampling frequency, SNDR and power consumption. The larger Schreier FOM the better the performance of the ADC.

2.1.5 Sampling Theory of an ADC

Nyquist Criterion The sampling theory is fundamental for understanding the operation of an ADC. At the core of this theory lies the Nyquist criterion, which establishes the conditions necessary for accurately converting an analog signal into a digital form without losing information [135] [104] [45].

Nyquist Theorem The Nyquist theorem states that to accurately reconstruct a continuous-time signal from its samples, the sampling frequency (f_s) must be at least twice the highest frequency component (f_{max}) present in the signal. Mathematically, this can be expressed as:

$$f_s \geq 2f_{max} \quad (2.18)$$

This minimum sampling rate is known as the Nyquist rate. Sampling at or above this rate ensures that the original analog signal can be perfectly reconstructed from its samples. If the sampling frequency is lower than the Nyquist rate, the phenomenon of aliasing occurs, where higher frequency components of the signal are indistinguishably mapped to lower frequencies, distorting the reconstructed signal.

Aliasing Aliasing is a critical issue that arises when the sampling frequency is insufficient. It causes different signal frequencies to become indistinguishable from one another. The mathematical expression of an aliased frequency f_{alias} can be described as:

$$f_{alias} = |f - nf_s| \quad (2.19)$$

where n is an integer representing the number of times the frequency exceeds half of the sampling rate. Aliasing can be visualized as shown in Figure 2.7.

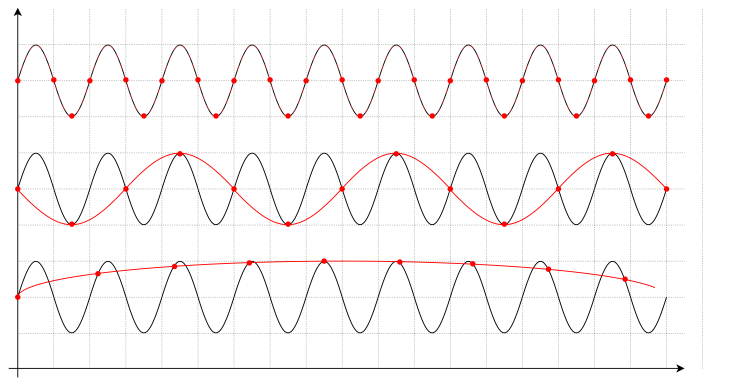


Figure 2.7. Illustration of Aliasing: When sampling below the Nyquist rate, different frequencies become indistinguishable. In the picture the original signal (black) is sampled at different rates. When the sampling frequency is too low and cannot respect the Nyquist criterion, the reconstructed signals (red) are incorrect (from the top, second and third waveform, suffer the effect of aliasing)

To mitigate aliasing, an anti-aliasing filter is often employed before the ADC to restrict the bandwidth of the input signal to below the Nyquist frequency, which is half of the sampling rate:

$$f_N = \frac{f_s}{2} \quad (2.20)$$

Reconstruction of the Signal When a signal is sampled at a rate satisfying the Nyquist criterion, it can be perfectly reconstructed using a LPF that passes frequencies up to the Nyquist frequency. The mathematical foundation for reconstruction is the Whittaker–Shannon interpolation formula:

$$x(t) = \sum_{n=-\infty}^{\infty} x[n] \cdot \text{sinc}\left(\frac{t - nT}{T}\right) \quad (2.21)$$

where $x[n]$ are the sampled values, T is the sampling period ($T = \frac{1}{f_s}$), and $\text{sinc}(x) = \frac{\sin(\pi x)}{\pi x}$. Figure 2.8 shows a graphical representation of the signal reconstruction process.

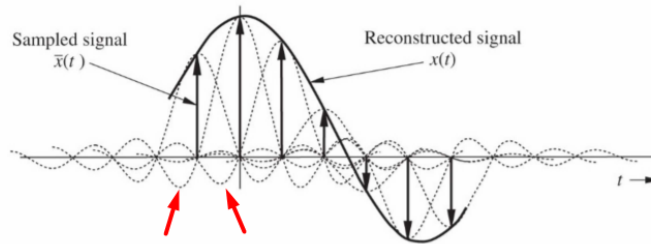


Figure 2.8. Signal Reconstruction: A continuous-time signal is reconstructed from its discrete samples using sinc interpolation [94].

Practical Considerations In practical ADC systems, achieving a perfect Nyquist rate sampling can be challenging due to various factors such as noise, jitter, and non-ideal filters. Therefore, oversampling is often used where the sampling frequency is significantly higher than the Nyquist rate. This simplifies the design of the anti-aliasing filter.

In conclusion, understanding and adhering to the Nyquist criterion is essential for effective analog-to-digital conversion, ensuring the integrity and accuracy of the digitized signal. By sampling at or above the Nyquist rate and employing proper filtering techniques, ADCs can effectively capture and reconstruct analog signals with high fidelity.

2.1.6 ADCs fields of application

ADCs have a fundamental role in modern electronics, converting analog signals into digital data that can be processed by digital systems. There are several fields of applications in which, depending on their structure and their characteristics, ADCs are involved [25, 27, 56, 66, 82, 95, 96, 128, 154] .

Consumer Electronics There are several products, in consumer electronics, that include ADCs in their circuits. They are mostly used in audio, video and in general multimedia devices but also in IoT devices, for the purpose of digitization of analog signal of the sensors.

Communication Systems ADCs are crucial in communication systems, both wired and wireless. They are used in mobile phones, transceiver stations, satellites and so on in order to digitize RF (Radio Frequency) modulated signals. ADCs are also fundamental in optic fiber and copper wire communications, converting analog signals into digital. Nevertheless, ADCs are involved in avionics and defense systems, like Radar and Beacon.

Medical and Biomedical Devices ADCs are involved in medical devices, like diagnostic instruments. ADCs are also used in biomedical wearable or sub-skin implanted devices, to digitize biological signals, like neural signals.

Process Control ADCs digitize sensor analog output signals (temperature, pressure, flow, etc.) into digital data for process monitoring and control.

Automotive Systems In modern vehicles, electronics plays a fundamental role, every part of the vehicles is monitored and controlled by electronic systems, ADCs are key components used to convert analog sensors signals to digital.

Electronic laboratory instrumentation and data acquisition system Every modern digital laboratory and measurement instrument involves ADC, for example multi-meter, oscilloscope, VNA (Vector Network Analyzer), SPA (Spectrum Analyzer) and so on. Designing ADCs for instruments with increasingly advanced characteristics is an engineering challenge.

2.2 SAR ADC

The SAR ADC is widely used for its balance between speed, accuracy, and power consumption. It operates by using a binary search algorithm to converge to the input signal level. The SAR ADC consists of a comparator, a DAC, and a SAR. SAR ADC topology is the core of the research activity reported in this thesis, it and each block that compose it will be described in detail in the next sections.

2.2.1 SAR working principle

The conventional conversion process involves the following steps:

1. The SAR sets the MSB (Most Significant Bit) and converts the digital value to an analog signal using the DAC.
2. The comparator compares this analog signal with the input signal.
3. Based on the comparator's output, the SAR retains or clears the bit.

4. This process repeats for each bit until the entire digital output is determined.

Figure 2.9 shows the output signals behavior during conversion, and figure 2.10 shows the conversion algorithm flowchart.

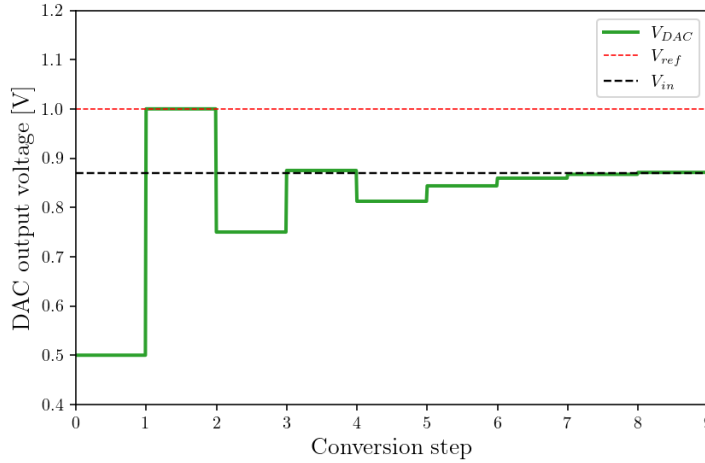


Figure 2.9. Output signal behavior in conventional single-ended SAR switching algorithm

2.2.2 SAR block scheme

The fundamental components of a SAR ADC are reported in the block scheme in figure 2.11; in particular there is a T&H (Track and Hold), that samples the signal at the edge of its clock and keeps its value during the conversion, the *comparator* used to compare the signal with the reference voltage, the DAC involved to convert digital output at every conversion step to analog signal and obviously the control logic and output registers, which manages the conversion algorithm and stores the output code, respectively.

2.2.3 SAR strength in modern literature

In most recent literature, the strength of SAR ADC is widely recognized due to several key factors:

1. **High Precision:** SAR ADCs are noted for their high-resolution capabilities, making them suitable for applications that require precise digital representation of analog signals.
2. **Energy Efficiency:** Their design relies on LP consumption, which is crucial for battery-operated and portable devices, ensuring longer operational life.
3. **Speed and Performance Balance:** While not the fastest, SAR ADCs offer a good trade-off between speed and accuracy, which is adequate for many practical applications, including data acquisition and communication systems.

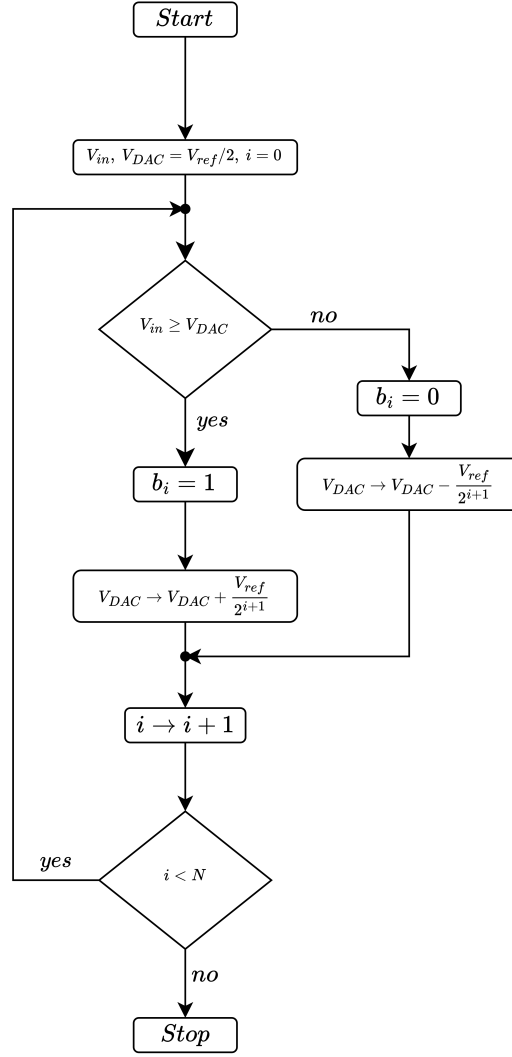


Figure 2.10. Flowchart of single-ended SAR switching algorithm

4. Technology scaling: SAR ADC performances are improved significantly along with the technology scaling, since in this ADC architecture there are no analog gain blocks.
5. Versatility: They are adaptable to a wide range of uses, from consumer electronics to industrial applications, due to their reliability and performance.

These attributes underscore the relevance and widespread adoption of SAR ADCs in contemporary research literature.

In support of what is described in the previous lines figure 2.12 shows the distribution of the different ADCs architectures FOM over the years and figure 2.13 depicts how the various ADCs architectures proposed in the literature in recent years are positioned on three plots in which the Cartesian axes are the ENOB, the sampling frequency or the power consumption.

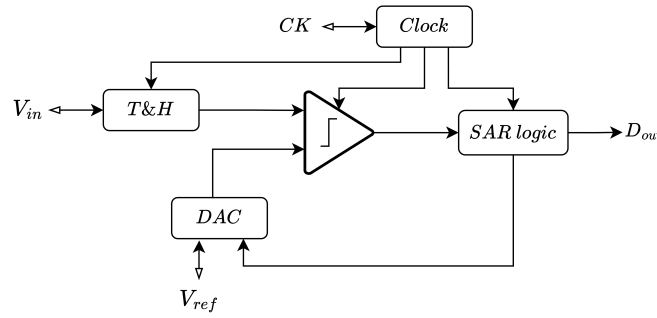


Figure 2.11. Block Diagram of a SAR ADC

2.2.4 Fully differential charge redistribution SAR

This thesis work is focused on the analysis and design of charge redistribution SAR, in particular, its fully differential version. In a charge redistribution SAR ADC, the DAC is implemented as a CDAC (Capacitive Digital-to-Analog Converter).

DAC, in SAR ADC, generates the voltage to be compared to the input signal, based on the partially generated output, at each conversion step. Each step resolves a bit of the output code. In charge redistribution SAR the DAC is a CDAC. The charge redistribution mechanism and the CDAC have received more attention in the recent years due to their better power efficiency than conventional resistive DAC. [104]

The block scheme of a fully differential charge redistribution SAR ADC is reported in figure 2.14. Fully differential topology offers several advantages, in terms of linearity, dynamic, rejection of common mode noise and degrees of freedom of the switching algorithm. In the fully differential topology of the SAR, T&H and CDAC are doubled, and each of them is connected to the comparator input. All of the SAR building blocks and the fully differential switching algorithm are described, in detail, in the next section.

2.3 SAR building blocks

In this section, the SAR building blocks are described more in details, in particular an entire section is dedicated to comparators, dynamic comparators have a key role in the research activities described in this thesis.

2.3.1 T&H of SAR ADC

T&H is a key component of all the ADC structures, it samples the signal at the instant it is triggered and keeps the sample during the conversion. Obviously T&H determines the bottleneck of overall ADC performances in terms of linearity and speed, in fact the samples converted by the ADC are collected by the T&H and so the distortions that it introduces set a limit on the minimum THD that the overall ADC can guarantee. Furthermore, if the T&H is too slow, it slows down the overall conversion process. [135] [104] [45].

Basic Configuration

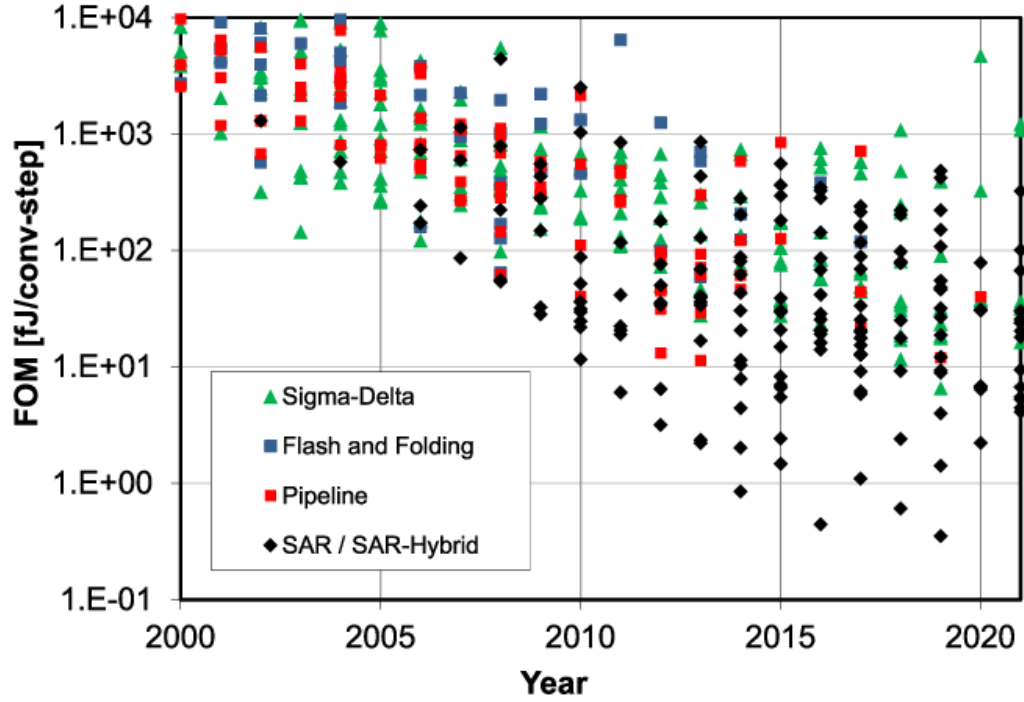


Figure 2.12. ADCs FOM distribution over the years [124]

- **Components:** The simplest T&H circuit includes a switch (S) with on-resistance (R_s) and a hold capacitor (C_H), it is reported in figure 2.15. The input voltage is sampled and held across the capacitor.
- **Key parameters:**
 - **Leakage:** a low leakage capacitor is crucial to minimize voltage droop and dielectric absorption.
 - **Bandwidth:** signal bandwidth is influenced by the switch resistance and source impedance. A reduced switch resistance improves performance. The bandwidth of the simplest T&H is: $f_{sdB} = \frac{1}{2\pi R_s C_H}$
 - **Acquisition Time:** The time required for the output to settle after a step change is affected by the switch resistance and source current, with reference to 2.15:

$$V_{out} = V_{in}(1 - e^{-\frac{t}{RC}}) \quad (2.22)$$

so the larger are R_s and C_H the slower is the settling of the output voltage.

- **Aperture Time Accuracy:** The precision of the sampling moment can be affected by finite rise and fall times of the sampling pulse, introducing distortion. Techniques such as bootstrapping or differential configurations can mitigate these effects.

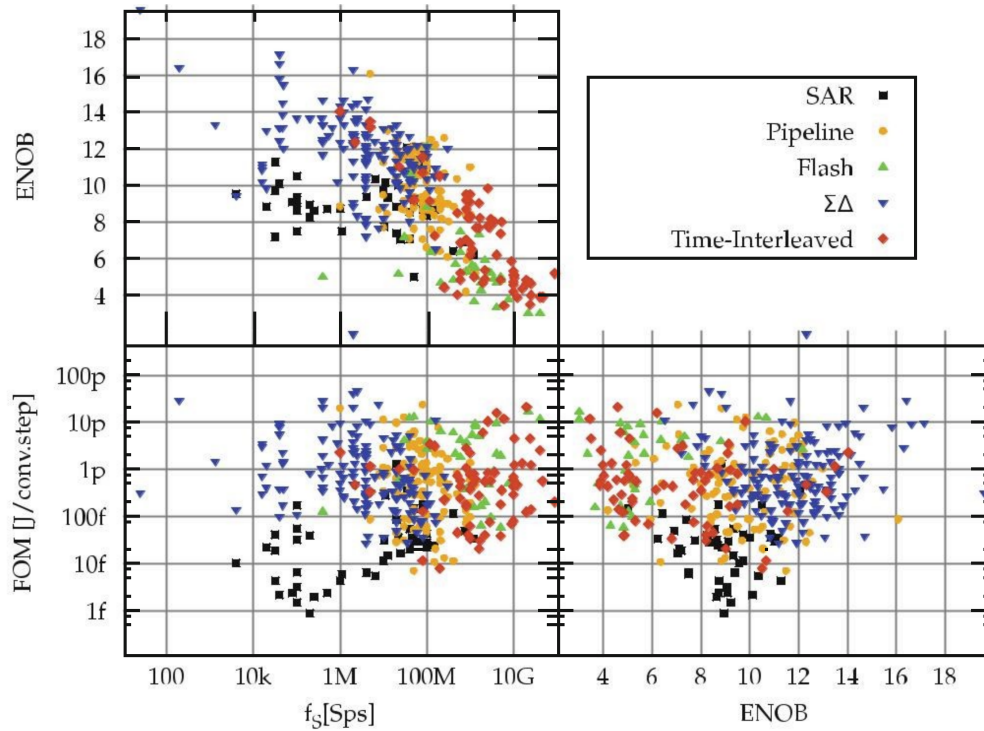


Figure 2.13. ADC performances comparison plot [124]

Performance Considerations

- **Signal Bandwidth:** The bandwidth is limited by the switch resistance and the output impedance of the source. Higher resistance can lead to reduced bandwidth and distortion.
- **Acquisition Time:** The time needed for the signal to settle to the desired accuracy is affected by the switch resistance and the capability of the input driver to supply sufficient current.
- **Slew Rate:** T&H characteristics are also determined by the slew rate, considering 2.15 maximum slew rate is: $\frac{dV}{dt} = \frac{I_{source}}{C_H}$ where I_{source} is the maximum current the source can apply to charge the capacitor.
- **Aperture Time Accuracy:** The sampling moment can be distorted due to the finite rise and fall times of the sampling clock, leading to non-uniform sampling intervals and potential distortion. Solutions include bootstrapping the control signal or using differential configurations.

Distortion Analysis

- **Sampling Moment Distortion:** Distortions arise from variations in the sampling moment due to the input signal and the rise/fall times of the clock. The distortion can be quantified and is influenced by the amplitude of the input signal, the rise time of the clock, and the clock amplitude.



- Bootstrapping** Increasing the amplitude of the sampling clock (V_{clock}) leads to a reduction in distortion, with a linear relationship where doubling V_{clock} results in approximately 6 dB of distortion reduction. While this may be sufficient for certain design constraints, further improvement might be necessary. A bootstrapping circuit can be used to enhance the sampling clock amplitude, as illustrated in Figure 2.16. In this circuit, the transistor labeled “Switch” acts as the sampling switch. When the input clock signal is high, the capacitor C_1 charges to $V_{dd} - V_{gs}$, and the output of the first inverter is low. This situation places transistor M_1 in the MOS diode mode, connecting one side of C_1 to V_{dd} . Transistor M_2 is off and the gate of the switch is set to ground through transistor M_3 . When the input clock signal becomes low, then the output of the first inverter becomes high. Capacitor is charged to about V_{dd} . This voltage adds to the output voltage of the first inverter and reverse biases the diode M_1 . The output of the second inverter becomes low and as a result transistor M_2 will be switched on and connects inverted clock voltage incremented

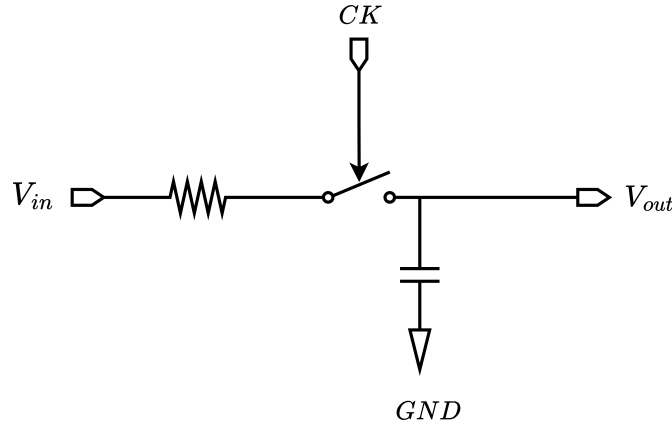


Figure 2.15. Basic structure of the simplest T&H

by the bootstrap capacitor voltage to the gate of the switch, this leads to about a doubling of clock voltage applied to the gate of the switch transistor. Bootstrap T&H circuits are described in this thesis, as part of SAR ADC structures designed for research purposes.

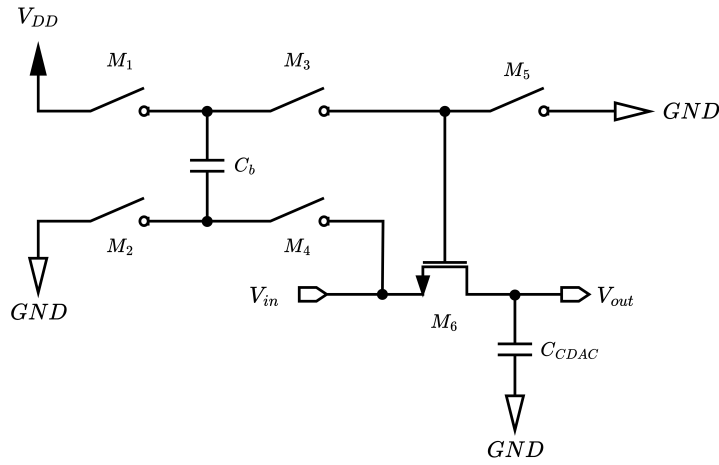


Figure 2.16. Example of T&H with bootstrap

2.3.2 DAC of SAR ADC

In charge redistribution SAR, the comparison signals update is slightly different to the conventional SAR. To understand how it works figure 2.17 is taken as reference.. [135] [104] [45].

CDAC working principle The CDAC is composed by a set of capacitors, of which, the capacitance values, are binary scaled ($1C, 2C, 4C, \dots, 2^{(N_{bit}-1)}C$ where C is the minimum capacitive unit value).

Top plates of all the capacitors are connected to T&H output and each bottom plate is connected to a switch controlled by the ADC logic, every switch can connect the capacitor to V_{ref}^+ or V_{ref}^- (V_{ref}^- is often GND) depending on its control signal. There is also another $1C$ capacitor, its bottom plate is connected to V_{ref}^- . For simplicity, in subsequent discussions, V_{ref}^- is assumed to be GND . When conversion starts, all the DAC switches are set to V_{ref}^+ , T&H samples the signal at the first clock edge of the conversion phase and the signal voltage is stored directly into all the CDAC capacitor that is:

$$C_{tot} = \sum_{i=0}^{N_{bit}-1} 2^i C + C = 2^{N_{bit}} C \quad (2.23)$$

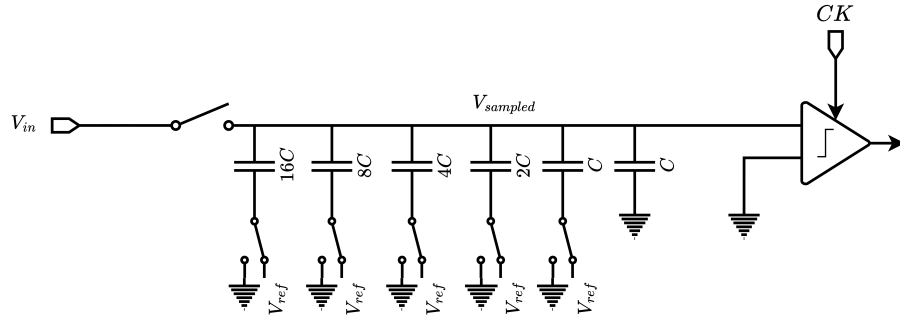


Figure 2.17. Example of charge redistribution SAR with CDAC

In the second phase of operation, the ground plates of the capacitors are switched to GND , one by one at each comparison step, by setting to high the respective bit, starting from MSB till the LSB (Least Significant Bit). When a plate is switched, the output voltage of the CDAC varies from V_{in} sampled at the beginning to:

$$V_{DAC} = V_{in} - \frac{2^{b_i-1}C}{C_{tot}} V_{ref}^+ \quad (2.24)$$

with b_i index of respective bit, so for example, for MSB :

$$V_{DAC} = V_{in} - \frac{V_{ref}^+}{2} \quad (2.25)$$

The demonstration of this relation is reported in the appendix in section A.1. If the output of the comparison is positive ($V_{DAC} > GND$) the respective bit, at each comparison step, is kept high and the switch remains on GND , otherwise the respective bit is set to low and the switch is set back to V_{ref}^+ .

CDAC noise The main noise sources in SAR ADC are the T&H, the comparator and the CDAC, the CDAC thermal noise RMS (Root-Mean Square) value is:

$$\sigma_{RMS} = kT/C_{tot} \quad (2.26)$$

with k thermal constant and T absolute temperature, obviously larger total capacitance means less thermal noise.

CDAC switches performance The CDAC capacitor switches may be implemented in several ways, the easiest implementation, in figure 2.18, is realized with a couple of PMOS-NMOS, in order to minimize on-resistance during the transient whether the input is GND or V_{ref} , avoiding saturation or interdiction during the output settling. Considering relation 2.22), the switch for a CDAC capacitor should have the lowest on-resistance possible, larger transmission gate transistors mean lower on-resistance at the cost of larger parasitic capacitance.

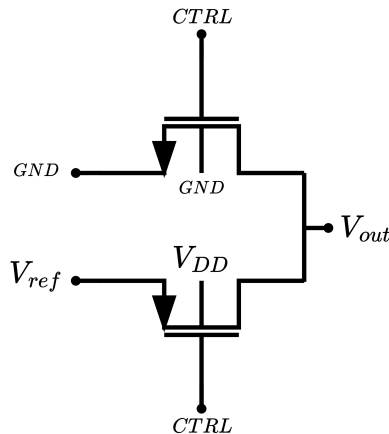


Figure 2.18. Typical CDAC switching scheme

Design considerations for CDAC Since every bit weight is directly proportional to every capacitor ratio in the CDAC it is clear that, the characteristic linearity of a charge redistribution SAR is very susceptible to parametric mismatch variations and parasitic effects. Parasitic effect can be calibrated by the designer thanks to a design centering process based on parasitic extraction tool of the simulator, but mismatch variations have to be taken into account during the formulation of the specifications. The designer must consider that, larger capacitors in the CDAC imply less degradation in linearity due to the reduced parasitic effects and mismatch variation and better performance in terms of noise at the cost of larger consumption and larger area occupation, for the same switch and T&H on-resistor, longer settling time of the output of the CDAC.

Bridge Capacitor The bridge capacitor technique consists of dividing the capacitors array into two sections placing a bridge capacitor between them. If the bridge capacitor is sized properly the capacitors values of the array section downstream of the bridge capacitor are perfectly scaled by a binary factor. In this way it is possible to implement small capacitance values with larger physical capacitors, in order to reduce parasitic capacitances and mismatch variations effect avoiding penalizing power consumption with large CDAC capacitors. Figure 2.19 shows an example of CDAC with bridge capacitor, C_b is the bridge capacitor.

In order to better understand how the bridge capacitor technique works, consider figure 2.20 in which, C_b is the bridge capacitor and C_a is a generic capacitance

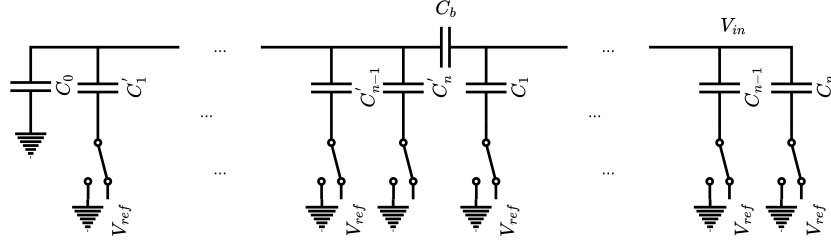


Figure 2.19. An example of CDAC with bridge capacitor

downstream of the bridge capacitor, in the CDAC.

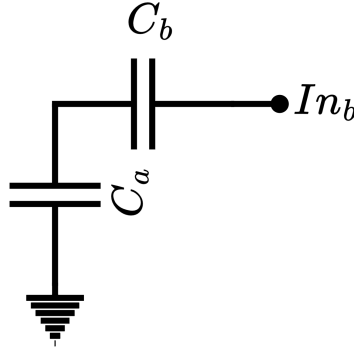


Figure 2.20. Simplified schematic of the bridge capacitor.

The equivalent capacitance C_{ds} at node In_b is:

$$C_{ds} = \frac{1}{\frac{1}{C_a} + \frac{1}{C_b}} = \frac{C_a C_b}{C_a + C_b} \quad (2.27)$$

Considering bridge CDAC of figure 2.19, it is necessary to divide by 2^n the split array capacitance downstream to the bridge capacitor in order to have :

$$C'_n = \frac{1}{2} C_1 \quad (2.28)$$

$$C'_{n-1} = \frac{1}{4} C_1 \quad (2.29)$$

$$\dots \quad (2.30)$$

$$C'_{n-j} = \frac{1}{2^{j+1}} C_1 \dots \quad (2.31)$$

$$C_0 = \frac{1}{2^n} C_1 \quad (2.32)$$

and so on, ensuring binary scaling of all the array. To obtain this scaling factor it must imposed that:

$$C_{ds} = \frac{C_a C_b}{C_a + C_b} = \frac{C_a}{2^n} \quad (2.33)$$

$$C_{ds} = \frac{C_b}{C_a + C_b} = \frac{1}{2^n} \quad (2.34)$$

$$C_{ds} = \frac{1}{C_a/C_b + 1} = \frac{1}{2^n} \quad (2.35)$$

$$C_b = \frac{C_a}{2^n - 1} \quad (2.36)$$

where C_a is the overall capacitance of the downstream split array, that is, in this case:

$$C_a = C_0 + \sum_{i=1}^n C'_i = \sum_{i=0}^{n-1} 2^i C + C = 2^n C \quad (2.37)$$

so:

$$C_b = \frac{C_a}{2^n - 1} = \frac{2^n}{2^n - 1} C \quad (2.38)$$

2.3.3 SAR ADC logic and switching algorithms

2.3.4 Fully differential SAR ADC

As said in the previous sections, involving a fully differential topology to convert an analog signal into a digital signal, has a lot of advantages. One of these is the discrete number of possible switching algorithms that can be adopted to convert the input signal [129]. The switching algorithm mainly defines, how the inputs of the two CDAC are switched, during the conversion, in order to obtain the final digital output code. In a fully differential SAR, the signal to be converted is the differential signal between the two inputs, that are sampled on the respective CDAC capacitances thorough the respective T&H and then, at each clock cycle during the conversion, the inputs of the two CDAC are switched in order to minimize the difference of the two CDAC output voltages at the input of the comparator, till the LSB is reached.

In figure 2.21 an example of CDAC, with SAR registers is reported. The input of each CDAC capacitors switch is controlled by the respective SAR register. SAR register is typically implemented with a D Flip-Flop (DFF), its D input is driven by the comparator output and each output of the registers is updated, sequentially, at each conversion step at the clock signals (c_i) rising edges. The SAR registers clock signals c_i are provided by a state machine, the most used is the so called, *thermometric counter* that is simply a counter composed of a series of DFF that switch to high sequentially at each clock cycle with an auto-reset at the end of the conversion cycle. An example of 3-bit thermometric counter is reported in figure 2.22, c_0 is the signal that triggers the T&H and c_3 is the last rising edge, that stores the last comparison results into the respective SAR registers (there is no need to update the CDAC for the last bit). At each clock cycle a register of the thermometric counter switches to one, until the last one activates an asynchronous reset which returns all the bits of the sequence to zero.

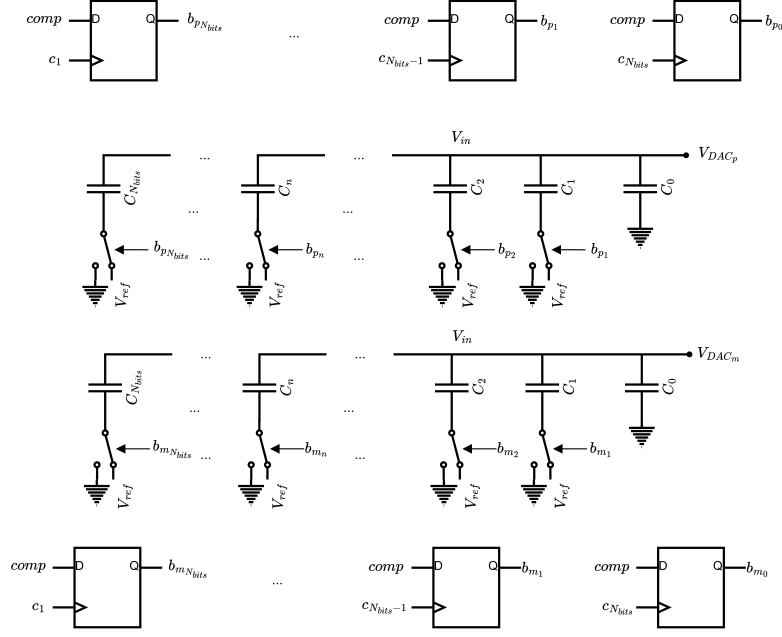


Figure 2.21. Simplified schematic of a fully differential CDAC, with SAR registers.

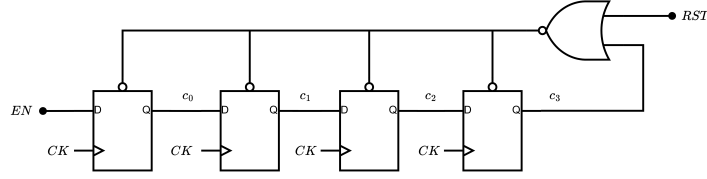


Figure 2.22. An example of 3-bit thermometric counter.

2.3.5 Switching algorithm

Following, a brief survey of the traditional switching algorithms and their difference is reported.

MS (Monotonic Switching) MS is the simplest switching algorithm for a SAR ADC. At the beginning of the conversion, when the signals are sampled by the T&H, CDAC inputs are all set to V_{ref} (or GND). After the inputs have been sampled, at each conversion step, the CDAC output with the larger (smaller) value of the two undergoes a negative (positive) voltage step with a value proportional to the current conversion bit. Figure 2.23 reports the CDAC output voltages transient behavior during the conversion in both descending (a) and ascending (b) cases.

MS is the simplest switching algorithm to perform a fully differential conversion, it requires the least number of logical components, however, there is no control over common mode voltage. Common mode voltage goes down or up (depending on the case) in monotonic way saturating to V_{ref} or ground. This behavior may be critical for comparator purposes, it may work in a stressful condition, degrading its performance.

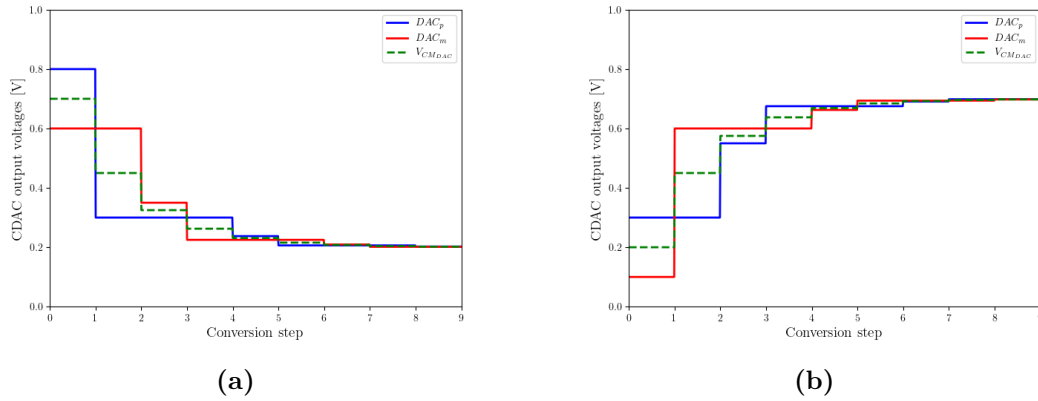


Figure 2.23. MS CDAC output voltages transient behavior a) descending case, b) ascending case

QMS (Quasi-Monotonic Switching) QMS is quite similar to MS, at the beginning of the conversion, when the signals are sampled by the T&H, CDAC inputs are all set to V_{ref} (or GND) except for the MSB that is set in the opposite way. The steps and the conversion logic are quite the same of MS but the first step transition occurs in the opposite direction, so if the MS scheme is descending, in the first conversion step lowest signal raises (in the same way of ascending MS) and vice versa. Figure 2.24 reports the CDAC output voltages transient behavior during the conversion in both descending (a) and ascending (b) cases.

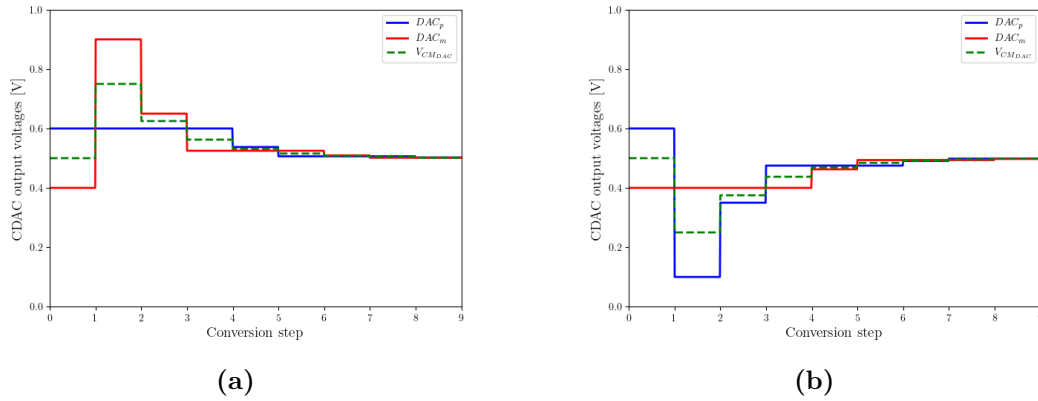


Figure 2.24. QMS CDAC output voltages transient behavior a) descending case, b) ascending case

QMS logic complexity is quite the same as MS, SAR registers with inverted output must be used for the MSB. Common mode voltage swing is reduced, compared to MS, but is still significant.

Generalized QMS QMS may be generalized in order to adjust common mode voltage final value and swing behavior, to do this it is sufficient to invert the behavior of other bits in addition to the MSB. In this way common mode voltage may be increased or reduced. Figure 2.25 shows an example assuming, MSB, LSB

and one other bit are reversed.

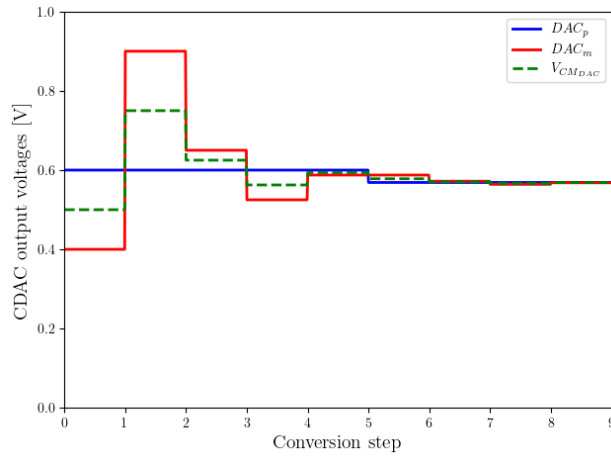


Figure 2.25. An example of generalized descending quasi MS

Split- MS Split MS (SMS) scheme makes possible maintaining a fixed common mode voltage during the conversion by means of the doubling of the CDAC arrays. Figure 2.26 shows the CDAC scheme. The control logic is exactly the same of conventional MS. For each bit in the CDAC there are two identical capacitors both with common bottom plate and with one switch on the top plate, one set to V_{ref} controlled by bottom registers and one set to GND controlled by top registers. For the other CDAC input, top and bottom registers control signals are switched. At each conversion step, the respective voltage step is divided equally between the two CDACs (so, for the MSB for example, instead of increasing the smaller voltage by $V_{ref}/2$ or reducing the larger one by $V_{ref}/2$, the smaller is increased by $V_{ref}/4$ and the larger is reduced by $V_{ref}/4$ at the same time). In this way, the initial common mode input voltage is maintained during all the conversion cycle. Figure 2.27 shows an example of this.

2.4 SAR ADC comparators

A comparator is a key component in ADC structures, it is the main block involved in the translation from analog to digital domain. The comparator is a mixed-signal component with two analog inputs and one or two complementary digital outputs. It has the purpose of comparing input signals and driving the outputs depending on the sign of the input differential-mode voltage [104].

2.4.1 Static and Dynamic comparators

Static comparators Static comparators are characterized by their continuous operation and stable behavior over time. These comparators maintain a constant bias current during their operation, which ensures accurate comparisons, independent of the timing of input signals. The decision-making process of static comparators

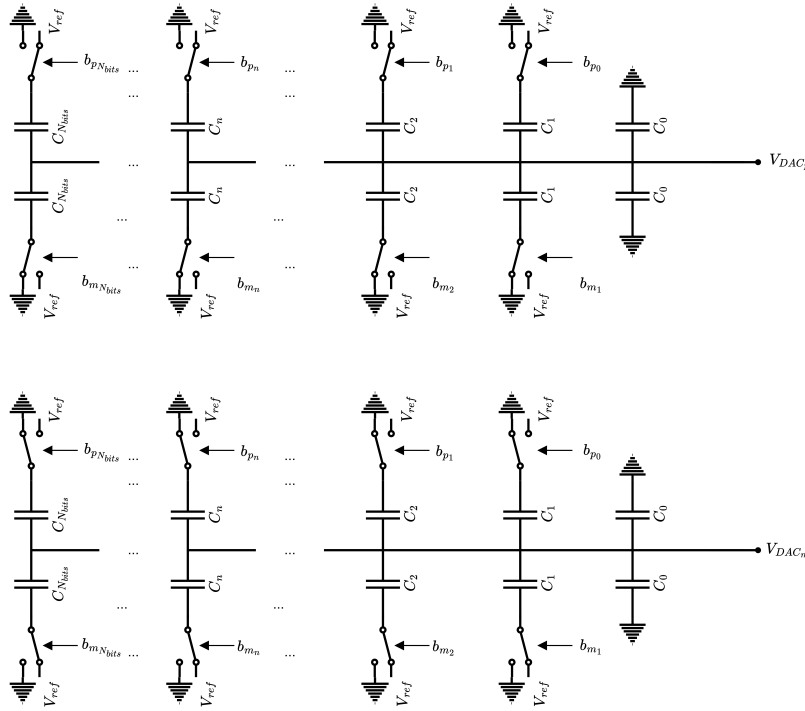


Figure 2.26. Split CDAC scheme

does not depend on any clock signal, making them suitable for applications where low-speed and high-accuracy operations are required. However, static comparators generally consume more power compared to dynamic comparators due to the continuous current flow. Moreover, they tend to have slower operation speeds [104].

Dynamic comparators Dynamic comparators, in contrast, operate based on clock signals, which trigger their decision-making process. These comparators are typically faster and more power-efficient than static comparators because they only consume power when the clock is active. The use of positive feedback during decision-making enables higher-speed operation and reduced latency, making them suitable for high-speed ADCs. Nevertheless, dynamic comparators may introduce meta-stability issues or errors when the input signals are close to the reference voltage, as their accuracy is somewhat dependent on the timing of the clock.

Main differences between static and dynamic comparators The fundamental difference between static and dynamic comparators lies in their power consumption and speed characteristics. Static comparators are power-hungry but offer high accuracy, whereas dynamic comparators are optimized for speed and power efficiency, making them ideal for high-speed applications. Additionally, the clocked operation of dynamic comparators introduces design trade-offs regarding the robustness of their decision-making process under varying input conditions [104].

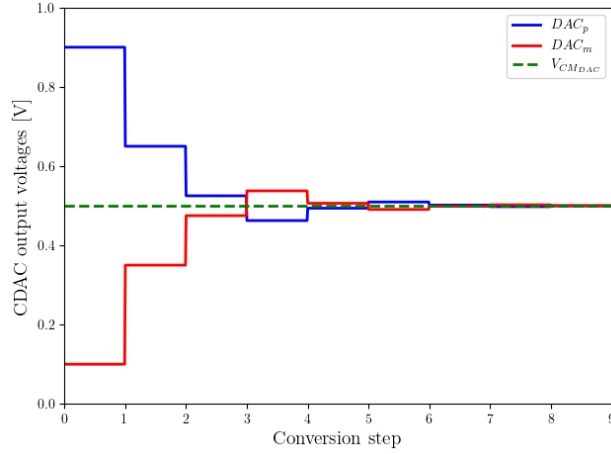


Figure 2.27. An example of split MS

2.4.2 Main types of dynamic comparators and working principles

There are a lot of dynamic comparators topologies in literature, which differ in a series of characteristics such as delay, maximum operative frequency, power consumption and so on. Following, is a survey of the main ones and their working principles [35, 116, 120].

Strongarm Latch Comparator The Strongarm latch, first introduced by Razavi [112], is one of the most widely used dynamic comparator topologies in SAR ADC architectures due to its simplicity, zero static power consumption, and high-speed performance. The basic structure of the Strongarm latch, reported in figure 2.28, consists of a cross-coupled inverter pair (M_3 - M_6), an NMOS differential pair at the input stage (M_1 , M_2), a clocked tail transistor (M_7) and a group of reset transistors (S_1 - S_4) connected to output and internal nodes.

Operation Principle The operation of the Strongarm comparator can be divided into three distinct phases: the reset (or pre-charge) phase, the pre-amplification phase and the evaluation phase.

- **Reset Phase:** When the clock signal is low, tail transistor is off, and current cannot flow in the latch and differential pair transistors, so there is no static consumption. During this phase, the output (V_{on} , V_{op}) and internal (p , q) nodes of the comparator are pre-charged to the supply voltage by means of reset transistors, avoiding the so called dynamic offset, that is a memory effect that makes internal and output nodes unbalanced in the next comparison, introducing a signal dependent offset.
- **Pre-amplification Phase:** When the clock signal toggles, the tail transistor turns on, and the circuit enters the pre-amplification phase. The input differential pair (composed of the two NMOS transistors) amplifies the difference between the input signals by discharging internal capacitances on nodes p and

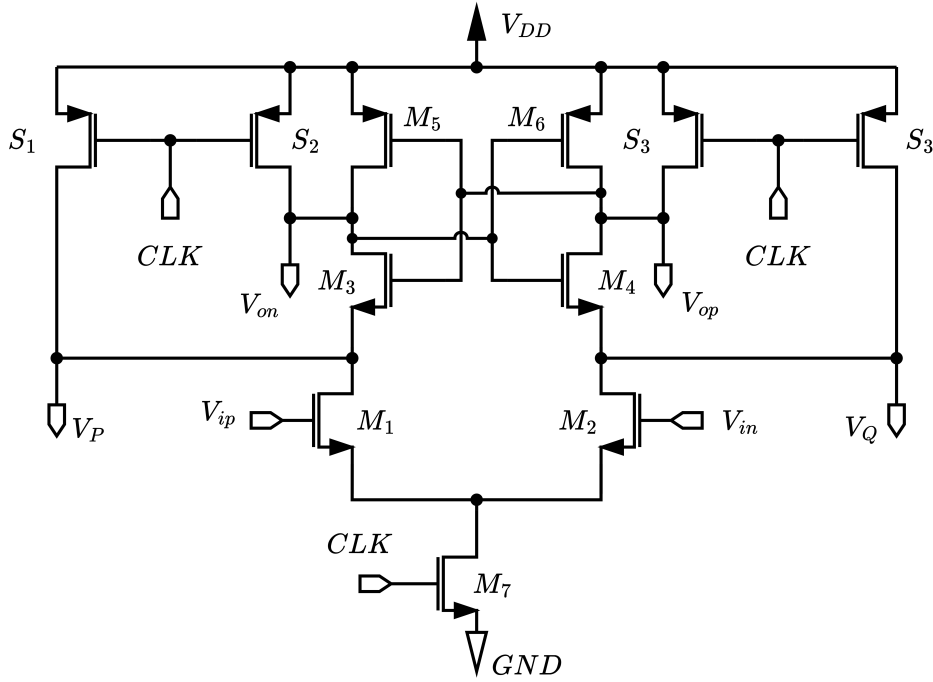


Figure 2.28. Schematic of the conventional Strongarm

q. This phase ends when the voltage of the internal nodes is such as to allow the latch transistors to turn on

- **Evaluation Phase:** At this point internal nodes *p* and *q* are unbalanced, The cross-coupled inverters provide positive feedback, which rapidly saturates the output to either the supply or ground, depending on the polarity of the input difference.

This architecture achieves high speed due to the regenerative feedback in the cross-coupled inverter pair, and it only consumes dynamic power during the evaluation phase. However, the Strongarm latch suffers from certain drawbacks, such as large input-referred kickback noise, which arises from the strong coupling between the input and output nodes during the regeneration process. This noise can degrade the performance of the comparator, especially in precision applications. Moreover, Strongarm comparator is not a good choice in LV applications due to the limited ICMR and the large number of stacked devices which leads to a rapid degradation of performance when the supply voltage is reduced [13].

Performance Metrics The Strongarm latch is known for its high speed, LP consumption, and small area. However, its performance can be affected by supply voltage variations and mismatches in the input transistors, which can result in offset voltage. Various techniques, such as offset cancellation circuits, have been proposed to address this issue.

Double-Tail Dynamic Comparator An alternative dynamic comparator topology commonly used to address some of the limitations of the Strongarm comparator is the Double-tail comparator. It was first introduced in [122]. This comparator improves upon the Strongarm architecture by decoupling the reset and evaluation functions using a double-tail structure, thereby enhancing its performance under low supply voltages by reducing the number of stacked devices. Moreover, by decoupling the two stages it is possible to bias them with different currents, in this way it is possible to reduce input pair current and increase latch bias current, for fast latching.

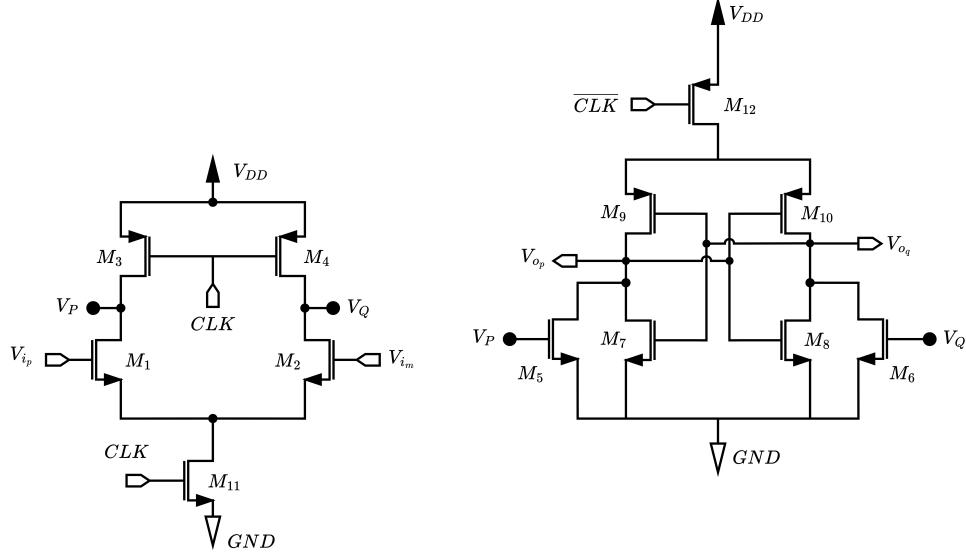


Figure 2.29. Schematic of the double-tail comparator

Structure and Working Principle The double-tail comparator schematic is reported in figure 2.29, it consists of two stages, each with its own tail transistor. The first tail transistor (M_{11}) is connected to the input differential pair (M_1 - M_2), while the second tail transistor (M_{12}) is connected to the latch stage (M_7 - M_{10}). Transistors M_3 - M_4 reset the internal nodes V_P and V_Q during the reset phase, and transistors M_5 and M_6 work like reset transistors of the output nodes during the reset phase and like pass transistors, that transmit the outputs of the first stage to the second, during the evaluation phase. This design separates the input and output stages, enabling faster operation and improved robustness to supply voltage variations.

The operation of the double-tail comparator is quite similar to the Strongarm one. It can be divided into three distinct phases: the reset (or pre-charge) phase, the pre-amplification phase and the evaluation phase.

- **Reset Phase:** During the reset phase, both tail transistors are off, the internal nodes are pre-charged to V_{DD} through the PMOS transistors (M_3 - M_4) connected to the supply voltage. In this way, M_5 and M_6 act like reset transistors, discharging the output nodes to GND , ensuring that the latch is reset properly.

- **Pre-amplification Phase:** When the clock signal toggles, the tail transistors turn on, and the circuit enters the pre-amplification phase. The input differential pair amplifies the difference between the input signals by discharging internal capacitances on nodes V_P and V_Q . This phase ends when the voltages of the internal nodes are such as to turn off M_5 and M_6 and so to allow the latch transistors to make the decision. M_5 and M_6 V_{gs} drop asymmetrically, depending on the first stage input, and so the final decision of the latch depends on the input differential signal.
- **Evaluation Phase:** At this point M_5 and M_6 are off, The cross-coupled inverters provide positive feedback, which rapidly saturates the output to either the supply or ground, depending on the polarity of the input difference.

Advantages and Limitations The double-tail comparator offers several advantages over the Strongarm latch:

- **LV Operation:** The double-tail structure enables better performance at lower supply voltages, as the input and latch stages are decoupled. This allows the input differential pair to operate efficiently even when the latch is weakly driven, which is particularly useful in ULV designs.
- **Reduced Kickback Noise:** By separating the input and output stages, the double-tail comparator significantly reduces kickback noise, improving accuracy in precision applications.
- **Power and Speed Trade-off:** While the double-tail comparator consumes slightly more power than the Strongarm latch due to the additional tail transistor, it provides better power-speed trade-offs, especially in applications where LV operation is critical.

There is an intrinsic limitation due to the coupling method of the two stages in fact, at the end of pre-amplification phase M_5 and M_6 are about to switch to off since their V_{gs} is approaching the sub-threshold value but, this is also the moment in which the unbalancing of V_P and V_Q is maximum and so, the designer might pay attention to the sizing of the transistors in order to optimize the transmission between the two stages.

Elzakker Dynamic Comparator Elzakker comparator [137] is a variant of the Double-tail comparator. It overcomes the limitation of the Double-tail due to the coupling method of the two stages. The working principle is similar to the one of the Double-tail comparator.

Structure and Working Principle The Elzakker comparator schematic is reported in figure 2.30, it consists of two stages, the first one is identical to the double-tail comparator (S_1 and S_2 are the reset transistor) second stage is similar but not identical, in fact, there are two additional PMOS (M_5 - M_6) interposed between NMOS (M_3 - M_4) and PMOS (M_7 - M_8) of the latch and transistor. They are controlled by the output voltages of first stage (V_P and V_Q). Transistors S_3 and

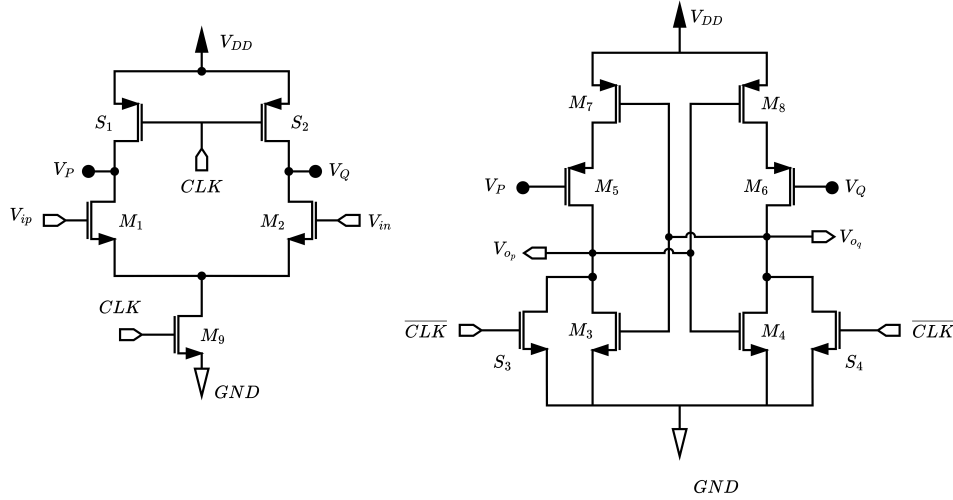


Figure 2.30. Schematic of the Elzaker comparator

S_4 are just reset transistors driven by $\overline{CLK}$ signal and not connected to the first stage. In this design coupling between first and second stage is improved, enabling faster operation and improved robustness.

The operation of the Elzaker comparator is quite similar to the double-tail one. The operation phases are the same, during pre-amplification phase the internal node voltages (V_P and V_Q) are transmitted to the second stage by means of transistors M_5 and M_6 . When V_P and V_Q are discharged so that M_5 and M_6 turn on, the latch starts to unbalance the output depending on the sign of differential voltage V_{pq} , that is obviously determined by the differential input of the transistors. Pre-amplification phase ends and evaluation phase starts, M_5 and M_6 are in saturation region so, at this point, the comparators works like double-tail.

Advantages and Limitations The Elzaker comparator clears the main limitation of the double-tail in fact, M_5 and M_6 are completely on when they reach the maximum unbalancing provided by V_P and V_Q , thus the coupling between first and second stage is improved.

2.4.3 Definition, characteristics and FOMs of the dynamic comparators

There are a lot of characteristics and FOM used to evaluate the performance of a comparator, following a survey of the main ones, specific for comparators, is reported [45, 104].

Delay This is one of the most important characteristics of a dynamic comparator. It defines the Δt between the clock rising edge and the output signal rising edge, thus the Δt between when clock signal crosses the threshold of 50 % of its peak value and output signal do the same (it makes no difference whether high and low transition). The figure 2.31 shows this definition graphically.

Maximum frequency This is also one of the most important characteristic for a dynamic comparator. It is the maximum possible clock frequency at which the comparator can function properly. It is directly conditioned by the delay.

ICMR The ICMR is the difference between the maximum and minimum input common mode voltage for which the comparator is able to work properly.

PDP The PDP is the product between delay and power consumption, it is a FOM defined in order to evaluate the trade-off between these two characteristics. Typically delay is reduced at the cost of increased power consumption (and vice versa) thus, PDP is a good indicator to evaluate this trade-off.

EDP The EDP measures the performance in a very similar way to the PDP but it is normalized with respect to the operating frequency of the comparator. Most of the comparator power consumption is directly proportional to the operative frequencies (more transitions in a temporal unit means more power consumption) therefore to make a comparison between two comparator topologies working at different frequency using EDP is more fair than using PDP.

Offset The offset, defines how much the comparator inputs are unbalanced due to mismatches and asymmetries, it represent an equivalent additive differential input voltage. Typically the offset is represented by a mean (μ_{off}) and a standard deviation (σ_{off}) value calculated by means of Monte Carlo simulation or by a set of measures of different chips of the same stock.

Noise The noise in a comparator is typically modeled as an equivalent input source and so it is defined by an RMS value that is the standard deviation of the input referred noise.

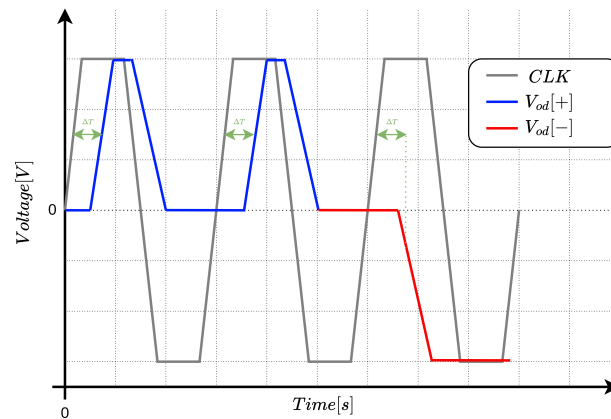


Figure 2.31. Diagram of the delay of a dynamic comparator

2.5 High speed and very high speed ADC

2.5.1 Context and Field of Applications of High-Speed ADC

High-speed ADCs play a critical role in a wide range of modern electronic systems, where fast and accurate digitization of analog signals is necessary. These ADCs are essential in applications such as telecommunications, where the advent of 5G and beyond has significantly increased the need for higher data rates and signal bandwidths. In such systems, high-speed ADCs are used to convert wide-band radio signals into digital form for further processing in base-band units. Furthermore, their role in high-frequency wireless systems, such as millimeter-wave communication, is pivotal, as they need to process signals at gigahertz frequencies.

In radar and defense systems, high-speed ADCs are vital for accurately capturing fast-moving targets by converting the analog radar signals into high-resolution digital data in real-time. These ADCs must handle large bandwidths and provide high sampling rates to meet the precision requirements of modern phased-array radar systems and electronic warfare applications.

Automotive systems, particularly in advanced driver-assistance systems (ADAS) and autonomous driving, rely on high-speed ADCs for radar and LIDAR signal processing. In these safety-critical applications, the ADCs must operate with both high speed and high accuracy to ensure timely and reliable decision-making. Additionally, high-speed ADCs are also utilized in various industrial applications, such as test and measurement equipment, where fast data acquisition and high resolution are paramount.

Nevertheless, modern digital laboratory instruments like VNA, SPA and DSO need very HS ADC to convert high band signals to be measured [98].

2.5.2 High-Speed ADC SAR: Literature Trends

As described in detail in the introduction in 1.1.2, recent trends in high-speed SAR ADCs focus on enhancing speed and resolution, often through time-interleaving techniques. SAR ADCs have gained increased relevance in the literature due to their ability to offer high resolution and energy efficiency at moderate to high sampling rates. As CMOS technology has advanced, SAR ADCs have become well-suited for applications in portable and energy-constrained devices, such as mobile systems and wireless communications.

The simple architecture of SAR ADCs allows for better scalability with shrinking technology nodes compared to other architectures like pipelined ADCs. Additionally, the use of digital correction techniques has improved their performance, allowing SAR ADCs to overcome mismatch errors, noise, and non-linearity at higher speeds. This makes them a promising option for achieving high-speed, high-resolution conversion with LP consumption [76].

2.6 ADC parallelization: Time Interleaving

TI SAR ADCs allow multiple ADC channels to operate in parallel, increasing the effective sampling rate. This technique is widely used to push SAR ADCs to

multi-gigahertz performance.

In synchronous TI, all channels share a synchronized clock, making phase alignment easier to manage, though careful calibration is necessary to mitigate timing skews. In ATI samplers, the word "asynchronous" means that the clock that drives the converters can be different and independent from the one that drives the front-end. ATI, while more flexible than TI, introduces challenges in data alignment and requires advanced calibration techniques to correct inter-channel mismatches [45, 76, 92, 101, 104].

2.6.1 Synchronous Time Interleaving

The idea is to use a high frequency clock and a clock divider to sample the signal using a set of ADCs, one ADC for each clock cycle until every ADC has been used. All consecutive digitized samples are then grouped together in the output thanks to a mux. [45]. This concept is illustrated in figure 2.32

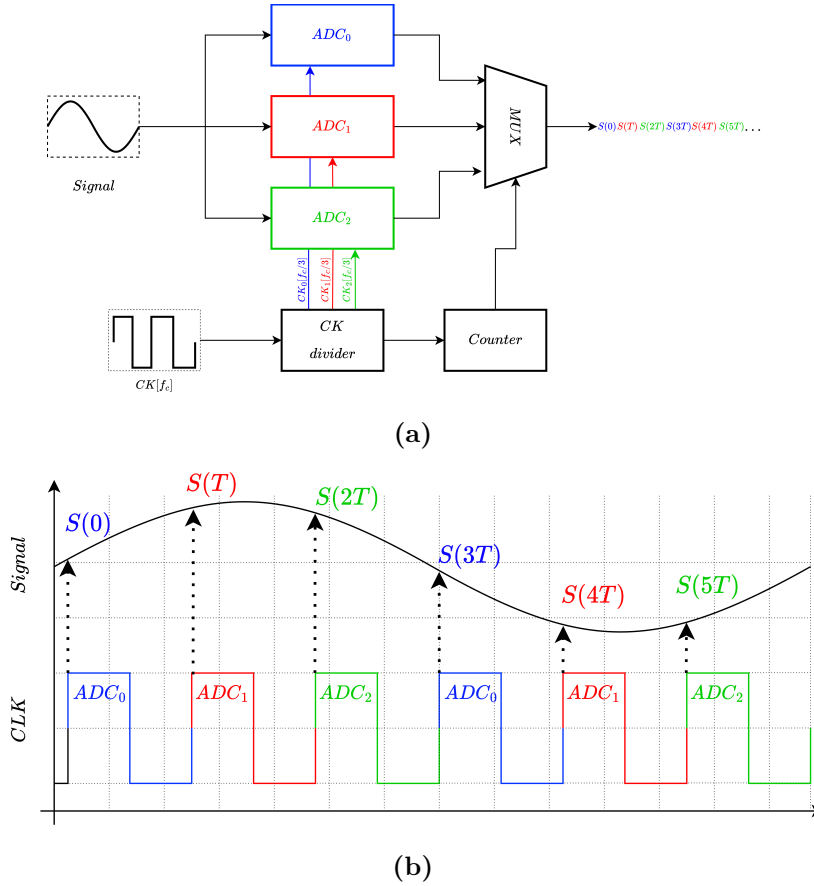


Figure 2.32. ADC TI

Assuming $t_m = mT - r_m T$ is the sampling instant for channel m , where r_m is the relative error in the sampling instant, with respect to T . Assuming $G_a(\omega)$ is the input analog signal spectrum, the digital spectrum of the TI ADC can be expressed

ad:

$$G(\omega) = \frac{1}{MT} \sum_{m=0}^{M-1} \left(\sum_{k=-\inf}^{\inf} G_a(\omega - k \frac{2\pi}{MT}) e^{-i(\omega - k \frac{2\pi}{MT})t_m} \right) e^{-im\omega T} \quad (2.39)$$

that is:

$$G(\omega) = \frac{1}{MT} \sum_{m=0}^{M-1} \left(\sum_{k=-\inf}^{\inf} e^{-i((\omega - k \frac{2\pi}{MT})r_M T + mk \frac{2\pi}{M})} G_a(\omega - k \frac{2\pi}{MT}) \right) \quad (2.40)$$

if there are no errors in the system the result is:

$$G(\omega) = \frac{1}{T} \sum_{k=-\inf}^{\inf} G_a(\omega - 2\pi k) \quad (2.41)$$

that is simply a signal sampled at sampling rate T .

2.6.2 Asynchronous Time Interleaving

An ATI ADC is a generalized version of STI parallelization architecture. An ATI consists of a cascade of three functional blocks for each parallelized channel: A sampler, a LPF and a digitizer. At the end of the channel cascades a DSP (Digital Signal Processing) is involved to merge the signals and build the output digital signal. The general idea behind the ATI architecture is to sample the signal at a frequency lower than the Nyquist frequency, generating aliasing and reconstructing the entire spectrum of the signal with digital and analog processing. This process aims to double (for two channels) the digitized signal bandwidth without doubling the sampling frequency. The two channels operates in TI as in STI, but sampler and digitizer can work asynchronously, with different and independent clock sources [20, 92]. The sampler of the two channels consists in a pulse generator that samples the two channels, the first on the rising edge the second, inverted, on the falling edge of the sampling clock. The block scheme of a 2-channel ATI is shown in figure 2.33.

Working principles and sampling theory of an ATI For the sake of simplicity, with the reference to figure 2.33, the analog input signal $x(t)$ is assumed to be band limited to $B = f_s$ where f_s is also the sample rate of the sampler, the digitizers clock frequency f_c is assumed to be equal to $f_s/2$. The input signal spectrum is composed by a Lower band component (from 0 to $f_s/2$, indicated with L in 2.33) and an Upper band component (from $f_s/2$ to f_s , indicated with U in 2.33). $l(t)$ is the pulse response of a LPF, assumed to be ideal, with a cut-off frequency of $f_s/2$. The signal, is sampled at f_s by the sampler generating aliasing, since the Nyquist frequency is $f_n = 2B = 2f_s$. The resulting spectrum of each channel is shown in figure 2.33. Due to the aliasing, the output spectrum of each sampler is the result of an overlap between the upper and lower bands of the input signal, both in the base band and in the translated band. The LPFs are involved to suppress the translated

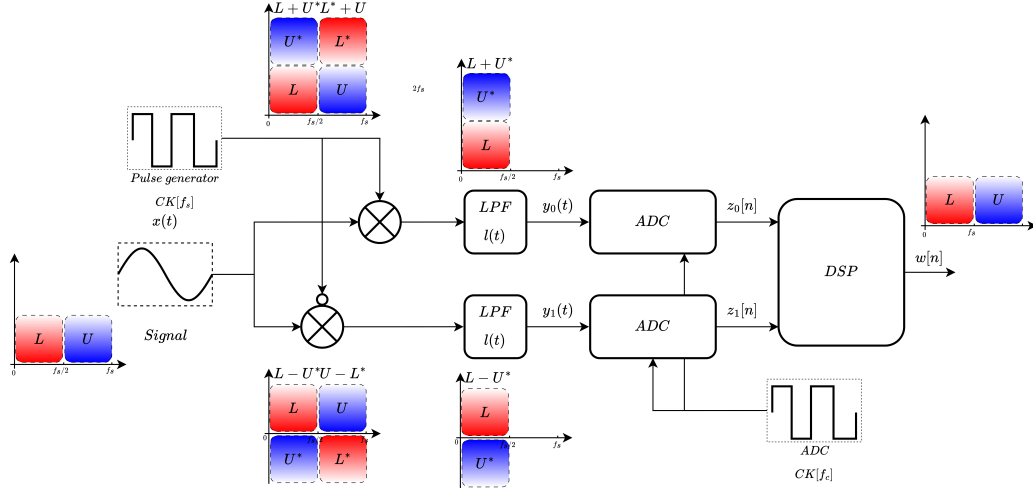


Figure 2.33. Block diagram of a 2-channel ATI architecture

band component of each channel, obtaining the signals:

$$y_0(t) = l(t) \sum_{n=-\infty}^{\infty} x(nT_s) \delta(t - nT_s) \quad (2.42)$$

$$y_1(t) = l(t)^* \sum_{n=-\infty}^{\infty} x((n + 1/2)T_s) \delta(t - (n + 1/2)T_s) \quad (2.43)$$

in 2.42 and 2.43, $*$ is the convolution operator, $l(t) = \text{sinc}(f_s t)$ is the impulse response of the ideal LPF with cut-off frequency equal to $f_s/2$, both samplers operate at f_s with a relative time delay of $T_s/2$ that is the effect of the inversion of the clock on the second channel. In this way first channel is sampled at the time instants nT_s and the second at $(n + 1/2)T_s$.

The respective spectrum of signals in 2.42 and 2.43 are:

$$Y_0(\omega) = \frac{1}{2} L(\omega) (X(\omega) + X(\omega - \pi)) \quad (2.44)$$

$$Y_1(\omega) = \frac{1}{2} L(\omega) (X(\omega) - X(\omega - \pi)) \quad (2.45)$$

where $L(\omega)$ is equal to 1 in $(-\pi/2, \pi/2)$ and zero at the other frequencies. In this condition, the signal is band-limited to $B/2 = f_s/2$ and can be digitized by the ADCs of each channel at $f_c = f_s/2$. The clock of the ADC of the second channel is inverted in order to introduce a relative time delay of T_s , in this way, the two ADCs alternately retrieve one sample for every two produced by the sampler of each channel. The relation between the signals at the output of the filters and those acquired by the ADCs is:

$$Z_0(\omega) = \frac{1}{2} (Y_0(\omega) + Y_1(\omega - \pi)) \quad (2.46)$$

$$Z_1(\omega) = \frac{1}{2} (Y_0(\omega) - Y_1(\omega - \pi)) \quad (2.47)$$

Taking into account that spectra of discrete signals are periodic ($X(\omega - 2\pi) = X(\omega)$) and substituting 2.44 and 2.45 in 2.46 and 2.47 the result is:

$$Z_0(\omega) = \frac{1}{2}(Y_0(\omega) + Y_1(\omega - \pi)) \quad (2.48)$$

$$Z_1(\omega) = \frac{1}{2}(Y_0(\omega) - Y_1(\omega - \pi)) \quad (2.49)$$

It is possible to obtain $X(\omega)$ from 2.48 and 2.49 to reconstruct the digital representation of the input spectrum:

$$X(\omega) = 2 \frac{Z_0(\omega) + Z_1(\omega)}{L(\omega) + L(\omega - \pi)} = 2(Z_0(\omega) + Z_1(\omega)) \quad (2.50)$$

this results is due to the fact that $L(\omega) + L(\omega - \pi) = 1$ in $(-\pi, \pi)$ that is the band of the digitized signals.

2.6.3 Aliasing and Filters

As is possible to see in the previous sections, the LPFs are fundamental in data acquisition chains, as conventional anti-aliasing filter and, especially in ATI architectures to suppress signal spectrum replicas in translated band. These systems require LPFs with bandwidths up to 10 GHz and beyond, especially in (ATI) architectures. High-order filters are needed for out-of-band suppression and linearity to maintain performance. [12, 98] .

2.6.4 Signal Calibration

Calibration techniques, especially in TI ADCs, are vital for correcting gain and timing errors. Advanced digital calibration methods continue to improve ADC performance in real-time [86, 101]. Theoretical working principles of TI and ATI, showed in the previous sections, are based on the assumption that all components and clock sources are ideal. In reality this assumption is not true there are a lot of error sources such as the jitter of the clock sources, the gain error of the filters, of the digitizers, of the samplers and of the pre-amplifiers. Digital calibration is strictly needed in high performance data acquisition systems.

2.7 Low-Power ADC

2.7.1 Context and field of applications of Low-Power ADC

LPADCs are crucial in applications where power efficiency is critical, such as biomedical devices, IoT sensors, and portable systems . These converters balance between power consumption and performance metrics such as speed and resolution. In particular, SAR ADCs are favored for their moderate resolution and energy efficiency [45, 106, 118, 133].

2.7.2 Low-Voltage and Ultra Low-Voltage definitions and key aspects

The drive towards lower power consumption necessitates designs that operate at low and ultra-low supply voltages. ULV ADCs are defined as those operating below 0.5V, with many state-of-the-art designs functioning in sub-threshold regions. The challenge in these designs is maintaining accuracy and stability despite the reduced headroom, which directly impacts comparator performance .

2.7.3 Low-Power SAR ADC

SAR ADCs have become the preferred architecture in LP applications. The charge-sharing technique is one approach that reduces the switching energy and overall power consumption of SAR ADCs . This method reduces the energy consumption during bit decision by sharing charge between CDAC stages, which results in more efficient power usage, in fact, dynamic power consumption in a generic mixed-signal circuit, can be approximated as:

$$P_{\text{switching}} = \alpha C_{\text{total}} \cdot V_{\text{DD}}^2 \cdot f_c \quad (2.51)$$

where α is the activity factor (representing the fraction of clock cycles during which the capacitance is charged or discharged), C_{total} is the total capacitance, V_{DD} is the supply voltage, and f_c is the clock frequency.

2.7.4 Low-Power critical issues and trade-offs

In LPADC designs, there are critical trade-offs between speed, resolution, and power consumption. A lower supply voltage leads to slower comparators, which affects the overall speed of the ADC . Another key consideration is the thermal noise, which scales inversely with power consumption.

2.7.5 Low-Power comparators

The comparator is a critical component in SAR ADCs, directly influencing the speed and accuracy of the conversion process. In LP designs, dynamic comparators with zero static power consumption are often used. There are several approaches used to reduce power consumption of the comparators that will be discussed in this thesis. [6]

Chapter 3

A Design of a 166 MS/s 10 bit SAR ADC

3.1 Introduction

The growing diffusion of ultra-wide-band communication systems and very high frequency measurement systems has led to the development of ADC [61, 79, 148] and digital-to-analog (DAC) [5, 69] converters operating at tens of GHz sample rate. Among various ADC architectures, SAR ADCs are particularly appealing due to their high energy efficiency, moderate-to-high resolution, and compatibility with CMOS technology scaling [22, 114]. These characteristics make SAR ADCs suitable for medium-speed and medium-precision applications.

A crucial design consideration for CDACs involves optimizing the output common-mode voltage range. In most SAR ADC configurations, the outputs of the capacitive DAC are directly linked to the comparator's inputs, which typically consist of a clocked regenerative latch. In these comparators, the differential input signal is initially amplified by a dynamic pre-amplifier, which sets the stage for the latch to regenerate the signal to a full-scale output. It is well established that the performance of the dynamic preamplifier is significantly impacted by the comparator's input common-mode voltage [129].

To achieve energy efficiency and improve overall performances of the ADC, novel switching schemes for the CDAC have been developed, achieving significant reductions in switching energy consumption [14, 40, 129].

In this chapter the design of a 166 MS/s 10 bit SAR ADC is presented, it represents a complete activity of designing for which each block of the ADC has been designed, sized, and post-layout simulated. A particular focus is reserved to the description of the switching algorithm which appears to be the most innovative element used in the ADC to optimize the performance of the comparator by keeping the common mode swing limited. In-depth simulations were obviously carried out on the entire ADC in post-layout in order to produce it in the foundry as part of the SHIFT project [1] for which, the ADC was designed as part of a D-band 5G transceiver demonstrator. The reminder of this chapter is organized as follow: In section 3.2 a general overview on the ADC specifications and architecture is provided, section 3.3 briefly describes the bootstrapped Track-and-Hold topology, In section

3.4 the innovative MQMS (Modified Quasi-Monotonic Switching) used in the ADC is described in detail, The simulation results and their comparison with the state of the art are reported in section 3.5 and section 3.6 concludes the chapter.

3.2 Description of the ADC architecture

The SAR ADC described in this section has been realized in 55nm CMOS STMicroelectronics technology. The ADC is a 10-bit 166 MS/s synchronous charge redistribution fully differential SAR, supplied with $V_{DD} = 1V$. Figure 3.1 presents the architecture of the ADC. The comparator utilized is a standard Razavi Strongarm latch, a widely recognized regenerative topology for its speed and energy efficiency, particularly in medium to high V_{DD} applications, described in detail in subsection 2.4.2. The T&H switches are implemented as bootstrapped switches to ensure sufficient linearity, as described in [104], the adopted topology is the Razavi bootstrapped switch in [110], described in section 3.3. To mitigate capacitive coupling between the ADC's inputs and the top plate nodes of the CDAC capacitors when the T&H is disabled, the T&H circuit incorporates cross-coupled capacitors, realized with NMOS transistors with grounded gates.

In the CDAC, the two least significant capacitors are connected to the main array via a series capacitor, employing a technique known as the bridge capacitor approach [104] described in paragraph 2.3.2, which helps reduce the overall capacitance by attenuating the impact of the smallest capacitors. Another bridge capacitor is inserted between the T&H and CDAC to reduce the capacitance experienced by the T&H switches, thereby easing the on-resistance requirements. The unit capacitance across all array elements is approximately 8.6 fF, while the total capacitance of the CDAC is about 1.1 pF. The switching algorithm used in this ADC is a modified version of the Quasi-Monotonic switching (MQMS) described in 2.3.5, it exploits a few additional logic cells to minimize the CDAC common mode voltage swing, in order to improve the comparator performances. The switching algorithm is described in section 3.4. Figure 3.2 shows the layout of the SAR ADC. The area footprint is $\approx 0.069 \text{ mm}^2$.

3.3 Bootstrapped T&H

the T&H switches are implemented as bootstrapped switches to ensure sufficient linearity, as described in [104], the adopted topology is the Razavi bootstrapped switch in [110]. Figure 3.3 shows the T&H topology, in 3.3a the switches used to implement the bootstrap are made explicit, whereas the scheme in 3.3b is the CMOS level detailed schematic.

The idea used in this topology consists in bootstrapping the voltage that drives the main switch (M_6 in figure 3.3) in order to keep constant its V_{gs} avoiding phase and amplitude distortion of the sampled signal due to V_{gs} modulation. In conventional switches V_{gs} value of the switch transistors depends on the input signal causing the sampling to introduce distortion. In this scheme V_{gs} is kept constant through a voltage sifter implemented as a pre-charged capacitor C_b . This capacitor is pre-charged to V_{DD} during hold phase and, in the sample phase, the input voltage

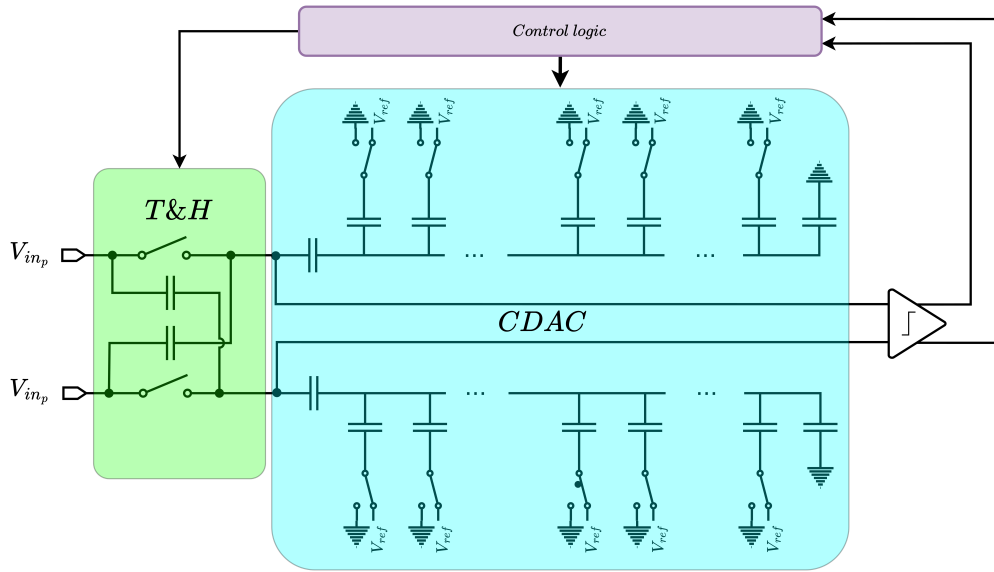


Figure 3.1. Architecture of the 10 bit SAR ADC with MQMS CDAC.

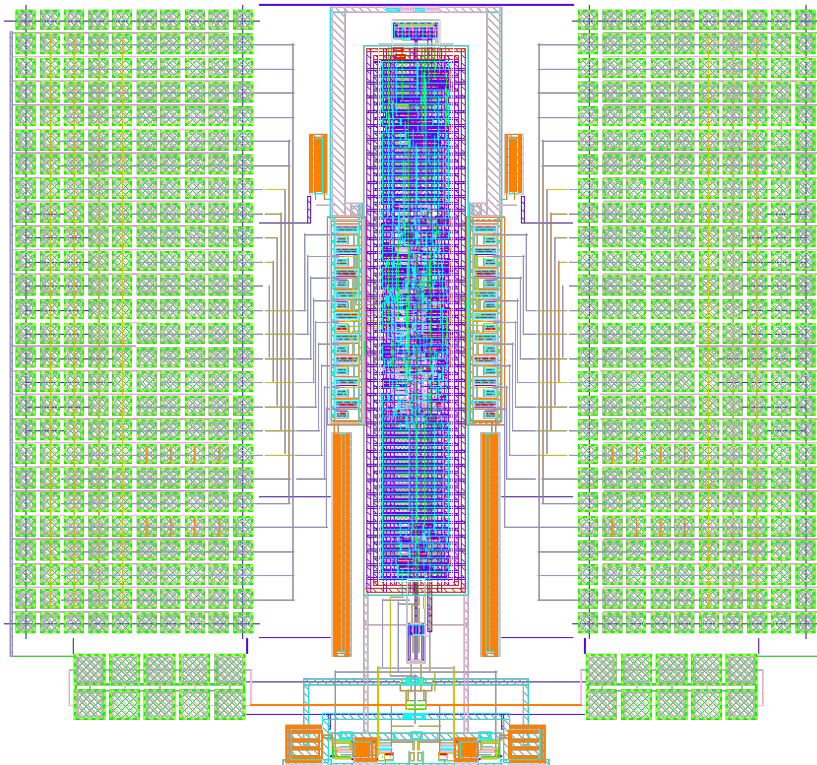
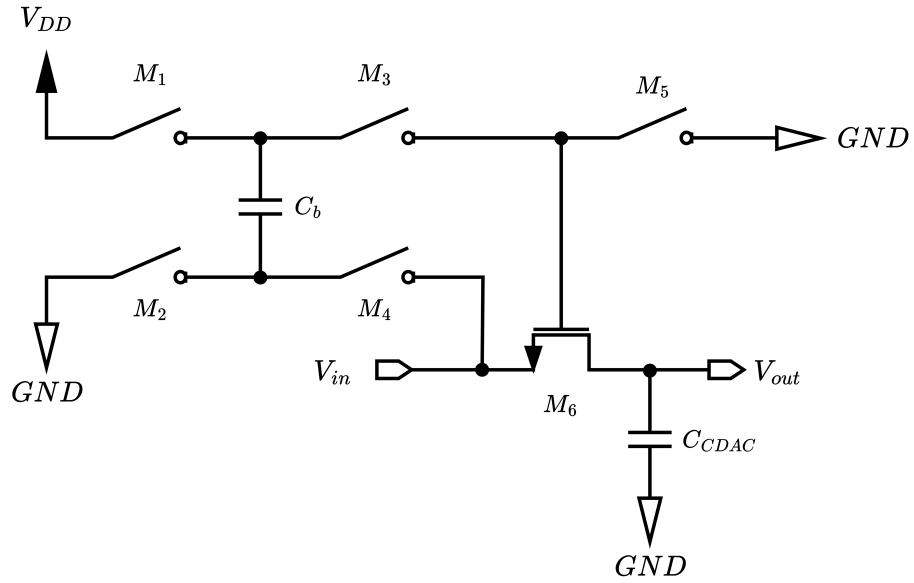
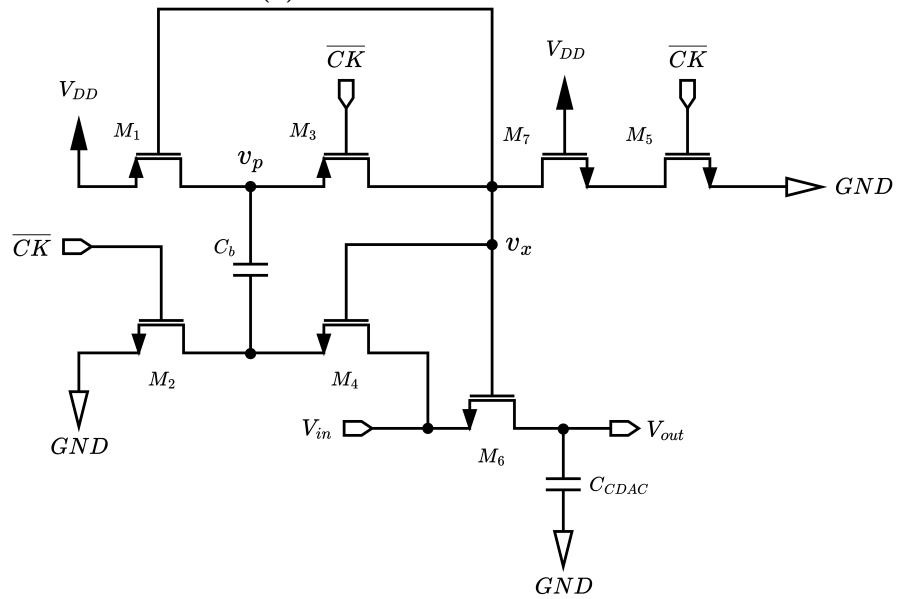


Figure 3.2. Layout of the 10 bit SAR ADC ($252\ \mu\text{m} \times 272\ \mu\text{m}$).



(a) Schematic with switches



(b) CMOS level scheme

Figure 3.3. Razavi bootstrapped T&H .

increased by V_{DD} is transferred to the gate of the main switch, maintaining the V_{gs} at a constant value. This is possible to the switches $M_{1,5}$ that pre-charge C_b to V_{DD} during hold phase ($M_{1,2}$) then, in the sample phase, they disconnect it from V_{DD} and ground and connect it between V_{in} and the gate of the main switch ($M_{3,4}$). Switch M_5 keeps the gate of M_6 to ground, turning it off, during hold phase.

Taking a look to the CMOS level scheme in 3.3b, it is possible to explain how the switches are implemented and how they work, assuming that when the CK is high the T&H is in sampling phase, whereas when CK is low it is in the hold phase. Since M_2 and M_5 have to connect the bottom plate of the capacitor C_b and the gate of M_6 respectively to ground during hold phase, they are simply implemented as NMOSs driven by $\overline{CK}$. Similarly M_3 , during sample phase, connect the top plate of C_b (that is $v_p = V_{in} + V_{DD}$) to the gate of M_6 and so it must be implemented as a PMOS driven by $\overline{CK}$. M_1 must be a PMOS for the same reasons of M_3 and its gate should be driven by CK but it is driven by v_x (that is the voltage at the main switch gate) instead. This is because v_p can rise above V_{DD} (since it is $v_p = V_{in} + V_{DD}$), inverting the role of M_1 source (that is connected to V_{DD}) and drain, if the gate voltage was V_{DD} the new source reach a voltage exceeding the gate voltage by more than one threshold and M_1 would turn on. To avoid this situation the gate of M_1 is bootstrapped to V_{in} as in figure 3.3b. NMOS M_4 implements the switch that senses the input voltage. Its gate is connected to v_x since its source is driven by the input signal and so, if its gate was at V_{DD} it may turn off or, at least, exhibits a large on-resistance for high values of V_{in} . To conclude, transistor M_5 has been cascoded with M_7 in order to reduce its V_{ds} (that, without the cascode is $V_{ds5} = v_x$ and may reaches values greater than V_{DD}) and prevent a stress-condition that may shorten the device lifetime.

3.4 MQMS algorithm

In this section is described the technique adopted to minimize the CDAC common mode voltage swing and make it convergent to a value that is decoupled from the initial input common mode voltage, at the cost of only a few additional logic gates. The novel algorithm is called MQMS since it is a modification of the Quasi-Monotonic Switching algorithm described in subsection 2.3.5. Before discussing the proposed technique, it is helpful to define the concepts of an upward transition and a downward transition already discussed in subsection 2.3.5. In an upward transition, the lowest output of the CDAC takes a positive step while the other output remains unchanged. Conversely, in a downward transition, the highest output decreases while the other stays constant. These transitions also influence the output common-mode voltage of the CDAC, denoted as V_{ocm} . Based on these definitions, the MS CDAC can be described as performing only upward or only downward transitions. In contrast, the QMS CDAC begins with an upward transition followed by a sequence of downward transitions. The proposed technique leverages this behavior to enhance flexibility and optimize the performance of the comparator. The key aspects of the MQMS CDAC are summarized as follows:

- Taking advantage of the alternation between upward and downward transitions to control the value to which V_{ocm} converges during the successive approxima-

tion process. This characteristic is crucial because it enables decoupling of the V_{ocm} level during conversion (especially during the resolution of the least significant bits) from the input common mode of the ADC, allowing it to be optimized for the comparator's ideal input common mode.

- Temporarily shifting V_{ocm} to reduce the output common-mode swing compared to the QMS scheme. This helps improve the comparator's performance in terms of delay, power consumption, input-referred offset, and noise.

The topology of the capacitive arrays in the MQMS CDAC, depicted in Figure 3.4, is identical to that of the QMS and MS configurations. The main difference from

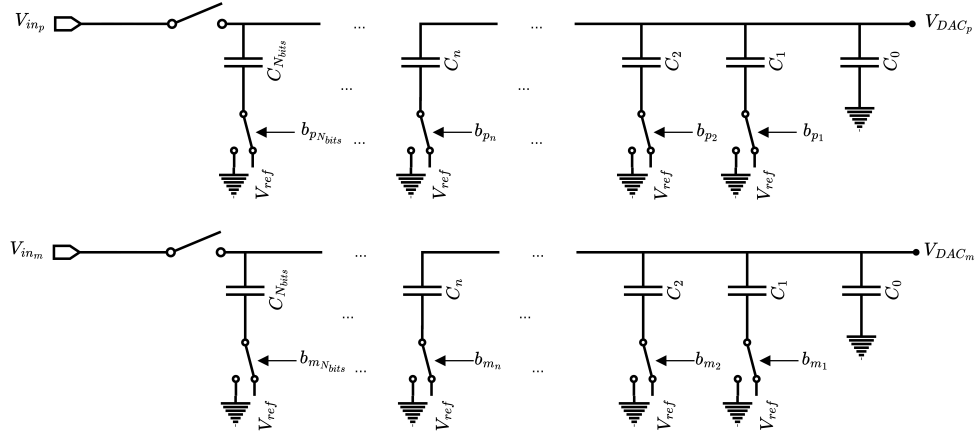


Figure 3.4. Capacitive array of the proposed MQMS CDAC.

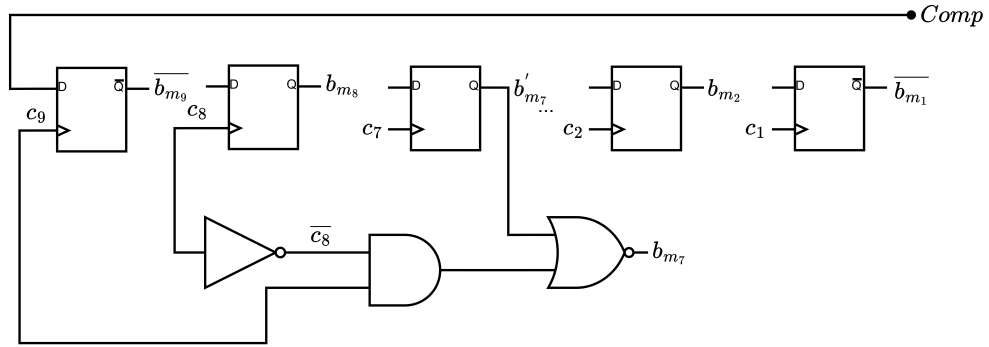


Figure 3.5. SAR register of the proposed MQMS CDAC. The figure shows one of the two registers. The other register is identical, except that its outputs are connected to the complementary switches in the CDAC (e.g., bm_i is replaced by bp_i).

the QMS CDAC lies in the control logic, particularly in the SAR register. The register's schematic is shown in Figure 3.4. The signals $c_9, c_8, \dots, c_1$ are used to sequentially sample the comparator's decisions into the SAR registers. By employing D-type flip-flops (DFFs) with both inverted and non-inverted outputs, any desired transition pattern for the CDAC can be achieved. In the configuration shown in

Figure 3.5, the CDAC starts with a downward transition, followed by five upward transitions and three downward transitions. Furthermore, V_{ocm} is shifted upward before the comparator's second decision and then shifted downward before the third decision. This behavior is enabled by the AND and NOR gates, which toggle the control signals bp_7 and bm_7 at the appropriate times. Consequently, the output common-mode swing of the CDAC is reduced to less than half of that in the QMS scheme. During the conversion, the comparator's input common mode stays roughly between 350 mV and 450 mV (assuming a 1 V supply). Within this range, the comparator operates at near-optimal levels for delay, power consumption, noise, and offset.

It is worth noting that, in most ADC designs, the SAR registers interface with the CDAC switches via at least one stage of logic buffers. As a result, replacing a buffer with a NOR gate of similar fan-out does not introduce a significant delay penalty in the affected path. The primary disadvantage of the MQMS DAC is the slight increase in power consumption due to the charge and discharge of the capacitors that cause the temporary shifts in common mode. However, this effect has a limited impact on performance since the shift involves only a small subset of elements, with capacitance representing a fraction of the total array capacitance. In the implementation shown in Figure 3.5, for example, the shift is generated by adjusting the bottom plate of C_7 , which accounts for 1/8 of the total capacitance in the single-ended array.

3.4.1 Effect of input common mode on comparator performance

As previously discussed, the performance metrics FOM of a dynamic regenerative comparator are significantly affected by the input common-mode voltage. Figure 3.6 illustrates the simulated behavior of the comparator used in the SAR ADC design, showing how its performance varies with respect to the input common-mode voltage, V_{icm}^{SA} . The delay has been calculated for a differential input voltage of $V_{id} = 1$ mV. The comparator design is based on the Razavi modification of the Strong Arm latch architecture [111]. Consistent with theoretical expectations, lowering V_{icm}^{SA} improves power consumption, input-referred noise, and input-referred offset, as shown in [143]. However, the comparator's delay reaches an optimal value near $V_{icm}^{SA} = 450$ mV, since the input transistors start operating in sub-threshold mode below a certain V_{icm} . Therefore, the optimal operating range for the input common-mode voltage lies approximately between 400 mV and 450 mV.

3.5 Simulation results and comparison

The ADC has been post-layout simulated in Cadence Virtuoso, with $V_{DD} = 1V$.

3.5.1 MQMS algorithm: CDAC voltages transient behavior

Figure 3.7 shows the transient behavior of the outputs of the SAR ADC CDAC during a conversion.

The two signals adhere to the transition scheme outlined in Section 3.4. The small, periodic fluctuations in V_{ocm} are due to the kickback current generated by

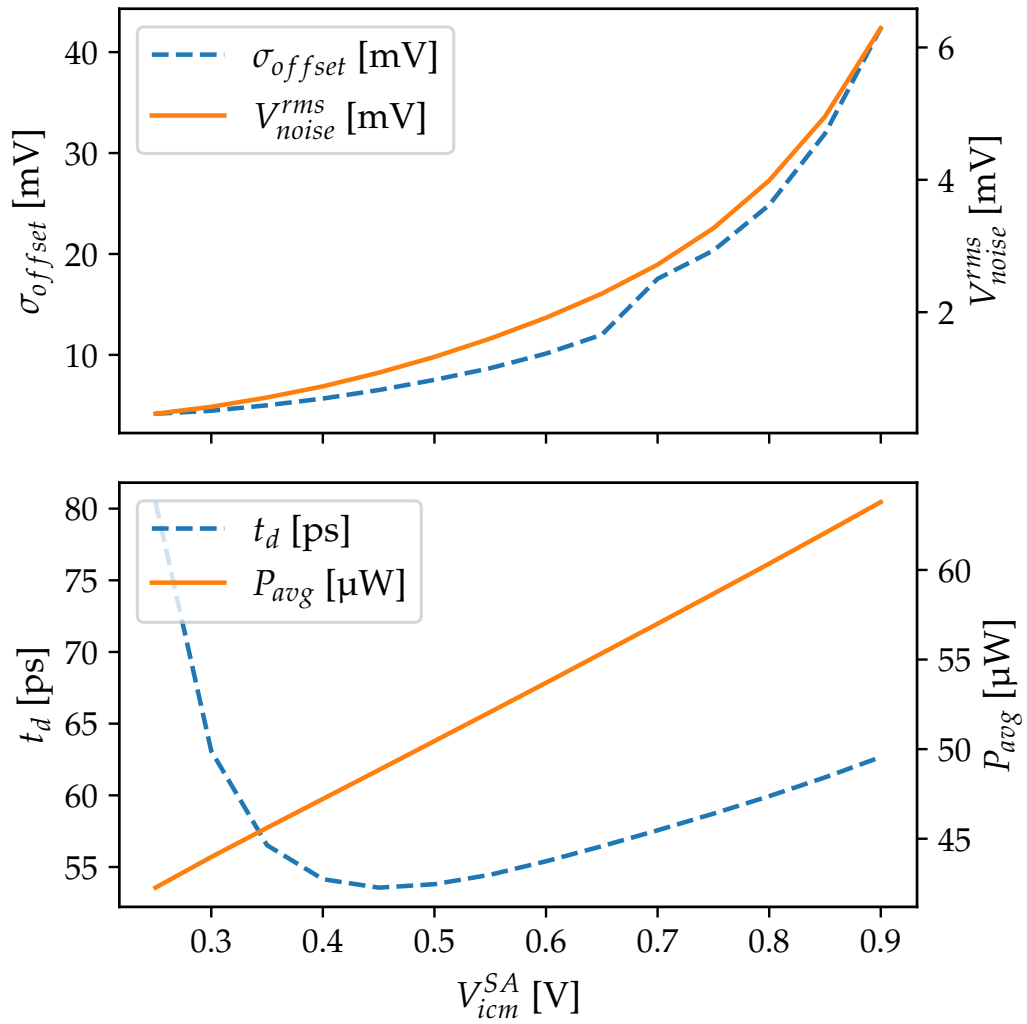


Figure 3.6. Key performance metrics (delay, power consumption, input-referred noise, and input-referred offset) as a function of input common-mode voltage in the Strong Arm comparator.

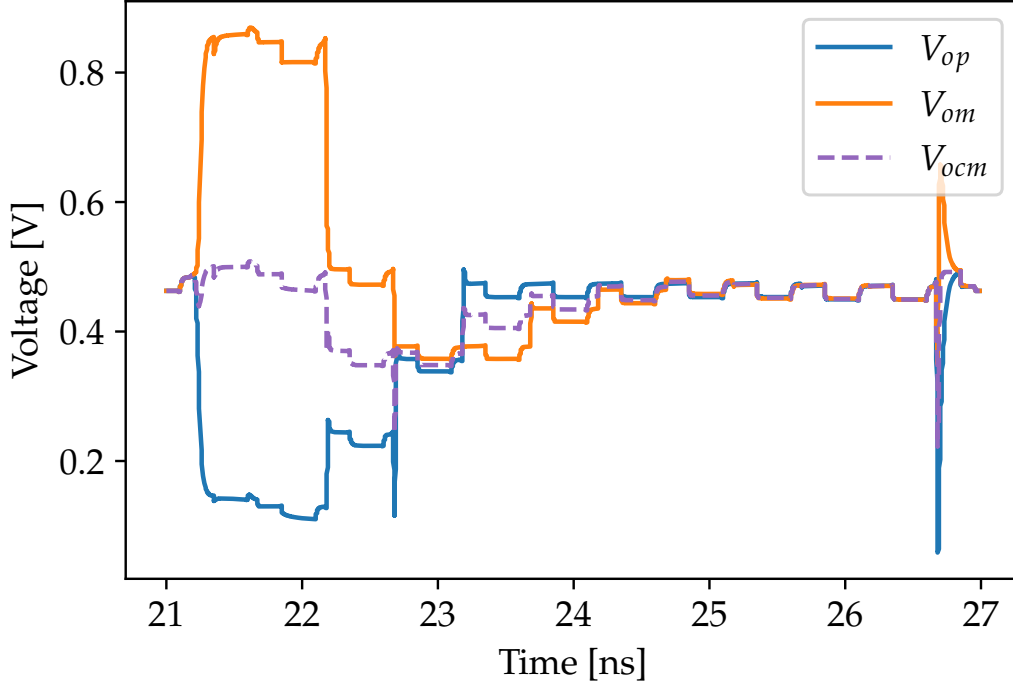


Figure 3.7. Transient behavior of the CDAC output voltages (single ended and common mode) during a conversion.

the comparator. A noticeable upwards shift in the common-mode voltage occurs around 22 ns, during the first update of the CDAC. This upward shift is repeated during the next iteration of the CDAC. The third decision made by the comparator is the most time-sensitive, as it takes place with an input common-mode voltage of approximately 350 mV. From figure 3.6, it can be observed that the delay at this specific input common-mode voltage is slightly below optimal (around 57 ps at $V_{id}^1 = 1$ mV, compared to the optimal delay of about 54 ps), but remains within acceptable limits. Furthermore, for the QMS CDAC, the worst-case input common-mode voltage would be near 750 mV, resulting in an even longer delay of around 59 ps. As the conversion progresses, V_{om} stabilizes around 450 mV. Thus, the output common-mode swing is limited to approximately 100 mV, which is less than $V_{DD}/8 = 125$ mV. This behavior can be attributed to two main factors. First, the input parasitic capacitance of the comparator attenuates the CDAC's output swing. Additionally, the final three iterations involve downward transitions, which further restrict the variations in V_{om} .

3.5.2 Performance in typical condition

The performance of the SAR ADC with MQMS switching is summarized in Table 3.1, which includes signal-to-noise-and-distortion ratio (SNDR) and power consumption data. The SNDR was measured using a sinusoidal input signal with a frequency of

¹ V_{id} : Differential input voltage of the comparator

$f_{in} = \frac{31}{64}f_s \approx 72.7$ MHz and a differential peak-to-peak amplitude of 1.44 V. The input amplitude is slightly lower than the theoretical 2 V due to the parasitic capacitance on the top plate of the CDAC, which constrains the input swing. The results are presented for the typical process corner, both with and without transient noise simulation. Additionally, 100 Monte Carlo simulations, accounting for mismatch and process variations, were conducted to evaluate the robustness of the design. All results stem from post-layout simulations. To mitigate the substantial simulation time, the Monte Carlo simulations were executed without transient noise. However, the expected difference in performance between Monte Carlo simulations with and without noise should align with the observed difference between the typical corner results obtained with and without noise. The Walden figure of merit (FOM_W), calculated from the transient noise simulation, is 71.2 fJ/conversion step.

Table 3.1. Post-layout performance summary of 10 bit SAR ADC at $f_s = 150$ MS/s.

	Typ.	Typ. (with noise)
SNDR [dB]	58.7	56.3
P_{avg} [mW]	6.03	6.03
ENOB	9.49	9.09

3.5.3 Switching algorithm performance comparison

The figure of merit (FOM) achieved in this work is significantly higher than that typically reported by most high-speed converters in recent studies, which generally exhibit an FOM ranging from 10 to 30 fJ/conversion step [52, 60, 121]. However, this discrepancy is primarily attributed to technological constraints unrelated to the proposed approach: the technology used for the ADC implementation is characterized by large parasitic capacitances that negatively impact the CDAC's linearity, effectively setting a lower bound on the total array capacitance. Consequently, the power consumption of both the CDAC and the buffers driving the CDAC switches is relatively high. Nevertheless, the results highlight that the proposed ADC maintains a high level of accuracy, primarily due to the optimized input common mode of the comparator. This is particularly notable considering that the ADC is fully synchronous and does not utilize error correction methods such as calibration or redundant arrays. For a fair comparison, both the QMS and MS techniques were implemented, and their performances were evaluated through post-layout simulations. As shown in Table 3.2, the proposed technique enhances accuracy with only a minor increase in power consumption. It is also worth noting that the area occupied by the three versions is virtually identical, as QMS does not require additional logic gates, and MQMS only necessitates the addition of two AND gates and the replacement of two buffers with NOR gates.

3.5.4 PVT and Montecarlo results

Table 3.3 summarizes the ADC performance under PVT variations. The most critical corner is SS. Whereas, table 3.4 reports the Montecarlo simulation results evaluated over 100 Mismatch and process iterations (without noise).

Table 3.2. Comparison between MQMS-, QMS- and MS-based SAR ADC.

	MQMS	QMS	MS
SNDR [dB]	56.3	53.4	48.4
P_{avg} [mW]	6.03	5.82	5.92
FOM_W [fJ/conv. step]	68.07	91.74	165.95

Table 3.3. Performance of 10b ADC under PVT variations.

Output	SS	FF	SF	FS	Tmin	Tmax	VDD,min	VDD,max
THD	44.5	53.2	56.29	58.14	59.09	56.55	58	59.04
Ptot	3.63	33.2	8.89	6.36	5.29	8.37	5.26	7.08
Pdig	2.99	25.4	6.88	4.96	4.22	6.46	4.15	5.58
Panalog	0.640	7.77	2.01	1.40	1.06	1.91	1.11	1.50

Table 3.4. ADC SNDR and consumption evaluated over 100 Montecarlo Mismatch and process iterations (without noise)

	μ	σ
SNDR [dB]	58.21	1.66
P_{avg} [mW]	6.68	1.83

3.5.5 Comparison with the literature

In table 3.5 the ADC performances are compared with the state of the art of high speed SAR ADC. As declared in the previous section the Walden FOM of the comparator is not competitive, since this technology is characterized by large parasitic capacitances that deteriorates the performances, in terms of consumption. Despite this the ADC is able to work at very high frequency maintaining high level of accuracy.

Table 3.5. Comparison with the state of the art of high speed SAR ADC.

	This work	[150]	[126]	[52]	[68]	[38]	[47]	[156]	[44]	[52]
Year	2024	2023	2022	2022	2024	2019	2021	2023	2023	2021
Technology [nm]	55	55	40	28	40	28*	28	28	28	28*
Resolution [bit]	10	10	10	12	10	10	11	10	10	10
f_s [MS/s]	166	200	100	150	100	500	500	300	700	500
V_{DD} [V]	1.00	1.20	1.10/1.30	0.90/1.30	1.20	1.10	0.90	0.90	0.95	1.10
THD [dB]	-58.7	-	-	-71.8	-	-	-	-	-	-
SNR [dB]	57.6	-	-	63.93	-	-	-	-	-	-
SFDR [dB]	65.8	66.30	76.3	72.2	-	62.49	81.73	79	-	72.7
SNDR [dB]	56.3	55.30	56.3	63.3	60.69	52.7	61.98	57.6	56.42	56.7
ENOB [bit]	9.06	8.90	9.06	10.22	9.79	8.46	10.00	9.28	9.08	9.13
P_{avg} [mW]	6.03	2.80	1.4	3.02	4.25	1.18	3.06	2.1	2.02	5.78
FOM_W [fJ/conv. st.]	68.07	29.31	26.23	16.85	48.04	6.69	5.96	11.29	5.33	20.69
Area [mm ²]	0.0850	0.008	0.027	0.023	0.075	0.0043	-	0.019	0.0027	0.005

*:FDSOI

3.6 Conclusion

This section presented a 10-bit 166 MS/s synchronous SAR ADC, supplied with 1 V and realized in 55 nm CMOS STMicroelectronics technology. The ADC is implemented with a fully differential charge redistribution SAR architecture. The comparator is a conventional Strongarm latch, in the CDAC two bridge capacitors have been involved to reduce the equivalent capacitance while maintaining larger physical capacitor. The T&H is a Razavi Bootstrapped switch with enhanced linearity. The proposed CDAC switching scheme reduces the output common-mode swing while preserving the majority of the efficiency and compact design characteristics of the MS CDAC. Additionally, this approach decouples the CDAC's output common-mode voltage from the ADC's input common mode. This separation allows for improved performance, as the CDAC's output common-mode range can be fine-tuned to meet the comparator's specific requirements. The ADC has been realized with a conservative approach, in order to produce it in foundry and perform real measurements on it. The technology that has been used to design the ADC implies limitation on the performance due to the high parasitic effect, in particular parasitic capacitances that worsen speed and power consumption performances. Despite this, post-layout simulations show that the ADC has a good level of accuracy, achieving an SNDR of 56.3 dB, an average power consumption of 6.03 mW and a Walden FOM of 68.07 fJ/conversion step.

Chapter 4

Low voltage and Ultra Low Voltage dynamic comparators

In this chapter a set of innovative LV and ULV dynamic comparator topologies are presented. In these works, issues of standard dynamic comparator topologies, in particular Strongarm comparator 2.4.2, at low and ultra low power supply voltage are analyzed and innovative LV and ULV solutions are proposed. The proposed topologies show possible solutions to maximize performance while keeping consumption low and guaranteeing operation at very low supply voltages for application that rely on battery supply or energy harvesting.

4.1 Introduction and Context

The continuous development of portable electronic devices such as smartphones, tablets, and wearable electronics has significantly influenced modern lifestyles, enabling seamless interaction with digital services like banking, health monitoring, traveling, and remote working. These devices, often battery-operated or relying on energy-harvesting techniques, demand an aggressive reduction in power consumption to prolong their autonomy. This goal is achieved through the minimization of current consumption and supply voltage [29, 30, 65, 118, 139]. Particularly, in biomedical applications, the autonomy of devices used for health monitoring and the study of neural disorders, such as Parkinson's and Alzheimer's diseases, is of paramount importance. Reducing power dissipation is essential in such applications to minimize heat generation and prevent potential damage to sensitive neural tissues [17, 33, 80, 153]. Consequently, biomedical data acquisition systems typically operate at ultra-low supply voltages (ULV) and with current consumption in the nanoamperes range, necessitating specific design strategies to ensure proper functionality under such stringent conditions.

For applications of ULV ADC, lowering the comparator supply voltage often reduces operating frequency, limiting the ADC's sampling rate and overall performance. However, in contexts like IoT devices, wireless sensor networks, and System-on-a-Chip (SoC) systems, maintaining high sampling rates is essential to ensure accurate and real-time data acquisition [73, 123, 151].

These applications frequently require power efficiency due to reliance on small

batteries or energy-harvesting technologies. Specifically, in IoT devices, medium-precision (8-12 bit) ADCs with high sampling rates are needed for real-time RF signal processing, such as in wireless communication and image capture, where fast and accurate data conversion is crucial.

ADCs are indispensable components in these systems, serving the crucial function of converting continuous analog signals into discrete digital data for subsequent processing. Due to the importance of achieving low power consumption and maintaining medium-to-high resolution (10-18 bit) for low-frequency signals (1-10 kS/s), certain ADC architectures, such as the successive SAR and sigma-delta ADC, are widely used in low-power applications [59]. These architectures are inherently robust and capable of operating at reduced supply voltages, but their performance, in terms of speed, resolution, and power consumption, is often dictated by the performance of the comparators embedded within them. The role of comparators in these architectures is to determine the polarity of their input signal, and therefore, their design significantly influences the overall performance of the ADC.

To address the challenges posed by operating at ultra-low supply voltages, many ULV comparator designs have been proposed in the literature. Comparators capable of functioning at supply voltages below 0.5V have emerged, with many leveraging Strongarm architecture [15, 48]. Various modifications, such as replacing conventional inverters with PMOS devices or adopting body-driven techniques, have been utilized to extend operation down to 0.3V [4], and even further to 0.2V [71]. Fully synthesizable analog circuits, which facilitate integration into mixed-signal systems, have been demonstrated to operate at supply voltages as low as 0.15V [16, 31, 32, 37, 140]. Despite these advancements, a significant challenge remains in minimizing noise and offset, particularly in body-driven configurations. Body-driven topologies, often employed to extend the input common-mode range (ICMR), suffer from reduced transconductance, which inherently increases noise and offset levels [34]. This issue is especially critical in ADC applications, where a low supply voltage results in a reduced quantization step size, making the system more susceptible to noise and offset effects, thereby limiting the effective number of bits (ENOB).

4.1.1 LV and ULV Comparators in Literature

In recent years, extensive research has been conducted to optimize comparator designs for operation at ultra-low voltages. Dynamic latched comparators, which utilize charge-discharge mechanisms for signal comparison, have become particularly attractive due to their favorable performance in digital processes. Many of these designs employ body-driven input pairs, which allow operation at extremely low supply voltages by eliminating the need for a tail transistor and reducing the number of stacked devices. This approach increases the voltage headroom of each device, thereby reducing the minimum operational voltage [31]. Despite these benefits, body-driven configurations introduce new challenges, such as increased input-referred offset due to the lower transconductance of the body terminal compared to the gate terminal. As a result, many body-driven comparators exhibit a degraded signal-to-noise ratio (SNR) and increased power consumption due to the need for additional circuitry to compensate for these drawbacks.

4.2 A 0.15-to-0.5 V body-driven dynamic comparator with rail-to-rail ICMR63

Various techniques have been proposed to mitigate these limitations. For instance, the use of capacitive degeneration has been shown to reduce input-referred noise by altering the effective g_m/I_D ratio of the input transistors [9]. Another technique involves the use of charge pumps to dynamically boost the voltage headroom during the comparison phase, which allows for higher operating speeds without significantly increasing power consumption [11]. However, despite these advancements, a comprehensive analytical framework for sizing these circuits and understanding their limitations is still lacking in the literature.

A significant amount of research has also focused on applying dynamic biasing to single-stage and multi-stage comparator topologies. This approach leverages a dynamic increase in gain during the comparison phase to achieve a lower input-referred noise at the expense of a longer delay [132]. Such techniques are particularly suited for applications where speed is not the primary concern, but rather, minimizing power and improving accuracy are of greater importance. Nonetheless, recent efforts have sought to adapt these dynamic biasing techniques for high-speed applications, exploring the trade-offs between speed, noise, and power consumption in the context of ULV operation.

4.1.2 Aim of the Presented Works

The main objectives of these works is to present a set of novel LV and ULV comparator architectures that address the limitations of conventional comparators, in particular Strongarm comparator. LV comparators works (0.5 V to 0.8 v supply voltage) are focused on the improvements of the performance particularly in terms of noise and offset while maintaining a low energy-delay product (EDP). ULV comparator works (0.5 V supply voltage and below) are mainly focused on the reduction of the power consumption . These works investigate topologies and techniques adopted in literature, like body-driven comparators and dynamic biasing highlighting the main issues and critical issues. Innovative solutions are proposed in order to address to these limitations relying on innovative topologies and techniques aimed at improving overall performance or a particular indicator or FOM.

4.1.3 Chapter Content Description

The remainder of this chapter is organized as follows. Section 4.2 describes an ULV body-driven comparator supplied and simulated at different V_{DD} , up to a minimum of 0.15 V, with a rail-to-rail ICMR, section 4.3 presents a technique, applied to the comparator in 4.2, that improves performance in terms of noise and offset, section 4.4 describes how to maximize operating frequency by means of a charge-pump based dynamic bias and in section 4.5 a calibrable dynamic-biased comparator with competitive EDP is presented.

4.2 A 0.15-to-0.5 V body-driven dynamic comparator with rail-to-rail ICMR

In this work a novel ULV body-driven comparator is proposed. It involves a pair of AND-gates to drive the gates of the input pair transistors. The AND-gates switch off

the input-pair transistor during reset phase, allowing for the removal of tail transistor, reducing the number of stacked device. During evaluation phase, the AND-gates connect input pair transistors gates to the PMOS latch of the comparator, in this way they become part of the latch contributing to the regenerative loop. The input signal of the comparator is applied to the bodies of the input pair transistors allowing for a rail-to-rail ICMR. The comparator is designed in a 130-nm ST-Microelectronics technology and is optimized to work with 0.3 V power supply and it is able to operate at a up to 2 MHz frequency with $V_{id} = 1\text{ mV}$. The comparator has also been simulated at 0.15 V with the same V_{id} demonstrating it remains fully operational, in this case it can work at up to 80 kHz frequency [34]. The remainder of this section is organized in this way:

4.2.1 Description of the proposed topology

The proposed ULV comparator is a modified version of the Strongarm comparator optimized to work with V_{DD} as low as 0.15 V. The schematic of the proposed comparator is reported in figure 4.1. In this topology the input signal is applied to the bodies of the input pair transistor while the gates are driven by the outputs of two AND gates that perform a logic-AND operation between the clock signal and the outputs. In this way it is possible to reduce the number of stacked devices to allow ULV operation, in fact the drain-source voltages of the transistors is maximized for a given supply voltage, resulting in a speed enhancement. Moreover, thank to the body-driven configuration the ICMR is rail-to-rail.

When the clock is low, during the reset phase, the AND gates outputs are set to low, switching off the input pair transistors and avoiding static consumption without the need of a tail transistors. During the evaluation phase, the AND gates connect the input pair transistor gates to the comparator outputs in a cross-coupling configuration, causing them to become part of the latch and contributing to the output regenerative positive loop.

Immediately after the clock is switched to high, both the output are still high, since the input pair has just started to discharge them. In this phase the input differential signal is pre-amplified. With reference to figure 4.1, when the clock toggles, both the AND gates drives high signal to the gates of the input pair transistors $M_{1,2}$ and they start to discharge the output nodes until one of the PMOS latch transistors $M_{3,4}$ turns on. At this point the output signals start to regenerate, activating the PMOS latch positive loop and to follow, by means of the AND gates also the NMOS positive loop, implemented by $M_{1,2}$. The role of $M_{1,2}$ is twofold, at the begin of the evaluation phase, they pre-amplification the input signal by discharging nodes V_p and V_q asymmetrically, then they contributes to the regenerative positive loop.

The comparator core must be followed by an SR-latch to keep the outputs during the reset phase. The operation of the proposed comparator can be synthesized in three phases:

- **Reset Phase:** when the clock is low the AND logic gates outputs are both low, so the two NMOS $M_{1,2}$ are turned off. The two PMOS $M_{5,6}$ pump current in the output nodes $V_{p,q}$, charging the output parasitic capacitances in order to reset their voltages to V_{DD} ;

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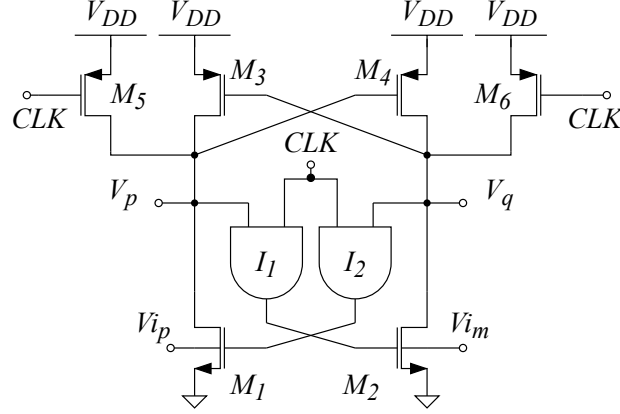


Figure 4.1. Proposed ULV comparator.

- **Preamplification Phase:** when the clock toggles, the reset PMOS $M_{5,6}$ are turned off, whereas the outputs of the AND logic gates switch to high, since output nodes initial condition is $V_{p,q} = V_{DD}$ and clock is also high. The input pair transistors turn on and start to discharge output nodes asymmetrically according to the input differential signal polarity. This phase ends when one of the two outputs is discharged so that the first latch PMOS turns on, starting the regenerative positive loop;
- **Regeneration Phase:** in the evaluation phase, the latch regenerates the outputs voltages thanks to the positive loop of the PMOS transistors $M_{3,4}$ and the NMOS $M_{1,2}$, at this point cross-coupled to the outputs like the PMOSs thanks to the AND gates. The SR-latch senses the differential output voltage $V_p - V_q$ and unbalances the outputs accordingly.

The Preamplification and Regeneration phases compose the Evaluation phase.

4.2.2 Theoretical analysis of the comparator

In this section, a theoretical analysis on the comparator behavior is performed obtaining an analytic model for the delay. The analysis is performed on the two phases in which the Evaluation phase is divided as described in 4.2.1: the Preamplification phase, that begins when the clock toggles and ends at the instant when $M_{3,4}$ turn on and the Regeneration phase corresponds to the time interval from the end of pre-amplification to when the signal is regenerated at the outputs.

Preamplification The equivalent model of the comparator during pre-amplification is reported in figure 4.2.

Preamplification phase ends when the output common mode voltage $V_{ocm} = (V_p + V_q)/2$ drops to a level that allows the PMOS load to turn sufficiently on. The devices are operating in sub-threshold and so the source-gate voltage of $M_{3,4}$ to be considered cannot be the MOS threshold voltage. Thus the threshold voltage is arbitrarily defined as V_{LIM} that is the voltage at which the drain current of $M_{3,4}$ equals that of $M_{1,2}$. Assuming a small differential input voltage $V_{id} = V_{i_p} - V_{i_m}$, it

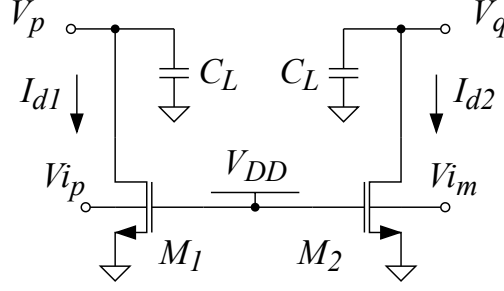


Figure 4.2. Equivalent circuit of the proposed comparator during pre-amplification.

is possible to approximately consider that the pre-amplification phase ends when the output common mode voltage V_{ocm} equals $V_{DD} - V_{LIM}$ and so, the length of this phase is given by:

$$t_{pre} = \frac{C_L V_{LIM}}{I_{cm}} \quad (4.1)$$

where I_{cm} is the common mode drain current, defined as $(I_{d1} + I_{d2})/2$.

According to the input differential voltage, M_1 and M_2 discharge asymmetrically nodes V_p and V_q during pre-amplification, the effect is an integration of the input difference V_{id} on the output nodes differential voltage. More in detail, the output differential voltage V_{od}^{pre} , can be expressed as

$$V_{od}^{pre} = \frac{Q_{od}}{C_L} = \frac{I_{dm} t_{pre}}{C_L} = \frac{I_{dm} V_{LIM}}{I_{cm}} = \frac{g_{mb} V_{LIM}}{I_{cm}} V_{id} \quad (4.2)$$

where Q_{od} is the difference between the amounts of charge stored in the parasitic capacitances at nodes V_p and V_q and I_{dm} is the differential drain current, defined as $I_{d1} - I_{d2}$. The pre-amplification gain is given by

$$A_v^{pre} \equiv \frac{V_{od}^{pre}}{V_{id}} = \frac{g_{mb} V_{LIM}}{I_{cm}} \quad (4.3)$$

where g_{mb} is the body transconductance. It is important underline that, differently from the Strongarm comparator, considering I_{d1} and I_{d2} constant is not an approximation, since the V_{gs} and V_{bs} of the devices are constant.

Regeneration During regeneration, the positive feedback loop of the latch formed by the PMOSs $M_{3,4}$ is activated and starts to regenerate the signal. The AND gates, work as buffers since $CK = V_{DD}$, contribute to the regeneration, in fact they turn off either M_1 or M_2 , depending on the sign of the output difference, becoming, in effect, part of the latch. Assuming that the inverting amplifiers formed by $M_{1,3}$ and $M_{2,4}$ operate in the linear region of their transcharacteristic, the behavior of the comparator can be described in the Laplace domain by the linearized circuit shown in figure 4.4. The initial conditions are defined by the generators $C_L V_p^{pre}$, $C_L V_q^{pre}$, CV_{g1}^0 , CV_{g2}^0 and V_{DD}/s (the power supply). with reference to figure 4.3, V_p^{pre} and V_q^{pre} represent the initial conditions for V_p and V_q , i.e. the output voltages at the end of pre-amplification. To make the analysis affordable, the buffers are modeled as first order systems that consist of g_{mA} and C . This is obviously an

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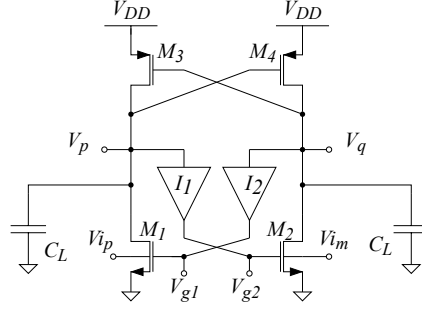


Figure 4.3. Equivalent circuit of the proposed comparator during regeneration.

approximation, because the AND gates should be represented as the cascade of two inverters. Moreover, the output resistances of the devices have been neglected. The PMOSs $M_{3,4}$ and the NMOSs $M_{1,2}$ have been sized in such a way that their transconductances are identical ($g_{m,p} = g_{m,n}$) and so, g_m of the PMOS devices is assumed to be identical to the g_m of the NMOS devices at the beginning of the regeneration phase.

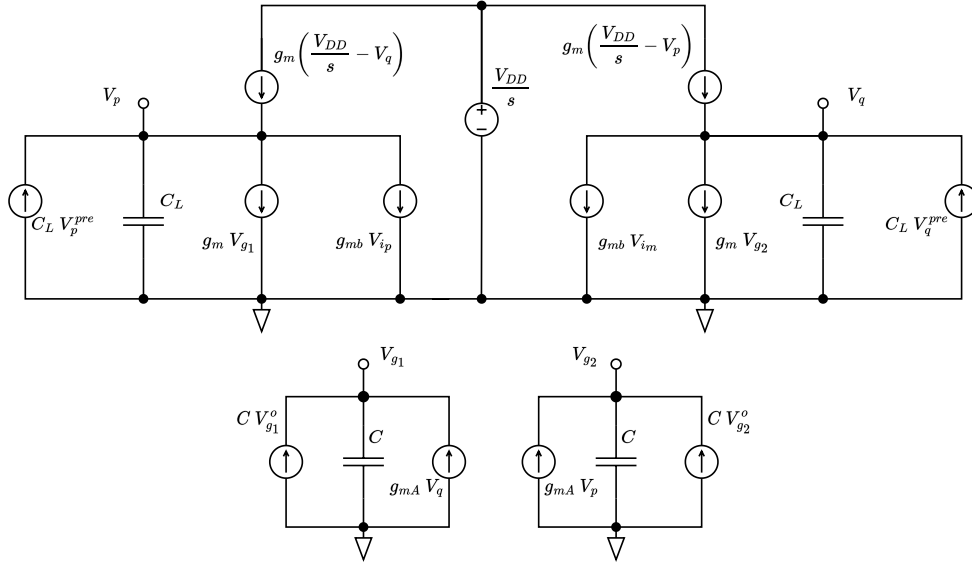


Figure 4.4. Equivalent circuit of the proposed comparator during regeneration, with explicit transistor models.

The circuit represented in figure 4.4 is the equivalent circuit of the schematic in figure 4.3 in which all the devices have been substituted with their explicit small signal models. By analyzing it, the following equations are obtained:

$$g_m(V_{DD}/s - V_q) = sC_L V_p - C_L V_p^0 + g_m V_{g1} \quad (4.4)$$

$$g_m(V_{DD}/s - V_p) = sC_L V_q - C_L V_q^0 + g_m V_{g2} \quad (4.5)$$

$$g_{mA} V_q = sC V_{g1} - C V_{g1}^0 \quad (4.6)$$

$$g_{mA}V_p = sCV_{g2} - CV_{g2} \quad (4.7)$$

The currents $g_{mb}V_{ip}$ and $g_{mb}V_{ip}$ have been neglected because they cause V_{od} to increase at a linear rate, which means their role is negligible with respect to the exponential behavior that results from positive feedback. Moreover, g_{mb} is several times smaller than g_m . By subtracting equation 4.5 from equation 4.4 and equation 4.7 from equation 4.6 the result is the system:

$$\begin{cases} g_m V_{od}(s) = sC_L V_{od}(s) - sC_L V_{od}^{pre} + g_m V_{gd}(s) \\ -g_{mA} V_{od}(s) = sC V_{od}(s) - sC V_{gd}^0 \end{cases} \quad (4.8)$$

where $V_{od} \equiv V_p - V_q$ is the output differential voltage and $V_{gd} \equiv V_{g1} - V_{g2}$ is the differential signal at the gate terminals of $M_{1,2}$. At the end of Preamplification phase and so at the begin of Regeneration phase $V_{g1} = V_{g2} = V_{DD}$, which implies $V_{gs}^0 = 0$ V.

The solution of 4.8 for $V_{od}(s)$ is:

$$V_{od}(s) = \frac{sV_{od}^{pre}}{s^2 - s\frac{g_m}{C_L} - \frac{g_m g_{mA}}{C C_L}} \quad (4.9)$$

The poles of $V_{od}(s)$ are given by

$$p_{1,2} = \frac{g_m}{2C_L} \left(1 \pm \sqrt{1 + \frac{4\tau_L}{\tau_{AND}}} \right) \quad (4.10)$$

where $\tau_L \equiv C_L/g_m$ and $\tau_{AND} \equiv C/g_{mA}$. Assuming:

$$\delta \equiv \sqrt{1 + \frac{4\tau_L}{\tau_{AND}}} - 1 > 0 \quad (4.11)$$

the consequence is that the two poles can be rewritten as

$$p_1 = \frac{g_m}{C_L} (1 + \delta) \quad (4.12)$$

$$p_2 = -\frac{g_m \delta}{2C_L} \quad (4.13)$$

Calculating the inverse Laplace transformation of 4.9, with a few additional straightforward passages the resulting expression is:

$$v_{od}(t) = \frac{V_{od}^{pre}}{2} \left(\frac{2 + \delta}{1 + \delta} e^{\frac{t}{\tau_1}} + \frac{\delta}{1 + \delta} e^{-\frac{t}{\tau_2}} \right) \quad (4.14)$$

where $\tau_1 \equiv 1/|p_1|$ and $\tau_2 \equiv 1/|p_2|$. Two observations can be made:

- The first term in the right side of equation (4.14) shows that the initial difference will be regenerated exponentially until the outputs saturate. The second term, instead, vanishes as $t \rightarrow \infty$, and is thus negligible.

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- In the case of absence of the AND gates, the regeneration time constant would be simply C_L/g_m , (since $\tau_{AND} \rightarrow \infty$ and δ would be 0) which is greater than $C_L/(g_m(1 + \delta)) = \tau_1$. This confirms that not only the addition of the AND gates improves power consumption by avoiding static consumption during reset phase by cutting the conductive path between V_{DD} and ground, but it also aids the regenerative phase improving the performances in terms of delay. The improvement with respect to the version without AND gates depends on the ratio τ_L/τ_{AND} : the smaller τ_{AND} is compared to τ_L , the larger the reduction in delay that is obtained by adding the AND gates. This is in accordance with intuition, because the advantage that derives from the AND gates becomes larger as their delay decreases.

By neglecting the exponentially decreasing term in equation (4.14), the full expression of the regeneration time is obtained in closed form; its expression is

$$t_{reg} = \tau_1 \ln \left(\frac{V_{DD}(1 + \delta)}{V_{od}^{pre}(2 + \delta)} \right) = \frac{C_L}{g_m(1 + \delta)} \ln \left(\frac{V_{DD}(1 + \delta)}{V_{od}^{pre}(2 + \delta)} \right) \quad (4.15)$$

As usual, the regeneration time has been calculated as the solution of $V_{od}(t) = V_{DD}/2$ for t that is the time required by the comparator to regenerate half the V_{DD} on its differential output voltage, starting from the initial difference V_{od}^{pre} .

By combining (4.1) and (4.15), an analytical estimate of the comparator's total delay is obtained:

$$t_d = t_{pre} + t_{reg} = \frac{C_L V_{LIM}}{I_{cm}} + \frac{C_L}{g_m(1 + \delta)} \ln \left(\frac{V_{DD}(1 + \delta)}{V_{od}^{pre}(2 + \delta)} \right) \quad (4.16)$$

Analysis of the input referred offset vs mismatch variations One of the main limitation of body driven stages compared to gate driven ones is the input referred offset, which is a main requirement in many comparator for ADCs input range purposes. In this section it has been evaluated the impact of the low body transconductance gain on the offset performance.

In [3] a detailed analysis of the input referred offset has been derived for gate-driven architecture as:

$$\sigma^2(V_{GS}) \approx \sigma^2(V_T) = \frac{A_{V_T}^2}{W L} \quad (4.17)$$

where $\sigma(V_{GS})$ is the standard deviation of the gate-source voltage, A_{V_T} is the area proportional constant for the V_{GS} voltage and W and L are the width and the length of the transistor, according to Pelgrom's law [125]. Similarly one can derive the input offset voltage for a body-driven architecture as:

$$\sigma^2(V_{BS}) \approx \sigma^2(V_T) = \frac{A_{V_T}^2}{W L} \cdot \frac{1}{\alpha^2} \quad (4.18)$$

Where, a further term α was added in order to take into account the threshold voltage dependence with respect to V_{BS} according to the following relation: $V_T = V_{th0} - \alpha \cdot V_{BS}$. The α term is lower than 1, thus, it is clear that with considering equal transistor sizes, the body-driven stages would degrade their performance with respect to gate-driven ones according to a given technology node or CMOS process.

Table 4.1. Transistor sizing of the proposed comparator.

Device	W	L
	$[\mu m]$	$[\mu m]$
$M_{1,2}$	2	2
$M_{3,4}$	40	0.2
$M_{5,6}$	2	0.2
$M_{7,8}$	5	1
$M_{9,10}$	1	1

4.2.3 Sizing and layout

The proposed comparator was designed and simulated in a commercial 130-nm technology by STMicroelectronics. Transistors sizing is the result of a trade-off between delay and input-referred offset. In detail, the comparator sizing has been optimized for the minimum delay while achieving an acceptable input-referred offset under mismatch variations. Then, the aspect ratio of the PMOS devices was chosen respecting the criteria $g_{m,n} = g_{m,p}$ when $V_{ocm} \approx V_{DD}/2$. This ensures that both outputs are fully regenerated (one to V_{DD} and the other to ground) even for small input differences. Suppose for instance that V_{id} is very close to zero. A $g_{m,p}$ too small compared to $g_{m,n}$ implies that M_4 would not be able to pull V_q all the way up to V_{DD} . Vice versa, a $g_{m,p}$ higher than $g_{m,n}$ implies that M_1 would not be able to pull V_p down to ground. The resulting device dimensions, optimized for operation at 0.3 V supply, are reported in Tab. 4.1. It is important to note that the use of body driving applied to NMOS devices requires a triple-well process and leads to an increase in overall area occupation. However, it should also be remarked that the design was optimized to minimize resource consumption as much as possible. The layout is reported in Figure 4.5, and shows an area of about $667.604 \mu m^2$ ($31.64 \mu m \times 21.10 \mu m$). Standard cells have been used for the AND gates.

4.2.4 Simulation results

The comparator has been post-layout simulated with Cadence Virtuoso. All simulations were carried out by loading the outputs of the comparator with minimum area inverters

Figure 4.6 shows the transient behavior of V_p , V_q , V_{g1} and V_{g2} during the evaluation phase. According to what has been explained in the theoretical analysis in subsection 4.2.2, during pre-amplification the output nodes are discharged linearly because I_{d1} and I_{d2} remain constant. The initial spike that causes V_p and V_q to rise above V_{DD} is the effect of clock feed-through. More in detail, the clock rising edge is coupled to the outputs through the C_{gd} of $M_{5,6}$ and through the equivalent parasitic capacitance between the AND gates inputs. As the output common-mode voltage reaches a certain threshold, the positive feedback loop activates, amplifying the signal until the outputs become saturated. Throughout the pre-amplification phase and into a portion of the regeneration phase, both V_{g1} and V_{g2} remain in a high state. Once V_p decreases sufficiently, V_{g2} transitions, deactivating M_2 and thereby interrupting the static current path that runs through M_2 and M_4 . Meanwhile, V_{g1}

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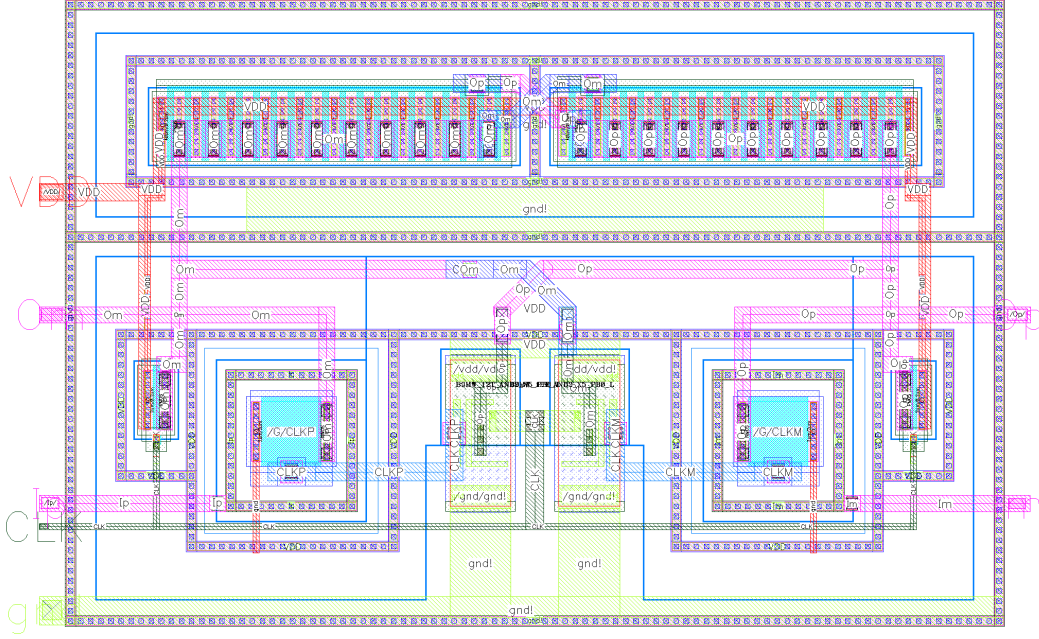


Figure 4.5. Layout of the proposed comparator.

stays high, allowing V_q to be fully driven down to ground potential.

Figure 4.7 illustrates how the comparator's performance shifts as the input common-mode voltage, V_{icm} , is varied throughout the full range from 0 to V_{DD} . As expected, the comparator achieves a full rail-to-rail input common-mode range (ICMR), ensuring consistent operation across the entire V_{icm} span. The power consumption remains largely stable, with fluctuations under 4%, while the comparison time varies by around 50%. Additionally, the standard deviation of the input-referred offset (σ_{offset}) shows a similar 50% variation, increasing as V_{icm} rises. This effect occurs because an increase in V_{icm} in an NMOS body-driven differential pair lowers the threshold voltage, leading to a higher overdrive. Since the gate-source voltage is fixed at V_{DD} (exceeding the threshold voltage when V_{DD} is 0.3 V), σ_{offset} is proportional to the overdrive voltage.

Table 4.2 provides a summary of the comparator's performance at $V_{id} = 1$ mV, evaluated for three different V_{DD} levels: 0.15 V, 0.3 V, and 0.5 V. The maximum clock frequency that ensures reliable operation under worst-case conditions is presented, along with data on comparator delay, power consumption, power-delay product (PDP), and energy-delay product (EDP). Owing to its energy-efficient structure with minimized stacked devices, the proposed comparator excels in both speed and power efficiency. Performance analysis shows that even at $V_{DD} = 0.3$ V, clock frequencies above 1 MHz are easily attainable, while slower operation is achievable at V_{DD} levels as low as 0.15 V.

To better understand the potential of the ULV comparator figure 4.8 reports the trend of the delay as the V_{DD} varies. $V_{DD} = 0.15$ V is the lower limit for the supply voltage since a lower supply voltage would result in excessive delays, whereas

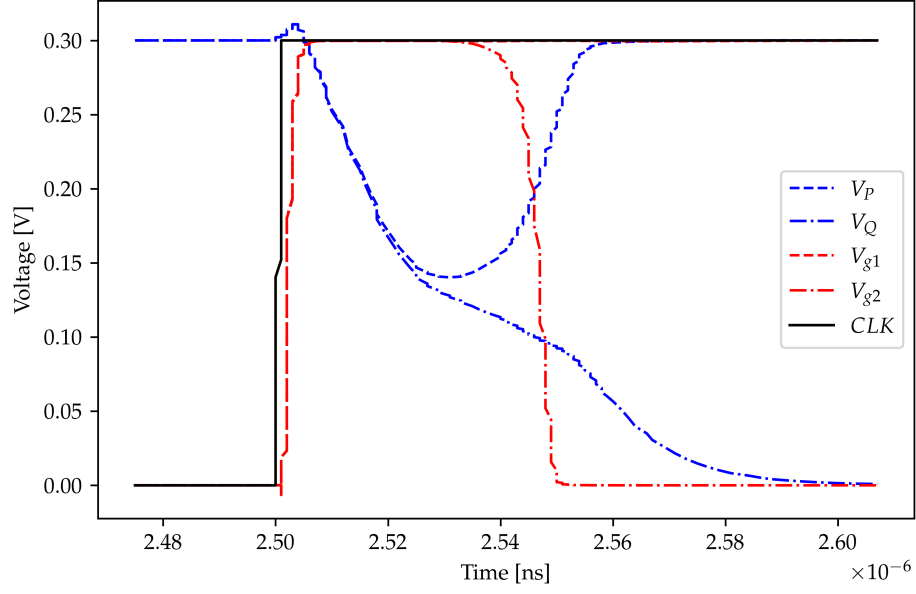


Figure 4.6. Transient behavior of V_p , V_q , V_{g1} and V_{g2} during the evaluation phase.

V_{DD} [V]	0.15	0.3	0.5
f_{ck} [MHz]	0.08	2	16
t_d [ns]	2200	59.27	9.26
P_d [nW]	0.856	52.50	12.96
PDP [fJ]	1.88	3.11	12.96
EDP [aJ/kHz]	23.584	1.556	0.810

Table 4.2. Performance summary of the proposed comparator vs V_{DD} , with $V_{id} = 1$ mV.

the upper limit to the supply voltage is set by the need of avoiding turning on the body-source junction.

In order to demonstrate that the the body terminal current absorption, which could be substantial, remains limited, a DC sweep simulation is performed on the comparator. The setup used to this end is as follow: the clock signal was set to V_{DD} and the output voltages V_p and V_q were set to the same value to deactivate the positive feedback loop. This was done to avoid tripping on the comparator outputs during the DC simulation, which would have created an asymmetry in the final result. The output common mode was chosen so as to ensure that $I_{d3,4} \approx I_{d1,2}$. Figures 4.9a and 4.9b show the static input currents versus the input differential voltage when $V_{DD} = 0.3$ V and when $V_{DD} = 0.5$ V, respectively. At 0.3 V supply voltage the input currents are negligible, since they do not even exceed 1 pA. As expected, their value increases significantly when the supply voltage raises to 0.5 V. The maximum current in this case is around 100 pA, which however is still acceptable for most applications. From figure 4.9a it can be seen that the sign of the current toggles when the single-ended input voltage falls below a certain threshold (which is

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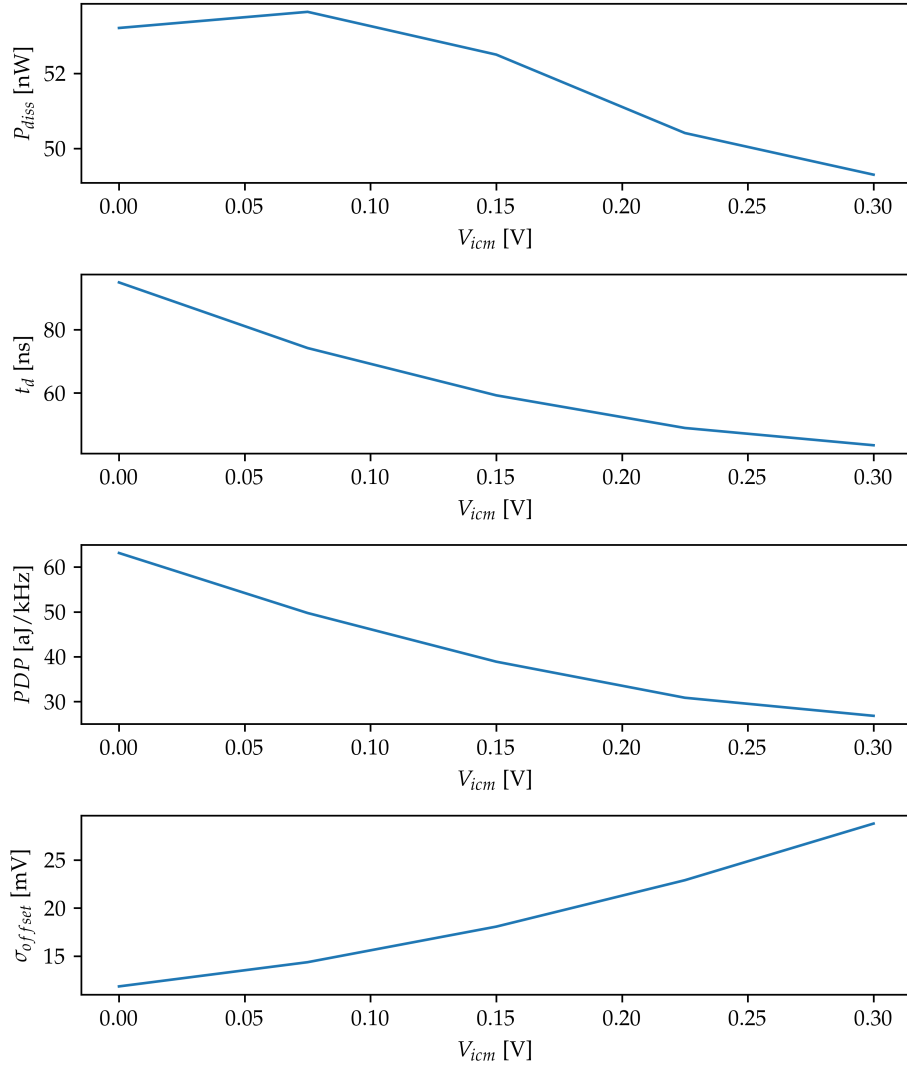


Figure 4.7. Performance of the proposed comparator when V_{icm} varies from 0 to V_{DD} .

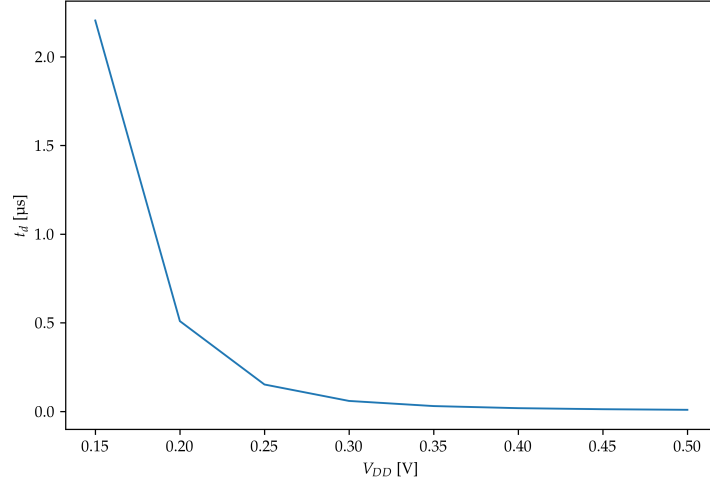


Figure 4.8. Delay of the proposed comparator vs V_{DD} .

around 100 mV). This phenomenon arises because the body current is determined by the difference between the forward current through the source-body junction and the reverse current through the drain-body junction. When V_{bs} is reduced to a sufficiently low level, the forward current term becomes smaller than the reverse current term. Consequently, this leads to a situation where the net current entering the body terminal of the transistor is negative. For brevity, static input current plots as a function of V_{icm} have been omitted, as the resulting curves are nearly identical to those shown in Figures 4.9a and 4.9b. The primary distinction is that one of the curves appears as a reflection across the y -axis.

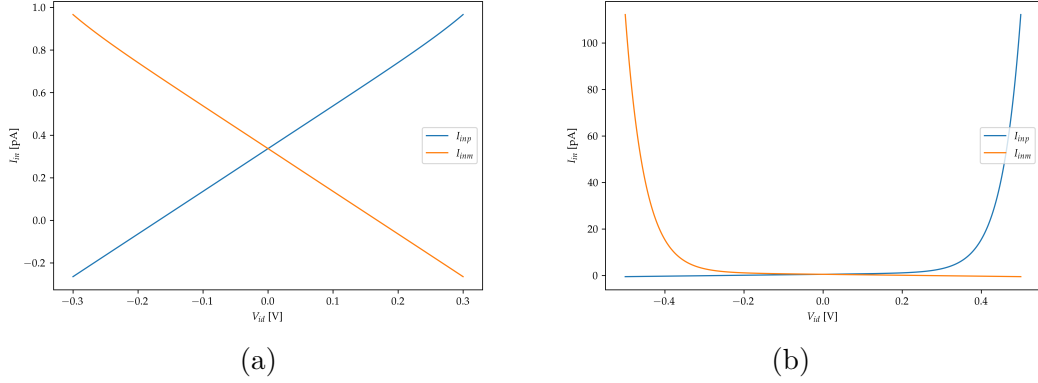


Figure 4.9. Static input currents of the proposed comparator vs input differential voltage (a), Static input currents of the proposed comparator vs input differential voltage (b) with $V_{icm} = V_{DD}/2$ and $V_{DD} = 0.3$ V .

The comparator has been tested under PVT (process, supply voltage and temperature) corners and mismatch in order to demonstrate its robustness. The PVT corners simulation results, at $V_{DD} = 0.3$ V and $f_{ck} = 2$ MHz are reported in table 4.3. The comparator shows good performance consistency under a wide range of operating conditions. Power consumption remains almost constant, since it is dominated by

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the dynamic component due to switching, whereas some variation of the delay is reported.

Table 4.3. Corners at $V_{DD} = 0.3$ V, $f_{ck} = 2$ MHz and $V_{id} = 1$ mV.

Performance	Nominal	Vddmin	Vddmax	Tmin	Tmax	SS	FF	SF	FS
t_d [ns]	59.27	97.94	39.4	74.09	44.85	81.78	44.38	79.97	49.08
P_d [nW]	52.5	42.35	65.62	41.84	71.6	48.9	57.72	51.63	53.71
PDP [fJ]	3.11	4.15	2.59	3.10	3.21	4.00	2.56	4.13	2.64
EDP [aJ/kHz]	1.56	2.07	1.29	1.55	1.61	2.00	1.28	2.06	1.32

The histograms in figures 4.10a and 4.10b show, respectively, the results in terms of power consumption and delay, of the Montecarlo process variations simulations that were carried out on the comparator. The results confirm the robustness of the circuit against process variations.

Figure 4.11 shows the histogram of the comparator's input-referred offset, derived from 100 runs of a Montecarlo mismatch simulation. The resulting standard deviation is approximately 18 mV, with an average value close to zero (less than 1 mV). The increased standard deviation, as compared to gate-driven designs, can be attributed to the fact that the body transconductance g_{mb} is significantly lower than the gate transconductance g_m . This is a characteristic challenge for body-driven comparators.

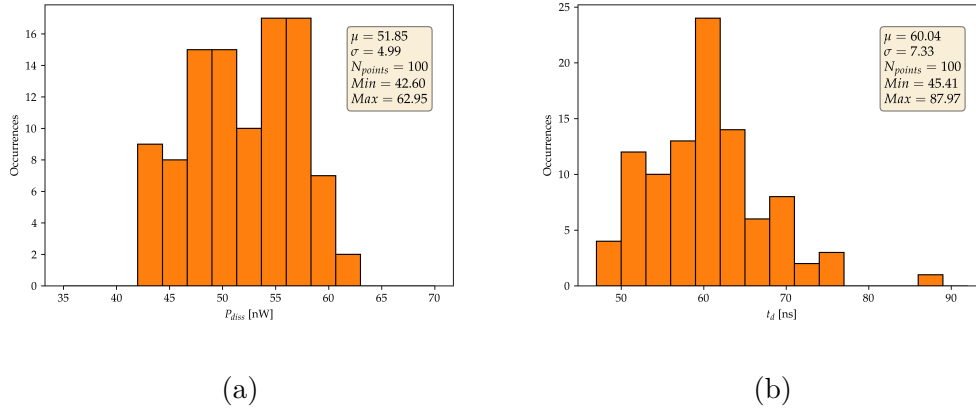


Figure 4.10. Histogram of power consumption (a) and delay (b) of the proposed comparator under process variations.

4.2.5 Comparison with the literature

In this section the proposed comparator performances are compared with the state of the art of ULV comparators. It is important to underline that, despite a lot of 0.5 V comparators have been presented in literature most of them have not been characterized.

In order to make the comparison fair enough some FOMs have been used or even defined. The main one is the EDP, already defined in 2.4.3.

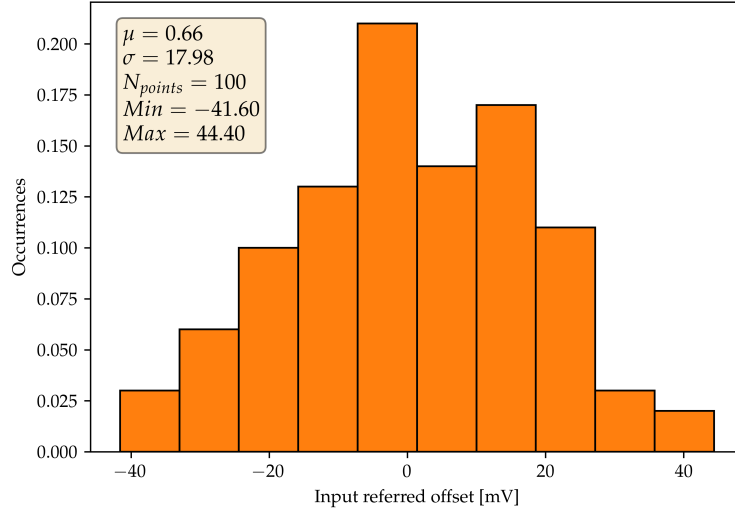


Figure 4.11. Histogram of input-referred offset (a), power consumption (b) and propagation delay (c) under mismatch variations.

Clearly, the lower EDP, the better the trade-off between power consumption and delay.

A further FOM has been defined for comparison purposes taking into account ICMR too, that is the EDP divided by the ICMR normalized to the supply voltage:

$$FOM = \frac{P_d}{ICMR/V_{DD}} \cdot \frac{t_d}{f_{ck}} = \frac{EDP \cdot V_{DD}}{ICMR} \quad (4.19)$$

Also in this case, a lower FOM indicates a better performance considering both the speed-power trade-off and the input common mode range. Normalizing the ICMR ensures a fair comparison between topologies that have been tested at different supply voltages.

Tab. 4.4 reports the performance of comparators operating at up to 0.5 V supply voltages; both analog comparators and standard-cell-based ones have been considered, since the latter are often used in applications at these low supply voltages. Performance of the proposed comparator was reported at 0.15, 0.3 and 0.5 V supply. When available, the performances of comparators in the literature have also been reported at different supply voltages. As shown in Tab. 4.4, the main performance metrics for each comparator are detailed, along with the simulation parameters, which include the input differential voltage V_{id} and the clock frequency f_{ck} . The table also specifies the type of input interface, whether gate-driven (GD) or body-driven (BD), and the specific comparator topology employed. Additionally, it encompasses other performance metrics such as area, supply voltage, and the Input Common Mode Range (ICMR). This data enables the computation of the power-delay product (PDP), energy-delay product (EDP), and the figure of merit (FOM) as defined in 4.19.

The only other comparator reported to function at 0.15 V is that presented by [2]. Comparators discussed in [152] and [71] were not characterized and therefore

4.2 A 0.15-to-0.5 V body-driven dynamic comparator with rail-to-rail ICMR77

omitted from comparison. The mentioned comparator exhibits a significantly higher delay, leading to poorer figures of merit. Its offset is also larger despite utilizing gate driving and having a larger area. The comparative table demonstrates that the proposed comparator surpasses other designs in the literature at supply voltages of up to 0.4 V. A comparable EDP at 0.3 V was documented by [4], though it lacks data regarding offset performance. Both the comparator from [4] and the one from [7] are notably efficient at a supply voltage of 0.5 V.

Table 4.4. Comparison with the state-of-the-art of ultra-low voltage comparators.

	this work			[2]	[2]	[4]	[70]	[7]	[51]	[24]	[4]	[88]	[7]
Topology	BD-SA			STD-CELL	STD-CELL	BD-SA	STD-CELL	BD-SA	DT	DT	BD-SA	SA	BD-SA
V_{DD} [V]	0.15	0.3	0.5	0.15	0.3	0.3	0.35	0.35	0.4	0.4	0.5	0.5	0.5
Technology [nm]	130	130	130	180	180	180	45	90	180	28	180	180	90
Type	BD			GD	GD	BD	GD	BD	BD	GD	BD	GD	BD
Area [μm^2]	670	670	670	900	900	-	59	-	-	-	-	-	-
ICMR [mV]	150	300	500	135	275	300	350	-	200	200	500	-	500
ICMR-rail-to-rail	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✓	✗	✓
Max. t_d [ns]	2200	59.27	9.26	442000	34700	980	2100	2.22	594	1330	16.4	5.77	0.5
V_{id} [mV]	1	1	1	10	10	0.5	10	-	0.1	0.1	0.5	2	1
f_{ck} [kHz]	80	2000	16000	10	10	62.5	10	50	100	100	5000	200000	333000
Offset (σ_{off}) [mV]	18.74	17.98	18.14	31	8	-	4.73	-	13.7	15.3	-	0.29	5.1
$\frac{\sigma_{off}}{V_{DD}}$ [%]	12.49	5.99	3.63	20.67	2.67	-	1.35	-	3.42	3.82	-	0.06	1.02
P_d [nW]	0.856	52.5	1400	0.027	0.024	0.1	-	184	4.48	14.6	20.2	34000	2300
PDP [aJ]	1883.86	3111.67	12964	11934	3088.3	98	-	408.48	2661.12	19418	331.28	196180	1145.4
EDP [aJ/kHz]	23.55	1.55	0.81	1193.4	308.83	1.57	-	8.17	26.61	194.18	0.07	0.98	0.003
FOM [pJ/kHz]	23.55	1.55	0.81	1326	336.9	1.57	-	-	53.22	388.36	0.07	-	0.003

SA: Strongarm; BD: Body-Driven; GD: Gate-Driven BD-SA: Body-Driven Strong Arm; DT: Double-Tail; STD-CELL: Standard-Cell-Based.

4.2.6 Conclusion

This section presents an ultra-low voltage latched comparator based on the Strongarm topology. Body driving is utilized to achieve a rail-to-rail ICMR. In this design, standard Strongarm topology inverters are replaced by simple cross-coupled PMOS devices, and the clocked tail current generator is removed, resulting in a core comparator with only two stacked devices. The clock signal is applied directly to the gates of the input devices, enabling on/off switching through a feedback path that minimizes power consumption.

The comparator operates at supply voltages as low as 0.15 V, delivering impressive speed and power efficiency, with an input-referred offset around 18 mVrms, comparable to other body-driven designs. Comparative analysis with existing literature demonstrates that the proposed comparator outperforms state-of-the-art designs at supply voltages up to 0.4 V, achieving power consumption of 856 pW (52.5 nW) at 0.15 V (0.3 V), an operating clock frequency of 80 kHz (2 MHz), and a maximum delay of 2.2 μ s (59.27 ns).

4.3 Enhancing Performance of Ultra-Low Voltage Body-Driven Comparators Through Clocked Supply Voltage

In this section a novel technique to enhance noise and offset performance of ULV comparators is presented. The technique consists in clocking the latch devices supply voltage in order to induce a positive step on the common mode output voltage at the begin of the pre-amplification phase. This causes the pre-amplification time to increase and, consequently, the pre-amplification gain is enhanced since the output nodes have to be discharged for a longer time before the latch activates. Increasing the pre-amplification gain leads to an improvements of noise and offset performance, as extensively discussed in [?]. This approach has been validated on the ULV comparator in section 4.2. Post-layout simulation results on commercial 130 nm node confirm the theoretical hypotheses showing a 20% and 15% reduction of input referred noise and offset respectively, while the EDP remains essentially unchanged [117]. This section is organized as follow: In section 4.3.1 the proposed technique is described and a theoretical analysis is performed, in section 4.3.2 the simulations results are reported and compared with the results of the same simulations on the comparator without the technique, in section 4.3.3 the results are compared with the state of the art and the conclusions are drawn in section 4.3.4.

4.3.1 Proposed technique

Recap on the ULV comparator topology The technique has been applied and validated on the ULV comparator of section 4.2. The topology and its working principles are described in detail in 4.2. The topology is kept completely unchanged, except for the latch PMOSs ($M_{3,4}$ with reference to figure 4.1 in the mentioned section 4.2) source nodes, that, in this case are connected to the signal V_{DDC} that is the output of a buffer driven by the clock signal. The resulting comparator schematic

is showed in figure 4.12 The buffer is used to provide the necessary amount of current drawn by the source nodes of the PMOSs; The buffer power consumption has been obviously taken into account in the evaluation of the performance of the comparator through the simulations.

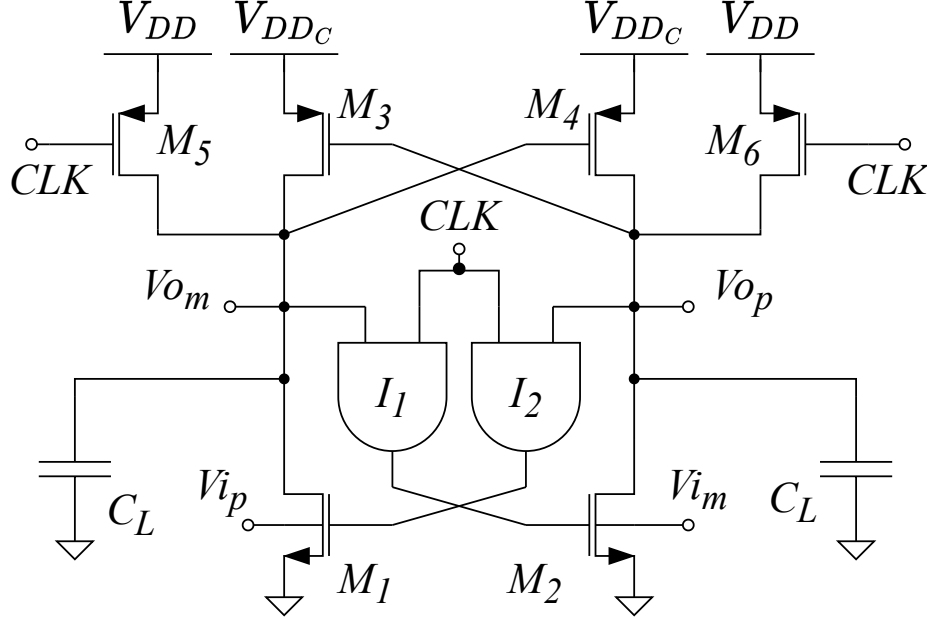


Figure 4.12. Proposed ULV body-driven comparator with the clocked supply voltage strategy.

Working principles of the technique To describe how the technique works and, in particular, how it can affect the pre-amplification performances, the working principles of the ULV comparator of section 4.2 are considered. In particular, with reference to subsection 4.2.1, the operation of the comparator (in general the operation of a Strongarm comparator see 2.4.2) can be divided in three phases: Reset phase, Preamplification phase and Evaluation phase that are detailed in the mentioned subsection. Applying the technique to the comparator does not substantially affect the reset phase, since the latch PMOSs are turned off during this phase and the fact that their source nodes voltages are set to ground has no relevance, the output nodes are normally reset. The effect of the technique can be appreciated when the clock toggles and the pre-amplification phase begins. In fact, the rising edge of the V_{DDC} signal, which is slightly delayed and smoothed by the buffer, is coupled to the output nodes through the parasitic capacitances. This causes the common-mode output voltage V_{ocm} to experience a positive step of amplitude V_{step} . Therefore, the pre-amplification phase continues as usual except for the initial output voltages to be discharged that is, in this case $V_{DD} + V_{step}$ and so the time that elapsed before Preamplification phase ends is larger and the pre-amplification gain becomes significant larger. Regeneration phase is identical to the conventional comparator.

Theoretical justification The positive effect of the technique described so far is that $V_{o_{cm}}$, at the begin of Preamplification phase, is increased by coupling the rising edge of V_{DDC} . To show how this translates into improved performances in terms of noise and offset, consider the expression of the gain of the dynamic pre-amplifier of [34], described in detail in subsection 4.2.2 :

$$A_v^{pre} = \frac{g_{m_{1,2}}}{I_{D_{1,2}}} \Delta V \quad (4.20)$$

where $g_{m_{1,2}}$ and $I_{D_{1,2}}$ are the transconductance and the drain current of the input pair, respectively. ΔV represents the amount by which $V_{o_{cm}}$ has to be discharged before the regeneration phase begins. In the conventional Strongarm comparator $\Delta V = V_{th_{3,4}}$, whereas, in ULV circuits $V_{th_{3,4}}$ has to be interpreted as the threshold above which the sub-threshold current of the PMOS becomes comparable with that of the input pair. This is because V_{DD} is often lower than the actual MOS threshold.

In the proposed configuration, the rising edge of V_{DDC} causes the output common mode to experience a positive step $V_{step} = \alpha V_{DD}$, where α represents a capacitive divider. Defining $C_{par,c}$ the parasitic capacitance between the output nodes and V_{DDC} , and $C_{par,g}$ the parasitic capacitance between the output nodes and ground, then α can be written as $\alpha = C_{par,c} / (C_{par,c} + C_{par,g})$. The effect of this capacitive coupling is that $V_{o_{cm}}$ needs to be discharged by $\Delta V + \alpha V_{DD}$ and the expression of A_v^{pre} becomes

$$A_v^{pre} = \frac{g_{m_{1,2}}}{I_{D_{1,2}}} (V_{th_{3,4}} + \alpha V_{DD}) \quad (4.21)$$

which is larger compared to the conventional topology in which $\Delta V = V_{th_{3,4}}$. Therefore the proposed technique helps to reduce input referred noise and offset , which are (to a first approximation) inversely proportional to the pre-amplification gain. What may seem like a drawback, namely that the duration of the pre-amplification phase increases because it is proportional to ΔV , is in reality not such. In fact, the total delay is only slightly influenced because the increase in pre-amplification time is compensated by the larger pre-amplification gain, that implies larger initial differential output voltage at the begin of Preamplification phase. In this the latch has to regenerate the signal from a more favorable initial condition, improving the regeneration time. In addition, forcing the V_{sd} of $M_{3,4}$ to 0 during the reset phase reduces leakage and thus power consumption.

Sizing and layout The comparator has been designed in a 130nm STMicroelectronics technology. Transistors sizes are reported in table 4.5 and the layout is depicted in figure 4.13.

Table 4.5. Transistor sizing of the proposed comparator.

Device	W [μm]	L [μm]
$M_{1,2}$	2	2
$M_{3,4}$	40	0.2
$M_{5,6}$	2	0.2

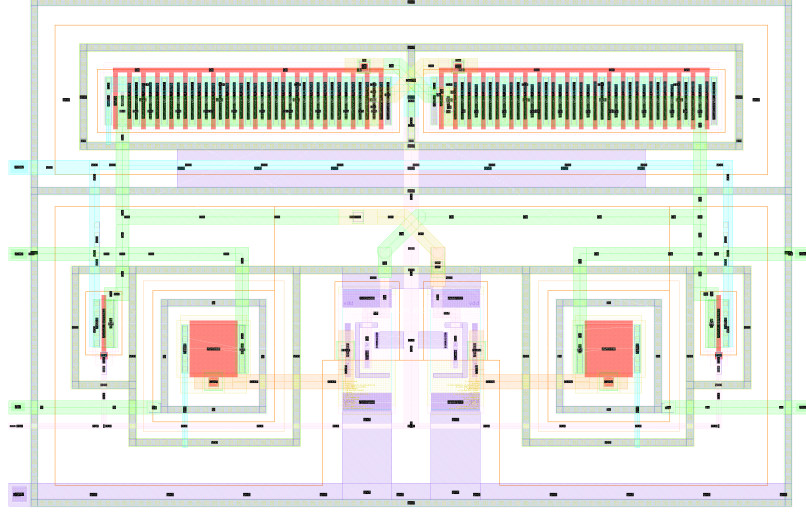


Figure 4.13. Layout view of the proposed comparator, the total amount of area is $667.604 \mu\text{m}^2$ ($31.64 \mu\text{m} \times 21.10 \mu\text{m}$).

4.3.2 Simulations results

The proposed approach has been validated through post-layout simulations performed with Cadence Virtuoso at a $V_{DD} = 0.3$ and a clock frequency of $f_{CLK} = 2$ MHz by applying an input differential voltage of 1 mV. As already specified, V_{DDC} has the same phase and duty cycle as the clock signal that drives $M_{5,6}$, but is provided by a buffer and so is slightly delayed with respect to the main clock signal. The transient behavior of the clock signals and of the output voltages of the comparator are reported in figure 4.14. The input differential voltage is also reported for better clarity.

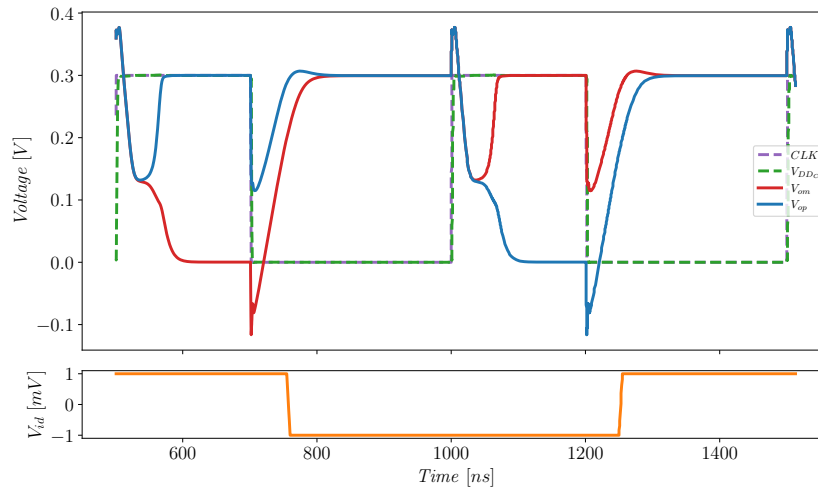


Figure 4.14. Transient simulation of the proposed comparator.

From what can be deduced from the figure 4.14, V_{DD_C} causes a rapid increase in $V_{O_{cm}}$ at the beginning of the pre-amplification phase. The amplitude of the step V_{step} is approximately 70 mV so it is possible to estimate α and $\alpha = \frac{V_{step}}{V_{DD}} \approx 0.23$. The outputs are then discharged at constant current by the input pair until the drain current of $M_{3,4}$ becomes significant and the positive feedback loop is activated. The improvement in gain is caused by the increase of the range of $V_{O_{cm}}$ during pre-amplification.

In order to make the comparison between the two version of the comparator topology with and without the technique and the others topologies in the literature fair, a FOM, taking into account the main Key parameters has been defined as follows:

$$FOM = \frac{EDP \cdot \sigma_{noise} \cdot \sigma_{off} \cdot VDD}{ICMR} \quad (4.22)$$

The proposed FOM accounts for noise, offset and normalized ICMR. Table 4.6 summarizes the performances of the proposed comparator in terms of: EDP, input-referred noise (σ_{noise}) and offset std. deviation (σ_{off}) and in terms of the FOM. Moreover, a comparison with the topology from [34] without the proposed technique is also shown in the table.

The analysis indicates a significant enhancement, achieving a reduction of 20% in noise and 15% in offset. Additionally, power consumption is marginally reduced due to a decrease in average leakage current. However, this optimization comes at the cost of a minor increase in delay, which is attributed to a longer pre-amplification phase. Nonetheless, this delay degradation is not critical for the intended use case since ULV systems typically operate at frequencies below the MHz range. Moreover, the proposed topology remains one of the fastest documented, achieving a clock frequency of 2 MHz for a differential input voltage of $V_{id} = 1$ mV.

Table 4.6. EDP, Noise and Offset comparison between comparator with and without the proposed technique.

-	[34]	Proposed	Improvement [%]
t_d	59.3	62.8	-5.6
P_d	52.5	51.2	2.5
EDP [aJ/kHz]	1.55	1.61	-3.7
σ_{noise} [mV]	2.45	2.08	19.7
σ_{off} [mV]	18.7	16.2	15.4
$\frac{ICMR}{VDD}$	1	1	0
FOM [aJmV ² /kHz]	72.2	53.9	34.0

Fig. 4.15 shows the histogram of the comparator's input-referred offset, which has been evaluated by running 200 Monte Carlo mismatch and process iterations.

Finally, tables 4.7 and 4.8 summarize the performance of the comparator with and without the proposed technique (respectively) under process, voltage and temperature (PVT) variations. As it can be noticed, the proposed topology exhibits good robustness, and the improvement in noise and offset is maintained in all the corners.

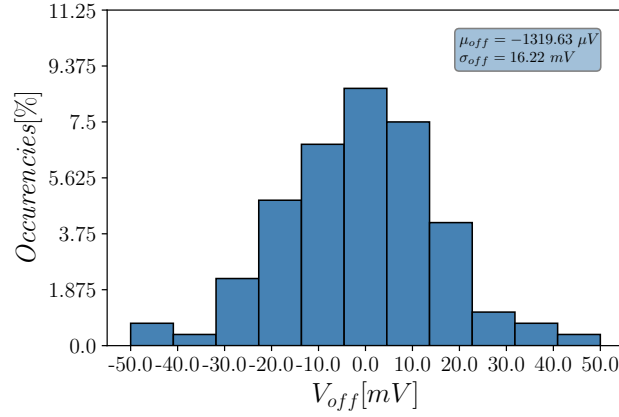


Figure 4.15. Histogram of the proposed comparator's input-referred offset.

Table 4.7. Performance of the proposed comparator *without* clocked supply voltage technique in the nominal corner and under PVT variations ($T^{min} = 0$ °C, $T^{max} = 80$ °C, $V_{DD}^{min} = 270$ mV and $V_{DD}^{max} = 330$ mV).

	TYP.	FF	SS	FS	SF	V_{DD}^{min}	V_{DD}^{max}	T^{min}	T^{max}
t_d [ns]	59.3	44.4	81.8	49.1	79.97	97.9	39.4	74.1	44.9
P_d [nW]	52.5	57.7	48.9	53.7	51.6	42.3	65.6	41.8	71.6
PDP [fJ]	3.11	2.56	4.00	2.64	4.13	4.15	2.59	3.10	3.21
EDP [aJ/kHz]	1.55	1.28	2.00	1.32	2.06	2.07	1.29	1.55	1.61
Noise [mV]	2.49	2.59	2.41	3.03	2.34	3.05	2.41	2.26	3.3

Table 4.8. Performance of the proposed comparator *with* clocked supply voltage technique in the nominal corner and under PVT variations ($T^{min} = 0$ °C, $T^{max} = 80$ °C, $V_{DD}^{min} = 270$ mV and $V_{DD}^{max} = 330$ mV).

	TYP.	FF	SS	FS	SF	V_{DD}^{min}	V_{DD}^{max}	T^{min}	T^{max}
t_d [ns]	62.8	46.8	87.1	51.8	83.7	103.7	41.5	79.6	46.5
P_d [nW]	51.2	56.6	47.8	52.7	49.4	40.4	61.1	41.2	69.8
PDP [fJ]	3.22	2.65	4.16	2.73	4.14	4.19	2.54	3.28	3.25
EDP [aJ/kHz]	1.61	1.33	2.08	1.37	2.07	2.09	1.27	1.64	1.62
Noise [mV]	2.08	2.13	2.04	2.53	1.98	2.66	1.86	1.89	2.78

4.3.3 Comparison with the literature

In table 4.6 the main performance indicators and the FOM of the body-driven ULV comparator with and without the technique are compared. As we already pointed out, the application of the clocked supply results in a significant improvement in noise and offset with respect to the reference topology from [34]. In Tab. 4.9 a full comparison with state of the art of ULV comparators is reported. Unfortunately, the performance in terms of FOM cannot be compared with most of the other works due to the fact that noise and/or offset performance is omitted. Reference [118], the only one for which the FOM can be computed, achieves a slightly better figure of merit. However, its maximum frequency is much lower than the proposed ULV

Table 4.9. Comparison with the state-of-the-art of ultra-low voltage comparators.

	This Work		Simulated		Simulated	Simulated	Simulated	Measured	Simulated
	$V_{id}=1\text{mV}$	$V_{id}=10\text{mV}$	[118]		[34]	[4]	[6]	[2]	[70]
V_{DD} [V]	0.3	0.3	0.15	0.3	0.3	0.3	0.35	0.15	0.3
Tech [nm]	130	130	180	180	130	180	90	180	180
Area [μm^2]	670	670	167.7	167.7	670	-	-	900	900
ICMR [mV]	300	300	150	300	300	300	350	135	275
ICMR-range %	100	100	100	100	100	100	100	90	91.67
Delay [ns]	62.8	48.2	39290	3390	59.27	980	2.22	442000	34700
V_{id} [mV]	1	10	10	10	1	0.5	-	10	10
f_{ck} [kHz]	2000	2000	6.21	71.5	2000	62.5	50	10	10
Offset (σ_{off}) [mV]	16.2	16.2	10.99	11.11	17.98	-	-	31	8
$\sigma_{V_{DD}}^{\sigma_{off}}$ [%]	5.4	5.4	7.33	3.7	5.99	-	-	20.67	2.67
P_d [nW]	51.2	39.8	0.02	0.41	52.5	0.1	184	0.03	0.02
PDP [aJ]	3215.36	1918.36	785.8	1389.9	3111.68	98	408.48	13260	694
EDP [aJ/kHz]	1.61	0.96	126.54	19.44	1.56	1.57	8.17	1326	69.4
Noise [mV]	2.08	2.08	0.24	0.12	2.49	-	-	-	-
FOM [$\text{aJ} \cdot \text{mV}^2/\text{kHz}$]	54.25	32.35	333.76	25.92	69.84	-	-	-	-
BD-SA-CSV			STD-CELL		BD-SA			STD-CELL	

BD-SA-CSV: Body-Driven Strongarm Clocked Supply Voltage, BD-SA: Body-Driven Strongarm; STD-CELL: Standard-Cell-Based.

comparator (as is the case for most references in the Table). Moreover, the EDP of reference [118] is several times larger.

4.3.4 Conclusion

This work explores a novel method for powering ultra-low voltage (ULV) comparators, which involves clocking the supply voltage to increase pre-amplification gain, thereby reducing input-referred noise and offset. The efficacy of the proposed method is demonstrated by applying it to a previously established comparator topology [34]. Post-layout simulations, performed on a 130 nm technology implementation, show improved noise and offset characteristics, with only a minor impact on the Energy-Delay Product (EDP). Additionally, the proposed technique is not limited to the specific topology analyzed in this study; it can be extended to other ULV comparator designs by leveraging clocked supply voltage.

4.4 A 2.5 GHz, 0.6 V body driven dynamic comparator exploiting charge pump based dynamic biasing

In this work a novel 0.6 V dynamic biased and body driven comparator topology is proposed. It is a modified version of the Strongarm comparator that exploits a double CPB dynamic biasing configuration to boost the effective voltage supply headroom. The input signals are applied to the body of the input pair transistors while the gates are driven by the clock, allowing the removal of the tail transistor. In this way the number of stacked devices is reduced and the drain-source voltages of the transistor is increased resulting in better performance at low voltage supply. Moreover, the body-driven enables a rail-to-rail ICMR. The result is a LV high-speed comparator that can work at frequencies up to 2.5 GHz with a competitive EDP of less than 3 fJ/GHz [13]. This section is organized as follow: The proposed topology is described and analyzed in section 4.4.1, section 4.4.2 describes the criteria that were used to size the comparator, the simulation results and the comparison with the

state of the art are reported in section 4.4.3 and section 4.4.4 concludes the work.

4.4.1 Topology description

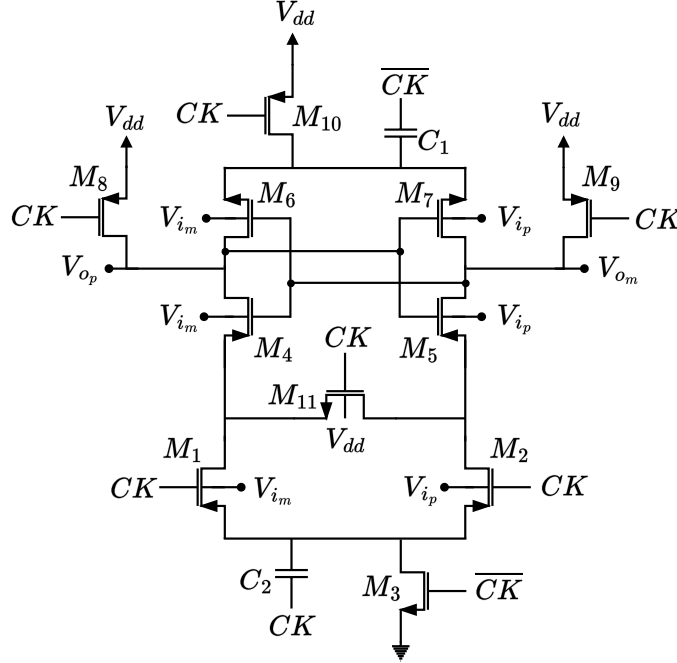


Figure 4.16. Proposed Strongarm-based topology.

The proposed low voltage comparator, reported in figure 4.16, is a modification of the conventional Strongarm comparator described in detail in 2.4.2, it has been modified in order to allow high-speed operations with a supply voltage as low as 0.6 V, the following modifications have been implemented:

- The gates of the input pair transistors are driven by the clock signal, in order to turn off them during pre-charge phase and so the clocked tail transistor can be removed reducing the number of stacked devices. While the input signals are applied to the transistors bodies. This enables a rail-to-rail ICMR since during the evaluation phase $V_{gs1,2} = V_{DD}$, regardless of the input common mode, so that $M1$ and $M2$ are necessarily on.
- The input differential signal is applied also to the body terminals of the latch transistors ($M4$ to $M7$) in order to increase the sensitivity of the comparator.
- The dynamic biasing technique utilizing a charge pump, as described in [9], is leveraged to improve the speed of comparison. In this proposed design, dynamic biasing is applied to both the upper and lower supply rails, enabling transient currents to be delivered through a pair of capacitors (C_1 and C_2). Unlike [9] and other similar approaches that incorporate dynamic biasing, this work emphasizes using charge pump-based dynamic biasing specifically at low supply voltages. This strategy increases the effective voltage headroom, allowing for operational frequencies that would otherwise be unachievable.

The operation of the proposed comparator can be synthesized in three phases:

- **Reset Phase:** When the clock is low the two input pair NMOSs $M_{1,2}$ are turned off. Similarly to the conventional Strongarm comparator, the reset transistors $M_{8,9}$ reset the output nodes voltages to V_{DD} while M_{11} equalizes the drain nodes of the input pair transistors avoiding dynamic offset; Nodes A and B (with reference to figure 4.16) are pre-charged by M_{10} and M_3 to V_{DD} and GND respectively;
- **Preamplification phase:** when the clock toggles, reset transistors ($M_{8,9}$ and M_{11}) and pre-charge transistors (M_3 and M_{10}) are switched off, M_1 and M_2 are switched on by the high clock signal on their gates. The effective voltage headroom are boosted by the coupling of $\overline{CK}$ falling edge, that lowers v_B below ground voltage and by the coupling of CK rising edge to the upper supply bar node that raises v_A above V_{DD} . M_1 and M_2 start pre-amplifying the input differential signal by discharging output nodes V_{op} and V_{om} , this phase ends when output nodes voltage is dropped so that latch transistors turn on activating positive feedback.
- **Evaluation phase:** at this point, the latch is on and can regenerates the signal based on the initial condition set in the pre-amplification phase according to the sign of differential input voltage.

It has to be remarked that during the comparison phase the current is provided by the two capacitors C_1, C_2 and thus no static power consumption occurs in this phase.

4.4.2 Circuit sizing

The LV comparator has been designed in a 55 nm CMOS technology to work at 0.6 V supply. The design has been optimized in order to minimize delay and power consumption. Offset optimization is out of the scope of this work, since several solutions have been proposed in literature and also in this thesis (see 4.4.3 and 5.3) to compensate static offset voltage.

one of the key parameters to be taken into account in the definition of trade-off between speed, power consumption and offset is the width of the input pair transistors. Larger input transistors result in better static offset, as the effect of the offset is minimized.

The transistor widths within the latch have been selected to optimize for minimal delay. It's important to note that increasing the latch transistor widths beyond a specific limit does not yield further improvements in regeneration speed; rather, it contributes to higher parasitic capacitance, ultimately leading to an increase in power consumption. For the pre-charge transistors, the widths were chosen at the minimum necessary value to ensure proper resetting of both output and intermediate nodes. The capacitors, C_1 and C_2 , are implemented as MOS capacitors, with the drain and source terminals of an NMOS shorted together. While larger capacitor values can reduce delay and lead to a greater overshoot on the output differential voltage, they do so at the expense of higher power usage. Table 4.10 outlines the final transistor sizing. Capacitors C_1 and C_2 were each sized to achieve a capacitance close to 16

fF. To provide a comparative reference, a conventional Strongarm latch was also sized and simulated, with the results included in Table 4.10. For components with identical names serving different functions in the two circuits, these distinctions are noted within the table. The conventional Strongarm latch was designed to minimize delay, with a power consumption constraint set at approximately 200 μ W.

Table 4.10. Sizing of the proposed comparator.

Device	Role	W [μ m]	
		Proposed	Reference
$M1, M2$	Same	8	80
$M4, M5, M6, M7$		1	20
$M8, M9$		1.2	5
$M3$	Different	6	100
$M10$		8	5
$M11$		1	5

4.4.3 Simulation and comparison

Nominal and PVT corners As previously discussed in Section 4.4.2, simulations of the proposed comparator topology were conducted using a 55 nm CMOS process at a 0.6 V supply voltage, with a clock frequency of 2.5 GHz. A single-ended load capacitance of 2 fF was connected to each comparator output to simulate a generic load.

The transient response of the output voltages for both the proposed comparator and a conventional Strongarm latch, with $V_{id} = 1$ mV, is reported in figure 4.17. As observed, dynamic biasing via the charge pump elevates V_{op} above V_{DD} , effectively reducing comparison time. This also benefits subsequent blocks, which are driven by voltages exceeding V_{DD} , thus improving their delay performance. Whereas, the conventional Strongarm latch struggles to regenerate the input difference properly, even though it consumes roughly 192 μ W—over twice the power of the proposed comparator. Notably, even with increased power consumption up to 500 μ W, the conventional Strongarm fails to reach the 2.5 GHz operating frequency.

Figure 4.18 presents the delay behavior of the proposed comparator as a function of V_{id} . As expected, the delay decreases logarithmically with increasing V_{id} , resulting in a linear trend on a log-scaled x-axis. This linear slope represents the delay sensitivity of the comparator, which for this design is approximately -28.7 ps/dec.

In figure 4.19, the delay, power consumption, and energy-delay product (EDP) are shown for varying V_{icm} values, swept across the range of $[0, V_{DD}]$. The results indicate stable performance across this range, with negligible power variation and only a minor $\approx 10\%$ increase in delay and EDP. This delay increase is attributed to a reduction in the body transconductance g_{mb} as V_{bs} rises.

The robustness of the comparator under varying supply, temperature, and process conditions has been confirmed, as shown in Table 4.11. These results demonstrate consistent performance across all corners.

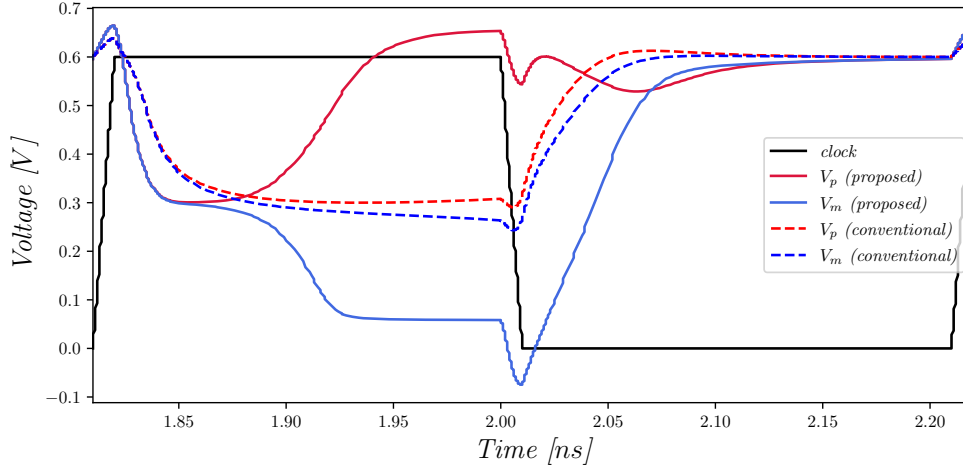


Figure 4.17. Transient response of the proposed comparator's output voltages.

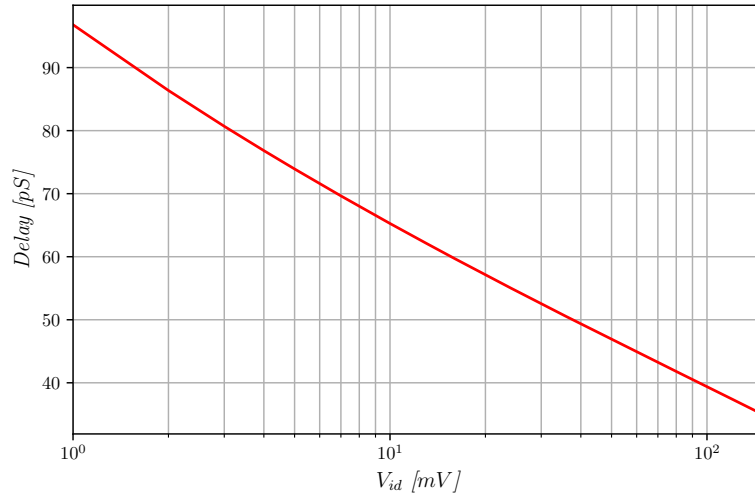


Figure 4.18. Delay of the proposed comparator as a function of input differential voltage.

Table 4.11. Performance of the proposed comparator under nominal and PVT conditions.

	Typ.	V_{dd}^{min}	V_{dd}^{max}	T^{min}	T^{max}	FF	SS	FS	SF
P [μ W]	75.9	59.3	94.2	74.7	78.5	77.3	72.0	75.4	74.8
t_d [ps]	98.3	124	82.3	94.4	106.7	89.3	100	97.7	99.9
PDP [fJ/conv.]	7.46	7.32	7.75	7.05	8.38	6.90	7.20	7.37	7.47
EDP [fJ/(GHz)]	2.98	2.93	3.10	2.82	3.35	2.76	2.88	2.95	2.99

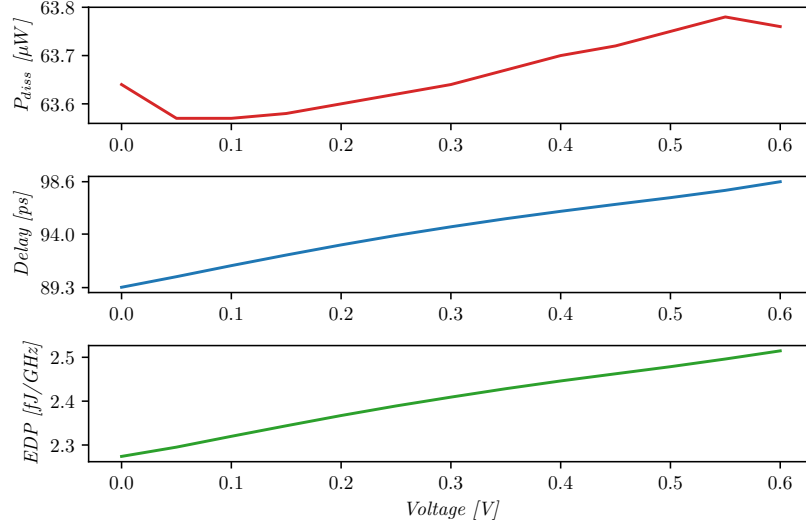


Figure 4.19. Delay, power consumption, and EDP for V_{icm} swept from 0 V to V_{DD} .

Offset Analysis The offset due to mismatch was evaluated through 1000 Monte Carlo simulations, revealing a Gaussian distribution with a mean and standard deviation of 0.27 mV and 51.08 mV, respectively. The body-driven comparator exhibits a higher offset compared to gate-driven designs, given that g_{mb} is generally lower than g_m .

Comparison with Literature A comparison of the proposed approach with recent low-voltage comparators is presented in Table 4.12. Only [109], using a 28 nm process, demonstrates a lower delay. However, our design achieves a 30% lower EDP, highlighting superior energy efficiency. Notably, the performance evaluation in [109] is based on an input differential voltage of 5 mV. At this voltage level, the proposed design achieves a similar delay (74.5 ps) but with a significantly better EDP (2.16 fJ/GHz).

4.4.4 Conclusion

This work introduced a high-speed, low-voltage comparator based on the Strongarm architecture. The proposed design utilizes a body-driven configuration to maximize the input common-mode range (ICMR) and reduce the number of devices in the stack. Additionally, CBP dynamic biasing boosts the effective supply voltage during the evaluation phase, significantly enhancing comparison speed. By combining these techniques, the comparator achieves outstanding delay performance at $V_{DD} = 0.6$ V. Furthermore, the proposed design attains the lowest energy-delay product (EDP) among comparable designs, indicating that the improvements in delay do not compromise energy efficiency. Offset optimization is not a purpose of this work, but this topic has been explored in greater depth in section 4.5 also from a theoretical point of view. Calibration techniques have been proposed and validated both in section 4.5 and in section 5.3

Table 4.12. Literature comparison of low-voltage comparators.

	This Work	[109]	[42]	[87]
Year	2023	2022	2007	2013
Tech. [nm]	55	28	120	180
V_{dd} [V]	0.6	0.6	0.5	0.5
V_{id} [mV]	1	5	-	1
P [μ W]	75.9	194	18	34
t_d [ps]	98.3	70	-	1300
f_{CK} [GHz]	2.5	4	0.6	0.2
EDP [fJ/(GHz)]	2.98	3.4	-	221
ICMR Rail-to-rail	Yes	No	No	Yes
σ_{off} [mV]	51.1	-	57	29.9

4.5 Two Novel 0.6 V, > 2 GHz Latched Comparators with Charge Pump-Based (CPB) dynamic biasing

This work analyzes in depth what was qualitatively assessed in the work in section 4.4 and analyzes the generalization of the advantages brought by the Charge pump-based (CPB) approach not only in terms of speed but also in the speed-noise trade-off. In this section the dynamic bias technique is applied to two single stage comparator operating at 0.6 V. The CPB is used to improve the speed-noise trade-off allowing the operation of the comparators at a supply voltage as low as 0.6 V. A Theoretical analysis of the technique is performed and the theoretical results are validated through simulations in 28 nm ST-microelectronics CMOS technology on the two comparator topologies. This work attempts to provide a theoretical analysis of the CPB dynamic bias in high-speed comparator context, with a focus on sizing criteria and the technique limitations on single stage comparators. The main contributions of this work are:

- A comprehensive theoretical analysis of CPB dynamic biasing in high-speed application. CBP is applied to a conventional single-tail comparator and to a pseudo-differential variant that enable foreground calibration.
- Two novel single-stage topologies are proposed. CBP is involved to maximize operating frequency at low voltage supply, this is obtained by means of the voltage supply headroom enhancement due to the CBP dynamic biasing effect and by the reduction of the number of stacked devices. Following sections are organized in this way: in section 4.5.1 theoretical analysis of CPB is presented, section 4.5.2 describes proposed comparators topologies and section 4.5.3 their sizing and layout, section 4.5.4 reports post-layout simulation results, and section 4.5.5 concludes the work.

4.5.1 Analysis of the charge-pump based dynamic biasing pre-amplifier

Single-tail pre-amplifier In figure 4.21 the equivalent circuit of the dynamic bias pre-amplifier is reported. This is the equivalent circuit the pre-amplifier in the comparator proposed in [11], in the first stage of the double-tail Elzaker comparator.

The inputs V_{ip} and V_{im} are fixed values. The resistance $R_s/2$ is the on-resistance of the CMOS switches that disconnect C_b from the input pair during the reset phase, when the tail capacitor is being pre-charged to ground. Capacitance and resistance values are doubled for ease of comparison with the pseudo-differential topology that will be analyzed in paragraph 4.5.1. It is assumed that M_1 and M_2 operates in saturation region and so their characteristic is linear. This is an approximation justified by the fact that M_1 and M_2 V_{gs} and V_{ds} is boosted by the clock edge coupling of the CPB dynamic bias, through C_{bp} . At this operative V_{DD} and with the modern technologies this is a not too very strong assumption. Then, the I_D - V_{gs} transcharacteristic of M_1 - M_2 is described by the relation in [134]

$$I_D = \mu \mathcal{E}_c C_{ox} W (V_{gs} - V_{th}) \quad (4.23)$$

where μ is the channel carrier mobility, W is the channel width, C_{ox} is the oxide capacitance and $\mathcal{E}_c$ is the critical value of the longitudinal electric field above which carrier velocity stops increasing. In this situation, the small-signal transconductance of the device is constant and is given by:

$$g_m \equiv \frac{\partial I_D}{\partial V_{gs}} = \mu \mathcal{E}_c C_{ox} W \quad (4.24)$$

An so (4.23) is equal to $I_D = g_m V_{ov}$, where $V_{ov} \equiv V_{gs} - V_{th}$ is the overdrive voltage.

Following the validity of this approximation is demonstrated in the event that the ratio C_b/C_L is large enough. The goodness of this approach is also confirmed by the simulations (see subsection 4.5.4).

Hereafter, the input differential-mode and common-mode voltages of the circuit are indicated with V_{id} and V_{ic} , respectively. Similarly, the output differential-mode and common-mode voltages are indicated with V_{od} and V_{oc} will be. Assuming that $V_{id} \ll V_{ic}$, it is possible to decline the hypothesis that M_1 and M_2 operate in saturation region as a condition on the input and output common-mode voltages: $V_{oc} - V_s > V_{ic} - V_{th} - V_s$, which can be simplified as $V_{oc} > V_{ic} - V_{th}$. Preamplification ends when the comparator latch transistors turn on and so the minimum value V_{oc} can assume during pre-amplification is $V_{DD} - |V_{thp}|$ and so the condition can be rewritten as $V_{DD} + V_{th} > V_{ic} + |V_{thp}|$. If V_{ic} is too close to V_{DD} , the condition is not satisfied. typical operative condition of the comparators, in many application is $V_{ic} \approx V_{DD}/2$, thus the hypothesis that M_1 and M_2 remain in saturation during pre-amplification is almost always plausible.

Since in this analysis it is assumed that the charge pump activates at $t = 0^-$ and the switch closes at $t = 0$ the effect of CPB dynamic biasing can be modeled as an initial condition on C_b . This is obviously a simplification: in reality, the clock edge has finite slope and V_b change during the initial part of pre-amplification. Despite

this, the resulting model yields goods predictions, as it is possible to see in subsection 4.5.4. Hereafter it is assumed that $V_{b_0} \equiv V_b(0^-)$.

In the absence of parasitic capacitances one would have $V_{b_0} = -V_{DD}$. In practice, parasitic capacitances towards ground create a capacitive divider that causes V_{b_0} to be equal to $-\alpha V_{DD}$, with $\alpha < 1$.

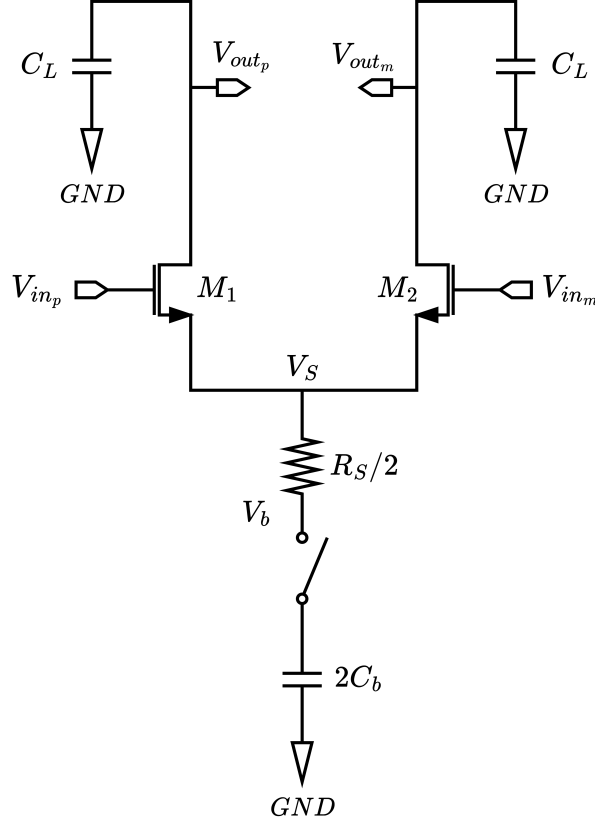


Figure 4.20. Model of the single-tail CPB pre-amplifier.

The current equilibrium for the model of figure 4.20 is described by the following equations:

$$\begin{cases} g_m (V_{ic} - V_s(t) - V_{th}) = G_s (V_s(t) - V_b(t)) & (a) \\ G_s (V_s(t) - V_b(t)) = C_{bp} \frac{dV_b(t)}{dt} & (b) \\ g_m (V_{ip} - V_s(t) - V_{th}) = -C_L \frac{dV_{op}(t)}{dt} & (c) \\ g_m (V_{im} - V_s(t) - V_{th}) = -C_L \frac{dV_{om}(t)}{dt} & (d) \end{cases} \quad (4.25)$$

In the above equations $G_s \equiv 1/R_s$ is the equivalent conductance of the switches. Note that the first two equations are decoupled from the last two since the drain-source resistance of M_1 - M_2 has been neglected. The first step is solving equations 4.25a and 4.25b to find the expression of $V_s(t)$:

$$V_s(t) = \frac{(g_m + G_s)(V_{ic} - V_{th}) - G_s \tilde{V} e^{-t/\tau}}{g_m + G_s} \quad (4.26)$$

where

$$\tau \equiv \frac{C_b}{g_m} \left(1 + \frac{g_m}{G_s} \right) \quad (4.27)$$

and

$$\tilde{V} \equiv V_{ic} - V_{th} - V_{b0} \quad (4.28)$$

Equation (4.26), describes an asymptotic trend for the source voltage $V_s(t)$ that saturates at $V_{ic} - V_{th}$ but this never happens. following the reason of that, assuming $V_{im} < V_{ip}$. V_s increases and eventually become greater than $V_{im} - V_{th}$. In this way M_2 would enter sub-threshold and M_1 would continue to charge the tail capacitor alone. In this simplified model, where $I_D(V_{ov} \leq 0) = 0$, this means that the differential-mode and the common-mode currents of the input pair go to zero. In reality, the input pair enters weak inversion and the pre-amplifier behaves like the conventional dynamic-biased pre-amplifier described in [10].

The overdrive voltages of M_1 and M_2 can be computed as: $V_{ov1,2} = V_{ip,im} - V_s(t) - V_{th}$:

$$V_{ov1,2} = \pm \frac{V_{id}}{2} + \tilde{V} \frac{G_s}{g_m + G_s} e^{-t/\tau} \quad (4.29)$$

By integrating equations (4.25c) and (4.25d), one has

$$V_{op,om} = V_{DD} \pm \left(-\frac{g_m t}{2C_L} \right) V_{id} - \frac{C_b}{C_L} (1 - e^{-t/\tau}) \tilde{V} \quad (4.30)$$

And so the output common-mode voltage is given by

$$V_{oc}(t) = V_{DD} - \frac{C_b}{C_L} (1 - e^{-t/\tau}) \tilde{V} \quad (4.31)$$

while the output differential-mode voltage is

$$V_{od}(t) = -\frac{g_m t}{C_L} V_{id} \quad (4.32)$$

From equation (4.32) it seems that the pre-amplification gain can grow arbitrarily by increasing pre-amplification time. This is a consequence of the simplifications that have been adopted to make the analysis affordable. In real condition, V_{od} cannot diverge because M_1 - M_2 's output resistance is finite.

In most regenerative comparators, the pre-amplification phase ends when V_{oc} drops below V_{DD} by V_t . The value of V_t depends on the particular topology that is being considered. For example, in the conventional dynamic biasing comparator based on Elzaker's topology, $V_t = |V_{thp}|$, where V_{thp} is the threshold voltage of the PMOS coupling devices in the second stage. In the proposed topologies, which will be introduced in the next section, V_t is the threshold of the PMOS devices that form the latch.

The pre-amplification time can be obtained by substituting $V_{oc} = V_{DD} - V_t$ in (4.31) and solving for t :

$$t_{pre} = \tau \ln \left(\frac{1}{1 - \frac{C_L}{C_b} \frac{V_t}{\tilde{V}}} \right) \quad (4.33)$$

The pre-amplification gain A_{pre} is the other key parameter to pay attention in this theoretical analysis. Assuming $V_{od}^{pre} \equiv V_{od}(t_{pre})$. Then, A_{pre} is given by:

$$A_{pre} \equiv \frac{V_{od}^{pre}}{V_{id}} = -\frac{C_b}{C_L} \frac{g_m + G_s}{G_s} \ln \left(\frac{1}{1 - \frac{C_L}{C_b} \frac{V_t}{\tilde{V}}} \right) \quad (4.34)$$

Thanks to the expressions just obtained it is possible to make some observations:

- Observing the expression of pre-amplification time, t_{pre} is a decreasing function of C_b with a horizontal asymptote given by

$$t_{pre}^{min} = \lim_{C_b \rightarrow \infty} t_{pre} = \frac{G_s + g_m}{G_s g_m} \frac{C_L V_t}{\tilde{V}} \quad (4.35)$$

consequently, A_{pre} is a decreasing function of C_b with a horizontal asymptote

$$A_{pre}^{min} = \lim_{C_b \rightarrow \infty} A_{pre} = \left(1 + \frac{g_m}{G_s} \right) \frac{V_t}{\tilde{V}} \quad (4.36)$$

these results indicate the existence of a trade-off between the reduction of the pre-amplification time and the increase of the pre-amplification gain in charge-pump dynamic biasing topologies. The pre-amplification time can be reduced at the cost of increased input-referred offset and noise by enlarging the bias capacitance. Clearly, increasing C_b also causes an increase in the power consumption of the circuit, which however may be secondary in high-speed applications. It is also interesting to note that the tuning of A_{pre} can be also afforded by acting on the g_m/G_s ratio.

- The functions $A_{pre}(C_b)$ and $t_{pre}(C_b)$ have a vertical asymptote in $C_b = C_b^{min}$, where C_b^{min} is given by

$$C_b^{min} \equiv \frac{V_t}{\tilde{V}} C_L \quad (4.37)$$

It is important to underline that, this result stems from a simplified linear model. To obtain better insight on this, it is interesting to compute the expression of the overdrive voltages at $t = t_{pre}$:

$$V_{ov1,2}(t_{pre}) = \pm \frac{V_{id}}{2} + \frac{G_s \tilde{V}}{G_s + g_m} \left(1 - \frac{C_L}{C_b} \frac{V_t}{\tilde{V}} \right) \quad (4.38)$$

Assuming $V_{id} > 0$ and $C_b = C_b^{min}$. Then, equation (4.38) denotes that M_2 enters weak inversion before V_{oc} reaches $V_{DD} - V_t$. If V_{id} is small enough, M_1 will also enter weak inversion shortly after. In reality, drain sub-threshold current is not 0 and so V_{oc} keeps decreasing and the input pair continues to amplify the signal for a while. After enough time has elapsed, the drain current of M_1 - M_2 becomes negligible. Obviously, A_{pre} does not approach infinity as $C_b \rightarrow C_b^{min}$: by observing the analysis developed in [10] shows that the pre-amplification gain of a dynamic pre-amplifier operating in weak inversion is proportional to g_m/I_D . According to theory, in weak inversion g_m/I_D is constant because the I_D - V_{gs} characteristic is exponential. Therefore, as C_b is

decreased towards C_b^{min} , A_{pre} can be expected to start saturating. In addition, A_{pre} is also limited by the finite output resistance of M_1 - M_2 . A more detailed analysis of the effect of M_1 - M_2 's output resistance is provided in subsection 4.5.4

- Letting $t \rightarrow \infty$ in equation (4.31) gives

$$V_{oc}^{\infty} = V_{DD} - \frac{C_b}{C_L} \tilde{V} \quad (4.39)$$

This quantity gives an expression of the theoretical value of the minimum V_{oc} that can be reached during pre-amplification. Similarly to the conventional dynamic biasing pre-amplifier, the variation of the output common mode is directly proportional to the ratio C_b/C_L [10]. The designer should consider that, if this variation is too small, the regeneration time of the comparator becomes very large because the latch (be it a cascoded latch, like the Strongarm latch, or a cascaded stage like the Elzackker comparator) is not allowed to turn on properly.

There are many aspect of the analysis that has been developed above to be taken into account. The pre-amplification gain of the charge pump dynamic biasing pre-amplifier can be tuned by acting upon C_b and the ratio between g_m and the on-state conductance of the tail device (G_s). C_b , in particular, is a key parameter that allows the designer to tune the pre-amplification-time/pre-amplification-gain trade-off and so the trade-off between speed and noise and offset performances. It is important to highlight that t_{pre} and A_{pre} also depend on C_L ; however our analysis takes C_b as the main design parameter for simplicity, the designer has typically less control over the comparator load. Moreover, it is reasonable to assume C_L to be given as a specification.

Pseudo-differential pre-amplifier As described in [83], it is possible to transform a dynamic biasing pre amplifier into a pseudo-differential structure to achieve threshold configurability. The authors of [83] propose to split the source nodes of the input devices to a pair of charge redistribution arrays similar to the CDACs used in SAR ADCs. The arrays create a differential voltage at the sources of the input pair before the start of the evaluation phase. In this way, the threshold can be configured and controlled by the codes that are applied to the array. However, the topology in question requires a 3-phase clock and the capacitive arrays must be given enough time to settle before the evaluation phase can start.

In this analysis a simpler alternative is proposed, that consist in tuning the value of the two tail capacitors (implemented as digitally programmable capacitors) to allow automatic offset calibration differently from [83] where the capacitive degeneration applied to the two sides of the circuit is identical. With this approach, no additional clock phases are needed but it is possible to control the comparator threshold properly but, in this case, the control cannot be linear. Despite this, it is possible to null the offset of the comparator anyway: driving the calibration inputs with a successive approximation loop it is also possible to approach a zero-offset condition.

The equivalent circuit of the pseudo-differential charge-pump dynamic biasing pre-amplifier is reported in figure 4.21. Similarly to the single-tail case, the R_s is the equivalent series resistance of the switches that disconnect C_{bp} and C_{bm} from the input pair during reset. This analysis relies on the same hypothesis adopted in the previous subsection: the input pair is approximated as linear, and the charge pump is modeled as an initial condition $V_{b_0} = -\alpha V_{DD}$ on both capacitors. Moreover, the output resistance of M_1 - M_2 is neglected.

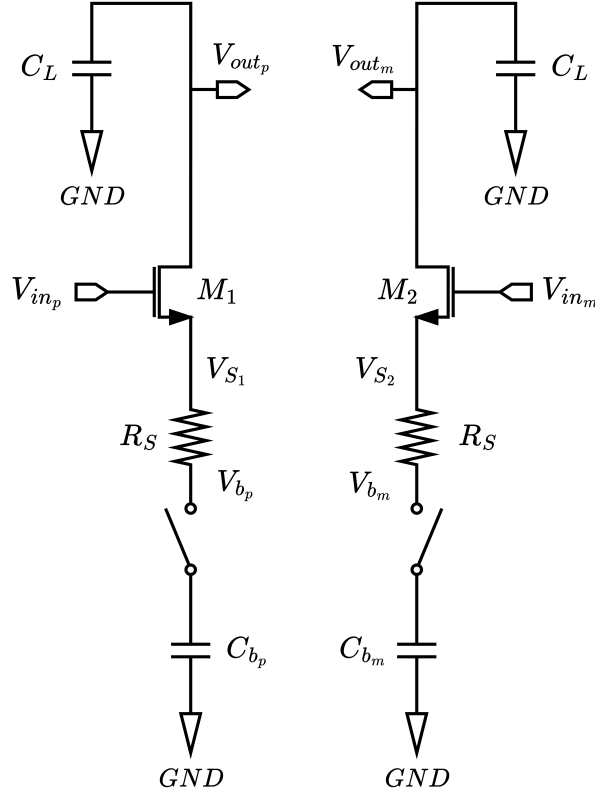


Figure 4.21. Model of the pseudo-differential CPB pre-amplifier.

The circuit is pseudo-differential and so it is possible to address the analysis of the two sides independently. We therefore focus on the left side, whose operation is described by the following equations:

$$\begin{cases} g_m (V_{ip} - V_{s1}(t) - V_{th}) = G_s (V_{s1}(t) - V_{bp}(t)) & (a) \\ G_s (V_{s1}(t) - V_{bp}(t)) = C_{bp} \frac{dV_{bp}(t)}{dt} & (b) \\ g_m (V_{ip} - V_{s1}(t) - V_{th}) = -C_L \frac{dV_{op}(t)}{dt} & (c) \end{cases} \quad (4.40)$$

As in the previous subsection, the overdrive voltage can be obtained by solving the first two equations:

$$V_{ov1} = \frac{G_s}{G_s + g_m} \tilde{V}_p e^{-t/\tau_p} \quad (4.41)$$

where the time constant τ_p represents the pre-amplification time constant for the left side and is given by $\tau_p \equiv \frac{C_{bp} g_m + G_s}{g_m G_s}$. $\tilde{V}_p$ is defined as $V_{ip} - V_{th} - V_{b_0}$. The expression

of the output voltage is obtained by integrating both sides of equation (4.40c):

$$V_{op}(t) = V_{DD} - \frac{C_{bp}}{C_L} \left(1 - e^{-t/\tau_p}\right) \tilde{V}_p \quad (4.42)$$

The output voltage of the right side of the circuit is equivalent to (4.42):

$$V_{om}(t) = V_{DD} - \frac{C_{bm}}{C_L} \left(1 - e^{-t/\tau_m}\right) \tilde{V}_m \quad (4.43)$$

where $\tau_m \equiv C_{bm}(g_m + G_s)/(g_m G_s)$ and $\tilde{V}_m \equiv V_{im} - V_{th} - V_{b0}$. Now two quantities are defined: $C_b \equiv (C_{bp} + C_{bm})/2$ and $\tilde{V} \equiv V_{ic} - V_{th} - V_{b0}$. Moreover:

$$\tau \equiv \frac{C_b}{g_m} \frac{g_m + G_s}{G_s} \quad (4.44)$$

In order to derive an expression for the pre-amplification time t_{pre} . Under these hypotheses that $\Delta C = 0$ and $V_{id} \neq 0$, one has $C_{bp} = C_{bm} = C_b$ and $\tau_p = \tau_m = \tau$ and so:

$$V_{od}(t) = -\frac{C_b}{C_L} \left(1 - e^{-t/\tau}\right) V_{id} \quad (4.45)$$

for the output differential-mode voltage and

$$V_{oc}(t) = V_{DD} - \frac{C_b}{C_L} \left(1 - e^{-t/\tau}\right) \tilde{V} \quad (4.46)$$

for the output common-mode voltage.

Since $V_{oc}(t)$ has the same expression of the single-tail case, the pre-amplification time equation is evaluated starting from (4.33). By substituting the expression of t_{pre} into equation (4.45) and dividing by V_{id} it is possible to obtain the expression of the pre-amplification gain of the pseudo-differential pre-amplifier:

$$A_{pre} = \frac{V_{od}^{pre}}{V_{id}} = -\frac{V_t}{\tilde{V}} \quad (4.47)$$

The only dependence of the pre-amplification gain to C_b is through α , by the definition of $\tilde{V}$. This implies the relation to the capacitive divider between C_b and the parasitic capacitances towards ground. Moreover, this expression is equivalent to the pre-amplification gain of a conventional Strongarm comparator assuming that $\tilde{V} = V_{ic} + \alpha V_{DD} - V_{th}$ is the effective overdrive voltage evaluated at $t = 0$. Note that the actual value of the overdrive voltage at $t = 0$ is $G_s/(G_s + g_m)\tilde{V}$.

Also in this analysis, the evaluation of the expression of A_{pre} is the key aspect of the analysis. By comparing this expression with the one of single-tail pre-amplifier (4.34) it result that the pre-amplification gain of a pseudo-differential configuration has fewer degrees of freedom. In fact A_{pre} of the pseudo-differential configuration is independent of the g_m/G_s ratio and does not exhibit a vertical asymptote as a function of C_b . Thus, the noise performance of this topology can be expected to be worse compared to the single-tail variant. The simulations presented in subsection 4.5.3 confirm this prediction.

Calibration In this paragraph a theoretical analysis of the proposed calibration technique is provided. Assume that there is mismatch in the comparator transistors which results in a input-referred offset V_{offset} . The aim of this analysis is showing that V_{offset} can be compensated by an appropriate choice of ΔC . In order to do this, it is assumed that the mismatch can be modeled with an equivalent voltage generator $-V_{offset}$ in series to the input. Moreover, the capacitance difference between the two capacitors is assumed to be $\Delta C \neq 0$. The starting point of the analysis is applying superposition to compute the ΔC that nulls the offset.

The first assumption is that $\tilde{V}_p = \tilde{V}_m = \tilde{V}$, which implies

$$V_{od}(t) = \frac{\tilde{V}}{C_L} \left(C_{bm} \left(1 - e^{-\frac{t}{\tau_m}} \right) - C_{bp} \left(1 - e^{-\frac{t}{\tau_p}} \right) \right) \quad (4.48)$$

The output differential voltage at the end of pre-amplification can be obtained by substituting t_{pre} into equation (4.48). Since the circuit is not symmetrical in this case, the expression that has been derived in 4.5.1 is not valid. Despite this, equation (4.33) represents an acceptable approximation of t_{pre} under the hypothesis that $\Delta C/(2C_b) \ll 1$. By substituting equation (4.33) into equation (4.48) the result is:

$$V_{od}^{pre} = \frac{\tilde{V}}{C_L} \left(C_{bp}(1 - \gamma)^{\frac{\tau}{\tau_p}} - C_{bm}(1 - \gamma)^{\frac{\tau}{\tau_m}} - \Delta C \right) \quad (4.49)$$

where

$$\gamma \equiv \frac{C_L V_t}{C_b \tilde{V}} \quad (4.50)$$

Now the goal is to calculate the value of ΔC that is needed to obtain an equivalent input-referred offset equal to V_{offset} , so as to compensate the offset caused by mismatch. Finding a solution of the equation $V_{offset} = V_{od}^{pre}/A_{pre}$ for the unknown ΔC aims to this goal. However, there is no analytical solution to this equation because V_{od}^{pre} is a transcendent function of ΔC since ΔC appears in the expressions of τ_p and τ_m . Despite this, assuming $\Delta C \ll 2C_b$ as hypothesis it is possible to derive an approximated closed-form solution. In this case, it can be shown that

$$V_{od}(t) \approx -\frac{\Delta C}{C_L} \left(1 - e^{-t/\tau} \left(1 + \frac{t}{\tau} \right) \right) \tilde{V} \quad (4.51)$$

The above expression is a linear function of ΔC . It is possible to evaluate the output differential voltage expression at the end of pre-amplification easily:

$$V_{od}^{pre} = -\frac{\Delta C}{C_L} ((1 - \gamma) \cdot \ln(1 - \gamma) + \gamma) \tilde{V} \quad (4.52)$$

Dividing V_{od}^{pre} by the pre-amplification gain it is possible to evaluate the value of the input-referred offset. Again, assuming $\Delta C \ll 2C_b$, A_{pre} can be approximated by equation (4.47). So the final expression for V_{offset} is:

$$V_{offset} = \frac{\Delta C}{C_b} \frac{(1 - \gamma) \cdot \ln(1 - \gamma) + \gamma}{\gamma} \tilde{V} \quad (4.53)$$

The ΔC that is needed to compensate the input-referred offset of the comparator can be therefore calculated in this way:

$$\Delta C(V_{offset}) = \frac{V_{offset}}{\tilde{V}} \frac{\gamma}{\ln[(1 - \gamma)^{1-\gamma}] + \gamma} C_b \quad (4.54)$$

Analyzing the above equations the conclusion is that there is a trade-off between resolution and range, which can be managed by adjusting C_b . Indeed, for a fixed ΔC , V_{offset} is a monotonic decreasing function of C_b in the interval $[C_b^{min}, \infty)$. This means that increasing the common-mode capacitance implies a better resolution at the cost of calibration range, and vice-versa.

4.5.2 Proposed topologies

Single-tail, single-stage comparator In this section the two novel single-stage regenerative comparators that exploit the charge pump dynamic biasing pre-amplifiers analyzed in section 4.5.1 are presented. The schematic of the first one, which will be referred to as the single-stage charge pump-based (STCP) latch, is reported in figure 4.22. The circuit is a modified version of the Strongarm comparator adapted to work at high-frequency and low supply voltage. The proposed proposed has several innovative features with respect to [63] in which the idea of applying dynamic biasing to single-stage comparators has been already presented :

- The NMOS latch devices have been eliminated. In the conventional Strongarm comparator, these devices avoids static consumption due to short-circuit between V_{DD} and ground during evaluation. In the proposed topology, however, static current consumption cannot occur because the lower supply bar is replaced by a capacitor. The removal of M_3 - M_4 decreases the number of stacked devices, allowing a reduction on the minimum theoretical supply V_{DD}^{min} from $2(V_{ov} + V_{gs})$ (in the Strongarm) to only $2V_{ov} + V_{gs}$. This is a considerable improvement even with respect to the Elzakker and the double-tail comparators, for which $V_{DD}^{min} = V_{ov} + 2V_{gs}$. A demonstration of the improvements in terms of speed thanks to the reduction of stacked devices is also showed in [34, 109].
- CPB dynamic biasing introduces further improvement in delay [11]. In fact, thanks to the coupling of the clock edges it is possible to boost the effective voltage headroom of the circuit, it permits to operate at frequencies that would otherwise be difficult to attain, providing an advantage that grows larger as V_{DD} decreases. It is legitimate to assert that, in a single-stage topology and at low V_{DD} , charge-pump dynamic biasing is particularly effective as it increases the V_{gs} of the latch devices, thus reducing the regeneration time constant. This is a key aspect of the proposed topology.

Transistors M_5 through M_8 play a crucial role in ensuring that, at the conclusion of regeneration, the “low” output is pulled to ground. This is achieved through the cross-coupled NMOS configuration formed by M_5 and M_6 . To comprehend the significance of these transistors, consider their absence and assume the polarity of V_{id} causes V_{op} to be driven towards V_{DD} during regeneration. In this case, M_3 injects current into the left output, while M_2 quickly shuts off, keeping V_{om} near ground. Consequently, a portion of the current from M_3 flows through M_1 , charging the source node of the input pair. Over time, the source voltage exceeds V_{om} , causing M_2 to reverse its drain and source roles, and it begins injecting current into its drain node.

The inclusion of a cross-coupled NMOS pair might seem to contradict the earlier statement about the proposed comparator having only one stacked V_{gs} . However,

these NMOS transistors only come into play after the PMOS transistors M_3 - M_4 have nearly completed the regeneration process. They are deliberately sized with small aspect ratios to avoid affecting the pre-amplification stage and to reduce the load on the outputs. As a result, the comparator operates as though these NMOS devices are not present, except for the final stage of regeneration when the outputs saturate.

The STCP comparator functions as follows:

- *Pre-charge Phase* ($CK = 0$ V): The transistors M_5 , M_7 , and M_8 are turned off. The top plate of the tail capacitor C_b is discharged to ground, while the outputs are pre-charged to V_{DD} and equalized via transistors M_{11} , M_{12} , and M_{13} .
- *Evaluation Phase* ($CK = V_{DD}$): Transistors M_{11} , M_{12} , and M_{13} are turned off, and the falling edge of $\overline{CK}$ is coupled to the source of the input pair through the tail capacitor. At this point, the input pair amplifies the signal by discharging the outputs. When V_{oc} drops below $V_{DD} - V_{thp}$, the cross-coupled transistors M_3 - M_4 activate and regenerate the signal based on the pre-amplified condition.

To reset the output nodes, an equalizing switch (M_{13}) is used in conjunction with pull-up devices. This configuration eases the trade-off between pre-charge time and the parasitics introduced by the pre-charge transistors [?].

Pseudo-differential, Single-stage Comparator The second proposed design is shown in Figure 4.23, referred to as the pseudo-differential charge pump-based (PDCP) latch. The programmable capacitive arrays C_{bp} and C_{bm} are shown in Figure 4.24. The source nodes of transistors M_1 and M_2 are separated, allowing for automatic offset correction.

The operation of the pseudo-differential comparator resembles that of the single-tail configuration, with the key difference being that the two tail capacitors can be independently adjusted to fine-tune the comparator's threshold. Another distinction is that the PDCP latch requires additional transistors (M_{12} to M_{15}) to equalize the internal nodes and tail capacitors during the reset phase. Notably, the cross-coupled NMOS pair is unnecessary because the source nodes remain independent.

The primary benefit of the proposed calibration method is that it leverages existing circuit components. Using digitally controlled capacitors connected to the drain nodes of the input pair, as discussed in [102, 144], would introduce significant overhead in terms of delay and power consumption. In contrast, the proposed approach is similar to foreground calibration using switched current sources [53], which avoids negatively impacting the energy-delay product (EDP) of the comparator.

It is important to note that the proposed method tends to shift the speed-power trade-off towards reducing delay, as higher calibration accuracy can be achieved by increasing the total capacitance of the arrays. Specifically, as discussed in subsection 4.5.1, the input-referred offset introduced by a given ΔC is inversely proportional to C_b . Thus, the resolution improves as C_b increases, provided that the minimum achievable ΔC remains constant.

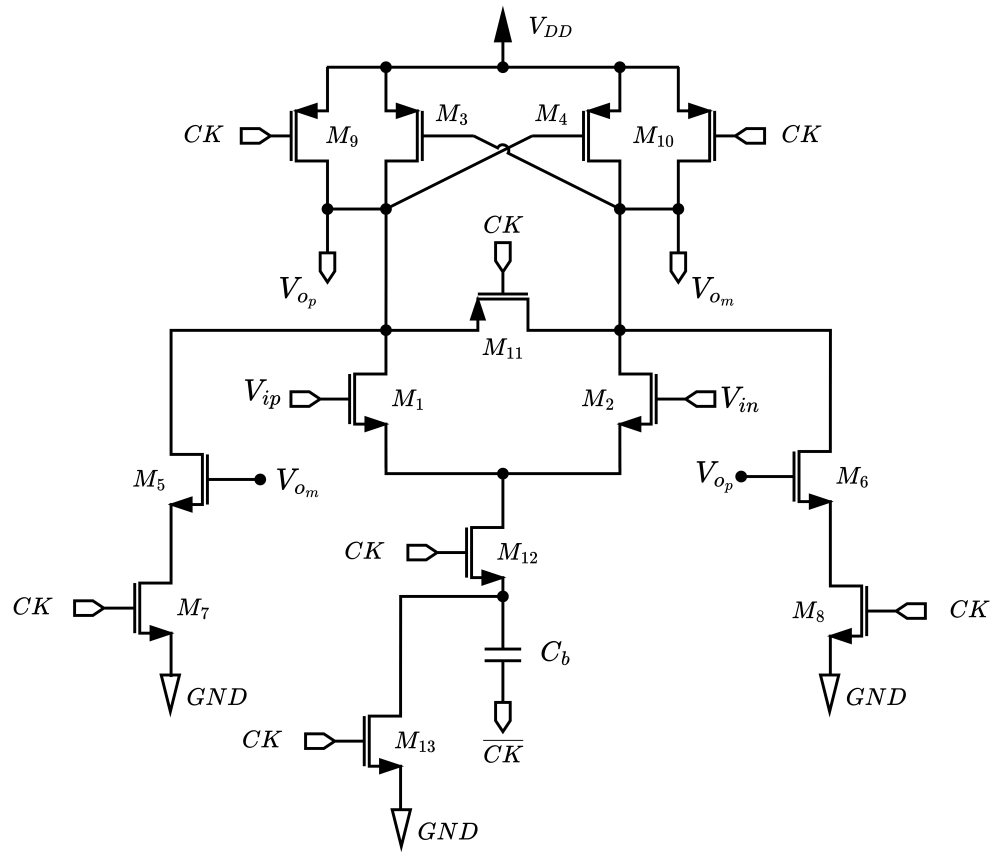


Figure 4.22. Schematic of the proposed STCP latch.

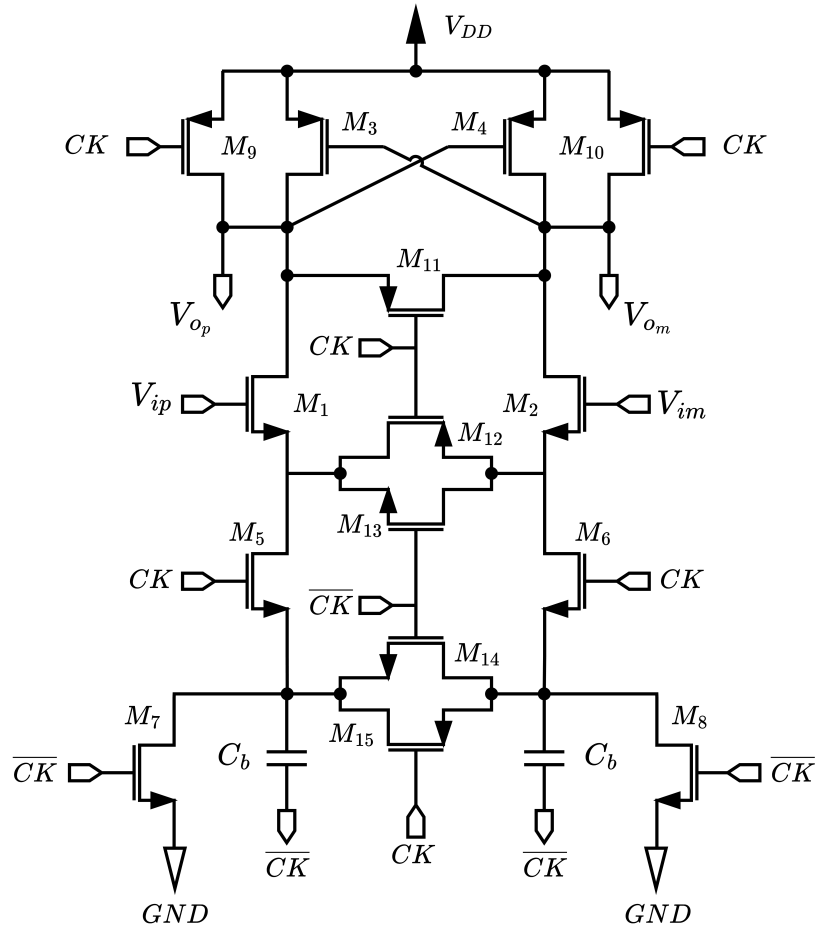


Figure 4.23. Schematic of the proposed PDCP latch.

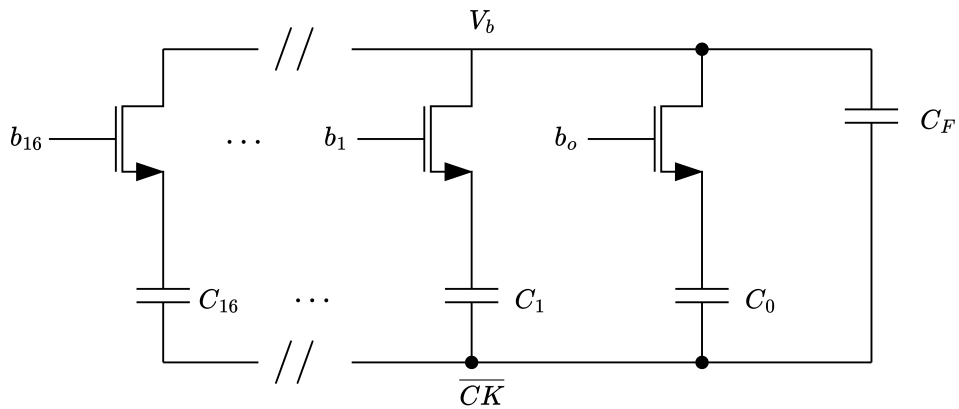


Figure 4.24. Implementation of the programmable capacitive array.

4.5.3 Sizing and layout

Sizing of the STCP and PDCP latches To evaluate the effectiveness of the proposed method, both the STCP and PDCP comparators were implemented using a 28 nm fully depleted silicon-on-insulator (FDSOI) technology provided by ST Microelectronics. The designs were configured for a supply voltage of 0.6 V without any forward body biasing. Post-layout simulations for both topologies were carried out using Cadence Virtuoso to verify their functionality.

Table 4.13 details the transistor sizing of the comparator cores. Both the STCP and PDCP were optimized to achieve a similar energy-delay product (EDP).

The sizing of each circuit was adjusted based on the theoretical insights from section 4.5.1. As a result, key differences arise between the two designs. For the PDCP latch, the design prioritizes speed by increasing the total capacitance of the programmable array, thus enhancing calibration accuracy (see paragraph 4.5.1). In contrast, the aspect ratio of transistors M_1 - M_2 in the STCP latch is significantly larger. This is because the gain of the pseudo-differential pre-amplifier is independent of g_m , as shown by equation (4.47). Increasing the W/L ratio in the input pair of the PDCP latch would only increase the load capacitance, thereby introducing greater delays. On the other hand, for the single-tail pre-amplifier, the gain A_{pre} can be improved by increasing the g_m/G_s ratio, making a larger g_m beneficial for suppressing noise.

Both designs feature an inverter that generates $\overline{CK}$, which has been modified by adding a PMOS device to enhance the pull-up network's fan-out. This modification steepens the rising edge of $\overline{CK}$, reducing the reset time and allowing the comparator to operate at higher clock frequencies. The PMOS in the STCP has been sized at $W = 4 \mu\text{m}$, while in the PDCP, it is set to $W = 3 \mu\text{m}$ (both using the minimum channel length). It is also noteworthy that while the inverted clock signal could be generated by two independent inverters, in this design, a single modified inverter was used for both the reset devices and charge pump clock to reduce circuit complexity. The sizing of the added PMOS transistor ensures an acceptable trade-off between speed, noise, and reset time.

Table 4.13. Transistor sizing of the proposed single-stage comparator topologies.

Device	W/L (STCP) [μm]	W/L (PDCP) [μm]
$M_1 - M_2$	4.00/0.03	0.70/0.03
$M_3 - M_4$	2.00/0.03	1.60/0.03
$M_5 - M_6$	0.10/0.03	0.90/0.03
$M_7 - M_8$	0.30/0.03	1.00/0.03
$M_9 - M_{10}$	0.40/0.03	0.40/0.03
M_{11}	0.80/0.03	0.80/0.03
M_{12}	1.00/0.03	0.33/0.03
M_{13}	1.00/0.03	0.40/0.03
M_{14}	-	0.40/0.03
M_{15}	-	0.50/0.03

Capacitor Array Sizing In the STCP topology, the tail capacitor C_b is implemented as a parallel configuration of four smaller capacitors to simplify layout. Each sub-capacitor is realized as a transistor with a width of 10 μm and a length of 50 nm. The top plate of the custom capacitor is formed by the gate terminal, while the bottom plate is the shorted drain, source, and substrate terminals.

Table 4.14 shows the sizing of the capacitors C_{bp} and C_{bm} used in the PDCP latch. The largest capacitors are realized using library MOS capacitors, while smaller ones are implemented as transistors with shorted source, drain, and body terminals.

To ensure accurate and reliable calibration, the capacitive array incorporates redundancy. The capacitors are sized such that $C_{i-1}/C_i < 2$ for $i = 1, 2, \dots, n$, enabling redundancy to correct potential calibration errors (such as mismatches between capacitors) [104]. The variable-radix redundancy scheme, which was optimized manually through simulations, also helps improve robustness against noise during calibration by averaging the effects of noise over multiple decisions.

Table 4.14. Sizing of the capacitor arrays for the PDCP latch.

Capacitors implemented as library MOS capacitors [fF]	
C_f	9.49
Capacitors implemented as MOS transistors (W/L) [μm]	
$C_0 - C_1$	0.50/0.03
$C_2 - C_3$	0.70/0.03
$C_4 - C_5$	1.20/0.03
$C_6 - C_7$	1.80/0.03
$C_8 - C_9$	3.00/0.03
$C_{10} - C_{11}$	5.00/0.03
$C_{12} - C_{13}$	7.00/0.03
$C_{14} - C_{15}$	11.0/0.03
MOS transistor switches (W/L) [μm]	
$M_{S_2} - M_{S_{15}}$	0.40/0.03
$M_{S_1} - M_{S_0}$	0.10/0.03

Layout Considerations For both technologies, special attention was paid to the layout to maximize symmetry and minimize systematic offset. Additionally, significant effort was made to reduce capacitive coupling between interconnects.

The layout of both comparator topologies is shown in Figure 4.25. The area footprint, including the capacitive arrays, is 79.6 μm^2 for the STCP latch and 341.0 μm^2 for the PDCP latch.

4.5.4 Simulations

Delay, Power Consumption, and Noise The performance of the proposed topologies was evaluated at a supply voltage of $V_{DD} = 0.6$ V, using a differential input voltage V_{id} such that $|V_{id}| = 5$ mV. Simulations were carried out at near-maximum clock frequencies, specifically 2.5 GHz for the STCP latch and 3 GHz for

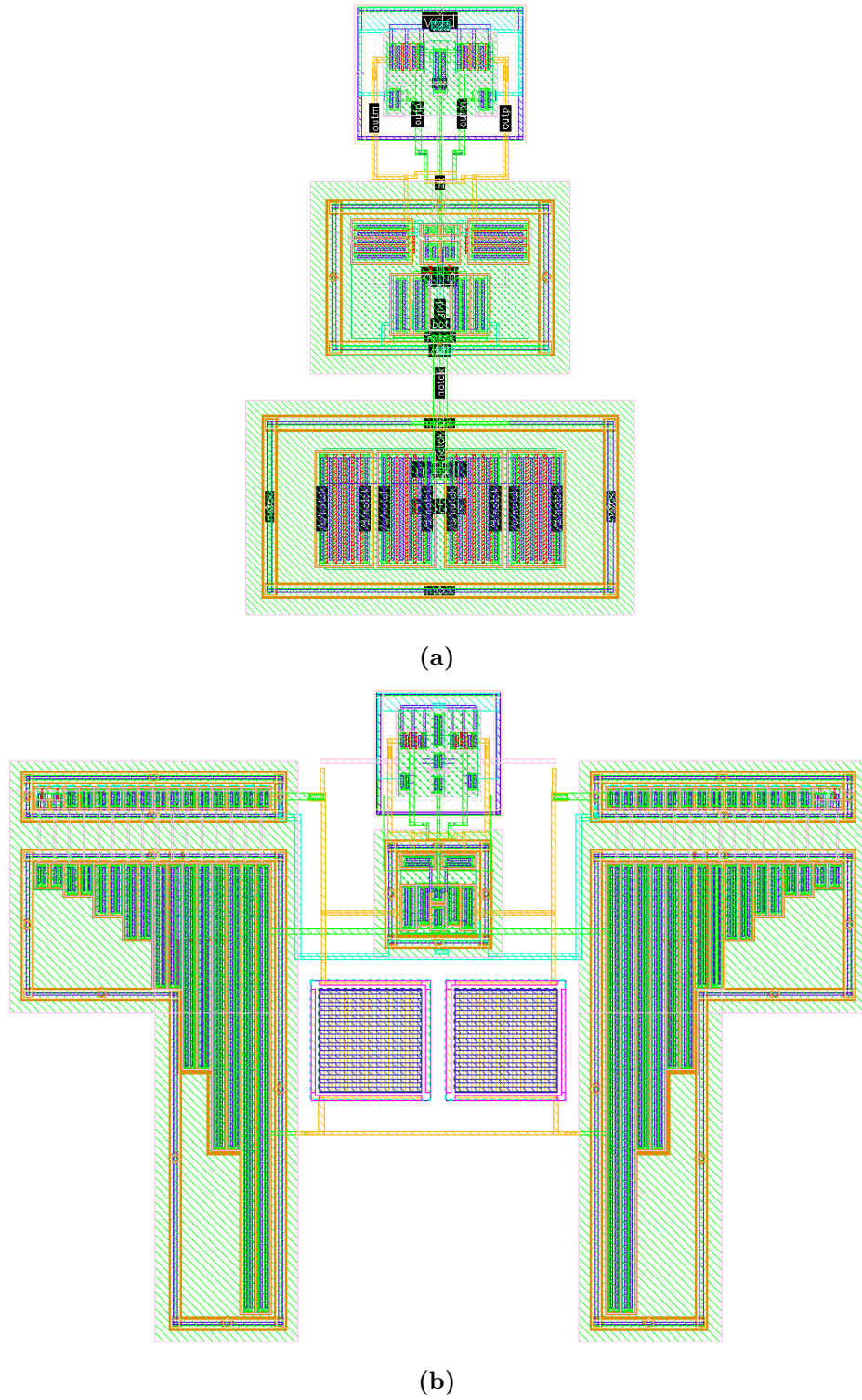


Figure 4.25. Layout of the proposed topologies: STCP a) ($11.19 \mu\text{m} \times 7.114 \mu\text{m}$) and PDCP b) ($21.18 \mu\text{m} \times 16.10 \mu\text{m}$).

Table 4.15. Performance comparison between the STCP and PDCP latches. Delay and power consumption measurements were taken with $|V_{id}| = 5$ mV.

	STCP	PDCP
f_{ck} [GHz]	2.5	3
t_d [ps]	95.1	78.5
P_{avg} [μ W]	49.8	65.2
Energy/comp. [fJ]	17.7	21.7
EDP [fJ/GHz]	1.69	1.71
σ_{IRN} [mV]	0.748	1.53

the PDCP latch. In the testbench, the sign of V_{id} alternates every 2 cycles during the core of the reset/pre-amplification phase, with a common-mode input voltage $V_{ic} = V_{DD}/2 = 0.3$ V applied across all simulations. Both topologies were connected to a minimum-area standard-cell inverter at the output. The PDCP topology was first calibrated in the foreground prior to estimating its delay, power consumption, and noise, ensuring reliable performance characterization.

Figures 4.26a and 4.26b illustrate the transient output behavior of the STCP and PDCP latches, respectively. The delay, defined as the time between the 50% clock transition and the 50% output differential voltage transition, was measured at 95 ps for the STCP and 78.5 ps for the PDCP.

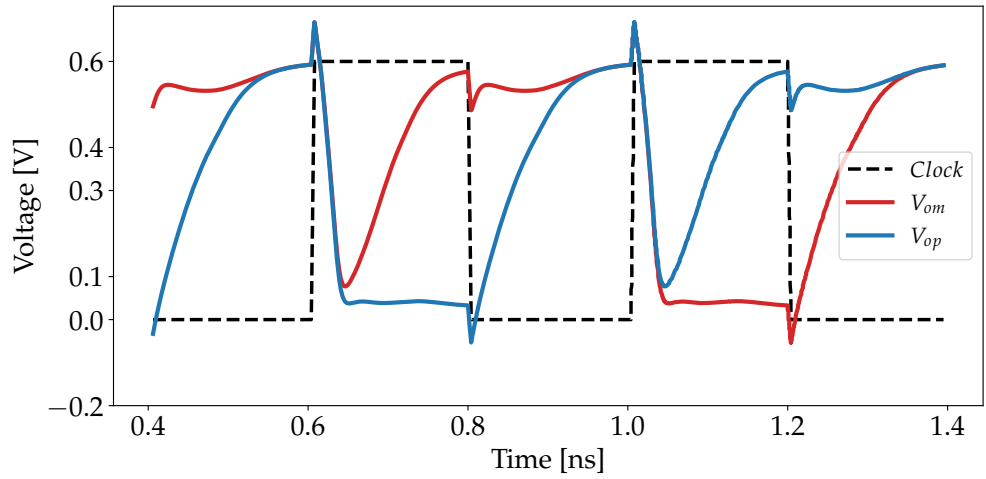
In the PDCP latch, the influence of the CPB dynamic biasing is evident from the fact that the lower output voltage settles below 0 V. This phenomenon does not occur in the STCP comparator, where the source node of the input transistors is shared, thereby limiting the V_{gs} of both M_1 and M_2 , and preventing the "low" output from fully discharging. As detailed in Section 4.5.2, transistors M_5 through M_8 ensure that the low output voltage remains near ground after the regeneration phase is complete.

Table 4.15 presents a performance summary of both topologies under typical corner conditions at 27°C. Power consumption is calculated as the average power over 10 clock cycles of operation. As expected from theoretical analysis, the input-referred noise of the STCP is substantially lower than that of the PDCP topology.

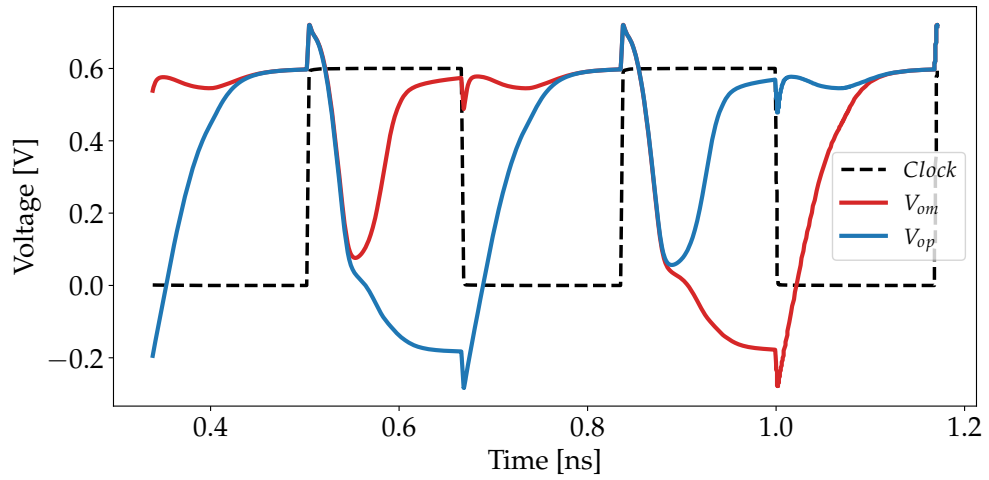
The comparison of these two circuits confirms the observations from Section 4.5.2. When a high pre-amplification gain is required to reduce noise, the single-tail configuration (STCP) is clearly preferable. However, the pseudo-differential topology (PDCP), while more susceptible to noise, facilitates automatic offset calibration, making it more suitable for applications where noise is not the primary concern. For instance, in time-interleaved SAR converters, system linearity depends, among other factors, on the offset mismatch between different channels.

Table 4.16 outlines the performance of the two proposed comparators across variations in process, supply voltage, and temperature (PVT). Both topologies demonstrate robust performance across a wide range of conditions.

Offset and Calibration The proposed approach for foreground offset calibration was validated using a dedicated testbench, illustrated in Figure 4.27. The testbench



(a)



(b)

Figure 4.26. Transient output behavior of the proposed comparator in a) 55 nm technology and b) 28 nm technology.

Table 4.16. Performance summary of the proposed comparators under PVT variations. In this table, $V_{DD}^{max} = V_{DD} + 10\%V_{DD}$, $V_{DD}^{min} = V_{DD} - 10\%V_{DD}$, $T^{max} = 80\text{ }^{\circ}\text{C}$ and $T^{min} = 0\text{ }^{\circ}\text{C}$.

		V_{DD}^{max}	V_{DD}^{min}	T^{max}	T^{min}	FF	FS	SF	SS
PDCP STCP	t_d [ps]	85.6	108	102	93.8	93.8	129	91.7	103
	P_{avg} [μW]	49.8	39.0	46.7	43.1	46.2	45.1	43.2	42.1
	EDP [fJ/GHz]	1.71	1.69	1.90	1.62	1.74	2.33	1.59	1.73
	t_d [ps]	72.7	88.4	80.6	77.7	73.5	76.4	422	86.2
	P_{avg} [μW]	78.6	51.5	70.6	61.4	72.0	61.8	65.0	58.2
	EDP [fJ/GHz]	1.90	1.52	1.89	1.59	1.76	1.57	9.13	1.67

operates as follows: in the first phase, the inputs of the PDCP latch are connected to the nominal input common-mode voltage, and the offset is calibrated automatically through a successive approximation loop. Afterward, the input differential voltage of the comparator is swept to estimate the post-calibration input-referred offset by performing a linear search.

To assess the performance of the calibration technique, a process + mismatch Monte Carlo simulation was conducted using the testbench. For comparison, the same simulation was repeated after disconnecting the comparator from the calibration circuit to observe the effect of the calibration.

Calibration was performed at a frequency of 1 GHz, which is lower than the nominal clock rate of both latch versions. This choice allows maximizing resolution, as the comparator requires a broader time margin to accurately resolve the least significant bits of the error code. The need to lower f_{ck} during calibration does not pose a significant limitation, as the comparator's clock can be easily scaled during calibration.

Figure 4.28 shows the comparison between the distribution of the calibrated and uncalibrated input-referred offset of the PDCP latch, evaluated over 500 Monte Carlo iterations. The standard deviation of the calibrated offset, σ_{offset} , is reduced to 0.35 mV, which represents a 30-fold improvement over the uncalibrated distribution.

It is worth mentioning that in practical applications, the calibration accuracy is also influenced by noise since the offset is estimated based on the comparator's decision. This limitation is typical of any automated offset cancellation technique applied to a fully dynamic comparator, as noise affects the precision of the calibration. However, two important points mitigate this issue:

- As previously noted, redundancy increases robustness against noise, effectively providing a form of averaging. The proposed calibration technique is particularly well-suited for implementing redundancy, as the number of array elements can be increased without negatively affecting the energy-delay product (EDP).
- Since this calibration scheme operates in the foreground, the impact of noise on calibration can be minimized by averaging during the calibration phase. Averaging incurs no additional cost as it only occurs at startup, apart from a slight increase in the area due to the additional control logic.

The (uncalibrated) input-referred offset for the STCP topology was found to

be 4.4 mV. Similar to the PDCP latch, this value was derived from a 500-iteration post-layout Monte Carlo simulation. While foreground calibration using capacitive degeneration is unavailable for the single-tail variant, its offset can still be compensated with minimal overhead using offline calibration techniques, such as the one proposed in [108].

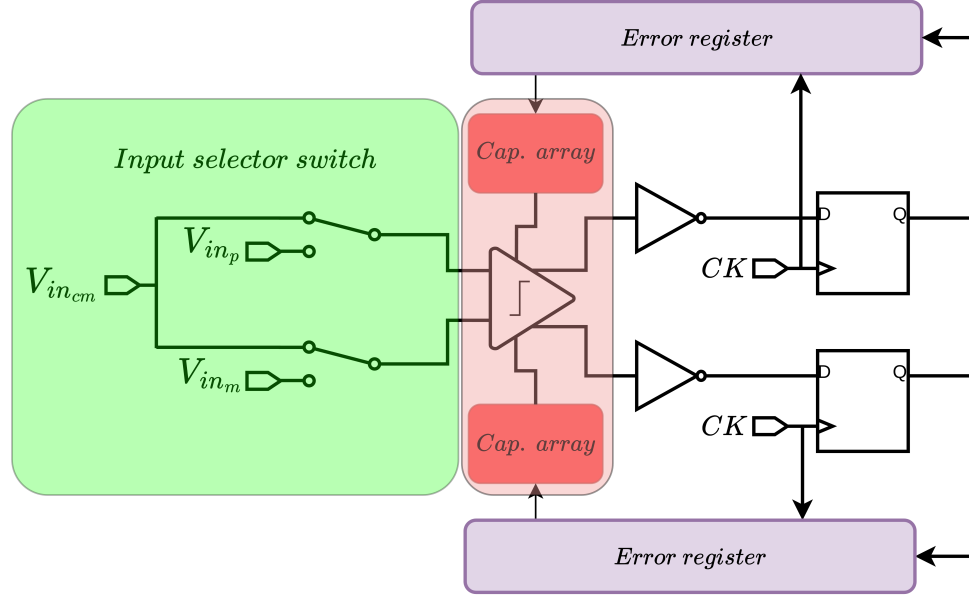


Figure 4.27. Schematic of the automated calibration testbench.

Validation of the Theoretical Analysis This subsection validates the analysis presented in section 4.5.1 for the single-tail and pseudo-differential pre-amplifiers through pre-layout simulations. A specialized setup was utilized, wherein both pre-amplifiers were tested with an ideal capacitive load of $C_L = 2$ fF. The impact of charge pump dynamic biasing was simulated by applying an initial condition of $V_{b_0} = -\alpha V_{DD}$ on the capacitors, with α set to $1/3$, resulting in $V_{b_0} = -200$ mV. This value closely approximates the minimum value of V_b observed during the evaluation phase in pre-layout simulations for both the STCP and PDCP latches.

The transconductance and threshold voltage that define the linearized transcharacteristic of the input devices were obtained from the simulator by executing a first-order Taylor series expansion of the transistors' I_D - V_{gs} curve at $V_{gs} = V_{gs}(t = 0)$ and $V_{ds} = V_{ds}(t = 0)$. The resistance R_s was estimated as the r_{ds} of the switch at $t = 0$. The common-mode voltage drop V_t , which signifies the end of pre-amplification, was selected as the threshold voltage of the PMOS devices in both the STCP and PDCP topologies. Additionally, the parasitic capacitive load C_{par} due to the input devices was estimated and included in the theoretical model alongside C_L . A summary of these parameters can be found in table 4.17.

Figure 4.29a presents a comparison between the theoretical and simulated pre-amplification times for both the single-tail and pseudo-differential topologies. There is a clear and excellent agreement between the simulated and theoretical results in both instances. As anticipated by the theory, t_{pre} adheres to a logarithmic

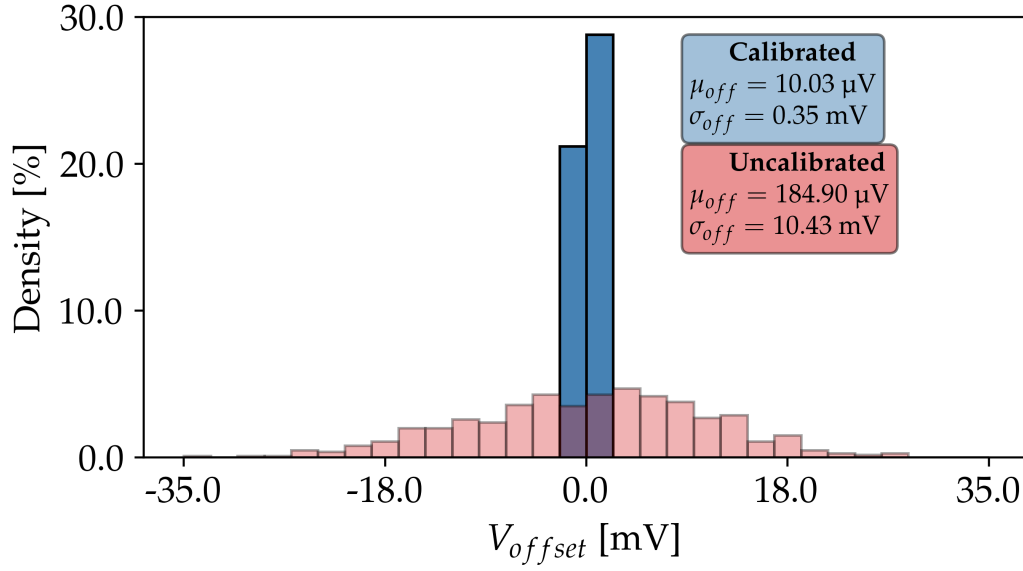


Figure 4.28. Offset distribution of the pseudo-differential comparator, with and without calibration.

Table 4.17. Circuit parameters extracted from the simulator for validating the analytical models of the single-tail (ST) and pseudo-differential (PD) CPB pre-amplifiers.

	g_m [mS]	V_{th} [mV]	R_s [Ω]	V_{thp} [mV]	C_{par} [fF]
ST	2.77	314	570	372	1.24
PD	0.739	353	480	374	0.240

relationship due to capacitive degeneration. The pre-amplification time of the single-tail circuit is shorter because its g_m is greater, resulting in a lower τ compared to that of the pseudo-differential version.

Figure 4.29b compares the theoretical and simulated gains of the two pre amplifiers. The theoretical prediction for the single-tail configuration shows a relative error of about 30% compared to the simulation for larger values of C_b . The model's accuracy can be improved by incorporating the output resistance of M_1 - M_2 , denoted as R_L . Consequently, the equivalent differential-mode circuit can be modeled as a current source $g_m V_{id}$ driving an RC load composed of the parallel combination of R_L and C_L . The output differential voltage of the pre-amplifier can then be expressed as:

$$V_{od}(t) = -g_m R_L \left(1 - e^{-t/\tau_L}\right) V_{id} \quad (4.55)$$

where $\tau_L \equiv R_L C_L$. For small t (i.e., $t \ll \tau_L$), the approximation $e^{-t/\tau_L} \approx 1 - t/\tau_L$ can be afforded, leading back to equation (4.32). By substituting $t = t_{pre}$ into equation (4.55) and dividing by V_{id} , the result is:

$$A_{pre} = -g_m R_L \left(1 - e^{-\tau/\tau_L} \left(1 - \frac{C_L V_t}{C_b \tilde{V}}\right)\right) \quad (4.56)$$

R_L , that is the output resistance, can be straightforwardly determined as a small-signal parameter. In the case of the single-tail pre-amplifier, this value is found to be $R_L = 5.3 \text{ k}\Omega$. As shown in figure 4.29b, when the single-tail pre-amplifier's gain is computed using equation (4.56), the relative error (in the asymptotic limit) reduces to around 20%.

While equation (4.56) may not provide significant design insight into the relationship between A_{pre} and the design parameters, equation (4.34) can serve as a valuable tool for designers seeking to derive qualitative guidelines for pre-amplifier sizing. Nevertheless, a more precise gain estimate can be achieved by factoring in the output resistance of the input pair, as outlined in equation (4.56).

The analysis of the output common-mode voltage does not take the influence of R_L into account, as including it would complicate the model without providing substantial benefits. The simplified model already demonstrates practical effectiveness, as evidenced in figure 4.29a. A qualitative understanding can be reached by using a perturbative approach: in the absence of R_L , the common-mode component of the voltage drop across R_L decays exponentially, with the same time constant that governs the decay of the drain current in the input pair. When R_L is introduced to the circuit, since g_m is generally much larger than $1/R_L$, the current through R_L is expected to produce only a small systematic error in the common-mode voltage. However, the differential-mode response is more significantly affected by R_L , as its presence causes V_{od} to follow a saturation-exponential pattern, as opposed to a purely linear trend.

For cases where $C_b \rightarrow 0$, a noticeable discrepancy arises between the theoretical predictions and simulated results for A_{pre} in the single-tail configuration. This can be attributed to the inherent non-linearity of transistors M_1 and M_2 : when C_b is very small, the input transistors rapidly enter the sub-threshold region, and their average transconductance quickly drops below the predicted value. In circuits

where $R_L \rightarrow \infty$, this effect would not limit gain to the same extent observed in our simulations. This is because, in dynamic pre-amplifiers, the gain depends on the g_m/I_d ratio (both in strong and weak inversion [10]), which tends to be higher when operating in weak inversion. However, according to equation (4.55), $V_{od}(t)$ cannot exceed $g_m R_L$ when R_L is finite.

Thus, if g_m decreases too much, the asymptotic value of $V_{od}(t)$ will also diminish, which in turn impacts the overall gain trajectory. This results in a reduction of the pre-amplification gain. Essentially, if g_m is too low, pre-amplification will be limited by the resistive shunt imposed by R_L . This limitation is important to consider, as it applies to any topology employing dynamic biasing: improving A_{pre} is constrained by the finite output resistance of the input transistors. Ultimately, pushing M_1 and M_2 too deeply into the sub-threshold region might even prove detrimental.

For the pseudo-differential topology, there is no straightforward correction to account for the finite output resistance R_L of transistors M_1 and M_2 . Fortunately, in this configuration, the value of R_L can be assumed to be significantly higher. Increasing the g_m/G_s ratio offers no substantial noise improvement and typically results in degraded speed (see section 4.5.3). According to the sizing outlined in section 4.5.3, the output resistance of the input pair is 63 k Ω . The agreement between theoretical models and simulations for both A_{pre} and t_{pre} indicates that R_L can be neglected: equation (4.47) predicts A_{pre} with an approximate relative error of 25%.

Theoretical predictions and simulations both indicate that the gain of the single-stage pre-amplifier (accounting for R_L) is roughly twice that of the pseudo-differential topology. Thus, the theoretical model also provides accurate insight into how the two topologies' gains compare.

Figure 4.30 shows the theoretical and simulated behavior of V_{od}^{pre} as a function of ΔC for the pseudo-differential pre-amplifier. The common-mode capacitance is set to 15 fF, and ΔC is varied within the range of $[-15 \text{ fF}, 15 \text{ fF}]$ with $V_{id} = 0$. The simulated behavior is compared to both the exact theoretical expression in equation (4.49) and the approximation given in equation (4.52). For small ΔC values, the approximated expression aligns well with the simulations, exhibiting a relative error of less than 10% when $|\Delta C| \leq 5 \text{ fF}$. For larger ΔC , the approximation diverges significantly from the simulations due to non-linearity. However, the exact theoretical expression remains accurate across the entire range, with an error below 10% even at $|\Delta C| = 15 \text{ fF}$.

Comparison In order to evaluate the performance of the proposed comparator circuits, several popular dynamic biasing-based comparator topologies were re-implemented using the 28 nm process technology. These designs were then benchmarked against the proposed circuits through pre-layout simulations. Specifically, the comparators used for comparison include the original dynamic biasing comparator from [10] and the CPB variant introduced in [11]. Additionally, the conventional Elzакker comparator [136] was simulated to serve as a reference for the dynamic biasing-based designs. The results of these comparisons are summarized in Table 4.18.

The four dynamic biasing comparators featuring a single-tail pre-amplifier were

Table 4.18. Pre-layout comparison between existing dynamic biasing-based topologies implemented in the technology at hand and the proposed comparators.

	STCP	PDCP	[136]	[10]	[11]
t_d [ps]	74.8	66.4	238	495	168
P_{avg} [μ W]	18.0	27.2	9.71	7.43	19.3
EDP [fJ/GHz]	1.35	1.8	2.32	3.68	3.26
σ_{IRN} [mV]	0.777	1.66	0.767	0.782	0.798
FOM [nJ $\cdot$ ns $\cdot\mu$ V ²]	0.815	4.96	1.46	2.25	2.08

sized to ensure equivalent input-referred noise levels. The input pair's aspect ratio was kept the same as that used in the STCP latch, while the second stage—when present—was optimized for speed by adjusting the W/L ratios to minimize delay. It should be noted that enlarging the aspect ratio of the latch transistors only improves performance up to a limit, after which the parasitic capacitances offset the benefits of higher g_m . The capacitive cancellation technique described in [11] was not applied to the two-stage CPB comparator because no significant advantage was observed in the target technology. It should also be highlighted that the PDCP comparator was not optimized for noise, as it is designed for applications where noise performance is less critical. Improving its noise performance would be challenging (since adjusting g_m would require increasing the load capacitance) and would negatively impact both speed and power efficiency.

Delay and power consumption estimations were carried out using $V_{DD} = 0.6$ V, $V_{icm} = V_{DD}/2$, $V_{id} = 5$ mV, and $f_{ck} = 1$ GHz. The clock frequency was reduced because many topologies from the literature are unable to operate at frequencies exceeding 1 GHz. To standardize the comparison, the figure of merit (FOM) from [11] was computed for each comparator. The FOM is defined as:

$$FOM \equiv \frac{t_d \cdot P_{avg} \cdot \sigma_{IRN}^2}{f_{ck}} = EDP \cdot \sigma_{IRN}^2 \quad (4.57)$$

As expected, traditional dynamic biasing techniques enhance input-referred noise performance at the cost of increased delay compared to the Elzakker baseline comparator. On the other hand, CPB dynamic biasing allows a trade-off between noise and delay, favoring faster response times. The dynamic biasing comparators from [10] and [11] have a less favorable FOM compared to the original Elzakker design, as they prioritize power reduction (in the case of conventional dynamic biasing) or delay improvement (in the case of CPB dynamic biasing), but do not significantly optimize for noise.

The proposed topologies achieve reduced delay times and competitive energy-delay product (EDP) metrics, mainly due to their single-stage architecture, which enhances V_{DD}^{min} and increases the overdrive voltage of the latch devices using CPB dynamic biasing. The STCP latch, in particular, demonstrates a notable FOM improvement of over 50% compared to the comparator from [11]. On the other hand, the PDCP latch is less power-efficient, and its FOM is limited by noise, primarily due to its pseudo-differential configuration. Despite this, the PDCP remains a viable option for applications where noise performance is a secondary concern, as it facilitates foreground calibration without sacrificing speed.

The ability to achieve higher clock frequencies provides an additional advantage, even if the PDCP and STCP latches are less power-efficient. Comparators such as those in [136], [10], and [11] are unable to reach the operating frequencies of the proposed designs, largely due to their higher V_{DD}^{min} requirements and the greater number of stacked V_{gs} . Our simulations indicate that the delays of these alternative topologies remain above 130 ps, even when tolerating higher input-referred noise.

Although Table 4.18 presents pre-layout performance metrics, it should be noted that the power efficiency of the proposed comparators is lower compared to the post-layout results shown in Table 4.15. This difference arises because the power efficiency of the STCP and PDCP latches tends to degrade as the clock frequency f_{ck} decreases. To understand this behavior, consider the STCP latch: once regeneration is complete and M_1 's drain reaches V_{DD} , the tail capacitor continues to charge slowly through the drain-source resistance of M_1 . This additional charge does not significantly affect the output voltage but does contribute to power dissipation. A similar phenomenon occurs in the PDCP topology. As f_{ck} decreases, the voltage swing across the tail capacitors increases, thereby reducing the efficiency of the circuit. However, this is a minor issue, as the proposed comparators were specifically designed for high-speed applications. Importantly, the proposed latches exhibit competitive performance in terms of EDP even at $f_{ck} = 1$ GHz, with the STCP latch achieving the best FOM by a substantial margin.

Post-layout results are not included for comparison, as the relative impact of post-layout parasitics is expected to be similar across all topologies under consideration (given the comparable transistor count). Excluding post-layout simulations reduces degrees of freedom and enhances the reliability of the comparison.

Table 4.19 provides a comparison of the post-layout performance of the proposed comparators with results from recent literature.

Table 4.19 compares the post-layout performance of the proposed comparators to the recent literature. The proposed comparator topologies offer strong performance in terms of both delay and power efficiency. Additionally, the STCP comparator demonstrates low input-referred noise, making it well-suited for applications requiring high speed and high accuracy.

In Table 4.19, the original CPB comparator from [11] exhibits a relatively high FOM, which can be attributed to it being tested at a V_{id} of only 300 μ V. To make the comparison more equitable, the STCP latch was simulated at $f_{ck} = 1$ GHz using the same input amplitude. Under these conditions, the STCP achieved a delay of 303 ps and a FOM of 3.44 nJ $\cdot$ ns $\cdot\mu$ V². Although this FOM is higher than that of the comparator in [11], it's important to note that the latter design suffers from greater delay and operates at a lower frequency (limited to 700 MHz) despite using a higher supply voltage and a more advanced process technology. Furthermore, as shown in Table 4.18, when both circuits are tested at the same supply voltage and process technology, the STCP latch outperforms the comparator from [11] in both FOM and delay.

The comparator presented in [83] also achieves a better FOM; however, it is implemented in 16 nm technology and only pre-layout results are provided in the paper. Similar to the PDCP latch, this design also exhibits significant input-referred noise due to its pseudo-differential architecture. This aligns with the analysis conducted in this study, reinforcing the idea that pseudo-differential pre-amplifiers

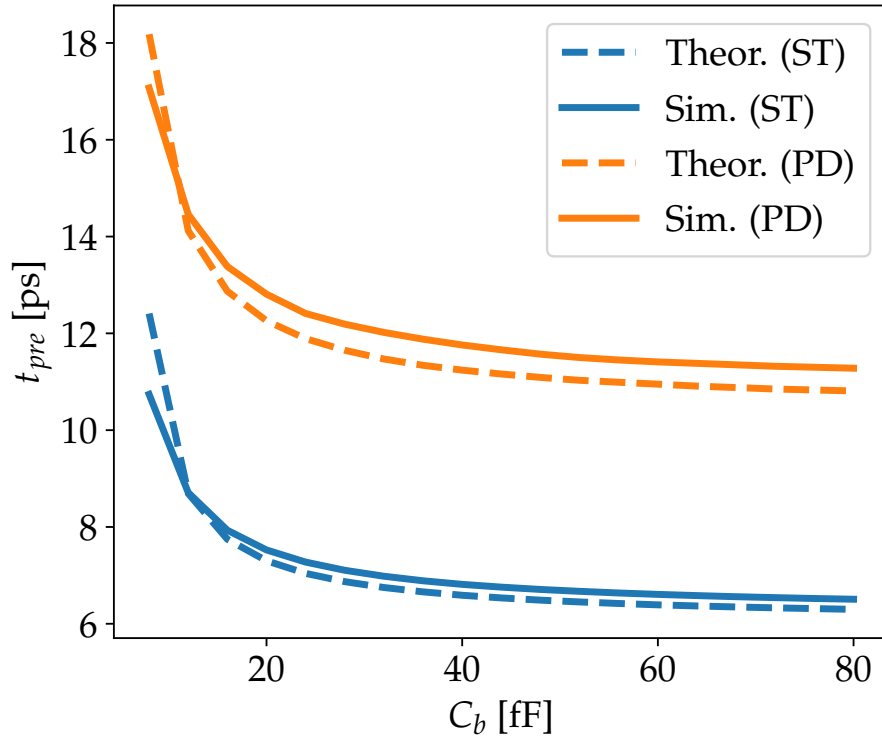
Table 4.19. Comparison between the state of the art and the proposed topologies.

	This work (STCP)	This work (PDCP)	[109]	[42]	[87]	[83]	[62]	[11]
Year	2024	2024	2022	2007	2013	2018	2015	2022
Tech. [nm]	28 FDSOI	28 FDSOI	28	120	180	16	65	22
V_{dd} [V]	0.6	0.6	0.6	0.5	0.5	0.8	0.6	0.7
V_{id} [mV]	5	5	5	-	1	1	4.2	0.30
t_d [ps]	95.1	78.5	70.0	-	1300	46	-	410
P_{avg} [μ W]	49.8	65.2	194	18	34	-	64	39.9
f_{CK} [GHz]	2.5	3	4	0.6	0.2	-	1.3	0.7
Energy/comp. [fJ]	17.7	21.7	48.5	30	170	12	49.2	57
EDP [fJ/(GHz)]	1.69	1.71	3.4	-	221	0.55	-	23.4
σ_{IRN} [mV]	0.745	1.53	0.89	-	-	1.5	0.5	0.30
σ_{offset} [mV]	4.4	0.35	-	57	0.288	-	7.5	-
FOM [nJ $\cdot$ ns $\cdot\mu$ V ²]	4.0	0.95	2.7	-	-	0.83	-	2.1
Area [μ m ²]	79.6	341	78	-	-	-	265	57
Offset calibration	yes	yes	no	no	yes	yes	no	no

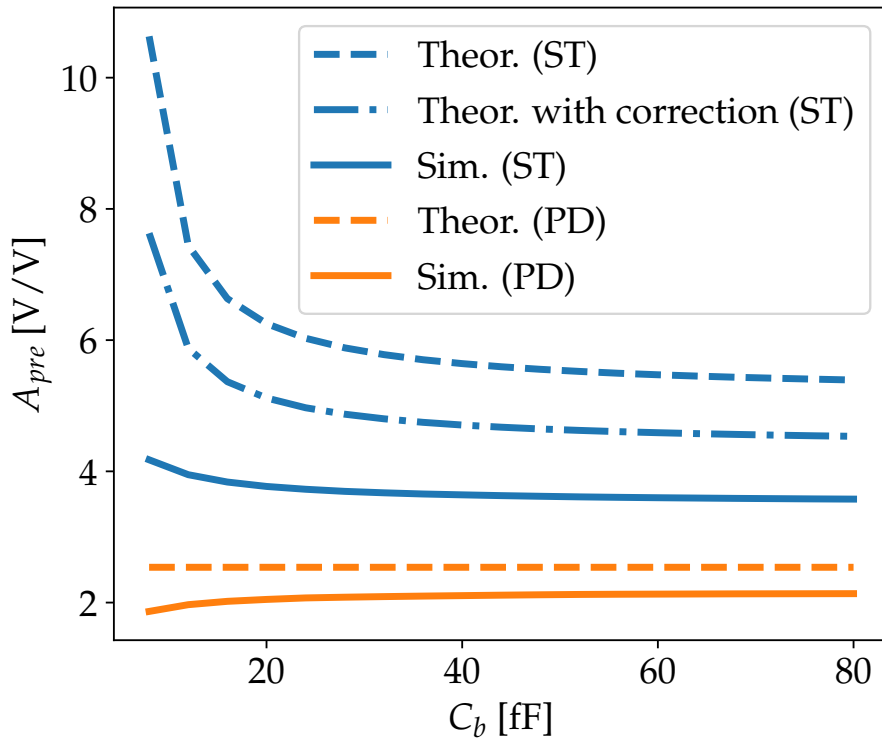
are less suitable for applications where low noise is critical.

4.5.5 Conclusion

Dynamic Biasing is a technique used in latch comparator to improve noise performance at the cost of speed. In this work the Charge Pump Based (CBP) dynamic bias has been used to improve noise-speed trade-off. An theoretical analysis on the CBP single-tail and pseudo-differential amplifier has been performed, demonstrating the improvements then the analysis has been validated applying the CBP to two novel 0.6 V 28-nm CMOS dynamic comparator topologies. The first one is a single-tail Strongarm based comparator while the second is the pseudo-differential version. In the pseudo-differential version a couple of digital-programmable capacitor array have been used in the charge pump allowing foreground offset calibration. The post layout simulation show that the two topologies are able to work at frequencies > 2 GHz despite the low voltage power supply demonstrating very competitive performances with respect to the literature.



(a)



(b)

Figure 4.29. Theoretical versus simulated behavior of pre-amplification time (a) and gain (b) as a function of C_b .

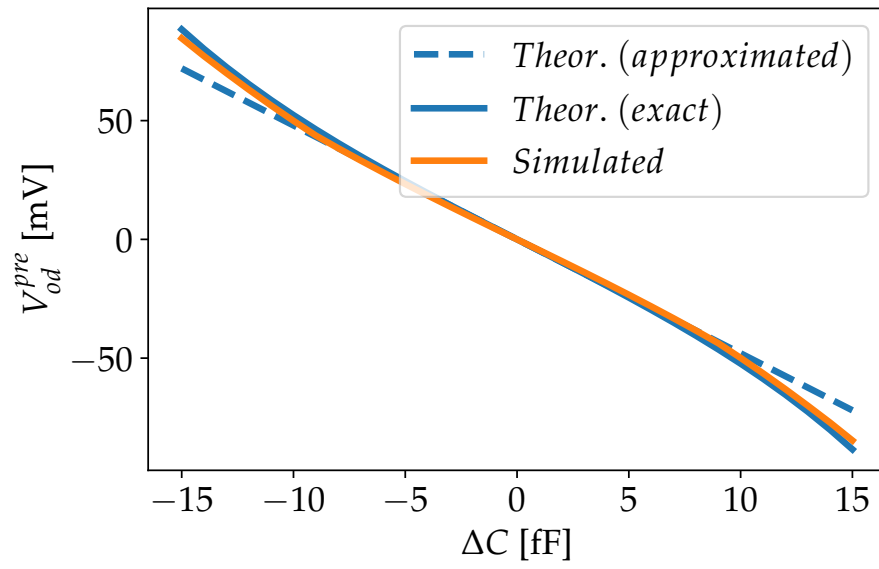


Figure 4.30. Theoretical versus simulated behavior of V_{od}^{pre} as a function of ΔC in the PDCP latch.

Chapter 5

An Ultra-Low Voltage 0.4V, 8-bit, 6.7 MS/s SAR ADC

In this chapter is described the design of an innovative ULV high speed ADC. The ADC is supplied with a V_{DD} of 0.4V and has a resolution of 8-bit and a maximum operating frequency of 6.7 MS/s. The chapter content is organized in this way: In section 5.1 the work is introduced and contextualized with reference to the literature, in section 5.2 the specification, the block diagram of the ADC and a brief description of the components are provided, in section 5.3 is described the novel ULV comparator of the ADC, the ADC and comparator simulation results are reported in section 5.4, in section 5.5 the results are compared with the literature and finally in section 5.6 conclusion are drawn.

5.1 Introduction and context

Analog-to-digital converters (ADCs) are essential components in a wide range of portable and biomedical devices. Converting analog signals to digital form with high accuracy while maintaining low power consumption is the challenge that designers must face. These devices, such as smartphones, laptops, and implantable biomedical systems, require energy-efficient operation to maximize battery life or leverage energy harvesting.

Energy harvesting may replace the battery or support it to supply wearable and portable devices. It consists in retrieving energy from the environment sources such as solar energy, vibration, electromagnetic irradiation, and so on. The limit of energy harvesting lies in the reduced available power and also in the low voltage energy harvested sources can generate. To exploit energy harvested power it is, almost always, necessary to use a DC-DC converter to obtain an higher voltage sufficient to supply standard devices.

A critical element influencing the performance and power efficiency of ADCs is the comparator. The advantage of develop ULV comparators and ADCs is related to the use and the design of DC-DC converts. DC-DC converters are significantly more efficient, if the voltage of the source has to be increased by a small factor [26].

The comparator, which needs to quickly detect small voltage differences and provide a stable logic output, represents in most cases a bottleneck in terms of

performances for the ADC, especially for the conversion rate.

Lowering the comparator supply voltage often comes at the cost of reduced operating frequency, which limits the ADC's sampling rate and overall performance. However, for applications such as Internet of Things (IoT) devices, wireless sensor networks, and System-on-a-Chip (SoC) maintaining high sampling rates is crucial to ensure accurate and real-time data acquisition.

These applications often require power efficiency due to their reliance on small batteries or energy-harvesting technologies. In IoT devices, ADCs with medium precision (8-12 bit) and high-speed sampling are needed for real-time RF signal processing, such as in wireless communication and image capturing, where quick and accurate data conversion is vital [73, 123, 151].

To address this challenge, innovative comparator designs have been developed that focus on achieving ultra-low power consumption without significantly sacrificing speed. Dynamic clocked comparators, such as the Strongarm architecture and body-driven comparators, have been proposed to operate efficiently at low supply voltages, down to 0.2 V or even lower. These designs utilize clever techniques like eliminating the tail current generator or employing cross-coupled PMOS devices to minimize power dissipation while still achieving fast response times.

In summary, while reducing power consumption in ADCs is essential for extending device autonomy and functionality, it is equally critical to maintain an adequate sampling rate. This balance can be achieved through advanced comparator designs and innovative circuit techniques that enable ultra-low voltage operation while minimizing performance trade-offs. Such advancements are key to enhancing ADC performance in power-constrained applications, enabling efficient, high-speed data conversion in compact and low-power systems. [34, 46]

5.2 ADC specification and block diagram

The ADC is an 8-bit fully differential charge-redistribution SAR. The block scheme is quite similar to the one in figure 2.14, there are some differences in the ADC logic in order to implement the desired switching algorithm, the effective block scheme of the ADC is reported in figure 5.1.

The ADC has been realized in 55 nm ST-microelectronic CMOS technology, the core and the most innovative element of the ADC is the ULV comparator. The comparator has been simulated in various supply voltage, from 0.2 V to 0.4 V. The comparator can be calibrated in foreground in order to reduce offset, all the details about the comparator are reported in section 5.3. The second innovative element in the ADC is the switching algorithm, that is a modification of the Quasi monothonic switching. This algorithm reduces CDAC common mode output voltage swing allowing the comparator to work in a more relaxed condition preventing a performance degradation due to high swing of the comparator input common mode voltage. the DAC is a conventional 8-bit binary scaled CDAC, the S & H involves clock boost to enhance linearity

Figure 5.1. Block Diagram of a fully differential charge redistribution 8-bit ULV SAR ADC

5.2.1 Switching algorithm

The switching algorithm used in this ADC is the one used in the ADC of chapter 3 that has been described in 3.4. It is a modification of the quasi-monotonic switching that noticeably reduces the common-mode CDAC voltage swing, and allows to decouple the final value of the CDAC common mode voltage to the input common mode voltage, allowing its optimization for comparator performances. In this way the comparator input common-mode voltage is always in the range that allows it to work correctly. In this particular case, the first and the last transition are upward the others are downward, as can be seen by observing the control logic in the block scheme in figure 5.1. The output common mode is maintained, during all the conversion, around its optimal value that is $V_{DD}/2 = 200\text{ mV}$.

5.2.2 Capacitive 8-bit DAC

The DAC of the ADC is a conventional 8-bit, binary scaled CDAC. The capacitors have been implemented as power of two multiples of the unit capacitor $C = 20\text{ fF}$, fixed capacitor $C_0 = C$ has been eliminated in order to reduce the shrinkage of the ADC differential mode range due to capacitive divider between CDAC capacitance and input parasitic capacitance of the comparator. The layout of the capacitor,

depicted in figure 5.2, has been realized following the common centroid criteria, it means that the capacitance distribution in the layout has a central symmetry (with the exception of $C_1 = C$ that is a single capacitor). In this way the production process gradient effect is minimized. To grant central symmetry and equivalent parasitic effect for each capacitor a set of dummy capacitor has been added to the CDAC design to fulfill the layout. Both the plates of the dummy capacitors are connected to GND and they are no active element in the schematic.

5.2.3 Track and Hold

The track and hold used in this ADC is quite identical to the one used in the ADC of chapter 3 that has been described in 3.3. The adopted topology is the Razavi bootstrapped switch in [110] depicted in figure 3.3. In this Topology the input signal is bootstrapped to the gate of the main switch ensuring constant V_{gs} during sample phase. In this way the linearity is maximized.

5.3 ADC ULV switch Comparator

The core of the ADC is the ULV comparator, the comparator is a switch-driven modified version of the Strongarm dynamic comparator with a double charge-pump dynamic bias. The comparator is able to work at a V_{DD} as low as 0.4 V and below, guaranteeing a maximum operating frequency of 200 MHz. Moreover, it is possible to exploit the charge pump capacitor arrays on the lower supply bar, to perform a foreground calibration on the comparator.

5.3.1 Topology description and working principle

Topology description The comparator is a modified version of the Strongarm comparator described in 2.4.2. The comparator is dynamic biased, the dynamic bias is implemented with a double charge pump on both the supply bar. The comparator scheme is reported in figure 5.3. This configuration has been already used in [13] (described in 4.4), Transistor M_7 and capacitor C_u implement the upper charge pump, but in this case the capacitor of the lower charge pump has been split on two sides, one for each transistor of the differential pair. The two capacitors (C_{b_p} and C_{b_m}) are implemented with a capacitor array with one pre-charge transistor (M_3 and M_4) for each capacitor. This configuration allows foreground calibration in a way quite similar to 4.5. The capacitor array is depicted in figure 5.4. The comparator is gate-driven but, in order to eliminate the tail transistor and reduce the number of stacked device, the gates of the input pair transistors (M_1 and M_2) are driven by a switch ($T_1 - T_2$ and $t_3 - T_4$). The switch is used to connect to ground the gates of the transistors during pre-charge phase avoiding static consumption. The advantage of the use of the gate instead of the body relies on the greater gate transconductance g_m compared to the body one g_{m_b} , this improves the preamplification gain ensuring better performance in terms of noise. Finally, like the comparator described in 4.5, the latch is implemented with just a pair of cross-coupled PMOS transistors (M_5 and M_6), the NMOS transistors have been removed to reduce the number of stacked devices reducing the minimum theoretical V_{DD} . In the conventional Strongarm ,

these devices avoids static consumption due to shortcut between V_{DD} and ground during evaluation. In this topology, however, static current consumption cannot occur because the lower supply bar is replaced by a capacitor. transistor S_1 and S_2 reset the output nodes to V_{DD} while S_3 equalizes nodes v_{b_p} and v_{b_m} .

Working principle The operation of the ULV switch comparator is as follow:

- **Pre-charge phase:** when the clock is low, transistors by M_3 and M_4 pre-charge bottom supply bar nodes v_{b_p} and v_{b_m} , connected to the top plates of the array capacitors, to ground (the bottom plate voltage is set to V_{DD} by the $\overline{CLK}$ signal), similarly, on the upper supply bar node, capacitor bottom plate node v_u is pre-charged to V_{DD} by M_7 (the top plate voltage is set to ground by the CLK signal). The input switches drive ground signal to the input pair gates in order to switch off transistors M_1 and M_2 avoiding a short-cut between V_{DD} and ground and so static consumption. Transistors S_1 and S_2 reset output nodes to V_{DD} and S_3 equalizes them, transistor S_4 equalizes v_{b_p} and v_{b_m} .
- **Preamplification phase:** when the clock toggles, reset transistors ($S_1 - S_4$) and pre-charge transistors ($M_3, v M_4$ and M_7) are switched off, input switches now drive input signals to the input pair gates, switching on M_1 and M_2 . The effective voltage headroom are boosted by the coupling of $\overline{CLK}$ falling edge, that lowers v_{b_p} and v_{b_m} below ground voltage and by the coupling of CLK rising edge to the upper supply bar node that raises v_u above V_{DD} . M_1 and M_2 start preamplifying the input differential signal by discharging output nodes V_{out_p} and V_{out_m} , this phase ends when output nodes voltage is dropped so that M_5 and M_6 turn on, activating latch positive feedback.
- **Evaluation phase:** at this point, the latch is on and can regenerates the signal based on the initial condition set in the preamplification phase according to the sign of differential input voltage.

Calibration As said at the begin of this section, the comparator can be calibrated in foreground, allowing a huge reduction of the input referred offset. This is possible thanks to the split of the lower supply bar in two nodes, connected to digital-programmable capacitor arrays (depicted in figure 5.4) in a way practically identical to the pseudo-differential comparator in section 4.5. The theory underlying the calibration has been detailed in 4.5.1 whereas the architecture and process implemented in the comparator are described in detail in 4.5.2.

5.3.2 Sizing and layout

The comparator has been implemented in 55 nm STMicroelectronics technology. The designs has been optimized for a supply voltage of 0.4 V (but it can work at a supply voltage up to 0.25 V as long as the operative frequency is reduced) without any forward body biasing.

Table 5.1 details the transistor sizing of the comparator core. It has been optimized to maximize the speed while maintaining a good (EDP).

Similarly to comparators in section 4.5, the sizing of each circuit was adjusted based on the theoretical insights from section 4.5.1. The design prioritizes speed by increasing the total capacitance of the programmable array, thus enhancing calibration accuracy (see paragraph 4.5.1) and the capacitance of the top capacitor. All the capacitors have been implemented with Increasing the W/L ratio in the input pair of the PDCP latch would only increase the load capacitance, thereby introducing greater delays. Larger W/L ratio would mean better performance in terms of mismatch, but the input referred offset can be mitigated through the foreground calibration and so the priority has been assigned to the speed in the trade-off. The PMOS devices have been sized in order to minimize delay. Sizing the PMOSs too large does not improve the speed characteristics but rather worsens them due to the greater parasitic capacitances. The transistors of the input switches are two NMOSs and have been sized based on these criteria: the transistors that drive the ground to the gate of input pair transistors have a minimum size, since during reset phase, the timing for the gate node discharge transient is relaxed and so the on-resistance can be larger. whereas the transistors that drive the input signal should have the minimum possible on-resistance, so their size should be as large as possible; however, making it too large implies a leakage current that can discharge the CDAC of the ADC during the phase in which the CLK signal is low, this means that, a large amount of leakage current combined with a slow clock translate into a voltages drop of the CDAC and so a degradation of the ADC linearity. The design features an inverter that generates $\overline{CK}$.

Table 5.1. Transistor sizing of the proposed single-stage comparator topology.

Device	W/L [μm]
$M_1 - M_2$	2.00/0.06
$M_3 - M_4$	5/0.06 3
$M_5 - M_6$	0.80/0.06
M_7	10/0.06
$S_1 - S_2$	0.60/0.06
S_3	1.00/0.06
$T_1 - T_3$	2.00/0.06
$T_2 - T_4$	0.50/0.06

Capacitor Array Sizing Table 5.2 shows the sizing of the top capacitor C_u and of the capacitors arrays C_{bp} and C_{bm} used in the comparators. The largest capacitors are realized using library MOS capacitors, while smaller ones are implemented as transistors with shorted source, drain, and body terminals.

To ensure accurate and reliable calibration, the capacitive array incorporates redundancy and so the capacitors in the array are not binary scaled. The capacitors are sized such that $C_{i-1}/C_i < 2$ for $i = 1, 2, \dots, n$, enabling redundancy to correct potential calibration errors (such as mismatches between capacitors) [104]. The variable-radix redundancy scheme, which was optimized manually through simula-

tions, also helps improve robustness against noise during calibration by averaging the effects of noise over multiple decisions. To enhance the calibration resolution, before the last four capacitors in the array there is a bridge capacitor C_b

Table 5.2. Sizing of the top capacitor and of the capacitor arrays .

Top Capacitor	
Capacitors implemented as library capacitor (C) [fF]	
C_u	200
Array Capacitors	
Capacitors implemented as library capacitor (C) [fF]	
C_0	8
C_1	11
C_2	9
Capacitors implemented as MOS transistors (W/L) [μm]	
C_3	1.50/0.06
C_4	1.00/0.06
C_5	0.80/0.06
C_6	0.50/0.06
C_7	0.30/0.06
C_8	0.20/0.06
C_b	0.06/0.06
C_9	0.02/0.06
$C_{10} - C_{12}$	0.135/0.06
MOS transistor switches (W/L) [μm]	
$M_{S_0} - M_{S_{11}}$	0.20/0.06

Layout Considerations In the layout special attention was paid to the layout to maximize symmetry and minimize systematic offset. Additionally, significant effort was made to reduce capacitive coupling between interconnects.

The layout is shown in figure 5.5. The area footprint, including the capacitive arrays, is xxx μm^2

5.4 Simulation results

All the simulations have been performed in post-layout, in Cadence Virtuoso. The comparator has been tested at a V_{DD} equal to 0.25 V, 0.3 V and 0.4 V using a differential input voltage $V_{id} = 5 \text{ mV}$ while the ADC only at $V_{DD} = 0.4 \text{ V}$. The ADC has been simulated at a sample frequency up to 6.67 MS/s. CK signal is provided by a real buffer chain, to generate a realistic clock waveform and $\overline{CK}$ signals is provided by a logic inverter Obviously the consumption of the buffer has been taken into account. The section is divided into two subsection, the first one reports the comparator performances and the second the ADC performances.

5.4.1 Comparator performances

All simulations were carried out by loading the outputs of the comparator with minimum area inverters. figure 5.6 shows the transient behavior of the output nodes voltages at $V_{DD} = 400 \text{ mV}$.

Analyzing figure 5.6 it is possible to recognize, in the correspondence of the clock rising edge, the voltage boost caused by the clock edges coupling on the top and bottom supply bars. This improves the performance in terms of preamplification gain since the output nodes have to be discharged for a longer time, as explained in sections 4.3 and 4.5. This boost and the reduced number of stacked device allows the comparator to work at a V_{DD} as low as 0.25 V. When the output nodes have been discharged up to about 100 mV, regeneration phase starts and the output signals are regenerated according to the sign of the input differential voltage. It should be noted that the high output voltage (V_{op} in figure 5.6) does not saturate at V_{DD} but it stops its raising at about 350 mV. This is because, the current that supplies the latch PMOSs during the regeneration phase is provided by the capacitor C_u . While C_u is discharging its bottom plate node voltage, that is the voltage of the two latch PMOSs sources, drops below V_{DD} and so the regeneration of the high output node voltage is stopped before V_{DD} is reached. This is not a problem for the comparator functionality, in fact, despite the low voltage drop, the comparator is able to drives the output inverters properly (for every V_{DD} at which the comparator have been tested) and its output signal are completely transferred at the correct voltage to the next stage.

Figure 5.7 shows the transient behavior of the voltage of node V_u and common-mode voltage of nodes V_{bm} and V_{bp} in figure 5.3. An additional signal V_{head} has been defined, representing the difference between V_u and V_{bcm} , that is the effective voltage headroom of the comparator. It is possible to observe that the top bar voltage rises above V_{DD} and the low bar voltages drop under zero at the begin of preamplification phase as expected. During regeneration phase C_u is discharged while nodes V_{bp} and V_{bm} rises above zero due to the current that flow through the circuit. This happens when the preamplification phase is concluded, and so this effect does not affect the comparator decision nor the comparison speed is worsened.

Table 5.3 reports a summary of the nominal performances of the comparator at $V_{id} = 5 \text{ mV}$, evaluated for three different V_{DD} levels: 0.25 V, 0.3 V, and 0.4 V. What can be highlighted is the value of the input referred noise variance σ_n that is about 1.4 mV in all the three cases. The clock frequency that has been selected for each cases is the maximum that ensures reliable operation. To better outline the operating range of the comparator figure 5.8 reports the trend of the delay as the V_{DD} varies. $V_{DD} = 0.25 \text{ V}$ is the minimum supply voltage at which the comparator can work properly. Under this voltage the performances are heavily deteriorated.

The comparator has been evaluated across PVT (process, supply voltage, and temperature) corners conditions to demonstrate its robustness. The simulation results for PVT corners, conducted at $V_{DD} = 0.4 \text{ V}$ and $f_{ck} = 200 \text{ MHz}$, are presented in table 5.4. The comparator exhibits consistent performance across a broad range of operating conditions. Power consumption remains nearly constant, as it is primarily dominated by the dynamic component from switching, although some variations in delay are observed.

V_{DD} [V]	0.4	0.3	0.25
f_{ck} [MHz]	200.00	100.00	20.00
t_d [ns]	0.49	1.23	3.08
P_d [μ W]	3.94	1.45	0.19
PDP [fJ]	1.93	1.78	0.60
EDP [fJ/GHz]	9.63	17.8	29.82
σ_n [mV]	1.43	1.41	1.41
σ_o [mV]	1.25	1.72	4.69

Table 5.3. Performance summary of the proposed comparator vs V_{DD} , with $V_{id} = 5$ mV.

Table 5.4. Corners at $V_{DD} = 0.4$ V, $f_{ck} = 200$ MHz and $V_{id} = 5$ mV.

Performance	Nominal	$V_{DD_{min}}$	$V_{DD_{max}}$	T_{min}	T_{max}	SS	FF	SF	FS
t_d [ns]	0.49	0.66	0.39	0.54	0.45	1.43	0.31	0.61	2.14
P_d [μ W]	3.94	3.10	4.93	3.66	4.82	2.68	4.98	3.96	3.19
PDP [fJ]	1.93	2.05	1.92	1.96	2.15	3.83	1.53	2.42	6.83
EDP[fJ/GHz]	9.63	10.25	9.58	9.82	10.74	19.15	7.65	12.11	34.14

Figure 5.9 depicts the input referred offset histogram of the comparator at $V_{DD} = 400$ mV. It is the result of a 200 iterations Montecarlo simulation considering mismatch and process variations. In the figure the histogram for the calibrated comparator (blue) is superimposed on that for the non-calibrated comparator (red) to highlight the effect of the calibration. In the figure is reported the calibrated $\sigma_o = 0.37$ mV and uncalibrated $\sigma_o = 15.42$ mV, the calibration reduces σ_o of about 97.6 %. The calibration also minimizes systematic offset due to layout asymmetries reducing μ_o to -11.30 μ V. In figure 5.10 are reported the input referred offset histogram of the calibrated comparator at $V_{DD} = 300$ mV (figure 5.10a) and at $V_{DD} = 250$ mV (figure 5.10b). The simulations have been performed with the same setup, it can be noted that the σ_o are slightly larger and the more V_{DD} is reduced the larger σ_o is. This is due to the reduced preamplification gain at lower supply voltage.

5.4.2 ADC performances

The ADC has been post-layout simulated in Cadence Virtuoso, with $V_{DD} = 0.4$ V and a clock frequency of $f_{ck} = 66.67$ MHz. The ADC needs 10 clock cycle to fully convert a sample so it operates at $f_S = 6.67$ MS/s. Figure 5.11 depicts the output sequence of the ADC, with a sinusoidal input of 180 mV amplitude and $f_{sin} \approx 104$ kHz and figure 5.12 its spectrum content.

Figure 5.13 illustrates the transient behavior of the SAR ADC CDAC outputs during a conversion process.

The two signals follow the logic of transition scheme described in Section 3.4 that has been used also in this ADC (see section 5.2.1). The small periodic fluctuations in $V_{o_{cm}}$ result from the kickback current generated by the comparator. In correspondence of the first transition, the switching algorithm involves the additional logic gates to apply a common mode positive shift to the output of the DAC that is removed in the next transition. In this way, as the conversion progresses, $V_{o_{cm}}$ (dashed green

line in figure 5.13) stabilizes near 200 mV, limiting the output common-mode swing to around 50 mV, which is the expected $V_{DD}/8 = 50$ mV.

Table 5.5 reports the performance of the ADC in nominal condition

Table 5.5. Post-layout performance summary of 8 bit SAR ADC at $f_s = 6.67$ MS/s and $V_{DD} = 0.4$ V.

	Typ.	Typ. (with noise)
SNDR [dB]	49.01	44.57
P_{avg} [μ W]	39.64	39.64
ENOB	7.85	7.11
FOM_W [fJ/conv. step]	25.75	43.02

As it is possible to see the noise impacts on the ADC performances, reducing the ENOB to 7.11.

Table 5.6 summarizes the ADC performance under PVT variations. The most critical corner in terms of linearity is T_{max} whereas the most critical in terms of Power consumption is SF. The SNDR is kept at good level across all the corners whereas the power varies significantly.

Table 5.6. Performance of 8b ULV ADC under PVT variations.

	Nominal	$V_{DD_{min}}$	$V_{DD_{max}}$	T_{min}	T_{max}	SS	FF	SF	FS
SNDR [dB]	49.18	48.22	49.27	49.46	46.14	47.25	48.76	49.34	46.85
P_{avg} [μ W]	39.65	30.83	50.42	23.94	97.00	46.96	114.4	123.80	61.15
ENOB [bit]	7.88	7.72	7.89	7.92	7.37	7.56	7.81	7.90	7.49
FOM_W [fJ/conv. Step]	25.29	21.96	31.82	14.78	87.79	37.40	76.43	77.51	51.00

5.5 Comparison with the literature

Table 5.7 reports the comparison of the ULV SAR ADC Performances with the state-of-the-art. Despite the Walden FOM is not competitive the ADC is able to work at a frequency as high as 6.67 MS/s, that is the highest for a V_{DD} equal to 0.4 V. The ADC guarantees good levels of accuracy, even in terms of noise despite the low supply voltage.

5.6 Conclusions

A novel 0.4 V 8 bit ADC topology is proposed in this work. The ADC relies on an ULV comparator that is able to work at a supply voltage as low as 0.25 V. The comparator has been optimized to work at 0.4 V in order to be inserted in the block scheme of the ADC. Moreover the ADC involves a bootstrapped Track and Hold to enhance linearity and an innovative switching algorithm that minimizes the CDAC common mode voltage swing and decouples it from the input common mode voltage. The ADC can work at an operative frequency as high as 6.67 MS/s and, despite the consumption is not competitive it guarantees good level of accuracy also in noise terms.

Table 5.7. Comparison with the state-of-the-art of ULV 8b SAR ADC

	This Work	[147]	[146]	[149]	[155]
Year	2024	2015	2012	2023	2015
Technology [nm]	55	40	40	40	180
Resolution [bit]	8	8	8	10	8
f_s [MS/s]	6.67	1.024	1.3	0.1	2
V_{DD} [V]	0.40	0.40	0.4	0.4	0.5
SNDR [dB]	44.57	44.80	44.3	59.07	48.11
ENOB [bit]	7.11	7.15	7.07	9.52	7.70
P_{avg} [μ W]	39.64	0.71	1.06	0.356	15.98
FOM_W [fJ/conv. st.]	42.98	4.88	6.08	4.85	38.44
Area [mm ²]	-	0.0153	0.0153	0.0363	0.21

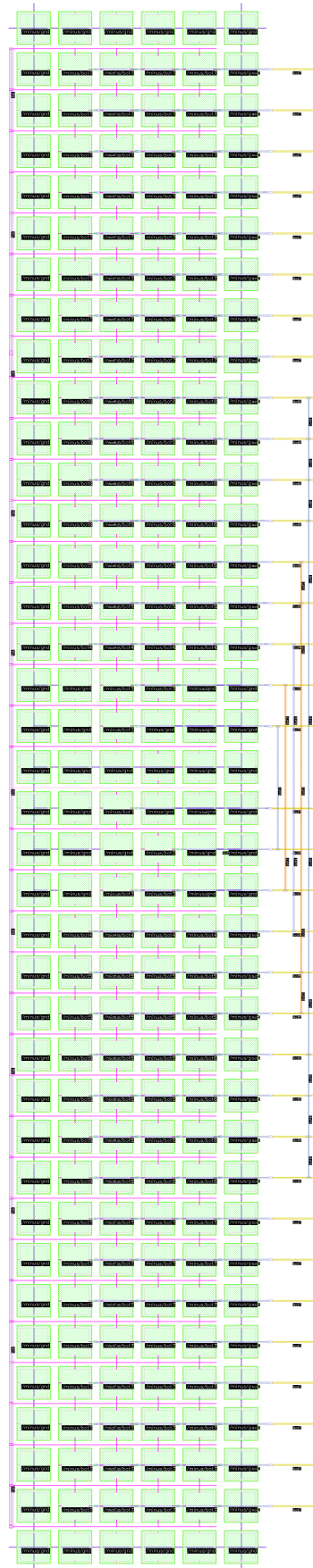


Figure 5.2. Layout of the 8-bit CDAC

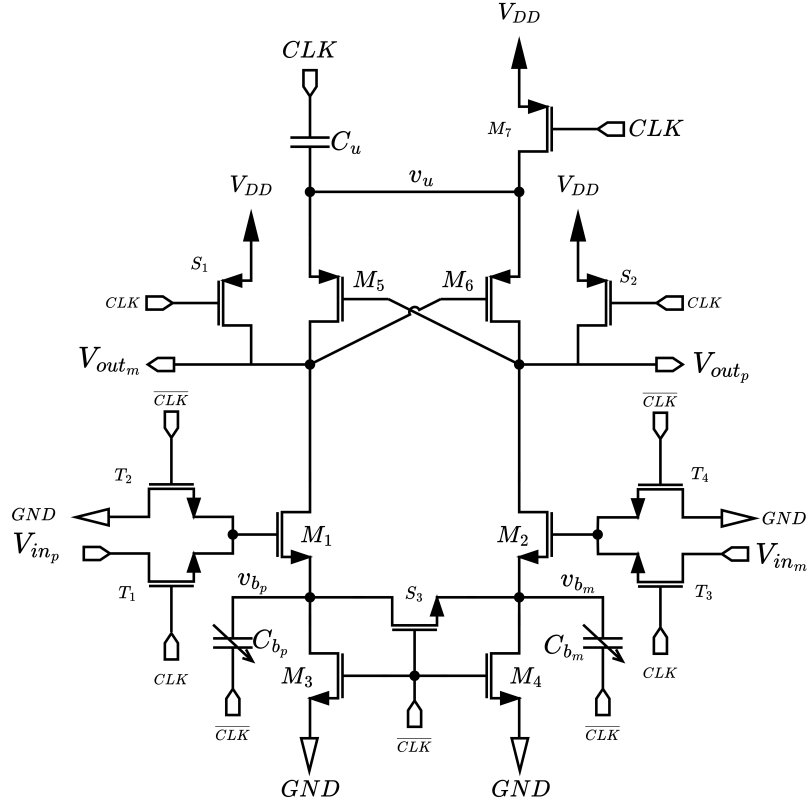


Figure 5.3. Schematic of the ULV dynamic biased switch-Strongarm comparator

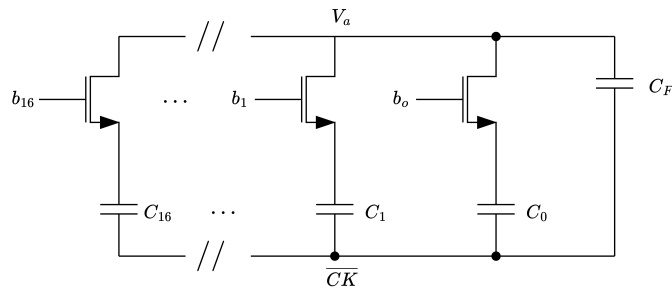


Figure 5.4. Schematic of the capacitor array used in the comparator

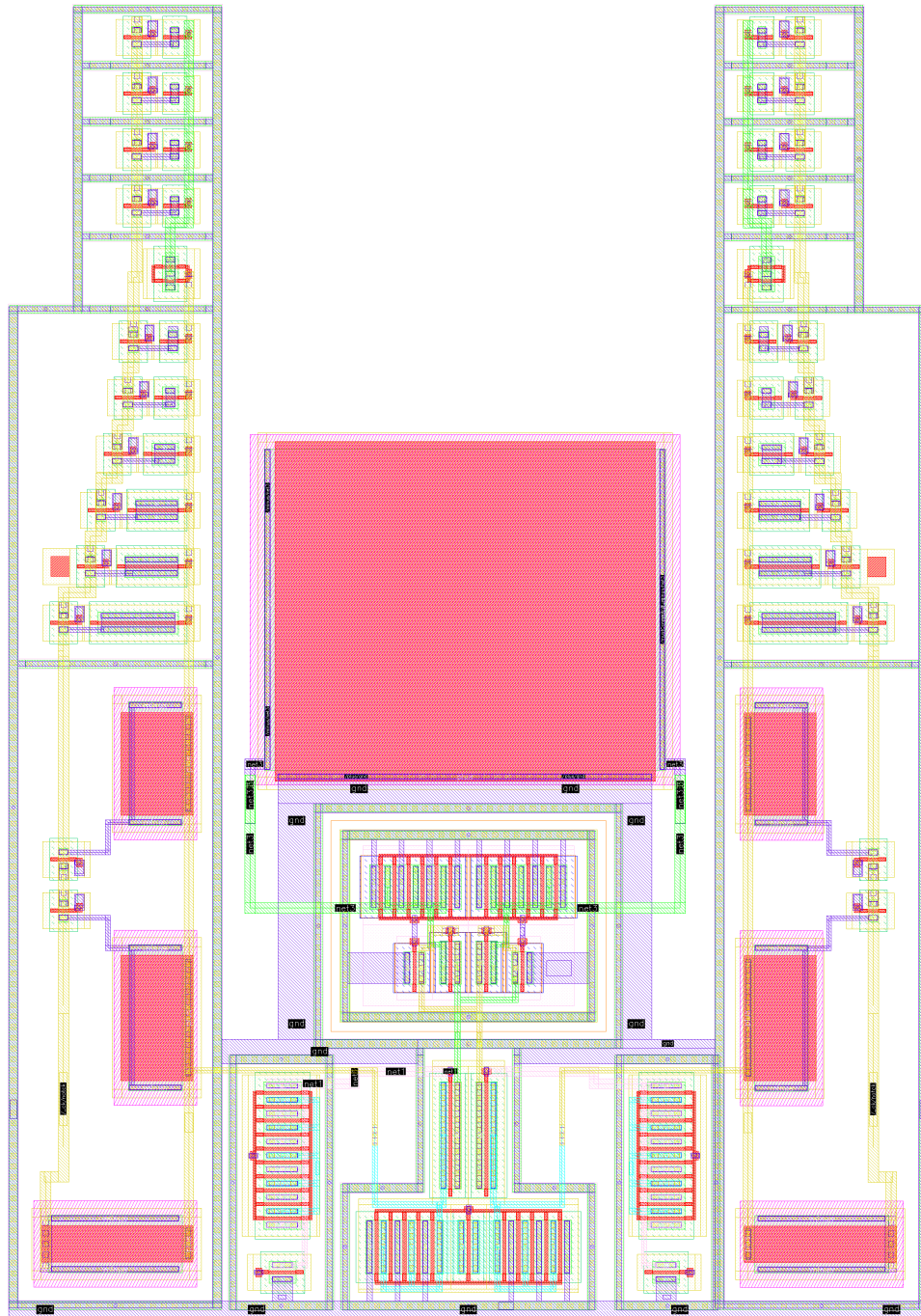


Figure 5.5. Layout of the comparator

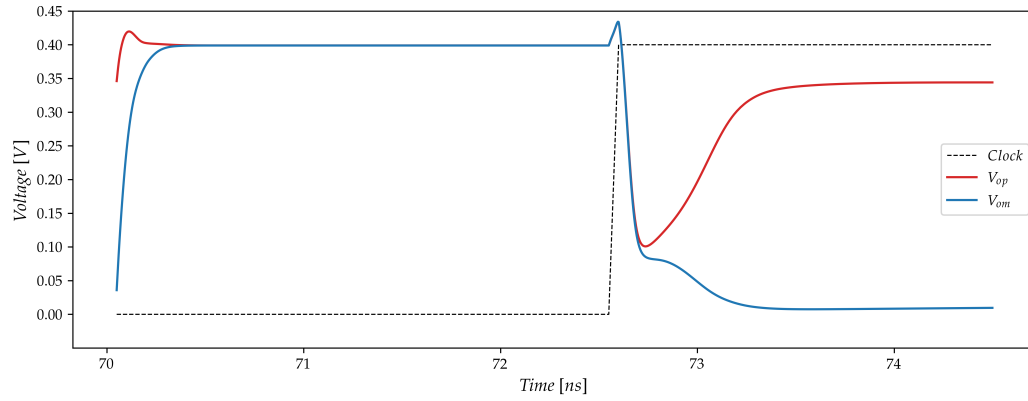


Figure 5.6. Comparator output signals transient behavior

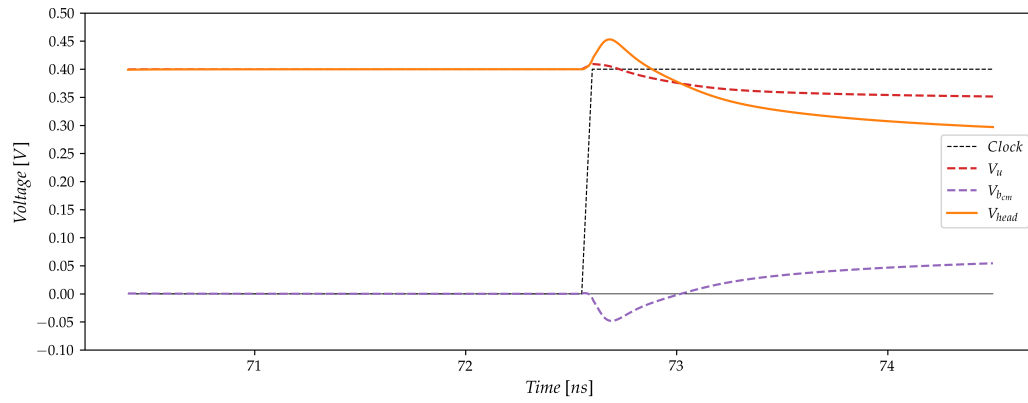


Figure 5.7. Comparator top and bottom supply bars voltages transient behavior

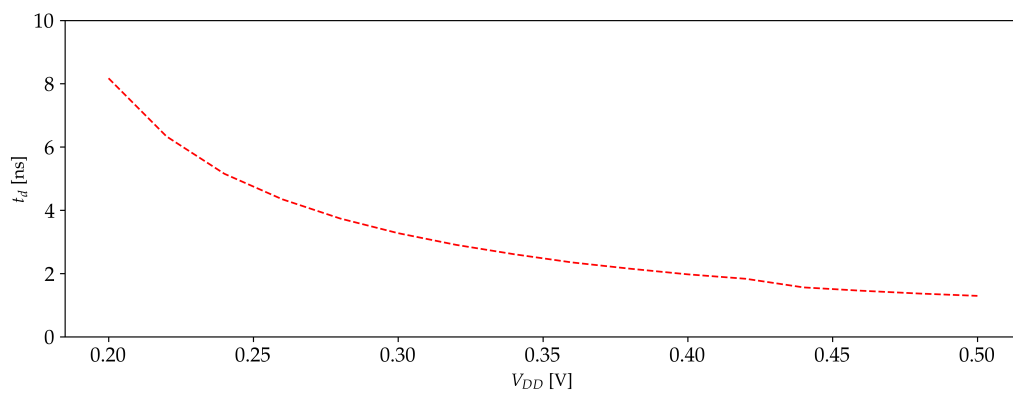


Figure 5.8. Delay of the proposed comparator vs V_{DD} .

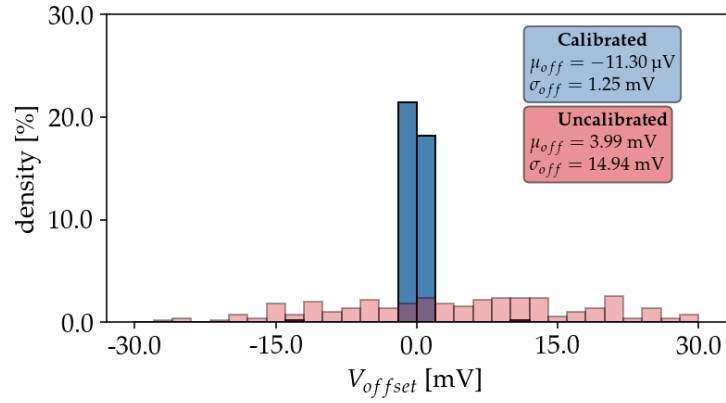


Figure 5.9. Histogram of the input referred offset under mismatch and process variations at $V_{DD} = 400$ mV for calibrated and uncalibrated comparator

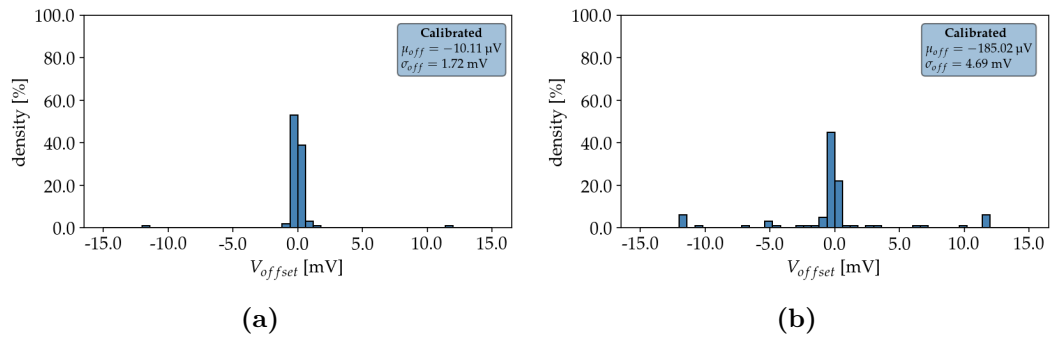


Figure 5.10. Histogram of the input referred offset under mismatch and process variations at a) $V_{DD} = 300$ mV and b) $V_{DD} = 200$ mV

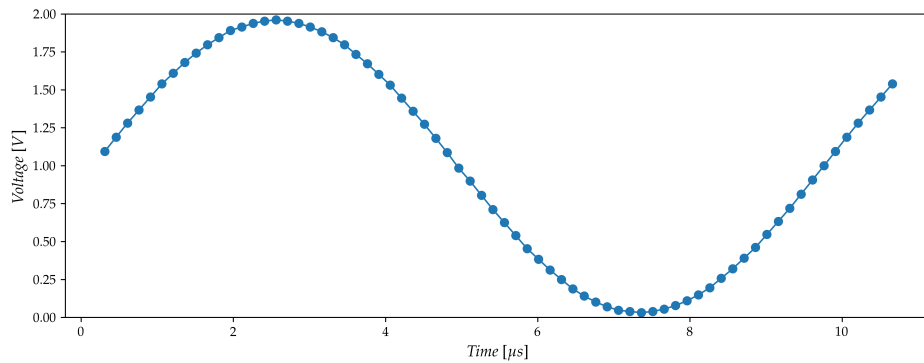


Figure 5.11. Output sequence of the ADC with a sinusoidal input

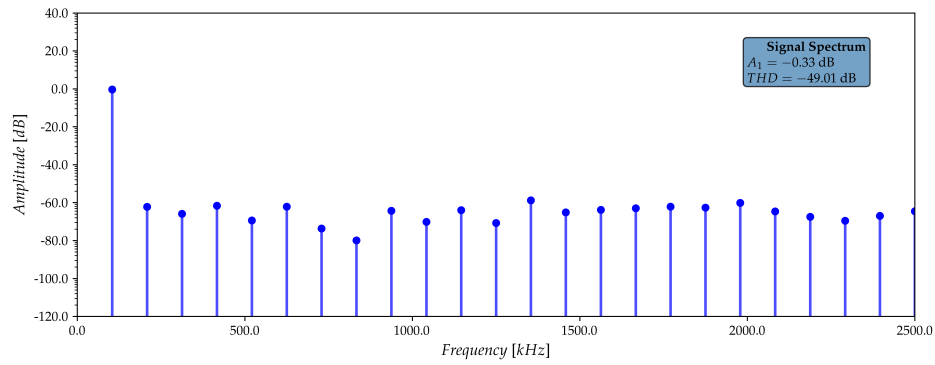


Figure 5.12. Spectrum of the Output sequence of the ADC with a sinusoidal input

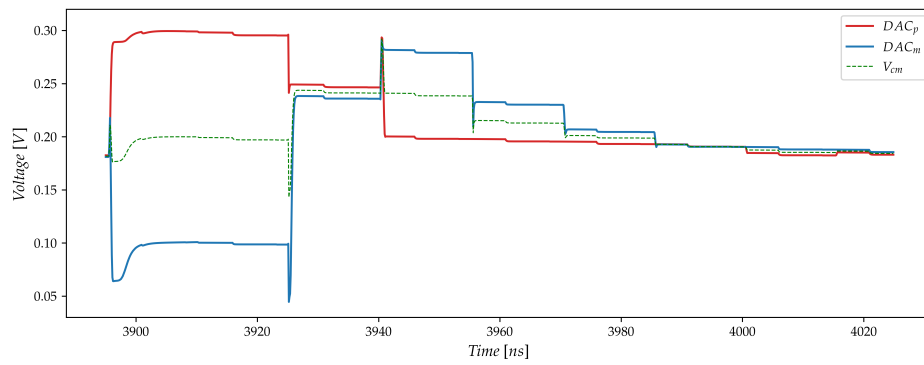


Figure 5.13. Transient behavior of the CDAC output voltages

Chapter 6

A design of 17 GHz inductor-less Quasi-Sallen Key low-pass filter

6.1 Introduction

In pursuit of higher speeds, time-interleaving has emerged as a popular method for increasing the effective sampling rate by operating multiple ADC channels in parallel. This technique enables speeds but introduces additional complexity due to channel mismatch issues, such as gain, offset, and timing skew [8, 99].

Such converters require low-pass filters, to be used as anti-aliasing and shaping filters, with a bandwidth from DC to 10GHz and beyond. Asynchronous time interleaving (ATI) architectures [20, 57, 90, 91] also require low-pass filters in the tens of GHz range. The main performance requirements on the filters are related to out-of-band suppression, forcing the use of high-order filters, and linearity, not to limit the ADC / DAC performance. Power and area consumption are also of interest in the light of integration of the filters together with the converters.

In this chapter a novel wide-band Low Pass Filter (LPF) topology is presented. It is an evolution of the Sallen-Key bi-quad architecture, suitable for applications at very high frequency. The pole of the buffer amplifier is exploited as one of the poles of the bi-quad, therefore overcoming the constraints it poses on the maximum resonance frequency that can be achieved. This allows designing low-pass filters with cutoff frequencies above 10GHz without using bulky inductors and with good linearity performance provided by the use of feedback. This approach has been exploited to design a bi-quad in a commercial SiGe BiCMOS technology with maximum f_T of about 320GHz. The bi-quad has been designed to provide a resonance frequency f_0 of 12GHz and a quality factor Q of 1.9; post-layout simulations show a cutoff frequency in excess of 17GHz, 15.75mW of power consumption, an equivalent input noise below $1\mu V_{rms}$ and -52dB THD for a 640mVpp input signal, with a very limited area consumption [12].

The paper is structured as follows: Section 2 presents the proposed pseudo-Sallen-Key approach and discusses its non-idealities, with particular emphasis on the effect of the output resistance of the active block. Section 3 presents the design of the bi-quad, discussing both system design and the adopted circuit topologies,

and post-layout simulations are reported in Section 4 together with a comparison with the state-of-the-art. Some conclusions are drawn in Section 4.

6.2 Proposed quasi-Sallen-Key bi-quad architecture

The Sallen-Key topology, as illustrated in Figure 6.1a, represents a filtering architecture utilizing a single amplifier stage. In this configuration, the resonance frequency f_0 and quality factor Q of the bi-quad are theoretically determined by the values of the external passive components (two resistors and two capacitors, responsible for setting the open-loop poles) and the amplifier gain K . These relationships are captured by the ideal transfer function of the Sallen-Key filter, shown in equation (6.1).

$$F(s) = \frac{K}{1 + s[(R_1 + R_2)C_2 + (1 - K)C_1]s + s^2 C_1 C_2 R_1 R_2} = \frac{K}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \quad (6.1)$$

Where the angular resonance frequency ω_0 and quality factor Q are given by:

$$\omega_{0SK_{ideal}} = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} \quad (6.2)$$

$$Q_{SK_{ideal}} = \frac{\sqrt{C_1 C_2 R_1 R_2}}{(R_1 + R_2)C_2 + (1 - K)C_1} \quad (6.3)$$

In real-world implementations, deviations from the ideal case arise due to the input/output impedance of the amplifier and its internal pole-zero characteristics. These factors can distort the transfer function, although the circuit approaches ideal behavior when the input impedance is significantly higher than the external resistances, the output impedance is much lower, and the amplifier poles are placed well beyond the filter's resonant frequency. The amplifier's limitations define the upper bound for the resonant frequency achievable with a given technology. Should these conditions not be met, the f_0 and Q values will also depend on the amplifier's internal poles, making the design more susceptible to variations in process, voltage, and temperature (PVT). This sensitivity becomes even more pronounced in high-frequency applications, such as those involving multi-GHz filters, where the amplifier would need to maintain a bandwidth in the tens of GHz range, increasing design complexity and PVT vulnerability.

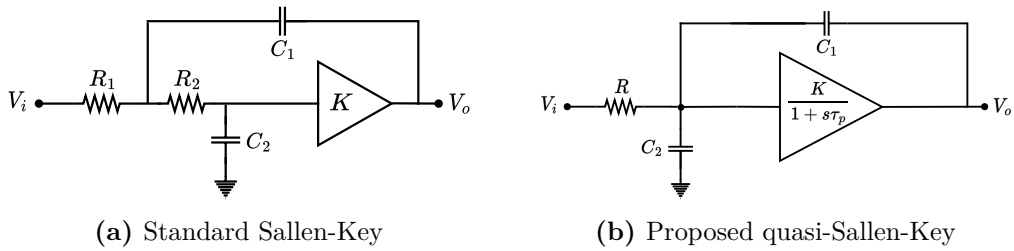


Figure 6.1. Comparison of conventional and proposed filter topologies.

To address these limitations, a quasi-Sallen-Key configuration is proposed, as depicted in Figure 6.1b. This design considers the amplifier's non-idealities by incorporating its internal pole as one of the bi-quad's open-loop poles, replacing one of the RC pairs in the standard configuration. A single-stage amplifier is assumed for simplicity, as shown in Figure 6.2, featuring a resistive load (such as a degenerated differential pair to stabilize gain and enhance linearity), followed by an emitter follower for DC level shifting and output impedance reduction. Additionally, a capacitor is added in parallel with the load resistor to define the desired amplifier pole, described by:

$$A_v(s) = G_m(R_c \parallel C_c) = \frac{K}{1 + s\tau_p} \quad \text{where } K = G_m R_c \text{ and } \tau_p = R_c C_c \quad (6.4)$$

In contrast to the traditional Sallen-Key structure, the amplifier in this topology physically separates the open-loop poles, functioning as a buffer inserted into the filter's architecture. To counter the amplifier's input capacitance, which could affect the transfer function, an explicit capacitor is added to the input of the amplifier (C_2 in Figure 6.1b). This approach grants greater flexibility in the bi-quad design and reduces sensitivity to the parametric variations of active devices.

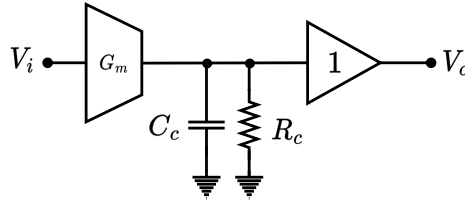


Figure 6.2. Block diagram of the amplifier in the proposed topology.

6.2.1 Analysis Under Ideal Conditions

Initially, the performance of the proposed architecture under ideal conditions are examined, neglecting the input and output impedance of the amplifier, and considering it to have a gain K and a single dominant pole with time constant τ_p . From the circuit in Figure 6.3, the transfer function is derived as:

$$F(s) = \frac{K}{1 + s[R(C_1(1 - K) + C_2) + \tau_p]s + s^2\tau_p(C_1 + C_2)R} = \frac{K}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \quad (6.5)$$

Where the DC gain of the first amplifier stage is $K = G_m R_c$. The ideal resonant frequency and quality factor can be calculated as:

$$\omega_0 = \sqrt{\frac{1}{\tau_p(C_1 + C_2)R}} = \omega_{0ideal} \quad (6.6)$$

$$Q = \frac{\sqrt{\tau_p(C_1 + C_2)R}}{[C_1(1 - K) + C_2]R + \tau_p} = Q_{ideal} \quad (6.7)$$

Here, the subscript "ideal" indicates that these expressions apply to the ideal architecture in Figure 6.1b. In subsequent sections, an analysis on how amplifier non-idealities influence ω_0 and Q is provided.

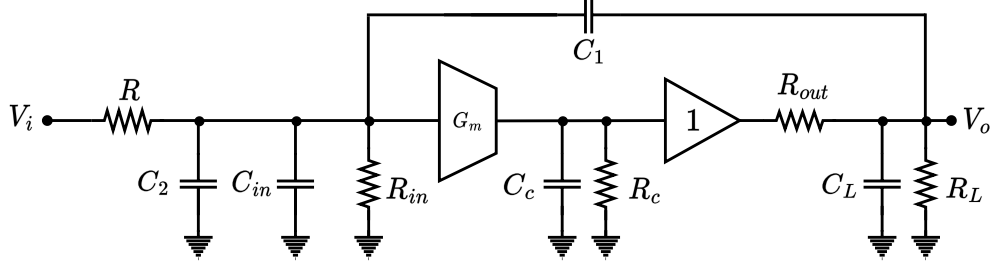


Figure 6.3. Proposed quasi-Sallen-Key architecture with non-idealities.

6.2.2 Input Impedance Effect

The amplifier's input impedance can be represented as a parallel combination of a resistance, R_{in} , and a capacitance, C_{in} . The input capacitance is effectively in parallel with C_2 , and its impact can be derived from the expressions for ω_0 and Q given in equations (6.6) and (6.7). Specifically, this effect is captured by substituting C_2 with $C'_2 = C_2 + C_{in}$. If C_2 is large enough, C_{in} becomes negligible, but otherwise, the external capacitor C_2 must be adjusted accordingly.

Similarly, the input resistance R_{in} is also in parallel with C_2 , and its influence can be accounted for by modifying sC_2 to $sC_2 + \frac{1}{R_{in}}$ in the denominator of equation (6.5). As a result, the resonance frequency and quality factor are calculated as follows:

$$\omega_0 = \omega_{0ideal} \sqrt{1 + \frac{R}{R_{in}}} = \sqrt{\frac{1}{\tau_p(C_1 + C_2)(R \parallel R_{in})}} \quad (6.8)$$

$$Q = \frac{\sqrt{\tau_p(C_1 + C_2)(R \parallel R_{in})}}{[C_1(1 - K) + C_2](R \parallel R_{in}) + \tau_p} \quad (6.9)$$

If C_{in} needs to be considered, C_2 can be replaced by C'_2 . From equations (6.8) and (6.9), it can be seen that R is effectively replaced by the parallel combination of R and R_{in} . Thus, the impact of the input resistance becomes negligible if R_{in} is much larger than R (for instance, when MOS devices are used, R_{in} approaches infinity).

6.2.3 Output Resistance Effect

One of the most significant non-idealities in an amplifier is the output resistance, R_{out} , particularly when coupled with the load impedance. For a general case, the load impedance is modeled as a parallel combination of a resistance, R_L , and a capacitance, C_L . It is essential to account for both the resistive and capacitive components since the load could simulate the effect of another bi-quad in a higher-order filter.

The analysis of the circuit in Figure 6.3, which considers the output resistance of the buffer and the load impedance, is presented in the Appendix. The output resistance introduces a third pole and two zeros to the transfer function, even when no load impedance is considered. Although these additional poles and zeros can be neglected when they occur at higher frequencies, they still affect the resonance frequency and quality factor. The resulting expressions for these parameters are:

$$\omega_0 \approx \omega_{ideal} \left(1 - \frac{R_{out} \parallel R_L}{2} \lambda_\omega \right) \quad (6.10)$$

where

$$\lambda_\omega = \frac{C_L}{\tau_p} + \frac{C_1 C_2}{\tau_p (C_1 + C_2)} + \frac{C_1 + C_L}{R(C_1 + C_2)} \quad (6.11)$$

and

$$Q \approx Q_{ideal} \left[1 + (R_{out} \parallel R_L) \left(\frac{\lambda_\omega}{2} - \omega_{ideal} Q_{ideal} \lambda_Q \right) \right] \quad (6.12)$$

where

$$\lambda_Q \approx \frac{C_1 C_2}{C_1 + C_2} + C_1 \left(1 + K \frac{R}{R_L} \right) \quad (6.13)$$

From equations (6.10) and (6.12), it is possible to infer that a specific limit must be set on the output resistance to minimize deviation from the ideal values of ω_0 and Q . Additionally, a resistive load helps in relaxing this limit.

6.3 Design of a fully differential bi-quad

In order to validate the functionality of the proposed architecture a bi-quad with a resonance frequency of 12GHz, a quality factor $Q=1.9$ and a dc gain $K=1.6$ has been designed. The design has been realized in a commercial SiGe BiCMOS technology by STMicroelectronics [23] that provides bipolar devices with a maximum f_T of 320GHz. A degenerated differential pair was used as amplifier block, so that its gain K is determined by the ratio of load resistance R_c and degeneration resistance R_e .

The passive components (R , C_1 and C_2) and of the amplifier time constant τ_p have been selected to meet the specifications of resonance frequency and quality factor according to equations (6.6) and (6.7). Table 6.1 reports the selected values, where $f_p=1/2\pi\tau_p$ is the amplifier bandwidth.

Table 6.1. Design values of the bi-quad.

Parameter	Value	Unit
K	1.6	[V/V]
C_1	125	[fF]
C_2	42	[fF]
R	101	[Ω]
f_p	15.6	[GHz]

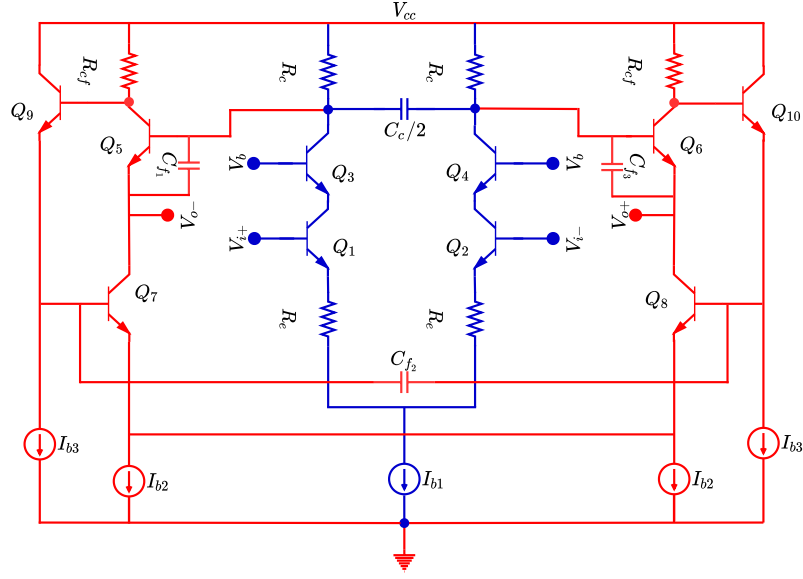


Figure 6.4. Schematic of the amplifier: gain stage (blue) and output buffer (red). Current generators are implemented with high-voltage NPN devices.

6.3.1 Gain stage

The amplifier stage has been implemented as a degenerated differential pair, since it results in a high input resistance and low input capacitance, thanks to the local feedback, moreover the gain can be set as the ratio of two resistors, desensitizing it from process variations. The detailed amplifier circuit, illustrated in blue in Figure 6.4, utilizes separate degeneration resistors instead of a single one across the emitters. This design choice allows for the use of a single tail current source, which helps in reducing noise. To enhance isolation between the input and output ports, transistors are cascoded. This configuration also minimizes the input capacitance and limits the collector-emitter voltage of the transistors, preventing potential breakdowns.

A bias current of 2.7mA is applied, and the sizing of the devices, as presented in Table 6.2, has been selected to optimize both noise performance and linearity. As a result, the input resistance is approximately $300\text{k}\Omega$, with an input capacitance of 2fF . The amplifier operates at a supply voltage of 2.7V , and the load resistor R_C is chosen to set the DC output voltage at 2.5V . This configuration allows for common-mode input and output voltages of 1.4V within the overall active circuit. The desired gain K is used to determine the degeneration resistor R_E . After selecting the load resistance, the capacitance C_c can be determined from the frequency f_p , as provided in Table 6.1.

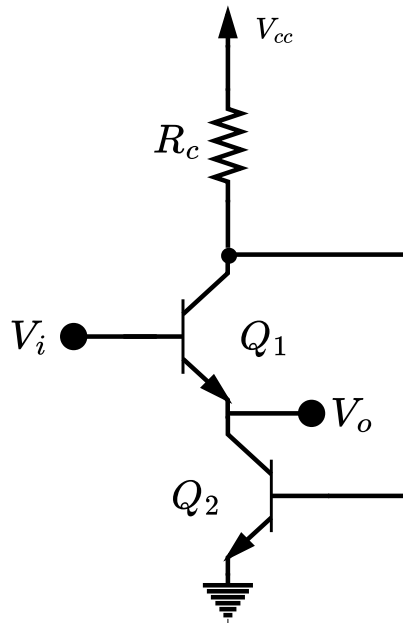
6.3.2 Output stage

Since the amplifier has to provide an extremely high current while ensuring very low output impedance a simple emitter follower, that provides an output resistance $1/g_m$, is not enough. For this reason, a FVF (Flipped Voltage Follower) topology is selected for the output buffer, to reduce the output impedance exploiting the

Table 6.2. Sizing of the amplifier gain stage. Emitter length and width are reported for the transistors.

Parameter	Value	Unit
R_c	320	$[\Omega]$
R_e	200	$[\Omega]$
C_c	17.4	$[fF]$
I_{b1}	2.7	$[mA]$
V_b	2.4	$[V]$
$Q_{1,2,3,4}$	1.8/0.2	$[\mu m]$
Q_{tail}	5.56/0.2	$[\mu m]$

internal feedback. Figure 6.5 shows the basic topology of the FVF, whose analysis provides an output resistance that is approximately $1/(g_m^2 R_c)$.

**Figure 6.5.** Basic flipped voltage follower topology.

Using an FVF in bipolar technology, especially when incorporating high-speed devices with low breakdown voltages in the signal path, can lead to potential biasing issues. Referring to Figure 6.5, it may be necessary to insert a level shifter between the collector of Q_1 and the base of Q_2 to ensure that the devices are biased with a collector-emitter voltage that maintains good linearity. However, the base voltage of Q_2 directly influences the bias current in the FVF, imposing limitations on the allowable voltages applied to the gate and drain of Q_1 .

This issue can be resolved by considering that the design includes a differential output stage, where some nodes are grounded only for differential-mode signals. A new differential FVF topology is proposed, in which the common-emitter stage Q_2 in the feedback loop is replaced by a differential pair. This modification effectively decouples the DC operating points from the signal path, enhancing performance.

The resulting topology is highlighted in red in Figure 6.4.

The FVF design aims to achieve an output resistance R_{out} that ensures a relative error in the resonance frequency of less than 15%. Using the equations (6.10)-(6.11) for a capacitive load C_L of 10fF and the component values from Table 6.1, the maximum allowable output resistance is determined to be 25Ω . This value has been validated using simulations that include the actual implementation of the output stage. Figure 6.6 illustrates the variation of f_0 and Q as a function of R_{out} . Simulation results reveal that additional factors, beyond output resistance, influence f_0 and Q , with a resonance frequency of $11.2GHz$ and a quality factor exceeding 2.2 even for zero output resistance. These discrepancies are mainly due to the un-modeled poles and zeros in the output stage. Therefore, simulations show that an output resistance of 15Ω achieves an error in the resonance frequency below 15%, corresponding to $f_0 = 10.47GHz$. To account for process variations and larger load capacitances, a more conservative final value of 13Ω is chosen for the output resistance.

The output resistance of the FVF is influenced by the bias current I_{b2} in the output transistors Q_5 and Q_6 and the loop gain, which depends on the resistor R_{cf} . The level shifter primarily affects the frequency response of the FVF. The design has been optimized with stability considerations in mind, resulting in the device sizing presented in Table 6.3, which yields an output resistance of 10Ω .

Table 6.3. Sizing of the amplifier output stage. Emitter length and width are reported for the transistors.

Parameter	Value	Unit
R_{cf}	320	$[\Omega]$
C_{1f}	89	$[fF]$
C_{2f}, C_{3f}	73	$[fF]$
I_{b2}	0.9	$[mA]$
I_{b3}	0.7	$[mA]$
$Q_{5,6,9,10,b2,b3}$	2/0.2	$[\mu m]$
$Q_{l7,8}$	4/0.2	$[\mu m]$

6.3.3 Layout design

The layout of the bi-quad is shown in Figure 6.7, where key components such as the gain stage, output stage, and external passive elements (R , C_1 , and C_2) are highlighted. The design prioritizes a fully symmetrical structure, with short interconnections and minimized coupling between signal traces to reduce parasitic effects. The total area occupied by the layout is $2843\mu m^2$. Additionally, the values of C_2 and C_c previously specified have been adjusted to account for the parasitic capacitance introduced by the layout.

6.4 Simulation results

The designed bi-quad has been post-layout simulated to evaluate its performances and demonstrate the robustness to PVT variations and mismatches. There is a good

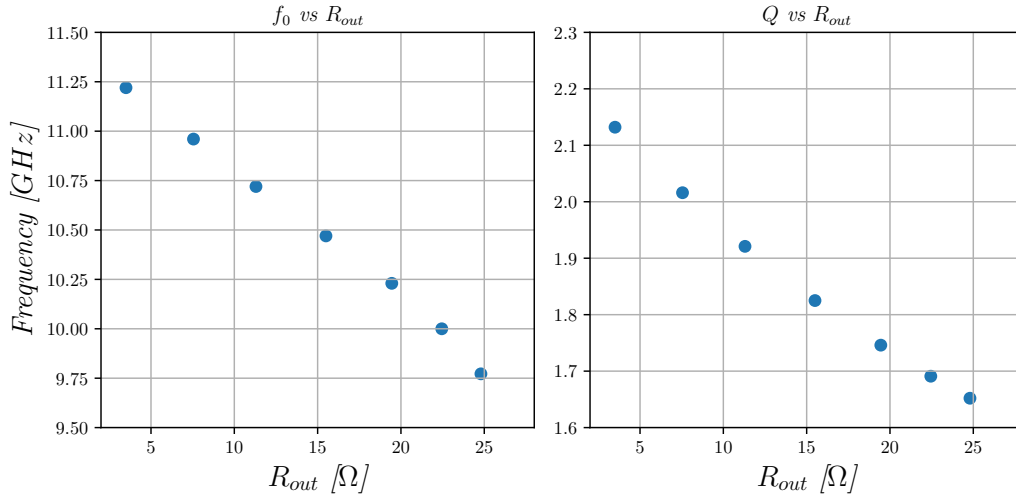


Figure 6.6. Effect of the output resistance on f_0 and Q .

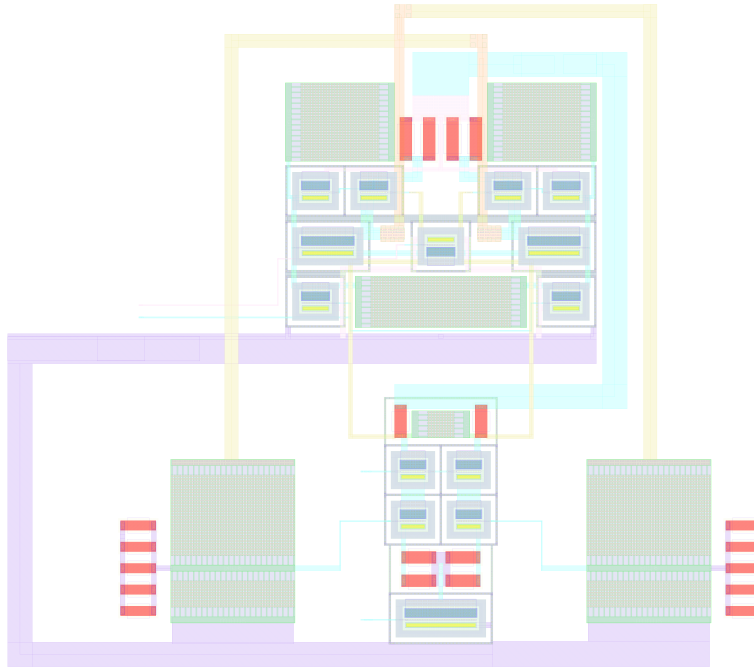


Figure 6.7. Layout of the proposed bi-quad.

agreement between pre and post layout simulation, therefore post-layout simulation results are reported in this section.

6.4.1 Simulated typical performance

Figure 6.8 shows the frequency response of the bi-quad. DC gain is 3.8dB, and the peak of 10.44dB at 10.47GHz is used to calculate a the quality factor that is $Q=2.15$.

For higher frequencies, the gain drops at 40dB/decade for about two octaves, then the zeros and poles of the FVF reduce the slope to 20dB/decade.

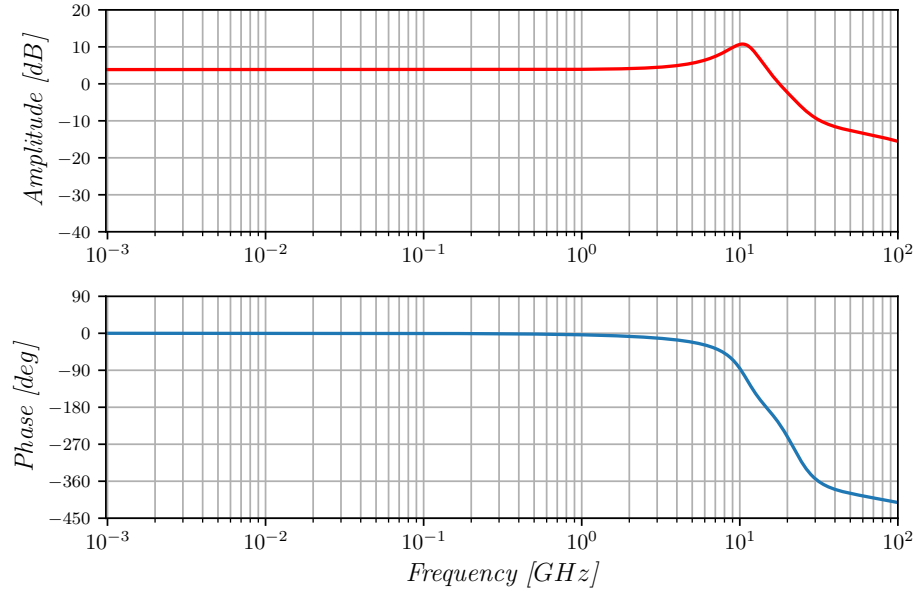


Figure 6.8. Frequency response of the filter.

In the Table 6.4 there is a comparison between the achieved values of resonance frequency and quality factor evaluated through the simulation with the theoretical ones provided by equations (6.6) and (6.7), showing an error of about 15%. This is justified by the effects of input and output resistances discussed in Section 3, and by the effect of poles and zeros of the FVF. In particular, poles and zeros of the FVF are the cause of a Q higher than the ideal one, despite equation (6.12) would predict a reduction of the quality factor.

Table 6.4. Comparison of the values of f_0 and Q with the theoretical ones.

	f_0 [GHz]	Q
Analytical Value	12	1.9
Post-Layout Simulation Value	10.47	2.15
Precision [%]	87	88

Moreover, as shown in figures 6.9, 6.10 and 6.11, there is consistency between analytical and simulated trends of f_0 and Q with respect to R , C_1 and C_2 .

The filter has also been characterized in terms of noise and distortions, to evaluate its dynamic range. Figure 6.12 shows the input-referred noise spectrum of the bi-quad, that shows a white noise floor of about $-166.8 \text{ dBV}/\sqrt{\text{Hz}}$ and a noise corner frequency of 1 MHz.

Figure 6.14 presents the signal-to-distortion ratio (SDR), defined as the inverse of the total harmonic distortion ($\text{SDR} = -\text{THD}$ in dB), plotted against the input amplitude for a 500 MHz input signal. As depicted in Figure 6.13, the distortion is primarily driven by the third harmonic, even at lower frequencies, where

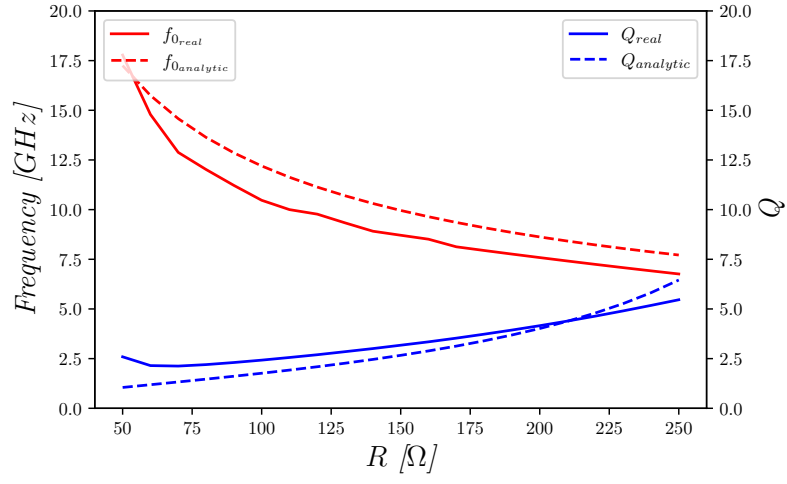


Figure 6.9. Trend of f_0 and Q vs R .

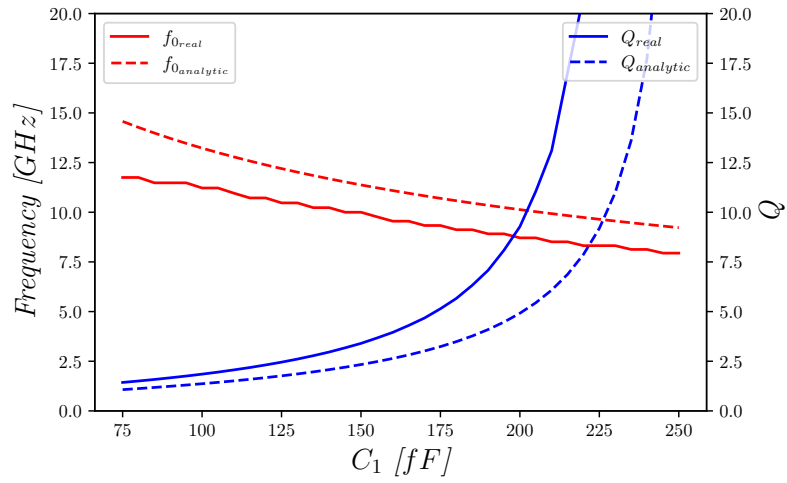


Figure 6.10. Trend of f_0 and Q vs C_1 .

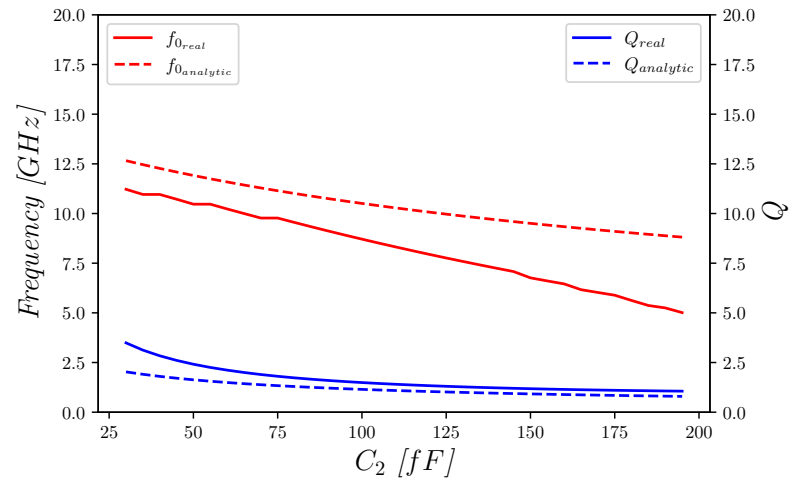


Figure 6.11. Trend of f_0 and Q vs C_2 .

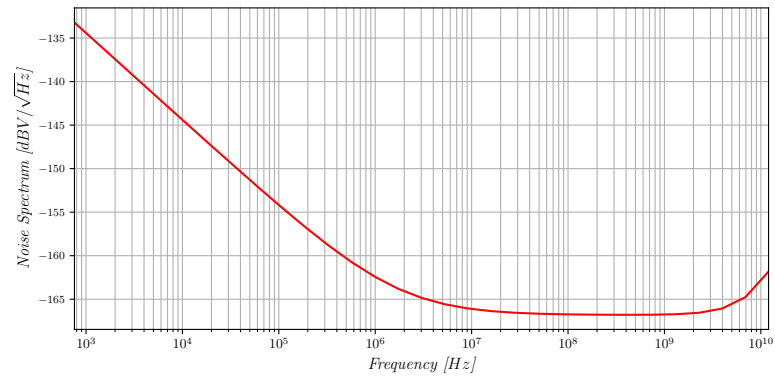


Figure 6.12. Equivalent output noise spectrum.

several harmonic components remain within the filter's bandwidth. As expected, THD increases with larger input amplitudes, while the signal-to-noise ratio (SNR) improves with higher signal levels. This leads to an optimal input amplitude that maximizes the signal-to-noise-and-distortion ratio ($SNDR$), which is used to determine the filter's maximum dynamic range (DR) [19]. Specifically, it has been shown [19] that the maximum dynamic range occurs when the SDR equals twice the SNR ($SDR = SNR + 3$ dB). For the filter in question, this point is reached with an input amplitude of approximately 640 mVpp, corresponding to an SNR of 47.8 dB. The maximum $SNDR$ is then calculated to be 46.13 dB.

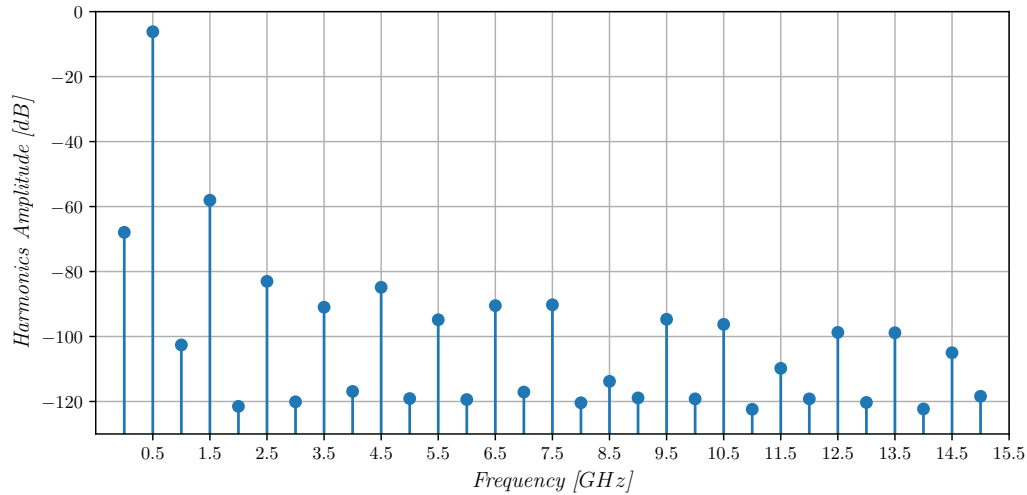


Figure 6.13. FFT of the output signal

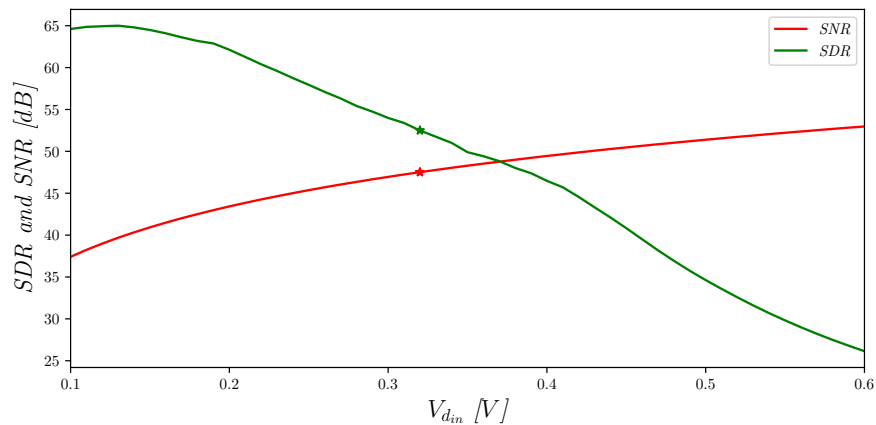


Figure 6.14. SDR and SNR vs differential input amplitude at 500MHz. The optimal input amplitude is highlighted.

Filter has been tested in nominal condition (27°C, nominal supply voltage of 2.7V) the results are synthesized in Table 6.5; THD and SNR are calculated for a 500MHz input signal of 640mVpp amplitude.

Table 6.5. Filter performance in nominal conditions (Typical corner, 27°C, nominal supply); post-layout simulation results.

Name	Value	Unit	Notes
f_0	10.47	GHz	Resonance frequency
Q	2.15		Quality factor
f_{3dB}	17.1	GHz	3dB cutoff frequency
K	1.55 (3.8)	dB	DC gain
A_p	3.33 (10.44)	dB	Peak gain
P_{diss}	15.89	mW	Average power consumption
V_{ocm}	1.38	V	DC common-mode output voltage
V_{opp}	620	mV	Peak-to-peak differential input voltage
SNR	47.89	dB	Signal-to-noise ratio
THD	-51.74	dB	Total harmonic distortion

6.4.2 Sensitivity to mismatches and PVT variations

To evaluate the effect of the mismatch Monte Carlo simulations have been performed on the filter; the results of 500 Monte Carlo mismatch post-layout simulations are reported in table 6.6. Mismatch variations do not heavily affects both f_0 and Q . In particular, Q has the worst standard deviation to average ratio (which is less than 4% anyway) due to the fact that it is proportional to a ratio between capacitance values and therefore suffers much more the effect of mismatch variations.

Table 6.6. Results of post-layout Monte-Carlo mismatch simulations at 27°C.

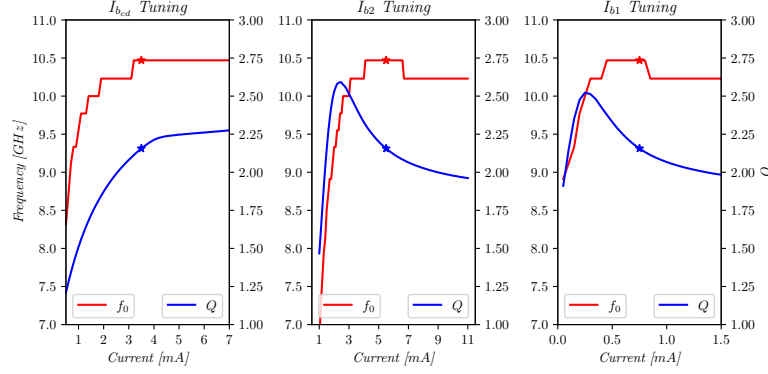
Name	Min	Max	μ	σ	Unit
f_0	10.23	10.72	10.4	0.116	GHz
Q	1.983	2.417	2.159	0.083	
f_{3dB}	16.53	17.66	17.1	0.19	GHz
K	1.47	1.631	1.544	0.028	
V_{ocm}	1.354	1.415	1.383	0.011	V

Table 6.7 presents the results from process corners simulations. As anticipated, the bi-quad demonstrates low sensitivity to the active components (with the corners Bmin, Bmax, Imin, and Imax reflecting the variations in β and the saturation current of the bipolar devices). This behavior is expected, as the filter's parameters are primarily governed by the passive elements. Consequently, the resonance frequency f_0 and quality factor Q exhibit sensitivity to variations in these passive components. Adjustments to the circuit's bias currents can mitigate changes in the quality factor Q , as depicted in Figure 6.15. However, the same figure indicates that compensation for resonance frequency variations is only feasible when f_0 needs to be reduced. As a result, the corners C_{max} and R_{max} pose the most significant challenges for the filter. This issue is common to any filter relying on passive components to define its transfer function, and various solutions have been proposed in the literature, including varactor-based tuning or resistive tuning using digital switches.

Finally, figure 6.16 shows supply voltage and temperature cross-corners simulation results: in each cell of the map, the percentage variation is shown for f_0 , Q and f_{3db}

Table 6.7. Process corners simulation results at 27°C.

Name	TYP	B_{max}	B_{min}	I_{max}	I_{min}	C_{max}	C_{min}	R_{max}	R_{min}	Unit
f_0	10.47	10.47	10.23	10.47	10.23	9.55	11.48	8.91	12.3	GHz
f_{3dB}	17.1	17.37	16.84	17.36	16.95	15.31	19.22	14.71	18.84	GHz
Q	2.15	2.18	2.06	2.17	2.08	2.17	2.04	2.10	2.17	

**Figure 6.15.** Effect of varying bias currents on f_0 and Q .

for the corresponding temperature and supply voltage variation.

6.4.3 Comparison with the literature

The performances of the proposed filter have been compared with other multi-GHz low-pass filters from the literature, with a special attention to inductor-less implementations. To allow a fair comparison, the following figures of merit (FOMs) commonly used to characterize filters [19] have been calculated:

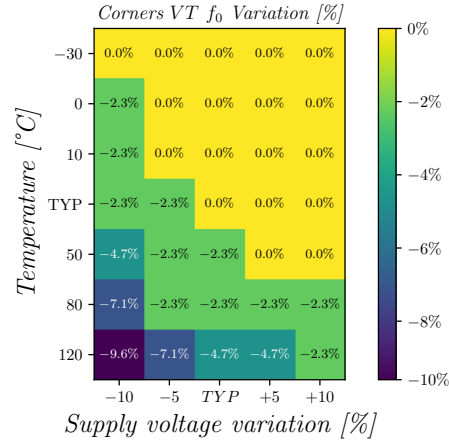
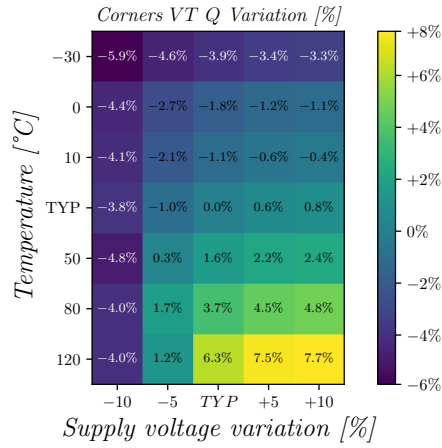
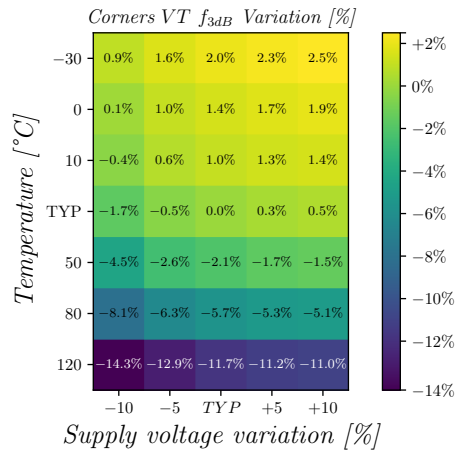
$$FOM_1 = \frac{P_{diss}}{N_{poles}} \quad (6.14)$$

$$FOM_2 = \frac{FOM_1}{f_{3dB}} \quad (6.15)$$

$$FOM_3 = \frac{FOM_2}{DR_{lin}} \quad (6.16)$$

In these formulas, N_{poles} represents the filter's order, P_{diss} refers to the power consumption, and DR_{lin} is the dynamic range expressed in linear scale. The figure of merit (FOM) in equation (6.14) evaluates the power dissipation per pole, while FOM (6.15) normalizes this value by the cutoff frequency. Since dynamic range is crucial for practical filter applications, FOM (6.16) also incorporates this factor by dividing FOM_2 by $DR_{lin} = 10^{DR/10}$.

The comparison highlights that the proposed filter delivers strong performance in terms of both FOM_1 and FOM_2 . Regarding the latter, which includes bandwidth considerations, only [142]—with a 3-dB bandwidth below 5 GHz—and [36]—which employs a physical inductor—show better results. Nevertheless, the proposed design offers a competitive dynamic range, with only [18] achieving superior results due to

(a) f_0 VT-corner(b) Q VT-corner(c) f_{3dB} VT-corner**Figure 6.16.** Supply voltage and temperature corner results for: a) f_0 ; b) Q ; c) f_{3dB} .

the use of a closed-loop gain stage that enhances linearity but restricts maximum frequency. This leads to an optimal FOM_3 value, as the gain stage no longer limits the maximum frequency, enabling a wider bandwidth with comparable power consumption and dynamic range.

Table 6.8. Comparison with the literature.

	[142]	[78]	[49]	[115]	[141]	[18]	[19]	[36]	This work
Technology	CMOS 180	BiCMOS 250	CMOS 65	CMOS 28	CMOS 40	BiCMOS 55	BiCMOS 55	CMOS 65	BiCMOS 55
Type	AL	GmC	GmC	GmC	TT	SK	AL	ind	QSK
V_{cc} [V]	1.8	3.5	1.4	1.1	1.1	3	3	1.2	2.7
f_{3dB} [GHz]	4.57	4.1	10	3.3	1.6	9.55	10.3	8	17.1
N_{pole}	5	5	3	5	4	2	6	2	2
Pd [mW]	1.6	100	140	30	17.6	18	43	2.64	15.75
$P_{noise_{in}}$ [dBm]	-44.8	-40.1	-56	-56	-46.8	-46.8	-45.9	-42	-50.38
SNR [dB]			45	39		46.4	44.7		47.9
THD [dB]	-56.9		-45	-40	-46	-64	-42.6		-51.7
@ $V_{in_{pp}}$ [mVpp]	100		264	126	400	800	400		640
Gain [dB]	5.2	-6.8	1.3	-1	10	-0.5	-0.2	1.5	3.8
IIP3 [dBm]		-5.5	5	-1	11		16.9	0.9	17.25
DR [dB]	33.4	21.5	42.2	36.6	41.4	49.1	41.4	22.1	46.1
Area [mm^2]			0.01	0.0912	0.12	0.0027	0.02	0.0176	0.0025
Area/pole [mm^2]			0.003	0.018	0.03	0.001	0.003	0.009	0.001
Meas./Sim.	S	M	M	M	S	S	M	S	S
FOM_1 [mW]	0.32	20.00	46.67	6.00	4.40	9.00	7.17	1.32	7.87
FOM_2 [mW/GHz]	0.07	4.88	4.67	1.82	2.75	0.94	0.70	0.17	0.46
FOM_3 [nW/GHz]	32.03	34681	270.9	400.6	194.9	11.48	50.77	1006.9	11.22

AL=active inductor; TT=Tow-Thomas; SK=Sallen-Key; Ind=physical inductor; QSK=Quasi-Sallen-Key.

6.5 Conclusions

An ideal Sallen–Key bi-quad, the gain block presents infinite bandwidth. In real implementations, the block presents at least one pole that has to be at a much higher frequency than the filter resonance frequency to not affect filter performance, and this limits the maximum frequency that can be obtained. In this paper, a novel quasi-Sallen–Key bi-quad architecture has been proposed. The gain block is used to set one of the open-loop poles of the bi-quad, so that the block is no longer a limit to scaling up the resonance frequency, and with a suitable technology, resonance frequencies in excess of 10 GHz can be achieved. A bi-quad is designed and simulated in a 320 GHz-f T BiCMOS technology to validate the approach. Post-layout simulations show a cutoff frequency of 17 GHz with low power consumption and good linearity, resulting in excellent values for the FOM. The resonance frequency and the quality factor are in suitable agreement with the theoretical values, and the error can be attributed to poles and zeros of the output buffer used to reduce the output resistance; this buffer exploits a differential implementation of the FVF to achieve low output resistance with low power consumption and suitable bias points for all the devices. Good robustness against mismatches is achieved, whereas a sensitivity to the values of the passive components setting the open-loop poles is present, as expected for the Sallen–Key architecture.

Chapter 7

Conclusion

This thesis introduced innovative topologies, designs, and techniques to enhance the performance of HS, LV, and ULV SAR ADCs.

The initial phase focused on designing a 10-bit, 166 MS/s synchronous SAR ADC operating at a 1 V supply voltage, implemented in a 55 nm CMOS technology by STMicroelectronics. This ADC design took a conservative approach to ensure manufacturability and enable physical testing. This ADC uses a fully differential charge redistribution SAR architecture, featuring state-of-the-art circuit topologies. A novel MQMS scheme is proposed for the switching of the CDAC, which reduces the output common-mode swing while retaining most of the efficiency and compactness of the conventional MS CDAC. This approach decouples the CDAC output common-mode voltage from the ADC input common-mode, optimizing performance by enabling precise tuning of the CDAC output common-mode range to match the comparator's requirements.

The chosen technology imposes performance limitations, primarily due to high parasitic capacitances affecting speed and power consumption. Nevertheless, post-layout simulations report aSNDR of 56.3 dB, an average power consumption of 6.03 mW, and a Walden FOM of 68.07 fJ/conversion-step.

Subsequent research concentrated on novel designs and techniques for LV and ULV dynamic comparators, ensuring high-speed operation. Several solutions are presented, including an ultra-low-voltage latched comparator based on the Strongarm topology with body driving to achieve rail-to-rail ICMR. This design replaces conventional inverters with cross-coupled PMOS devices and eliminates the clocked tail current generator, resulting in a compact comparator with only two stacked devices. The clock signal directly controls the gates of the input transistors, facilitating efficient on/off switching and minimizing power consumption.

Operating at supply voltages as low as 0.15 V, the comparator demonstrates remarkable speed and power efficiency, with an input-referred offset of around 18 mV_{rms} comparable to other body-driven comparators. Compared to similar designs in the literature, this comparator performs exceptionally well at supply voltages up to 0.5 V, consuming 856 pW at 0.15 V and 52.5 nW at 0.3 V, with a maximum delay and operating frequency respectively of 2.2 μ s at 80 kHz and 59.27 ns at 2 MHz.

This comparator was further optimized by applying a novel clocked supply voltage technique that increases preamplification gain, thus reducing input-referred

noise and offset. Post-layout simulations, conducted in a 130 nm technology, show improved noise and offset characteristics with minimal impact on the EDP. This technique can extend to other ULV comparator designs by leveraging clocked supply voltage.

The research also presents a high-speed, low-voltage comparator based on the Strongarm architecture, utilizing body-driven configuration for maximum ICMR and a reduced device stack. Additionally, CPB dynamic biasing enhances the effective supply voltage during evaluation, improving speed without sacrificing energy efficiency. At $V_{DD} = 0.6$ V, the comparator demonstrates excellent delay performance and achieves the lowest EDP among comparable designs.

The CPB dynamic biasing technique was further explored through theoretical analysis on single-tail and pseudo-differential amplifiers, demonstrating performance improvements. These findings were validated in two 0.6 V, 28-nm CMOS dynamic comparator designs: a single-tail Strongarm comparator and a pseudo-differential version. The pseudo-differential design includes a digital-programmable capacitor array for foreground offset calibration. Post-layout simulations show both designs operate above 2 GHz, with low-voltage power supplies, achieving competitive performance relative to existing literature.

Building on this theoretical validation, the CPB technique enabled the development of an advanced ULV comparator operating at supply voltages as low as 0.25 V. Optimized for 0.4 V, this comparator reaches frequencies up to 200 MS/s. An innovative 0.4 V 8-bit ULV ADC topology was also designed, integrating this comparator and employing a novel switching scheme that minimizes the CDAC common-mode swing and decouples it from the input common-mode voltage. This ADC achieves an operating frequency of 6.67 MS/s, maintaining high noise performance and accuracy despite sub-optimal power consumption.

Finally, a novel inductor-less wide-band LPF was developed for ADC front-ends and ATI architectures. The quasi-Sallen–Key filter topology uses a bi-quad architecture inspired by the Sallen–Key design. Here, the gain block sets an open-loop pole, removing its limitation on resonance frequency scaling. With suitable technology, resonance frequencies exceeding 10 GHz are achievable. A bi-quad implemented in a 320 GHz f_T BiCMOS technology was simulated, yielding a cut-off frequency of 17 GHz, low power consumption, and good linearity, with favorable FOM values. The filter buffer leverages a differential FVF to achieve low output resistance with low power consumption and well-defined bias points across devices. The design demonstrates robustness to mismatch while maintaining sensitivity to passive component values that set open-loop poles, as typical of Sallen–Key architectures.

Appendix A

Appendix: Analog-to-Digital Converters: context and definitions

A.1 Charge redistribution SAR: CDAC

The working principle of a Charge redistribution SAR is based on the Capacitive DAC, the signal is sampled directly into the CDAC and the DAC bits are switched consequently to the comparator decision, at each conversion step. Below is a demonstration of the equation 2.24. With reference to figure A.1, C_n is the capacitor of bit b_{n-1} , its value is: $C_n = C * 2^{n-1}$.

At the end of sample phase the CDAC is the coupled from de S/H and is only connected to the high impedance input of the comparator, so it can be assumed that the charge is retained on the top plate and it is possible to apply charge conservation law of the capacitors: $Q_{tot_i} = Q_{tot_f}$.

The totale amount of charge at this point is:

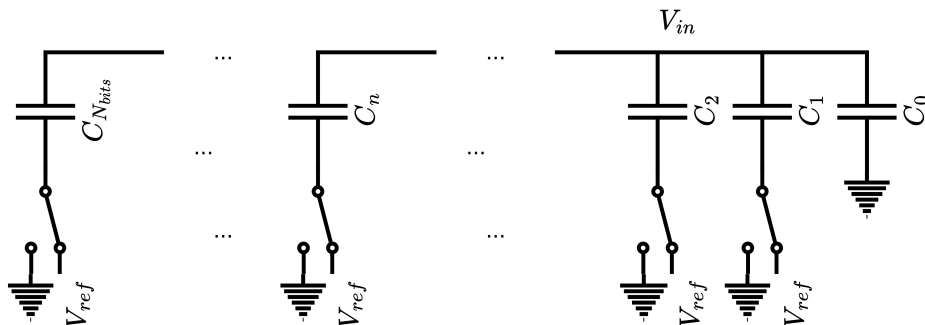


Figure A.1. conventional CDAC topology

$$Q_{tot_i} = V_i C + \sum_{i=1}^{N_{bits}} 2^{i-1} C (V_i - V_{ref}) = V_i C + \sum_{i=0}^{N_{bits}-1} 2^i C (V_i - V_{ref}) \quad (A.1)$$

$$Q_{tot_i} = V_i C + (2^{N_{bits}} - 1) C V_i - (2^{N_{bits}} - 1) C V_{ref} \quad (A.2)$$

$$Q_{tot_i} = (2^{N_{bits}}) C V_i - (2^{N_{bits}} - 1) C V_{ref} = C_{tot} V_i - (C_{tot} - C) V_{ref} \quad (A.3)$$

during the conversion phase the CDAC bottom plates of the capacitor are switched to GND or kept on V_{ref} depending on comparator output, so the total amount of charge in any point of the comparison is:

$$Q_{tot_f} = (C + \sum_{b_{GND}} C_i) V_x + (\sum_{b_{V_{ref}}} C_i) (V_x - V_{ref}) \quad (A.4)$$

where V_x is the output voltage of the DAC, that is the updated signal to be compared at each conversion step, b_{GND} are the switched-to-ground bits and $b_{V_{ref}}$ are the bits of the capacitors bottom plates kept to V_{ref}

$$Q_{tot_f} = (C + \sum_{b_{GND}} C_i + \sum_{b_{V_{ref}}} C_i) V_x - (\sum_{b_{V_{ref}}} C_i) V_{ref} \quad (A.5)$$

$$Q_{tot_f} = C_{tot} V_x - (C_{tot} - C - \sum_{b_{V_{GND}}} C_i) V_{ref} \quad (A.6)$$

equalizing the two charges expression $Q_{tot_f} = Q_{tot_i}$ it is possible to obtain:

$$C_{tot} V_x - (C_{tot} - C - \sum_{b_{V_{GND}}} C_i) V_{ref} = Q_{tot_i} = C_{tot} V_i - (C_{tot} - C) V_{ref} \quad (A.7)$$

$$C_{tot} V_x + (\sum_{b_{V_{GND}}} C_i) V_{ref} = C_{tot} V_i \quad (A.8)$$

and so:

$$V_x = V_i - \frac{(\sum_{b_{V_{GND}}} C_i) V_{ref}}{C_{tot}} \quad (A.9)$$

with explicit capacitor values:

$$V_x = V_i - \frac{\sum_{i|b_i \rightarrow GND} 2^i C}{2^{N_{bits}} C} V_{ref} \quad (A.10)$$

$$V_x = V_i - \sum_{i|b_i \rightarrow GND} \frac{1}{2^{N_{bits}-i}} V_{ref} \quad (A.11)$$

The calculation in the case where the bottom plates are initially at GND and then switch to V_{ref} is quite similar, the case in which the initial state of the switches is mixed is also similar. In general one has:

$$V_x = V_i - \sum_{i|b_i:V_{ref} \rightarrow GND} \frac{1}{2^{N_{bits}-i}} V_{ref} + \sum_{i|b_i:GND \rightarrow V_{ref}} \frac{1}{2^{N_{bits}-i}} V_{ref} \quad (A.12)$$

Appendix B

Appendix: A design of 17 GHz inductorless Quasi-Sallen Key low-pass filter

B.1 Non-idealities effect

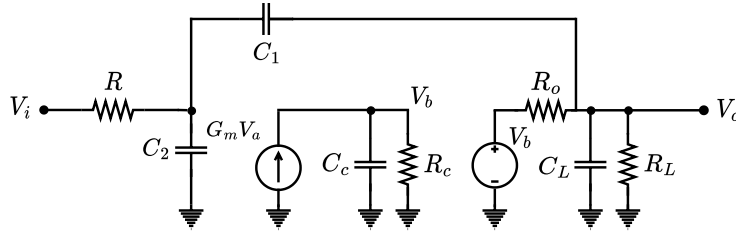


Figure B.1. Small signal schematic of the filter, with R_{out} and load.

The effect of the output resistance of the amplifier can be derived by the analysis of the circuit in figure B.1, that shows the small-signal model of the amplifier, providing a gain $K = G_m R_C$ and a pole $1/\tau_p$, and of the unity-gain output buffer with an output resistance R_{out} . A generic load impedance modeled as the parallel connection of a resistance R_L and a capacitance C_L is also considered.

The analysis of the circuit in figure B.1 provides a transfer function

$$F(s) = \frac{R_L}{R_L + R_{out}} \frac{K + sC_1 R_{out} + s^2 C_1 R_{out} \tau_p}{1 + a_1 s + a_2 s^2 + a_3 s^3} \quad (\text{B.1})$$

where:

$$\begin{aligned} a_1 &= (C_1 + C_2)R + (C_1 + C_L)(R_{out} || R_L) + \tau_p - KC_1 R \frac{R_L}{R_L + R_{out}} \\ a_2 &= R(C_1 C_2 + C_1 C_L + C_2 C_L)(R_{out} || R_L)R + \tau_p(C_1 + C_2)R + \tau_p(C_1 + C_L)(R_{out} || R_L) \\ a_3 &= \tau_p(C_1 C_2 + C_1 C_L + C_2 C_L)R(R_{out} || R_L) \end{aligned} \quad (\text{B.2})$$

with two zeros and three poles. From equation (B.1) the zeros are derived as

$$z_{1,2} = -\frac{1}{2\tau_p} \left(1 \pm \sqrt{1 - \frac{4K\tau_p}{C_2 R_{out}}} \right) \quad (\text{B.3})$$

and are complex conjugate for $R_{out} < 4K\tau_p/C_2$. We require that the modulus of the zeros is much higher than the resonance pulsation to make them negligible; by using the ideal pulsation value (6.6) we obtain the condition

$$\frac{1}{(2\tau_p)^2} \left[1 + \left(\frac{4K\tau_p}{C_2 R_{out}} - 1 \right)^2 \right] > \frac{1}{R(C_1 + C_2)\tau_p} \quad (\text{B.4})$$

hence

$$R_{out} < KR \frac{C_1}{C_2} \quad (\text{B.5})$$

From the analysis of the denominator

$$D(s) = 1 + a_1 s + a_2 s^2 + a_3 s^3 = (1 + s\tau_3) \left(1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2} \right) \quad (\text{B.6})$$

and assuming that the third pole $1/\tau_3$ is at much higher frequency than ω_0/Q , we can get the approximate expressions

$$\begin{aligned} \tau_3 &\approx \frac{a_3}{a_2} \\ \omega_0^2 &\approx \frac{1}{a_2} \\ \frac{1}{\omega_0 Q} &\approx a_1 - \frac{a_3}{a_2} \end{aligned} \quad (\text{B.7})$$

The second equation provides

$$\omega_0^2 = \frac{1}{\tau_p R(C_1 + C_2)(1 + \epsilon_\omega)} \quad (\text{B.8})$$

with

$$\epsilon_\omega = (R_{out} || R_L) \left(\frac{C_L}{\tau_p} + \frac{C_1 C_2}{\tau_p (C_1 + C_2)} + \frac{C_1 + C_L}{R(C_1 + C_2)} \right) = (R_{out} || R_L) \lambda_\omega \quad (\text{B.9})$$

that gives

$$\omega_0 \approx \omega_{0ideal} \left(1 - \frac{\lambda_\omega}{2} \right) \quad (\text{B.10})$$

By assuming a small value for R_{out} , we have

$$a_2 \approx \tau_p R(C_1 + C_2); \quad (\text{B.11})$$

the third of the (B.7) thus provides

$$\frac{1}{\omega_0 Q} = (C_1 + C_2)R + \tau_p - KC_1 R \frac{R_L}{R_L + R_{out}} + (C_1 + C_L)(R_{out} || R_L) - \chi \quad (\text{B.12})$$

where χ is:

$$\chi = \frac{\tau_p(C_1C_2 + C_1C_L + C_2C_L)R(R_{out}||R_L)}{\tau_pR(C_1 + C_2)} \quad (B.13)$$

that can be written as

$$\frac{1}{\omega_0 Q} = \frac{1}{\omega_{0ideal} Q_{ideal}} + \gamma \quad (B.14)$$

with

$$\gamma = (R_{out}||R_L) \left[\frac{KC_1R}{R_L} + C_1 + C_L - \frac{C_1C_2 + C_1C_L + C_2C_L}{C_1 + C_2} \right] = (R_{out}||R_L)\lambda_Q \quad (B.15)$$

Multiplying equation (B.14) by (B.10), neglecting second order terms and taking the reciprocal we obtain

$$Q \approx Q_{ideal} \left[1 + \left(\frac{\epsilon_\omega}{2} - \omega_{0ideal} Q_{ideal} \gamma \right) \right] \quad (B.16)$$

The approximate expression of the third pole is

$$\frac{1}{\tau_3} = \frac{\tau_p R(C_1 + C_2)}{\tau_p(C_1C_2 + C_1C_L + C_2C_L)R(R_{out}||R_L)} = \frac{1}{(R_{out}||R_L) \left(C_L + \frac{C_1C_2}{C_1 + C_2} \right)} \quad (B.17)$$

This pole has to be much higher than ω_0 to be negligible, and this poses a further condition on the output resistance.

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