A class-AB linear transconductor with enhanced linearity

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Abstract

In this paper a novel linear transconductor topology is proposed, where class-AB behavior based on adaptive biasing is exploited to improve the linear range. The adaptive biasing circuit is based on the Winner-Take-All topology already used for class-AB OTAs, and optimized to improve the linearity, and the proposed transconductor features a gain control input for tunability. The transconductor provides a gain of 43μS while consuming 70μW. The linear range (1% variation of the dc transconductance gain) is 470mVpp, about 4.5 times larger than for the corresponding class-A cell. Total harmonic distortion is improved by about 15dB, and good result in terms of linearity and noise are reported with respect to the state-of-the-art. Simulations of a Gm-C biquad filter based on the proposed transconductor are also reported to validate the design.

Keywords: linear transconductor, Gm-C filters, class-AB, low power design

1. INTRODUCTION

The Gm-cell, or linear transconductor [1], is a basic building block with applications in many analog circuits, such as Gm-C filters [2]-[3], current-mode filters [4], and variable-gain amplifiers [5]-[7]. The linearity of the Gm-cell is critical for performance, also due to its use in open-loop configurations, which cannot exploit feedback to reduce distortions. Low power consumption is also a fundamental requirement for electronic circuits, that more and more often find application in battery-operated devices, or even harvest their energy from the environment. The linear

transconductor presents a tradeoff between linearity, power consumption and dynamic range, and class-AB operation can be a key to alleviate this tradeoff. Operating the transconductor in class-AB can increase the maximum dynamic current beyond the biasing current, and can be used to linearize circuit behavior.

Several linearization techniques have been presented in the literature for linear transconductors, based on different principles: source degeneration with resistors [1] or equivalent active devices [8], cross-coupled differential pairs [9]-[10], triode-biased input devices [11]- [12], adaptive biasing [13]- [21], floating-gate devices [22]-[23], and nonlinearity cancellation techniques [24]- [27]. Sometimes two or more techniques are used together to improve linearity. Among the proposed approaches, adaptive biasing techniques are particularly interesting, since they imply class-AB behavior, also allowing a reduction of power consumption.

A number of class-AB implementations of linear transconductors has been presented in the literature and often used to realize Gm-C filters. Elwan in [14] proposed a class-AB linear transconductor that exploits class-AB buffers to apply the input signal across a resistor, which sets the transconductance gain. A similar approach has been presented by Yodtean in [19] for a very low-voltage body-driven transconductor. Lopez-Martin in [22] presented a transconductor based on a class-AB current conveyor, exploiting the quasi-floating gate technique for linearization; a Gm-C filter based on this block was presented in [23]. A transconductor that exploits adaptive biasing through feedback has been presented by Chilakapati in [16]. Several Authors [13],[15],[18],[20] have presented adaptively biased transconductors where the bias current is proportional to the squared input differential voltage, to linearize the V/I characteristic according to the quadratic law behavior of MOS devices. Sengupta in [17] proposed an adaptively biased transconductor based on a differential pair where the tail current source MOS devices are driven by a copy of the input signal. Adaptive biasing has also been used by Ibrahim in [21] in a transconductor that exploits the multi-tanh [28] principle for linearization. Different approaches to class-AB transconductors have also been proposed: Laguna in [29] presented a transconductor based on the class-AB topology by Peluso [30]-

[31], and Galan in [32] exploited the class-AB input stage by Ramirez-Angulo [33] to implement a linear multiplier-based transconductor.

In this paper a class-AB Gm-cell topology is proposed that exploits an adaptive bias circuit to generate bias currents that increase with the differential input voltage. The class-AB behavior is optimized to improve the linearity of the Gm-cell, resulting in a 15-dB lower total harmonic distortion (THD) with respect to the basic degenerated differential pair transconductor, and interesting results with respect to the state of the art. The paper is structured as follows: the proposed topology is presented and analyzed in Section 2. Simulation results of the transconductor are reported in Section 3, and Section 4 presents the application of the circuit in a Gm-C biquad filter. Section 5 concludes.

2. PROPOSED LINEAR TRANSCONDUCTOR

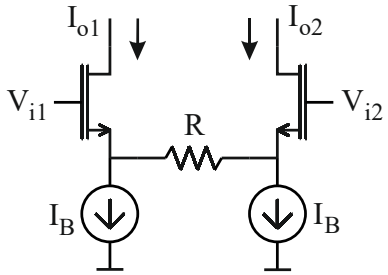

Figure 1. Transconductor based on a degenerated differential pair.

The differential pair represents the simplest form of transconductor. Its linearity is however limited, and a better transconductor can be obtained by exploiting resistive source degeneration, as shown in Figure 1. In a first-order analysis, MOS devices can be seen as ideal buffers, so that the differential input signal $V_{id} = V_{i1} - V_{i2}$ is applied across the degeneration resistor. The output current can therefore be expressed as

$$I_{o1} = -I_{o2} = V_{id}/R \tag{1}$$

showing that the degeneration resistor sets the transconductance gain $G_m = I_{o1}/V_{id}$. A more detailed analysis however has to take into account the fact that the gate-source voltages V_{GS} of the MOS devices depend nonlinearly on their current, thus the output current has to be expressed as

$$I_{o1} = \frac{V_{id} - \left(V_{GS1} - V_{GS2}\right)}{R} \tag{2}$$

where the term between the parentheses is the main source of nonlinear distortion of the transconductor. When plotting the transconductance gain (i.e., the derivative of (2)) with respect to V_{id}, a bell-like shape is obtained, showing the nonlinear behavior of the circuit.

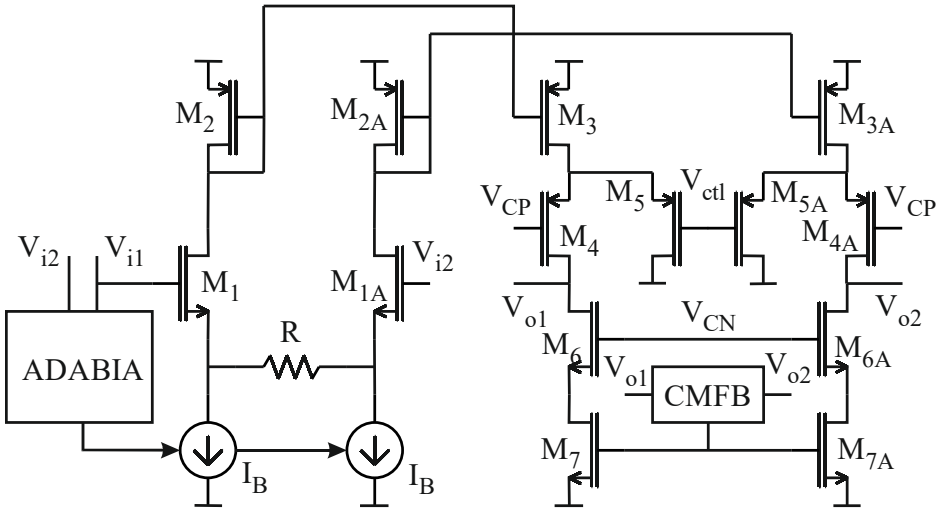

Figure 2. Proposed linear transconductor.

Furthermore, the analysis of the circuit in Figure 1 shows that the bias current I_B limits the maximum output current of the transconductor. The limit is reached when one of the transistors cuts off, and the other carries a current $2I_B$: in case of large transconductance gains (i.e., small values of the resistor R), this effect could also set the limit to the maximum allowable input swing.

A tradeoff therefore results between power consumption, input and output swings, transconductance gain and nonlinearity. Class-AB operation through adaptive biasing can help overcoming this tradeoff, by making the current I_B variable, depending on some even-symmetric function of the differential input voltage, so that a higher current is available when a large input signal is applied.

Based on these considerations, the proposed transconductor (Figure 2) exploits an adaptive biasing block to make the current I_B dependent on the differential input voltage. To achieve high output impedance while allowing a low supply voltage, the output currents of the differential pair are

mirrored to a cascode output stage, and a common-mode feedback loop (CMFB) is used to set the output voltage.

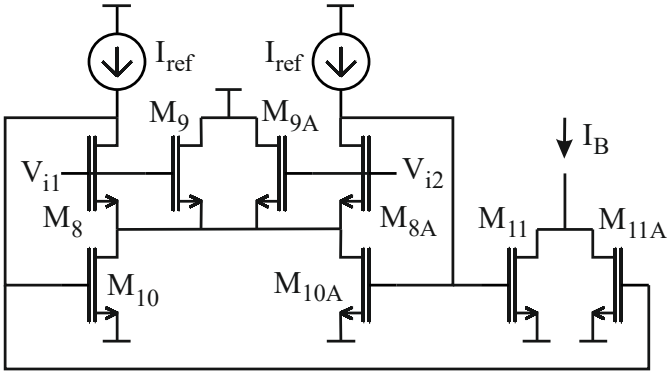

Figure 3. Proposed adaptive bias block (ADABIA).

When considering the standard quadratic-law MOS model, it can be shown analytically that a bias current that increases with the squared differential input allows linearizing the transconductor, providing a transconductance gain that is constant with respect to the input voltage. However, deep submicron devices cannot be described by this model, thus making the quadratic control law of the adaptive bias inadequate for linearization. In general terms, it has to be noted that the increase of the tail current with the input voltage has to be tailored to avoid overcompensation and achieve a transconductance gain with a relatively constant behavior in the desired range of the input voltage. Having a bias current that increases too much with the input signal does not linearize the circuit, but results in a novel source of distortion.

The proposed adaptive bias block (ADABIA) is shown in Figure 3: it is based on the topology of the flipped voltage follower (FVF) [34]- [35], and inspired by the Winner-Take-All (WTA) input stage topology proposed in [36]. In the WTA topology in [36], the common source node of M_8 and M_{8A} follows the lowest[1] of the input signals V_{i1}, V_{i2}, and this was exploited to make the common mode current flowing into M_9 and M_{9A} increase with the input signal. With reference to the circuit in Figure 3, the currents I_{ref} in M_8, M_{8A} and the currents in M_9, M_{9A} flow into M_{10} and M_{10A}. The

[1] In the complementary version based on PMOS devices presented in [36], the source node follows the highest input, hence the WTA name.

feedback paths due to the FVF adjust the gate voltages of M_{10} and M_{10A}, resulting in one of the currents much higher than the other, and an overall current higher than the quiescent current. To allow low voltage operation, we exploit this topology by mirroring the currents in the source generators M_{10} and M_{10A} as the bias current I_B of the transconductor (or, more in general, by using the gate voltages to drive the current sources M_{11}, M_{11A}): the sum of these currents is used to achieve the required even symmetry.

The shape of the transcharacteristic V_{id}-I_B depends on the sizing of the devices, and in particular of M_9 and M_{9A}: the larger those transistors, the faster the current increases with the absolute value of the input signal, since the current flowing in M_{10}, M_{10A} results more dependent on V_{id}. Figure 4 shows the curves for the current I_B and the gate voltage for different ratios of the widths of M_9 and M_8. We have optimized the design of the ADABIA block with the goal of maximizing the linearity of the transconductor, i.e., the input signal range where the transconductance gain remains approximately constant. The best performance is achieved when M_9 and M_{9A} are not used: in this case, the current I_B remains approximately constant for small input voltages, then increases abruptly when one of the gate voltages saturates to V_{DD}. The overall transcharacteristic V_{id}-I_B is also affected by the sizing of M_8, M_{8A}, as shown in Figure 5, since this determines the behavior of the FVF.

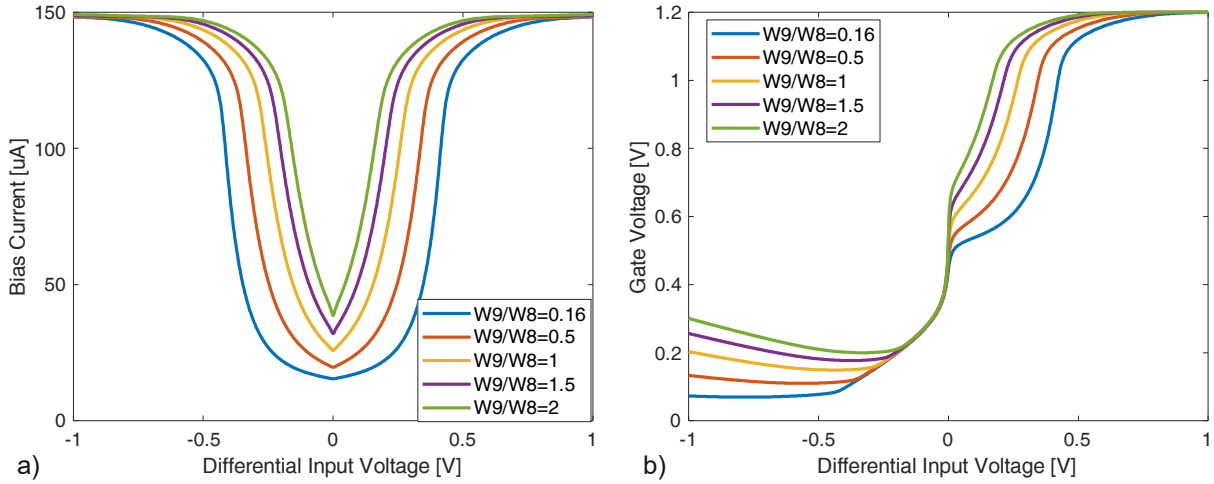

Figure 4. Bias current I_B (a) and gate voltage of M_{10A} (b) vs. differential input voltage, for different ratios of gate widths of M_9 and M_8.

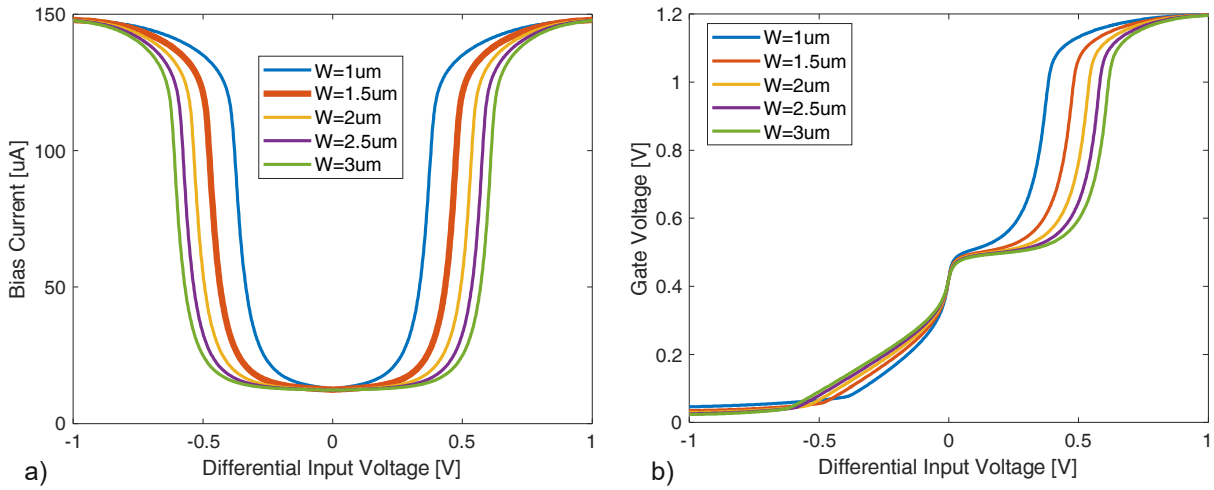

Figure 5. Bias current I_B (a) and gate voltage of M_{10A} (b) vs. differential input voltage, for different widths of M_8, in absence of M_9. The thickest curve corresponds to the effective design,

The resulting characteristic of the adaptive biasing block is highlighted in Figure 5a. The current of the ADABIA block has been scaled with respect to the transconductor to minimize power consumption, and the size of the transistors has been optimized to allow the ADABIA block to operate over all the signal bandwidth, thus allowing class-AB behavior. The dynamic bias current I_B has in fact to follow the input signal, to allow improving the linearity of the transconductor over the whole bandwidth.

The transconductor has been made tunable by adding M_5 and M_{5A} to the output stage: they divert a fraction of the current from the output, reducing the transconductance gain from the value set by the degeneration resistor, and by the current mirror gain (that in this case is unitary). M_5 and M_{5A} form differential pairs with the PMOS cascode devices of the output stage, and for $V_{ctl} = V_{CP}$ the gain is halved.

The adaptive biasing approach makes the common mode current of the transconductor dependent on the input signal: this requires for the CMFB in Figure 2 a large enough bandwidth to follow these variations. The CMFB amplifier has been implemented exploiting the differential-difference amplifier (DDA) approach, as shown in Figure 6. This avoids the reduction of the output

impedance of the transconductor, and the diode loads provide a low impedance node to achieve adequate bandwidth.

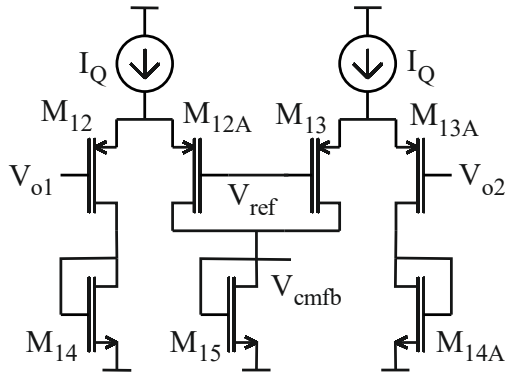

Figure 6. Schematic of the CMFB block.

3. CIRCUIT SIMULATIONS

The transconductor has been designed and simulated using the 130nm CMOS technology by STMicroelectronics, to operate in the hundreds of kHz range; large devices have been used to minimize noise and optimize matching. The supply voltage is 1.2V. Table 1 reports the size of all the devices, with reference to Figure 2, Figure 3 and Figure 6. A 15 kΩ polysilicon degeneration resistor is used. To highlight the advantages of the proposed topology, a transconductor based on a degenerated differential pair with constant biasing has also been designed for comparison.

Table 1. Device dimensions.

Devices	**W (μm)**	**L (μm)**
M_1, M_{1A}	24	0.6
M_2, M_{2A}, M_3, M_{3A}	72	1
M_4, M_{4A}, M_5, M_{5A}	36	0.8
M_6, M_{6A}	9	1
M_7, M_{7A}	18	1
M_8, M_{8A}	1.5	3

M_9, M_{9A}	--	--
M_{10}, M_{10A}	2.5	2.5
M_{11}, M_{11A}	5	2.5
M_{12}, M_{12A}, M_{13}, M_{13A}	6.645	0.39
M_{14}, M_{14A}	0.95	1
M_{15}	1.9	1

Figure 7 shows the input voltage-output current characteristic of the proposed and reference transconductors: the proposed transconductor shows a higher peak output current and a wider linear range. However, the adaptive biasing approach has been optimized to improve linearity over the same linear range of the class-A transconductor, i.e., 500mVpp differential input.

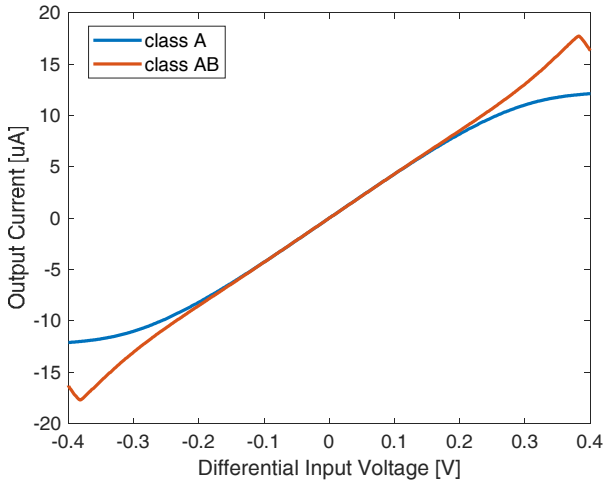

Figure 7. Voltage-current characteristic of the proposed linear transconductor.

Figure 8 shows the transconductance gain versus input voltage for different values of the control voltage V_{ctl}; the gain of the reference class-A transconductor is also reported. The curves show both the linear range of the transconductor and its tunability. The transconductance gain presents a maximum value of 43 µS; the gain varies of 3.9% for a 500mVpp differential input. The variation of the transconductance gain of the class-A transconductor over the same range is 28.9%, thus

highlighting the improved linearity. For the class-AB transconductor, the optimization of the ADABIA characteristic allows a gain curve that is almost flat over a wide range of the input signal, by increasing the bias current when the transconductance drops, and this results in lower distortion.

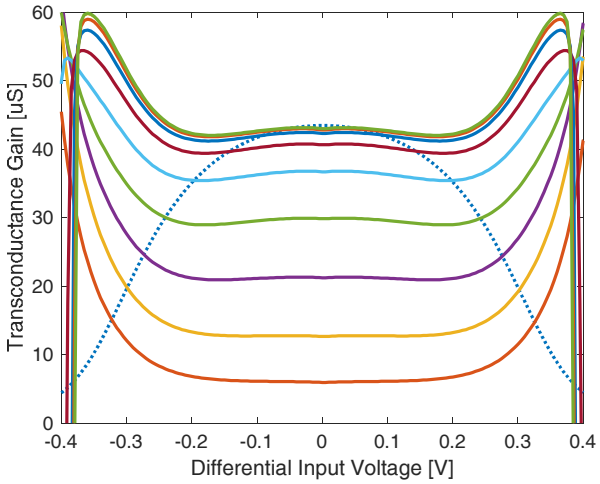

Figure 8. Transconductance gain vs. differential input voltage, for control voltage V_{ctl} ranging from 0.5 to 1V. The dotted curve is the transconductance gain for the class-A case.

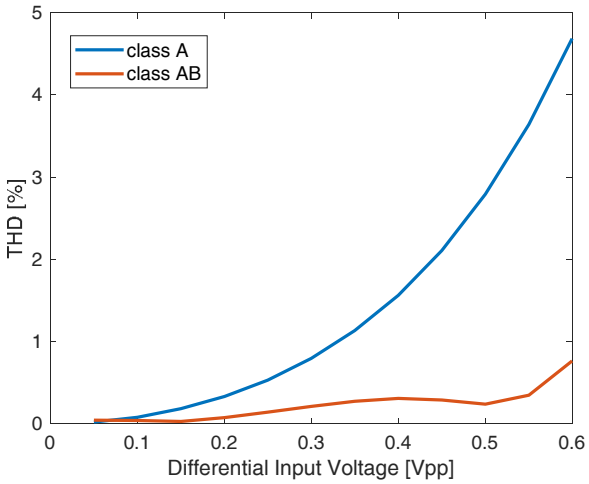

Figure 9. Total Harmonic Distortion (THD) vs. input amplitude for a 10kHz signal.

Figure 9 and Figure 10 compare the linearity performance of the proposed transconductor with the reference one: total harmonic distortion (THD) is much better for the class-AB cell, remaining below 0.3% (50 dB) up to 500mV differential input, and is however lower than that of the class-A

also for higher input voltages. This advantage is confirmed for input signals up to 5MHz, where the frequency limitations of the ADABIA block and of the CMFB become significant.

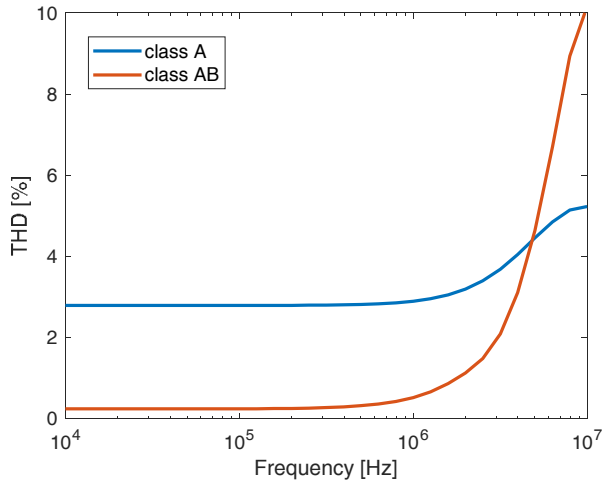

Figure 10. Total Harmonic Distortion (THD) vs. frequency for a 500mVpp differential signal.

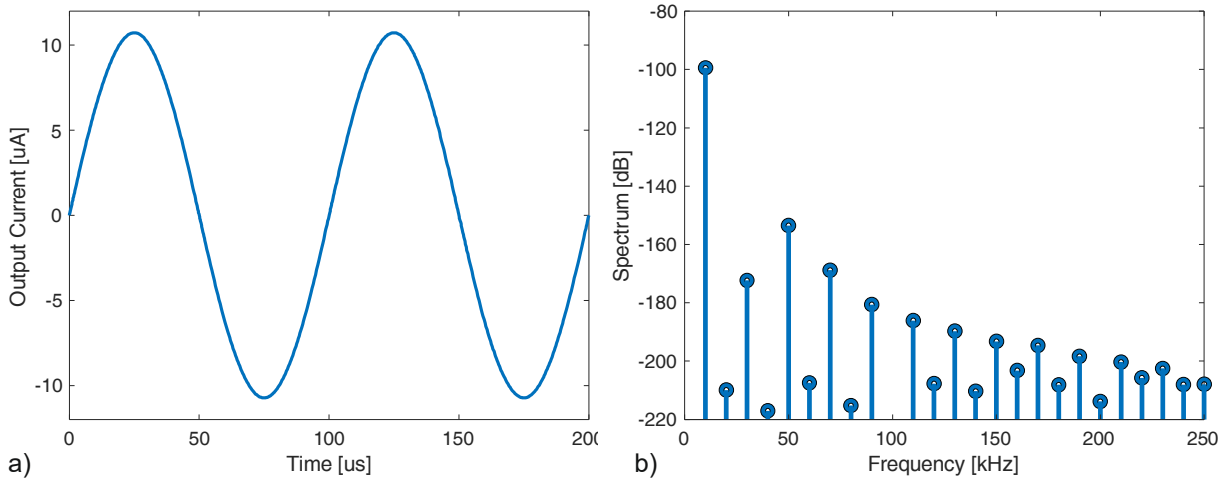

Figure 11. Output current waveform for a 10kHz 500mVpp input (1Ω differential load) (a) and relative spectrum (b).

Figure 11 shows an example output waveform for a 10kHz 500mVpp input signal on a 1Ω differential load resistor, highlighting the linearity of the circuit.

Figure 12a shows the tuning curve of the proposed transconductor, plotting the transconductance gain vs. the control voltage V_{ctl}. Ideally the transconductance gain could be reduced to zero, by diverting all the current to the idle path. However, Figure 12b, reporting the distortion for

a 10kHz 500mVpp differential input versus the control voltage, shows that the linearity drops for low control voltages, when the gain is reduced, and the minimum transconductance gain to guarantee good linearity over the 500mVpp input range is 12.6 µS, corresponding to V_{ctl}=0.55V.

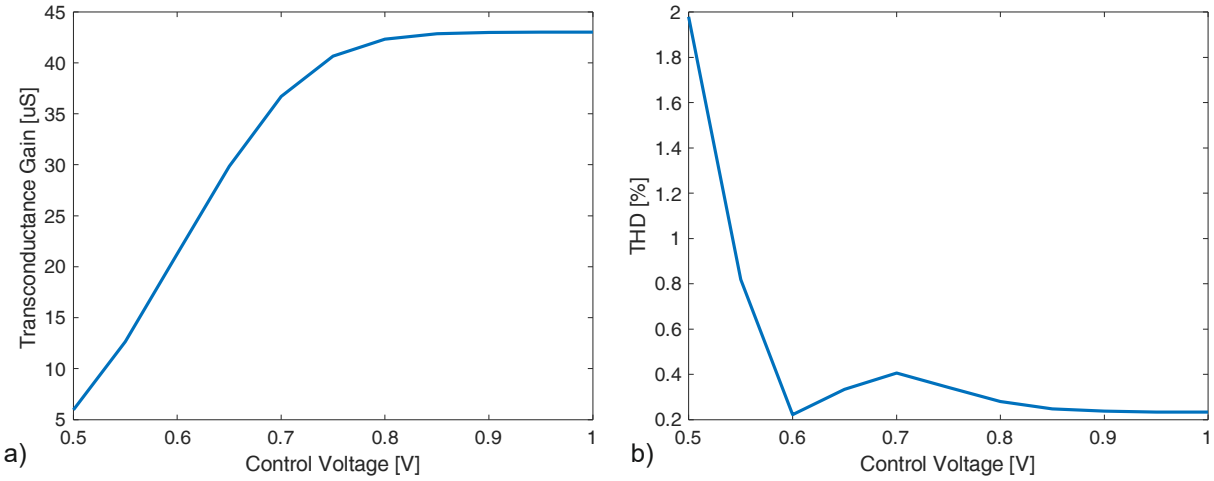

Figure 12. Tuning of the transconductance gain (a) and Total Harmonic Distortion (THD) vs. control voltage Vctl for a 10kHz 500mVpp differential input signal (b).

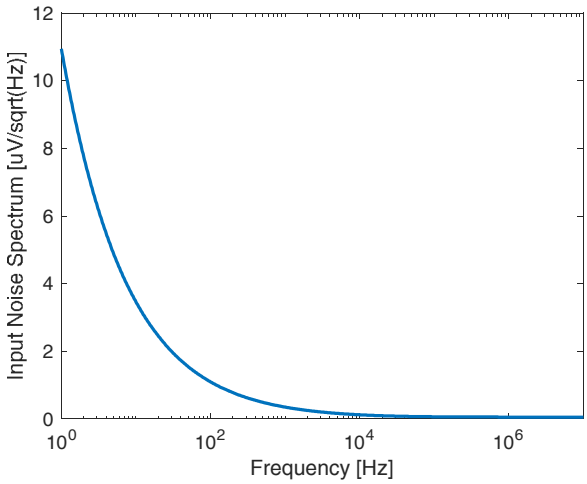

Figure 13. Input spectral noise density.

Figure 13 shows the input referred spectral noise density of the proposed transconductor: the white noise level is 55.3 nV/√Hz, and the rms noise integrated over a 1MHz bandwidth amounts to 67.74µV.

Table 2 synthesizes the simulated performance of the proposed transconductor; the bandwidth of the transconductance gain (i.e., short-circuit output) is 42.27MHz, and dc open-circuit voltage gain and differential output impedance are reported. The performance of the class-A transconductor is reported for comparison. The differential input voltage corresponding to a 1% variation of the transconductance gain is also reported, highlighting the extended linear range of the proposed solution.

Table 2. Simulated performance of the proposed transconductor.

Performance	**Proposed**	**Class-A**
Transconductance Gain G_m	12.6 – 43 μS	43.48 μS
Bandwidth *BW*	42.27 MHz	43.48 MHz
Voltage Gain A_V	64.1 dB	64.3 dB
Power Dissipation P_d	69.9 μW	62.6 μW
THD (0.5Vpp, 10kHz)	-52.3 dB	-31.1 dB
Output Resistance R_o	37.4 MΩ	37.3 MΩ
Output Capacitance C_o	16.7 fF	16.7 fF
Input-Referred Noise *IRN*	67.74 μVrms	77.45 μVrms
Input @ 1% ΔG_m	469 mVpp	103 mVpp

Extensive parametric and Monte Carlo simulations have been performed to evaluate the robustness of the proposed topology to process, temperature and supply voltage (PVT) variations and to mismatches. Table 3 shows the results of 500 Monte Carlo iterations where mismatches are taken into account, and the effects of temperature and supply voltage variations are reported in Table 4, highlighting the robustness of the circuit. While small-signal performance results quite constant, the large-signal behavior is somehow sensitive to process variations, with THD dropping to -37.5dB in

some process corners. However the transcharacteristic of the ADABIA circuit can be tuned by acting on the body voltage of M_8 and M_{8A}, allowing to compensate this effect, as reported in Table 5 (V_{body} is 300mV in typical conditions).

Table 3. Monte Carlo mismatch simulation results.

Performance	**Mean**	**Std. Deviation**
Transconductance Gain G_m	42.98 µS	1.135 µS
Bandwidth *BW*	42.31 MHz	2.14 MHz
Power Dissipation P_d	69.95 µW	0.87 µW
THD (0.5Vpp, 10kHz)	-50.28 dB	2.73 dB

Table 4. Effects of temperature and supply voltage variations.

Performance	**0° C**	**80° C**	**V_{DD} -5%**	**V_{DD} +5%**
Transconductance Gain G_m	43.03 µS	42.67 µS	42.92 µS	43.04 µS
Bandwidth *BW*	43.64 MHz	40.05 MHz	42.21 MHz	42.33 MHz
Power Dissipation P_d	69.65 µW	70.56 µW	66.21 µW	73.56 µW
THD (0.5Vpp, 10kHz)	-47.74 dB	-49.43 dB	-51.80 dB	-52.58 dB
Input @ 1% ΔG_m	498.8 mVpp	389.6 mVpp	472.6 mV	465.2 mV

Table 5. Effects of process parameters variations.

Performance	**FF**	**FS**	**SF**	**SS**
Transconductance Gain G_m	43.28 mS	43.1 mS	42.9 mS	42.71 mS
Bandwidth *BW*	43.35 MHz	40.96 MHz	43.74 MHz	41.25 MHz
Power Dissipation P_d	70.35 mW	70.13 mW	69.87 mW	69.62 mW
THD (0.5Vpp, 10kHz)	-54.06 dB	-54.49 dB	-53.38 dB	-53.67 dB

Input @ 1% ΔG_m	445.4 mVpp	444.4 mVpp	441.2 mVpp	439.6 mVpp
Body voltage of M_8 (V_{body})	100 mV	140 mV	420 mV	490 mV

Table 6 compares the performance of the proposed transconductor with recent results from the literature, showing a good tradeoff between linearity, noise and efficiency. To simplify the comparison, a figure of merit that extends the one used in [39] by considering also noise and distortion has been defined as

$$FOM = \frac{G_m}{P_d}\frac{V_{IIP3}}{IRN} \quad (1)$$

where V_{IIP3} is the input amplitude at the third-order intercept point and can be derived from HD3 (third-order distortion) data, and *IRN* is the input-referred noise spectral density. The proposed transconductor shows state-of-the-art performance, with better values of the FOM reported for some circuits operating at higher supply voltage and higher power consumption, that show a very low IRN.

Table 6. Comparison of the transconductor performance with the state-of-the-art.

Ref.	**Year**	**Tech.**	**VDD**	**P_d**	**Gm**	**IRN**	**Linearity**	**FOM**
[5]	2008	0.35	1.8	1100	630-1310	13.5 nV/√Hz @ 50MHz	THD -58dB @ 0.15Vpp, 10MHz	220.8
[37]	2012	0.35	0.8	0.04	0.066	80 μVrms (up to 200Hz)	THD -48.2dB @ 0.6Vpp, 10Hz	1.6
[19]	2013	0.18	0.8	8.3	0.03-3	1000 nV/√Hz	THD -40dB @ 0.8Vpp, 100kHz	1.7
[38]	2013	0.18	1.8	450	110	28 nV/√Hz @ 5MHz	HD3 -61dB @ 0.5Vpp, 5MHz	10.3

[8]	2015	0.18	1.8	139.2	24.4	55 nV/√Hz @ 10MHz	HD3 -49dB @ 0.8Vpp, 10MHz	24.7
[20]	2015	0.18	1.8	478	8.2-47	39 nV/√Hz @ 1MHz	IM3 -55dB @ 0.5Vpp, 20MHz	29.0
[39]	2015	0.18	1.8	0.59	0.72	2890 nV/√Hz @ 100Hz	THD -67dB @ 0.1Vpp, 100Hz	1.2
[40]	2016	0.25	1.6	4.73	0.001-0.015	9674 nV/√Hz	THD -46.4dB @ 0.2mVpp, 100Hz	5e-7
[21]	2017	0.13	0.6	9.81	11.5	184 μVrms (up to 500kHz)	HD3 -47.6dB @0.614Vpp, 5kHz	24.7
[27]	2017	0.18	1.8	859.5	18-289	12 nV/√Hz @ 1MHz	THD -64dB @ 0.6Vpp 1MHz	386.4
[41]	2017	0.09	1.2	140	0.025-0.3	3904 nV/√Hz @ 100Hz	HD3 -63.3dB @ 0.02Vpp, 100Hz	2.4e-4
[42]	2018	0.09	1.2	669.6	11.65-95.3	139 nV/√Hz @ 1MHz	HD3 -66dB @ 0.4Vpp, 10MHz	10.4
[43]	2020	0.13	0.4	0.36	0.76	988 nV/√Hz	THD -41.6dB @ 0.2Vpp, 10kHz	2.7
[44]	2020	0.18	1.8	64	6.12	--	HD3 -74.3dB @ 0.6Vpp, 1MHz	--
This work	*2021*	*0.13*	*1.2*	*69.9*	*21–43*	*55.* nV/√Hz *3 @ 100kHz*	*THD -52.3dB @ 0.5Vpp, 10kHz*	*65.2*
		μm	V	μW	μS		dB	S √Hz /pW

4. CLASS-AB Gm-C BIQUAD FILTER

To verify the validity of the proposed approach, we have used the linear transconductor to design a Gm-C biquad filter, with the standard architecture shown in Figure 14. All the transconductors are equal, with a gain of 43 µS, and the capacitance values are 24.36pF and 3.84pF for C_1 and C_2 respectively, providing f_0 = 468 kHz and Q = 2.065, as shown in Figure 15a. The dc gain of the filter is 0dB, and the 3-dB bandwidth results 685kHz.

The overall power consumption of the filter is 241 µW; Figure 15b shows the total harmonic distortion (THD) for different input amplitudes and frequencies, highlighting good linearity. The input-referred noise of the biquad is 207µVrms when integrated up to 1MHz.

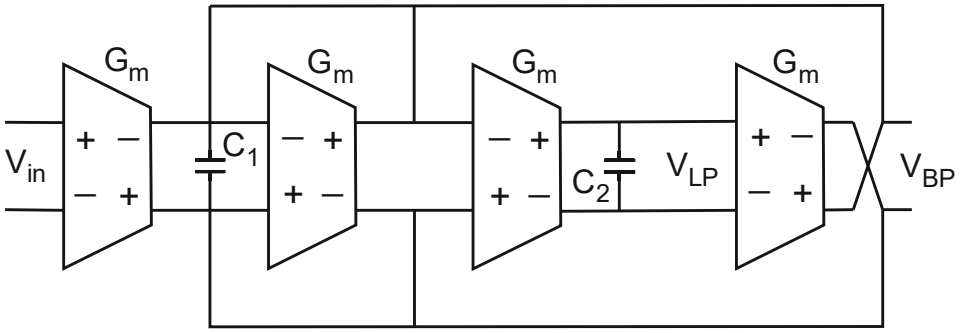

Figure 14. Gm-C biquad filter.

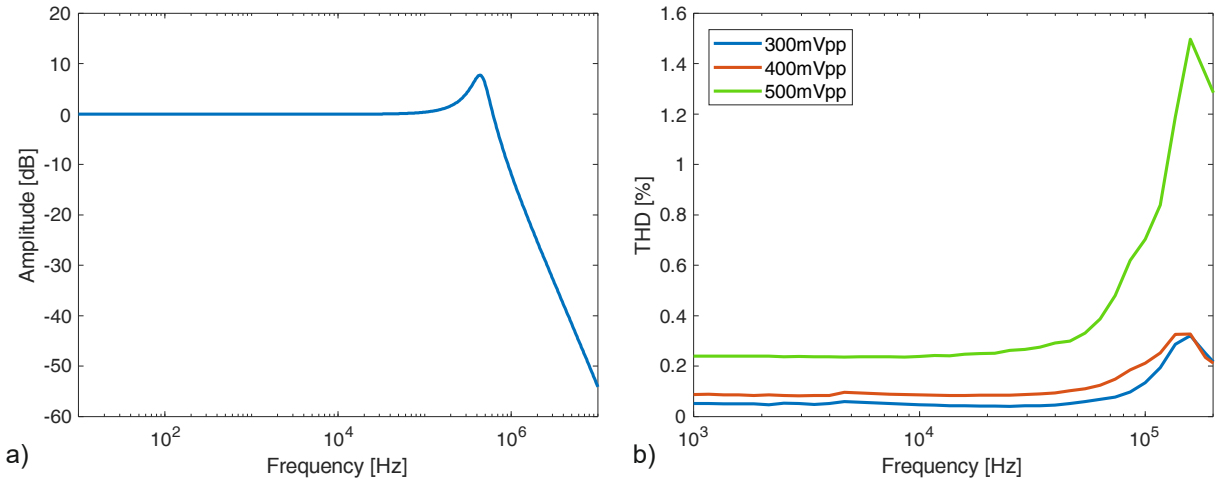

Figure 15. Transfer function of the biquad filter (a) and THD vs. input frequency, for different input amplitudes (b).

5. CONCLUSIONS

In this paper we have presented a novel topology for a linear transconductor, where class-AB behavior based on adaptive biasing is exploited to improve the linear range, by increasing the bias current when the transconductance gain begins to drop. A net improvement of linearity with respect to class-A biasing is obtained, and noise and linearity performance comparable with the state-of-the-art are achieved with limited power consumption. The transconductance gain can be reduced up to zero, with increasing distortions for very low gains. The transconductor has been used to simulate a Gm-C biquad with good linearity performance.

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