A Very Low Voltage Frequency Divider in Folded MOS Current Mode Logic with Complementary n- and p-Type Flip-Flops

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Abstract—**In this paper, a static frequency divider based on Folded MOS Current Mode Logic (FMCML) is presented. The design is based on alternating FMCML Flip-Flops with complementary PMOS or NMOS input differential pairs, since common-mode problems arise by using only one type of FMCML Flip-Flops.**

The design is carried out after a detailed theoretical modeling and analysis versus the Flip-Flop bias current, thus allowing to define optimized design strategies for the maximum speed, or the minimum power-delay product (PDP). The frequency divider architecture and design strategies are validated considering a commercial 28nm FDSOI CMOS technology. Post-layout simulations of a divider-by-16 show a maximum frequency of about 12 GHz with 74 μW power consumption for the high-speed design and a maximum frequency of 10 GHz with 53 μW power consumption for the minimum PDP design.

Index Terms—**Current Mode Logic, frequency divider, logic design, nanometer CMOS, delay model.**

I. INTRODUCTION

MANY high-speed analog/RF and digital applications require frequency dividers as key building blocks, when the generation of subharmonic signals from a high frequency source is required. Examples include PLL-based frequency synthesizers, clock generators, high-speed SerDes subsystems and time-interleaved analog-to-digital converters [1-6].

Several architectures are adopted in the literature for high-speed frequency dividers, such as static frequency divider (SFD) [7], regenerative frequency divider (RFD) [8], and injection-locked frequency divider (ILFD) [9]. Among them, the SFD presents the advantages of a very wide frequency range (from dc to very high frequencies) and of a structure that only uses standard digital blocks. This simplifies the design and allows design reuse and application in reconfigurable systems, making them the most common frequency divider architecture, unless extremely high frequencies are required.

Most of the above applications refer to mixed-signal integrated circuits, that set additional requirements on the

frequency divider block: in addition to a suitable frequency range for the specific application, low phase noise, and low area footprint, to ease integration, low sensitivity to noise (e.g., from substrate and supply rails) and low di/dt noise (not to disturb sensitive analog blocks) are required. Furthermore, minimization of power consumption is a fundamental issue for such systems, to enable a very high level of integration, ease portability, and simplify the design of packaging and heat dissipation. Among the available techniques to cope with this issue, reduction of the supply voltage can be adopted, due also to the reduction of breakdown voltage of scaled MOS devices.

In fact, the scaling of CMOS technology now provides devices with high frequency performance up to tens of GHz (transition frequencies up to 350/200 GHz for NMOS and PMOS devices [10]), that require low supply voltages around 1V or less, and provide a lower power consumption with respect to their bipolar counterparts. For high frequency applications, these devices are used to build logic families based on current steering in a differential approach, to exploit the benefits of fast switching, low sensitivity to common-mode noise and disturbances, and low power supply switching noise, that eases integration of analog and digital blocks in mixed-signal integrated circuits. The reference logic family is therefore the MOS Current Mode Logic (MCML) [11]-[12], that allows higher maximum speed than standard CMOS logic, and could even provide lower power consumption at frequencies that are still suitable for CMOS [13].

The MCML exploits series gating to implement logic functions, and typically just two stacked levels are used to limit the supply voltage. This allows implementing And-Or-Inverter (AOI) gates that can be exploited to build every complex combinatorial function, as well as XOR, MUX and D-type latch. Even for a 2-level gate, the minimum supply voltage cannot be lower than

$$V_{DD,min} = 2V_{TH} + 3V_{ov} + V_R \qquad (1)$$

where V_{TH} is the threshold voltage of the devices, $V_{ov} = V_{GS} - V_{TH}$ is the overdrive voltage and V_R is the dc voltage drop across

the load resistor, whose value is constrained by the need to fully switch the differential pairs.

Several solutions [14]-[16] have been proposed in the literature, by modifying the standard MCML, to reduce the minimum supply voltage of current mode logic gates, thus allowing sub-1V operation, and application in a very low-voltage environment. Among them, the Folded MCML (FMCML) approach seems particularly promising [17]-[19]. The FMCML exploits the complementary nature of CMOS technology, using a PMOS differential pair for the lower level of the stack, and a current mirror to connect it to the upper level NMOS differential pairs. This allows reducing the minimum supply voltage to

$$V_{DD,min} = V_{TH} + 2V_{ov} + V_R \qquad (2)$$

which is equal to the one of the MCML gates with stack levels reduced by one. Moreover, an approach named Multi-Folded (MF) MCML which generalizes the FMCML topology idea, thus allowing a minimum power supply equal to a single-level MCML (i.e., the MCML inverter) regardless the number of inputs, was also proposed [20].

In this paper we present a static frequency divider architecture realized with the FMCML which exploits the complementary nature of CMOS technology, and thanks to the derived dedicated design criteria allows to achieve high performance at very low voltage. Note also that MCML frequency divider design approaches previously treated in the literature [21]-[22] are not suited for the proposed architecture. Indeed, design procedures which are based on the conventional MCML style do not take into account the peculiarities of FMCML. In particular, as will be shown in the following of the paper, unlike from the standard conventional MCML, the FMCML logic style has a weak dependence on the bias current, thus very different design criteria arise.

The paper is structured as described in the following. In Section II we describe the proposed frequency divider architecture which exploits the FMCML D-latch as basic building block. In Section III we present a complete analysis of the clock-to-output propagation delay of the basic FMCML divide-by-2 (DIV2) cell, which is then exploited in Section IV to derive design guidelines for multistage frequency dividers. Validation of the proposed models and design case studies referring to a 28nm FDSOI CMOS technology are reported in Section V. Finally, some remarks and the conclusions are drawn in Section VI.

II. THE FREQUENCY DIVIDER ARCHITECTURE

Static frequency dividers are realized as the cascade of DIV2 stages, implemented as Toggle Flip-Flops (TFFs) with the input T set to one (see Fig. 1a), in order to toggle at every rising clock edge. Referring to the MCML logic style, such behavior can be easily obtained by using a D Flip-Flop (DFF) and connecting in feedback the input to the inverted output as shown in Fig. 1b.

In a FMCML implementation, the DFF is based on a Master-Slave configuration (i.e., a topology realized cascading two D-latches with counter-phase clock signals), and the schematic of a single D-latch, which is the main building block, is reported in Fig. 2. In a 2^N divider, N DFFs are used, with the output of

each DFF connected to the clock input of the next one. Referring to the schematic in Fig. 2, this requires the not feasible interconnection between the output of a NMOS differential pair and the input of a PMOS differential pair (the clock input).
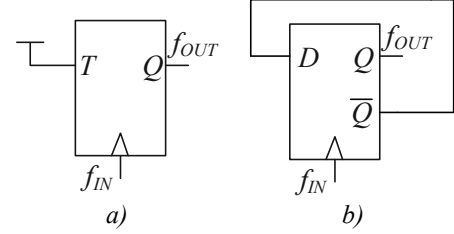

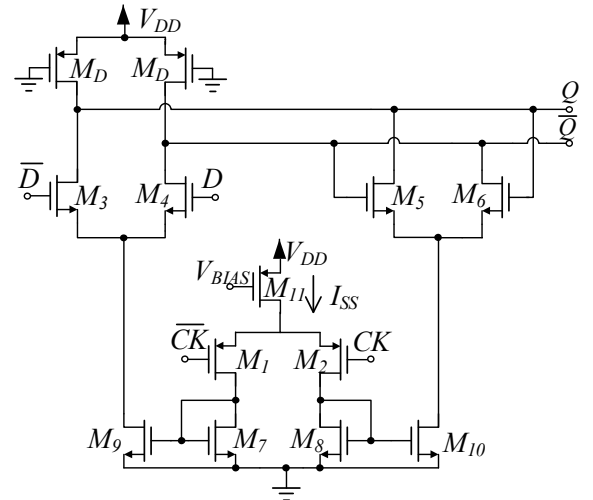Fig. 1. Static frequency divider: a) based on TFF; b) based on DFF.

Fig. 2. FMCML D-latch with PMOS input at the lower level (nType).

Indeed, considering the output common-mode voltage, $V_{CM,o}$, of the D-latch in Fig. 2 (equal to the output common-mode voltage of a DFF realized with this D-latch), we can write

$$V_{CM,o,nType} = V_{DD} - \frac{V_{SW}}{4}, \qquad (3)$$

where the voltage swing is defined as

$$V_{SW} = 2\Delta V = 2R_D I_{SS} \qquad (4)$$

where I_{SS} is the tail current (see Fig. 2) and R_D is the equivalent resistance of the triode PMOS load M_D.

The maximum input common-mode level which has to be guaranteed for the PMOS differential pair of the latch is

$$V_{CM,imax,nType} = V_{DD} - |V_{DSsat}| - |V_{GS}| = V_{DD} - |V_{TH}| - 2V_{ov} \qquad (5)$$

where the terms V_{TH} and V_{ov} are the MOS threshold voltage and the overdrive voltage, $V_{ov} = V_{DSsat} = |V_{GS}| - |V_{TH}|$, respectively. Thus, usually the value from (5) is significantly lower than the one provided by (3). For example with a deep submicron CMOS technology, where $|V_{TH}|$ is typically lower than 0.35V, the minimum V_{ov} can be about 50mV and a suitable value of V_{SW} is about 600mV, we get a $V_{CM,imax,nType}$ at least 300mV lower than $V_{CM,o,nType}$.
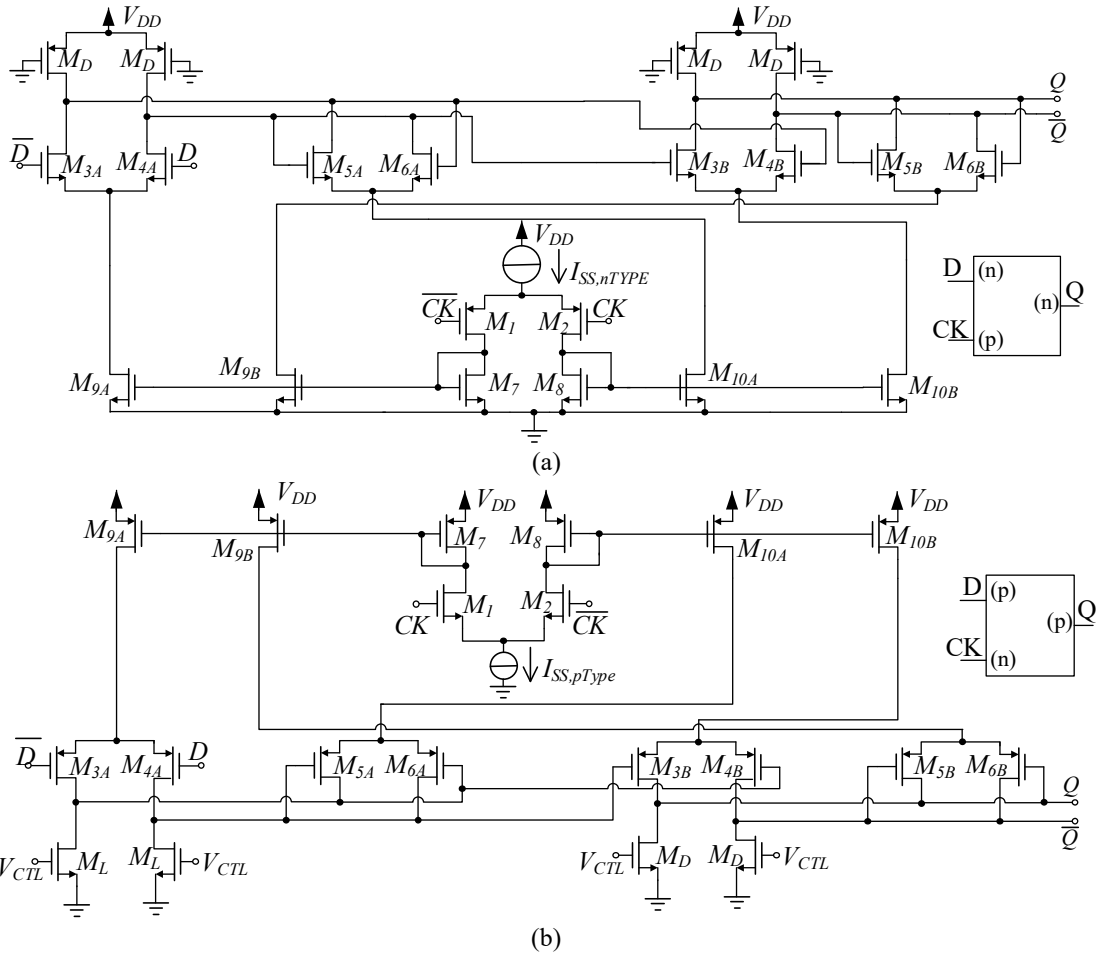
Fig. 3. Topology of a nType (a) and pType (b) D Flip-Flop in Folded MCML logic style.
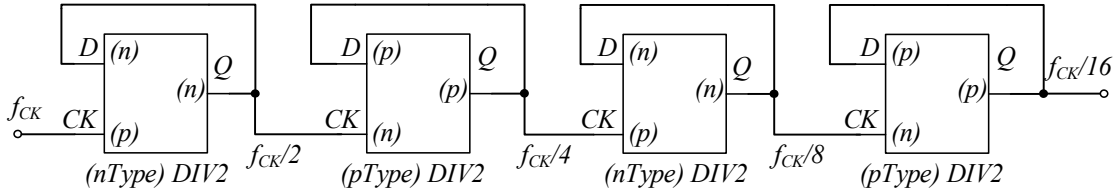

Fig. 4. Proposed architecture for the implementation of a frequency divider by 16.

The typical solution to this problem is the use of a source follower as level shifter between the *DFF*s; this however increases the power consumption, and, for maximum speed performance, the power of the source follower can result a significant fraction of the overall power consumption. In this paper we propose a different approach: input and output common-mode levels of each divide-by-2 (*DIV2*) block are made compatible by alternating complementary FMCML *DFF* stages, thus avoiding any additional stage in between. In fact, by considering the dual of the D-latch in Fig. 2, designed using complementary devices, the minimum input common-mode voltage is

$$V_{CM,imin,pType} = V_{GS} + V_{DSsat} = V_{TH} + 2V_{ov} \qquad (6)$$

that results fully compatible with (3), and similarly the output common-mode voltage is now

$$V_{CM,o,pType} = \frac{V_{SW}}{4} \qquad (7)$$

that is suited to drive the next D-latch with PMOS input.

In the following we will refer with nType (pType) to the *DFF* with the output given by an NMOS (PMOS) differential pair.

The schematic of the nType and pType FMCML *DFF*s are reported in Fig. 3a and in Fig. 3b respectively. By using these building blocks, we can realize a 2^N generic static frequency divider combining them as shown in Fig. 4 for the example of a frequency divider by 16.

III. DELAY MODEL OF THE FMCML

Usually, the speed performance of a static frequency divider is set by the *TFF* maximum toggle frequency [21], [23], which

is imposed by the clock-to-output propagation delay[1], t_{CKQ}, of the latch used to realize the *DFF*. In fact, referring to a generic master-slave *DFF* as the one reported in Fig. 3a or in Fig. 3b, the t_{CKQ} of the whole *DFF* is equal to the t_{CKQ} of the slave latch. Furthermore, since our divider core is based on a unitary feedback *DFF* as shown in Fig. 1b, in order for the basic divider cell to operate properly, the minimum period of the input clock signal has to be greater than $2t_{CKQ}$. In fact, starting from one clock edge, we have to guarantee the t_{CKQ} time of the slave latch for the stable intermediate output (output of the master latch) to become the output of the *DFF* and at the same time the new input of the master latch (due to the unitary feedback). From this instant an additional t_{CKQ} of the master latch is required to have a stable signal at the output of the master latch (intermediate output) before the next clock edge.

In the following, the clock-to-output propagation delay of the basic FMCML frequency divider by 2 (*DIV2*) cell is derived and used to estimate the speed response of the proposed frequency divider architecture.

A. FMCML time constants

To evaluate the t_{CKQ} of the FMCML *DFF*, we have to evaluate the propagation delay from the clock input node to the output of the FMCML *DFF*, which can be calculated, as shown in [16], by using the open-circuit time-constant method on the linearized circuit model.

The small-signal differential half-circuit model for the evaluation of the clock-to-Q delay of the FMCML *DFF*s in Fig. 3 is reported in Fig. 5 (this model applies to both *DFF*s in Fig. 3a and in Fig. 3b).

Referring to Fig. 5, the signal path is divided into three main sections:

- the clock input section from v_i to v_D: it includes the differential pair M_1-M_2 whose parameters are denoted with the suffix *CK*, loaded by the diode connected devices M_7-M_8 whose parameters are denoted with the suffix *CM*; the admittance $Y_{diode}=g_{mCM}+s(C_{gsCM}+C_{dbCM})$ is shown in Fig. 5;
- the folding from v_D to v_S, given by the unity-gain current mirror (hence parameters are denoted with the suffix *CM*); in particular, we consider the current mirror output towards the slave latch M_{9B}-M_{10B};
- the output section from v_S to v_o, implemented by the track differential pair of the slave latch M_{3B}-M_{4B}, whose parameters are denoted with the suffix *DP*, loaded by the triode devices M_D. For the differential half-circuit model, the loading effect of M_{4B} capacitances on the source node of M_{3B} has been taken into account through the capacitances C_{gsDP} and C_{sbDP} in the dashed box denoted as "*Load at source of M_{3B}*."

The loading admittance Y_{iCM} in Fig. 5 represents the loading effect of the current mirror branch towards the master latch $(M_{9A}$-$M_{10A})$, whereas Y_{LATCH} accounts for the loading effect of the hold differential pair $(M_{5B}$-$M_{6B})$ of the slave latch.
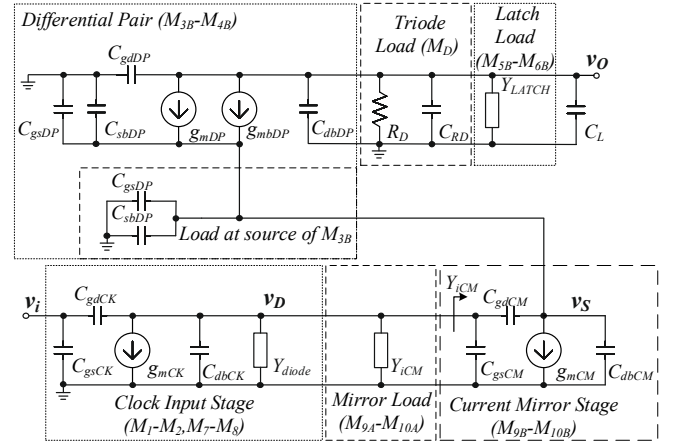

Fig. 5. Small-signal equivalent circuit of the FMCML *DFF*s in Fig. 3.

According to this modeling strategy, the t_{CKQ} of the *DFF*s in in Fig. 3a and in in Fig. 3b can be expressed as follows:

$$t_{CKQ,nType} = ln2(\tau_{1,nType} + \tau_{2,nType} + \tau_{3,nType}) \qquad (8a)$$

$$t_{CKQ,pType} = ln2(\tau_{1,pType} + \tau_{2,pType} + \tau_{3,pType}) \qquad (8b)$$

where the three time constant $\tau_{1,nType}$, $\tau_{2,nType}$, $\tau_{3,nType}$ (and $\tau_{1,pType}$, $\tau_{2,pType}$, $\tau_{3,pType}$) are related to the three main sections along the *CK-to-Q* signal path of the slave latch.

Without loss of generality, considering the nType *DFF* in Fig. 3a and assuming unity-gain current mirrors, the three time constants can be written as:

$$\tau_{1,nType} = \frac{C_{gdCK}+C_{dbCK}+C_{dbCM}+3C_{gsCM}+3C_{gdCM}}{g_m} \qquad (9)$$

$$\tau_{2,nType} = \frac{C_{gdCM}+C_{dbCM}+2C_{gsDP}+2C_{sbDP}}{g_{mDP}+g_{mbDP}} \qquad (10)$$

$$\tau_{3,nType} = R_D(C_{gdDP} + C_{dbDP} + C_{LATCH} + C_{RD} + C_L) \qquad (11)$$

where C_{RD} is the parasitic capacitance of the triode transistor M_D which provides the equivalent resistive load R_D [8], C_L is the load capacitance, and C_{LATCH} accounts for the load effect of the hold differential pair:

$$C_{LATCH} = C_{gDP} + C_{sbDP} \qquad (12)$$

where C_{gDP} is the capacitance seen at the gates of the latch differential pair with the source at ground. Finally, the other parameters have the usual meaning of MOS small-signal parameters.

B. Clock-to-Q delay versus bias current

Following the transistor sizing strategy in [11], we start by setting the voltage swing

$$V_{swing} = 2\Delta V = 2R_D I_{SS,nType}, \qquad (13)$$

and the required noise margin, that can be expressed as follows:

$$NM = \Delta V\left(1 - \frac{\beta}{A_V}\right), \qquad (14)$$

where A_V is the small signal gain of the gate:

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[1] The propagation delay is defined as the time taken by the output to reach 50% starting from the point in which the input has reached its 50% variation.

$$A_v = g_{mCK} R_D \tag{15}$$

and β is a factor ranging from $\sqrt{2}$, for the quadratic MOS model, to 1 for a submicron linear MOS model. From (13)-(15), considering the α-power MOS model [24], we can express the gate width of the transistors of the input clock stage as:

$$W_{CK} = \frac{2^{\alpha-1}}{K_{CK}}\left(\frac{A_V}{\alpha \Delta V}\right)^{\alpha} I_{SS,nType}, \tag{16}$$

where K_{CK} and α are technology parameters which tend to 1 and $v_{sat} C_{ox}$, respectively, in a short channel device, but are equal to 2 and $\mu_p C_{ox}/2L_{CK}$ if we can assume a long channel device, and A_V can be derived from (14).

Again, setting a suitable overdrive voltage and considering all the NMOS transistors with equal aspect ratios (i.e., transistors with suffix *CM* equal to the ones with suffix *DP*), the resulting gate width is

$$W_n = \frac{I_{SS,nType}}{2K_n V_{ov}^{\alpha}}. \tag{17}$$

Unless for C_{RD} and C_L, all the capacitances in (9)-(11) are proportional to the device width; considering the dependence of (16) and (17) on bias current and substituting them into (9) and (11), since both numerator and denominator are directly proportional to the current, the time constants $\tau_{1,nType}$ and $\tau_{2,nType}$ can be assumed to be constant with respect to bias current variations. Regarding the third time constant, $\tau_{3,nType}$, we can consider it composed by three terms:

$$\tau_{3,nType} = \tau_{3MOS,nType} + \tau_{RD} + R_D C_L \tag{18}$$

with

$$\tau_{3MOS,nType} = R_D\left(C_{gdDP} + C_{dbDP} + C_{LATCH}\right) \tag{19}$$

and

$$\tau_{RD} = R_D C_{RD}. \tag{20}$$

In particular, the term $\tau_{3MOS,nType}$, like $\tau_{1,nType}$ and $\tau_{2,nType}$, is independent on $I_{SS,nType}$, while the behavior of τ_{RD} as a function of the bias tail current is dependent on the implementation of the load, a MOS in triode region or a true resistor [25]. Focusing on VLSI applications, where area minimization is mandatory, a MOS triode load is considered and, unless for very low tail currents, we can again assume τ_{RD} to be constant[2].

Regarding the last term in (18), we have to estimate the value of the load capacitance C_L. In this specific application in which a *DIV2* is implemented, the *DFF* has a unitary feedback and is also loaded by another *DFF*, but whose input differential pair is made up with complementary transistors type with respect to the driver gate. Hence, for the example under consideration with a nType *DIV2* as driving cell and a pType *DIV2* as load cell, we can assume the load as the sum of two contributions. The first contribution is given by the input capacitance of the track NMOS differential pair of the slave latch within the driving *DIV2* stage, which we denote as $C_{in,n,nType}$. The second contribution is the input capacitance at the *CK* input of the load

pType *DIV2* stage (which is an NMOS differential pair), denoted as $C_{in,n,pType}$. Note, however, that the capacitive contribution $C_{in,n,pType}$ of the loading *DIV2* stage depends on its bias current $I_{SS,pType}$.

In conclusion, by expressing $C_{in,n,nType}$ and $C_{in,n,pType}$ as follows:

$$C_{in,n,nType} = c_{in,n,nType} \cdot I_{SS,nType} \tag{21a}$$

$$C_{in,n,pType} = c_{in,n,pType} \cdot I_{SS,pType} \tag{21b}$$

to show the bias current dependence of the input capacitances, we can summarize the nType clock-to-Q delay equal to:

$$t_{CKQ,nType} = \ln 2\left(\tau_{int,nType} + c_{in,n,pType}\frac{I_{SS,pType}}{I_{SS,nType}}\Delta V\right), \tag{22}$$

where

$$\tau_{int,nType} = \tau_{1,nType} + \tau_{2,nType} + \tau_{3MOS,nType} + \tau_{RD} + R_D C_{in,n,nType} \tag{23}$$

includes all the effects independent from the *DFF* bias current, $I_{SS,nType}$, and the last term in the brackets depends on the ratio of the bias currents of the loading and driving *DIV2* stages, that are of complementary type. By exchanging nType and pType, the same equations are valid for the CK-to-Q delay of the pType *DIV2* stage loaded by an nType *DIV2*.

IV. FMCML *TFF* AND DIVIDER DESIGN

In the following, starting from the analysis and considerations carried out above, we focus on the design strategies for the frequency divider, and in particular we start with the design guidelines of the single *TFF* (*DIV2* stage).

A. *TFF design guidelines*

The proposed frequency divider architecture shown in Fig. 4 is based on alternating complementary FMCML *TFF* stages. Since the first *TFF* has to provide the minimum propagation delay t_{CKQ}, it has to be implemented through the nType topology. In fact, assuming the same bias current, a pType *TFF* stage will surely be slower, due to the lower transition frequency of PMOS devices. However, considering that the second *TFF* stage works with the divided-by-2 signal, in order to guarantee that the speed performance is set by the propagation delay $t_{CKQ,nType}$ of the nType stage, the propagation delay $t_{CKQ,pType}$ of the pType *TFF* has to fulfill the following condition:

$$t_{CKQ,pType} \leq 2t_{CKQ,nType}. \tag{25}$$

Otherwise, the divider speed performance will be limited by the second divide by 2 stage (i.e., the pType *TFF*).

By inspection of (22), in order to provide the minimum *TFF* propagation delay, we have to set $I_{SS,nType}$ sufficiently higher with respect to $I_{SS,pType}$. As we will show in the next section, the contribution of the propagation delay due to $\tau_{int,nType}$ is about the 75% of the whole $t_{CKQ,nType}$ when $I_{SS,nType} = I_{SS,pType}$. Thus, a current $I_{SS,nType}$ two or three times

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[2] In practical cases also with a resistive load, since τ_{RD} is inversely proportional to I_{TAIL}^2, the contribution of τ_{RD} to the overall propagation delay

can be neglected (especially if high-resistivity polysilicon resistors are used) [25].

higher than $I_{SS,pType}$ allows a $t_{CKQ,nType}$ value very close to the ideal asymptotic minimum value.

On the other hand, a different goal is to minimize the power-delay product (PDP), that is given by:

$$PDP = 3 \cdot I_{SS,nType} \cdot t_{CKQ,nType}. \qquad (26)$$

In this case, we have to use the minimum allowable $I_{SS,nType}$ value, since (22) and (26) show that the delay decreases with the current much more slowly that the increase in power consumption, due to the constant term $\tau_{int,nType}$.
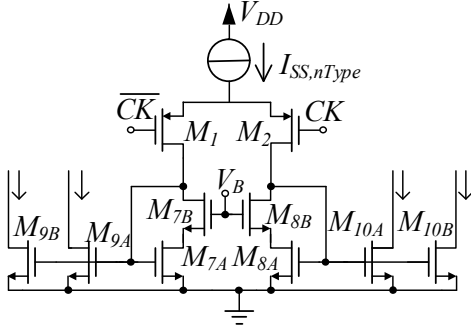

Fig. 6. Detail with adopted improved current mirror for the nType *TFF*.

TABLE I. Main process parameters of the 28 nm FDSOI CMOS technology.

$\mu_n C_{ox}$	$210 \frac{\mu A}{V^2}$
$\mu_p C_{ox}$	$78 \frac{\mu A}{V^2}$
V_{TN}^*	$0.3V$
$|V_{TP}^*|$	$0.38V$
W_{min}	$80nm$
L_{min}	$28nm$

*In FDSOI processes V_{TN} and $|V_{TP}|$ can be adjusted by means of body bias. In our design the body of NMOS and PMOS devices has been connected to ground and V_{DD} respectively.

TABLE II. Design Parameters for the *TFF* in Fig. 3 at minimum PDP.

	nType *TFF*	pType *TFF*
L	$28nm$	$28nm$
V_{DD}	$800mV$	$800mV$
$V_{CM,D}$	$650mV$	$150mV$
$V_{CM,CK}$	$150mV$	$650mV$
$V_{CM,Q}$	$650mV$	$150mV$
ΔV	$300mV$	$300mV$
I_{SS}	$5\mu A$	$7\mu A$
R_D	$60k\Omega$	$43k\Omega$
$W_D/L_D/V_G$	$80nm/45nm/100mV$	$98nm/60nm/500mV$
$W_{1,2}$	$500nm$	$700nm$
$W_{3A,4A,5A,6A}$	$250nm$	$700nm$
$W_{3B,4B,5B,6B}$	$250nm$	$700nm$
$W_{7A,8A,7B,8B}$	$125nm$	$700nm$
$W_{9A,10A,9B,10B}$	$125nm$	$700nm$

B. Divider design strategies

Considering the 2^N frequency divider implemented through the cascade of *N TFF* building blocks as shown in Fig. 4, we can follow a minimum *PDP* design strategy, and according to the analysis in the previous sub-section, we can design and use nType and pType *TFF*s with minimum bias current, provided that relationship (25) is satisfied. To be more precise, as shown in [25], the optimum bias current to minimize the *PDP* is the current that corresponds to minimum-size triode load devices: for lower currents, the resistance of the triode load is scaled by varying its gate voltage, thus making the time constant τ_{RD} inversely proportional to the current.

In the case we want to maximize the divider speed performance, we can simply modify the first nType *TFF* by increasing its bias current. The bias current of the second stage will be chosen as the minimum current which fulfils (25), whereas all the other stages will be biased with the minimum current.

V. CASES OF STUDY AND SIMULATION RESULTS

To validate the analysis and the proposed design strategies, we consider the commercial 28nm FDSOI CMOS technology from STMicroelectronics [26], whose main technology parameters are reported in Table I. However, we choose not to exploit the specific features of FDSOI technologies, to present more general results.

A. TFF simulations and model validation

In order to minimize the channel length modulation effect, and thus improve the accuracy of the current mirrors involved in the clock switching part of the *TFF*, the topology shown in Fig. 6 [19] has been used. According to Fig. 6, transistors M_7 and M_8 in Fig. 3a are replaced by transistors M_{7A}, M_{7B}, M_{8A} and M_{8B}. Furthermore, transistors M_{7B} and M_{8B} are equally sized to M_3 and M_4, thus, setting the bias voltage V_B equal to the common-mode voltage of the *D* signals, the drain-source voltage V_{DS} of M_{7A}, M_{9A}, M_{9B}, M_{8A}, M_{10A} and M_{10B} is equalized. The complementary improved current mirror has been adopted for the pType *TFF* Fig. 3b.

From preliminary simulations on the 28nm CMOS process, we have found that the minimum allowable tail current of the nType cell $I_{SS,nType}$ to keep all the devices in the strong inversion region is 5µA. Surely the divider could be operated with the devices in subthreshold region, but we chose to avoid it since our model was not derived for that condition. 5µA is also the current corresponding to the minimum width for the triode PMOS load device.

Regarding the pType cell, the current $I_{SS,pType}$ that corresponds to the minimum width for the NMOS triode load is 7µA: for higher currents, the value of R_D is changed by acting on the width of the load transistor, whereas using lower currents requires acting on the gate voltage [25] and results in an increased propagation delay. Also in this case, bias currents below 5µA result in subthreshold operation.

Using the minimum gate length for all the devices except M_D to minimize parasitic capacitances, and setting the gate widths according to the required noise margin and gate-source voltages, we get the transistor dimensions summarized in Table II for the case of optimum currents (those minimizing PDP), corresponding to minimum width for the load devices. Transistor widths are scaled with bias current to keep current densities constant, and the number of gate fingers is modified accordingly. The width of the load devices M_D is increased

when increasing the bias current[3].

The behavior of the propagation delay of the nType *TFF* versus the bias current $I_{SS,nType}$ at different pType bias currents of the next stage and for different ratios between pType and nType bias currents is reported in Fig. 7a and Fig. 7b, respectively. Fig. 7 shows that the weight of the second term in (22) increases with the pType bias current, providing a nType propagation delay that shows some dependence on the nType bias current. Such dependence is however limited, unless for very large pType-to-nType current ratios.

The propagation delay of the pType *TFF* versus the bias current $I_{SS,pType}$ is shown in Fig. 8a, for different bias currents of the nType load, and in Fig. 8b, for different nType-to-pType current ratios. Similar considerations apply to the complementary case, but now the dependence of propagation delay on bias current is even weaker, due to the increased weight of the constant term in (22) for the pType cell, that can be attributed to the larger time constant of the PMOS current mirror. A sharp increase of the delay below 7μA is observed, due to the effect of the triode NMOS load.

cases, we can estimate the weight of the constant term in (22) as about the 70% and 87% of the overall delay at unitary current ratio for the nType and pType cells respectively. The higher value for the pType is due to lower speed of PMOS devices in the current mirror, and this justifies a weaker dependence of the propagation delay when varying the load. A comparison of the curves in Fig. 7 and Fig. 8 also shows that the pType cell is about 30% slower than the nType one as expected, thus implying that the first *DIV2* block has to be of nType.

A more detailed analysis of the propagation delays shows that, for $I_{SS,pType}$ of at least 7μA, the delay of the pType cell, even when heavily loaded, is always less than twice the delay of the nType cell driving it, thus satisfying (25). As an example, the delay of a pType cell biased at 7μA is between 116ps (unloaded case) and 175ps (when loaded by a nType cell biased at 30μA). The delay of a nType cell loaded by the 7μA pType cell is, instead, between 91ps (when the nType cell is biased at 30μA) and 125ps (nType cell at the minimum 5μA current). Furthermore, in the case of a pType cell loaded by a nType cell (e.g., second and third stage of the divider), the dual of (25) is always satisfied.
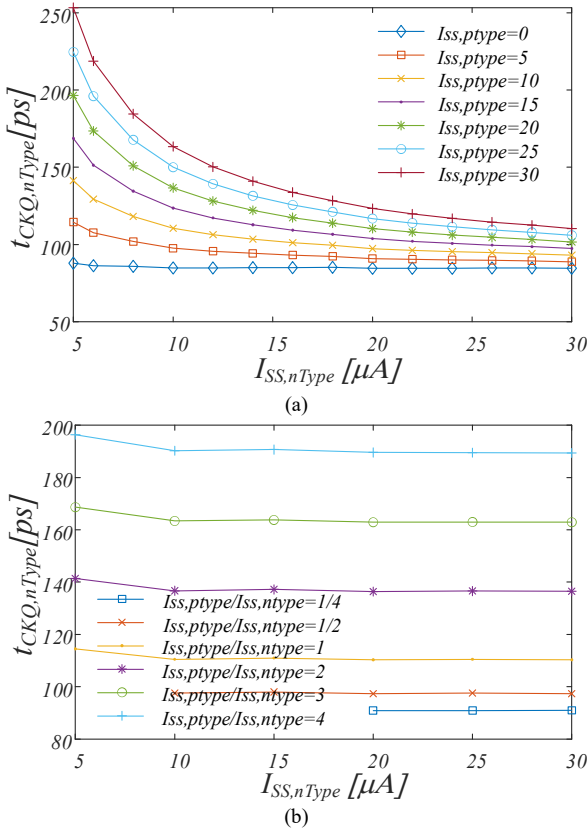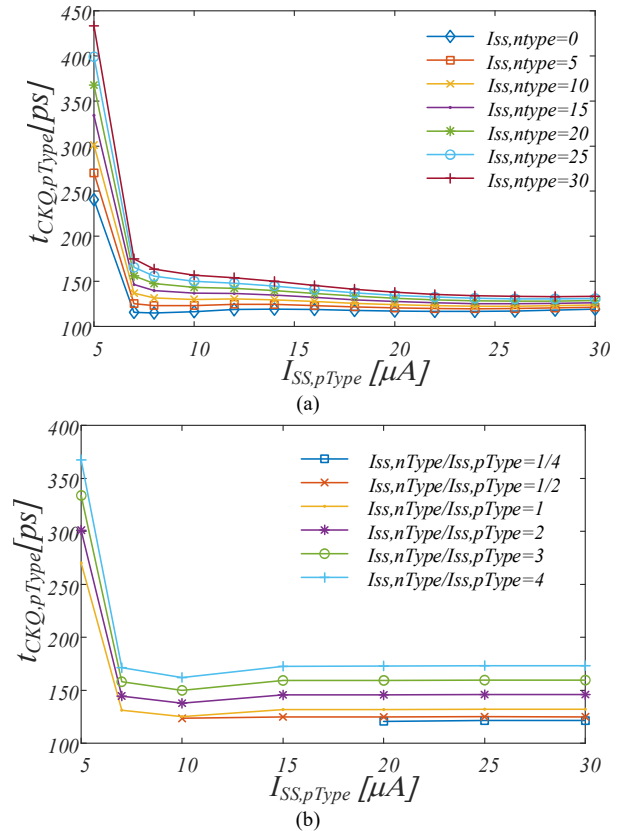

Fig. 7. Propagation delay of the nType *TFF* versus bias current: (a) for different bias current of the next pType *TFF* (I_{pType}=0 means unloaded nType *TFF*); (b) for different current ratios between the next stage and current stage bias currents.

Fig. 8. Propagation delay of the pType *TFF* versus bias current: (a) for different bias current of the next nType *TFF* (I_{nType}=0 means unloaded pType *TFF*); (b) for different current ratios between the next stage and current stage bias currents.

By using data in Fig. 7 and Fig. 8, some considerations on the performance of nType and pType cells and on the design guidelines discussed in the previous section can be drawn. First of all, by comparing the delays of the loaded and unloaded

B. PVT variations, mismatches, and supply voltage scaling

To analyze the sensitivity of the delay to process, supply voltage and temperature (PVT) variations, we have considered

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[3] For lower currents the transistor width is kept constant, and the resistance of the triode device is changed by acting on the gate voltage. In this case, τ_{RD} depends on the bias current, resulting in an increase of t_{CKQ} as shown in Fig. 8 for the pType cell below 7μA.

the clock-to-Q propagation delay of both nType and pType cells biased at 10μA and loaded by the cell of the opposite type. Simulations have been performed using a suitable loop to properly bias the gates of the triode loads to keep the voltage swing approximately constant [27].

Tab. III reports the values of t_{CKQ} for the different process corners and for a ±10% variation of the nominal 800mV supply voltage, and Fig. 9 shows the dependence of the delay on the temperature. These results highlight the robustness of the proposed architecture to PVT variations. We have also considered the effect of mismatches between devices: a Monte Carlo analysis has revealed a standard deviation to mean value ratio of 11% and 12% respectively for the delay of nType and pType cells.

TABLE III. CLOCK-TO-Q DELAY VARIATION DUE TO PROCESS AND TEMPERATURE

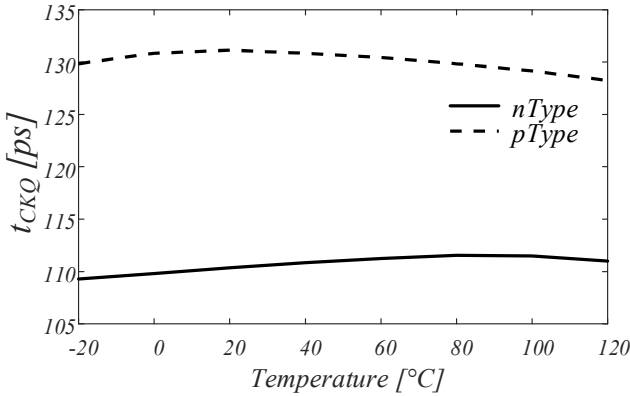| Process Corner	nType	pType
TT	110.53 ps	130.14 ps
FF	107.56 ps	128.94 ps
FS	111.66 ps	115.86 ps
SF	109.47 ps	139.76 ps
SS	113.00 ps	129.16 ps
Supply Voltage	nType	pType
720mV (-10%)	109.65 ps	130.74 ps
880mV (+10%)	111.00 ps	126.14 ps

Fig. 9. Temperature dependence of the t_{CKQ} for nType and pType cells.

Since the FMCML approach is aimed at very low-voltage applications, we have also evaluated the behavior of the divider cells for lower supply voltages. Simulations have shown that the nType and pType cells can operate with supply voltages as low as 475mV and 550mV respectively, without significant variation of the propagation delay.

C. Dividers design and validation

According to the design strategies presented in the previous Section and the results on the FMCML *TFF*s reported in Fig. 7 and Fig. 8, the frequency divider architecture reported in Fig. 4 can be implemented by sizing the first *TFF* to achieve the minimum *PDP* with 5μA bias current. The second stage of the divider has to be implemented through a pType *TFF* biased with the minimum bias current which allows to fulfil (25): this current has been found to be 7μA. Considering that the third (nType) and fourth (pType) stages of the divider operate at lower frequencies they can both be implemented with 5μA bias current which is the minimum value to avoid subthreshold operation.

It has to be noted that the frequency divider can also be designed to achieve minimum power consumption, by using in all the stages the minimum bias current of 5μA. In this case, the achieved maximum operating frequency of the divider is strongly reduced with respect to the minimum *PDP* design, since its speed is limited by the pType *TFF* (the second stage of the divider), and the maximum frequency results:

$$f_{max} \leq min\left\{\frac{1}{2t_{CKQ,nType}} ; \frac{1}{2t_{CKQ,pType}}\right\} = \frac{1}{2t_{CKQ,pType}} \qquad (27)$$

If a divider which maximizes the speed performance is required, according to the results in the previous sub-section, we can set the current $I_{SS,nType}$ of the first *TFF* to be about two times higher than $I_{SS,pType}$ to allow a $t_{CKQ,nType}$ value very close to its asymptotic minimum value. The maximum speed design is therefore obtained by setting $I_{SS,nType}$ to 14μA in the first stage and keeping $I_{SS,pType}$ to 7μA in the second stage. The third and fourth stages can still be biased with the minimum current.

Of course, considering the divider power consumption and denoting with $P_{DIV2,i}$ the power consumption of the i-th *DIV2* block in the cascade of n stages, since in any design case all the *TFF*s after the first nType and the first pType stages will be equally sized, we can express the total power consumption P_{TOT} for both the design strategies as follows:

$$P_{TOT} = P_{DIV2,1} + P_{DIV2,2} + (N - 2)P_{DIV2,3}. \qquad (28)$$

Thus, the divider power consumption, which linearly increases with *N*, for the maximum speed performance shows a power consumption increase, with respect the minimum *PDP* design, which may be not so significant and reduces with the increase of *N*.

TABLE IV. SUMMARY OF CASE STUDIES.

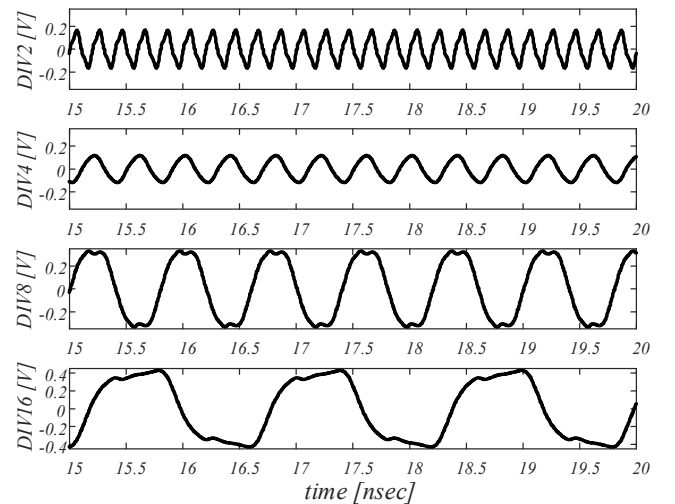| TFF1 nType I_{SS} (μA)	TFF2 pType I_{SS} (μA)	TFF3 nType I_{SS} (μA)	TFF4 pType I_{SS} (μA)	Power (μW)	$t_{CK,MIN}$ (ps)	$f_{CK,max}$ (GHz)
5	7	5	5	52.8	95	10.5
14	7	5	5	74.4	82	12.2
5	5	5	5	48	>200	<5

Fig. 10. Output waveforms of the FMCML static frequency divider designed for minimum *PDP* and simulated at the maximum speed with an input t_{CK} of 95ps.

All the cases we have designed and analyzed are summarized in Table IV. The output waveforms at the maximum operating frequency of the *DIV2* stages of the frequency divider designed for the minimum *PDP* are reported in Fig. 10 for an input clock signal with a period t_{CK} equal to 95ps and an amplitude of 0.3V. Simulated phase noise is about -107.5 dBc/Hz at 100kHz offset after the first DIV2 stage, and 3dB higher for the divided-by-16 output.

D. Design of the layout

The results reported in Tab. IV refer to post-layout simulations, since at high frequencies it is important to take the effect of layout parasitics into account. A modular layout approach based on the divide-by-4 (the cascade of a nType and a pType cell) has been adopted, and Fig. 11 shows the layout of the first divide-by-4 for the minimum PDP case (i.e. $I_{SS,nType}$=5µA and $I_{SS,pType}$=7µA).
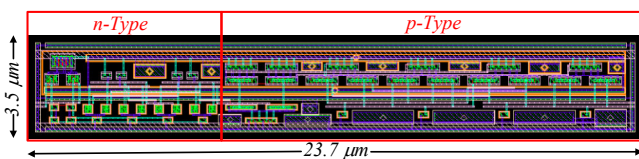

Fig. 11. Layout of a divide-by-4 divider (nType cell biased at 5µA and pType cell biased at 7µA).

The layout has been optimized to minimize the length of interconnections and to maintain the symmetries of the original structure [28], according to the design practices of analog high frequency applications, resulting in an area footprint of 23.73 x 3.5 µm² for the divide-by-4 (total area is approximately doubled for the full divide-by-16, taking also into account the bias generators).

VI. CONCLUSION

A novel architecture, in which complementary nType and pType low-voltage FMCML *DFF*s are exploited to implement high-speed and power-efficient static frequency dividers, has been presented in this work.

Thanks to a detailed analysis of the propagation delay of the FMCML Flip-Flops, two design strategies have been also presented; the first one in which minimum *PDP* is achieved and another one in which the maximum speed performance is pursued.

The two strategies have been validated designing divide-by-16 circuits with a 28nm FDSOI CMOS technology. The results reported in Table IV, which are in good agreement with the theoretical analysis, confirm the effectiveness of the proposed architecture and design strategies. In particular, a maximum operating frequency higher than 12 GHz is achieved with a power consumption as low as 74.4µW. The power consumption can be further reduced (of about 30%) adopting the minimum *PDP* strategy, with a reduction in the maximum speed performance of about 15%.

Tab. V compares the performance of the proposed divider with CMOS frequency dividers operating in the multi-GHz range. A figure of merit (FOM) that takes into account maximum operating frequency, total power consumption and

the division factor has been computed as:

$$FOM = \frac{f_{MAX}}{P_{TOT}/ln_2 N_{DIV}}. \qquad (29)$$

TABLE V. COMPARISON WITH THE LITERATURE.

Ref.	Arch.	Tech.	V_{DD}	P_{TOT}	f_{MAX}	N_{DIV}	FOM
[29]	TSPC	90	0.5	0.25	7.2	2	28.8
[30]	DFD	32	1	4.8	70	4	29.2
[8]	RFD	65	0.4	1.6	64.2	2	40.1
[7]	MCML	65	1	6.25	67	4	21.4
[31]	ILFD	65	0.42	1.2	62	2	51.7
[32]	MCML	65	1.3	0.78	21.5	2	27.6
[33]	TSPC	22	0.9	0.35	70	2	195
[33]	TSPC	22	0.4	0.0244	25.7	2	1058
This work[4]	FMCML	28	0.8	0.0528	10.5	16	795
	FMCML	28	0.8	0.0744	12.2	16	656
		nm	V	mW	GHz		GHz/mW

TSPC: SFD exploiting true single-phase clock logic style
DFD: dynamic frequency divider
RFD: regenerative frequency divider
MCML: SFD exploiting MCML logic style
ILFD: injection-locked frequency divider
FMCML: SFD exploiting folded MCML logic style

Tab. V shows a very high efficiency for the proposed approach, as highlighted by the FOM; comparable or even higher values for the FOM are achieved using SFDs based on true single-phase clock (TSPC) logic style, that however presents a higher sensitivity to noise, due to its single-ended nature, and a much higher power supply switching noise, that could disturb other blocks on the same chip.

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