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The front end electronics for the drift chamber readout in MEG experiment upgrade

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Abstract: Front-end electronics plays an essential role in drift chambers for time resolution and, therefore, spatial resolution. The use of cluster timing techniques, by measuring the arriving times of all the individual ionization clusters after the first one, may enable to reach resolutions even below 100 µm in the measurement of the impact parameter. A high performance front-end electronics, characterized by low distortion, low noise and a wide bandwidth has been developed with the purpose to implement cluster timing techniques in the new drift chamber for the upgrade of the MEG experiment at Paul Sherrer Institut (CH) [1].

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Particle tracking detectors (Gaseous detectors); Wire chambers (MWPC, Thin-gap chambers, drift chambers, drift tubes, proportional chambers etc)

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Contents

2020 JINST 15 C07009

1 The MEG II drift chamber

The MEG II Cylindrical Drift Chamber (CDCH) is a single volume detector, whose design was optimized to satisfy the fundamental requirements of high transparency and low multiple scattering contribution for 50 MeV positrons, sustainable occupancy (at 7×10^7 μ^+/s stopped on target) and fast electronics for cluster timing capabilities (figure 1) [2, 3].

In order to permit the detection of single ionization clusters, the electronic read-out interface has to process high speed signals. For this purpose, a specific high performance 8-channels front-end electronics board (FE) has been designed with commercial devices, such as fast operational amplifiers [4]. The FE was designed for a gain which must produce a suitable read-out signal for further processing, low power consumption, a bandwidth adequate to the expected signal spectral density and a fast pulse rise time response, to exploit the cluster timing technique [5, 6].

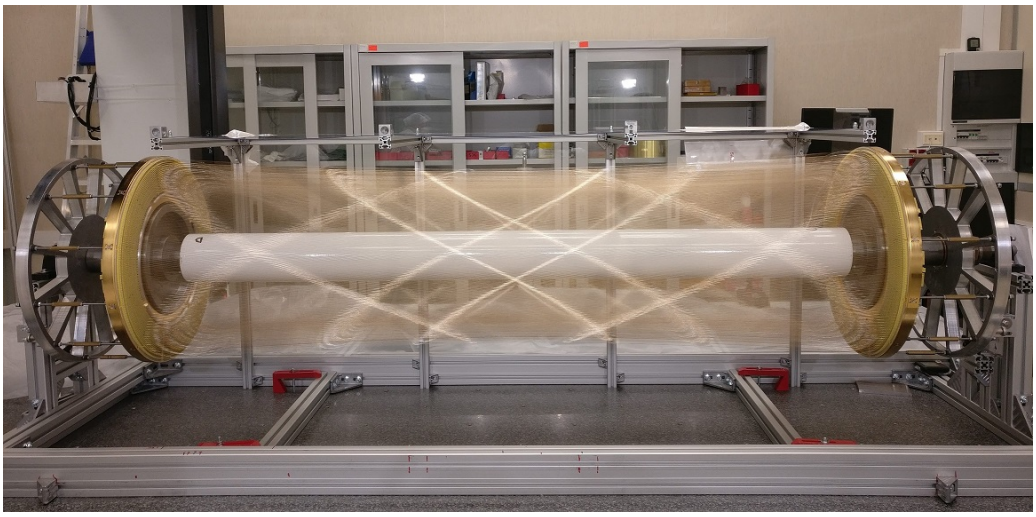

Figure 1. The MEG II drift chamber after completing wiring and before to be sealed.

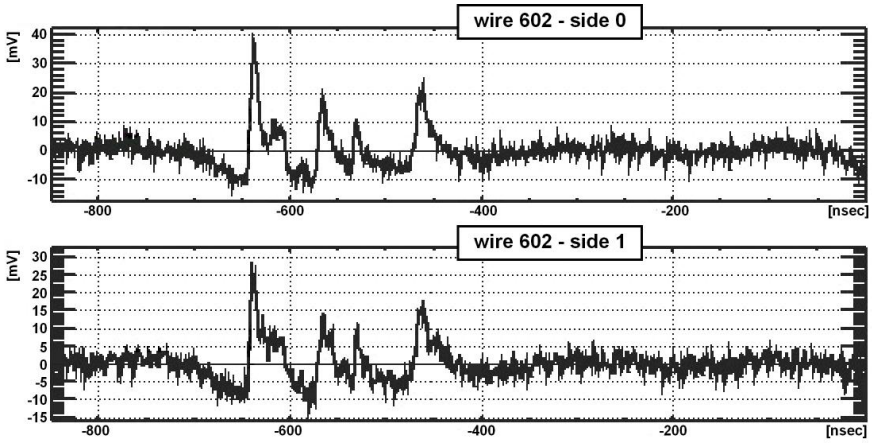

Figure 2. Typical signal waveforms measured at both the ends of a drift cell in the MEG II CDCH.

2 Electric parameters of the drift cells

Each drift cell of the CDCH is approximately square, 6.6 mm (at the lowest radius) to 9.0 mm (at the highest radius) wide, with a 20 µm diameter gold plated tungsten sense wire, surrounded by 40 µm diameter silver plated aluminium field wires, in a ratio of 5 : 1. The mean active length of the wires is 1.9 m. Therefore, the mean distributed resistance is 140 Ω/m, the mean distributed inductance is 1.2 µH/m and the mean distributed capacitance is 9.4 pF/m; the distributed conductance is negligible. Due to the significant resistance of the wires, the resulting characteristic impedance of the drift cell depends on the frequency, nevertheless its variation is less then 10 % from the mean value of 354 Ω, for frequencies greater then 200 MHz.

Typical signal waveform acquired from the CDCH is a pulses train (figure 2): time separation between the different pulses goes from few nanoseconds to a few tens of nanoseconds. Main signal information is contained within a bandwidth in the order of 1 GHz.

3 The schematic

The schematic of the FE board is shown in figure 3. The input network provides decoupling, protection and matching to the mean characteristic impedance of the drift cell. The matching resistance is the parallel combination of the termination resistance and the input resistance of the first gain stage. Signal amplification is realized with a double gain stage made by ADA4927 and THS4509 operational amplifiers:

- Analog Device's operational amplifier ADA4927 works as a first gain stage: it is a low noise, ultra-low distortion, high speed, current feedback differential amplifier. The current feedback architecture provides a loop gain that is nearly independent of the closed-loop gain, achieving wide bandwidth, low distortion, and low noise at higher gains (input voltage noise is only 1.3 nV/$\sqrt{\text{Hz}}$) and lower power consumption than comparable voltage feedback amplifiers [7].
- The THS4509 by Texas Instruments is used as a second gain stage and output driver. It is a wide-band, fully differential operational amplifier with a very low noise (1.9 nV/$\sqrt{\text{Hz}}$), and

2020 JINST 15 C07009

low harmonic distortion (-75 dBc HD_2 and -80 dBc HD_3 at 100 MHz). The slew-rate is 660 V/µs with a settling time of 2 ns to 1 % for a 2 V step [8].

Both the devices are ideal for pulsed applications.

The differential output of the FE is connected to the digitizing unit (see later) through a custom made cable 5 m long, designed to have a stable, flat frequency response (Amphenol Spectra Strip SkewClear [9]). This cable is made by shielded parallel pairs, each pair being individually shielded; an overall ground jacket is also present, giving a maximum attenuation of 0.75 dB/m at the frequency of 625 MHz. Some pairs of the output cable are used for powering the FE board.

In order to balance the attenuation of the output cable, a pre-emphasis on both gain stages has been implemented. The pre-emphasis introduces a high frequency peak that compensates the output cable losses, resulting in a total bandwidth of nearly 1 GHz. The gain at middle bandwidth is ~ 20 dB on 120 Ω load. Mean non-linearity is less then 0.1 % for input short pulses (rise time on the order of 1 ns) in the range of amplitudes 15 mV ÷ 75 mV. Noise level measured is less then 2 mV (RMS), after the output cable, on 120 Ω load.

Pre-amplified differential signals are successively digitized by the WaveDREAM board [10] at a (programmable) speed of 2 GSPs with an analogue bandwidth of 1 GHz.

The current consumption for each channel is 60 mA at a voltage supply of ±2.5 V; this correspond to a total power dissipation per end-plate of about 300 W, therefore an appropriate cooling system made both with recirculation of coolant fluid and with forced dry air is used.

4 The layout

Due to the size of the FE output connector socket and considering the available space between the CDCH wire layers, three different board versions have been designed, one with the output connector on the right, one in the center and one on the left. The layout of the FE is shown in figure 4, the pileup of the FE boards on one endplate of the CDCH is shown in figure 5.

The gain stages are located on the same PCB layer (bottom) to eliminate losses due to vias inductance. Each channels have their own ground plane to reduce cross talk between channels, all the ground planes are connected to the same point close the output connector. Cross talk between adjacent channels obtained in this way is ~ 1 %, cross talk to next channel is negligible (< 0.5 %).

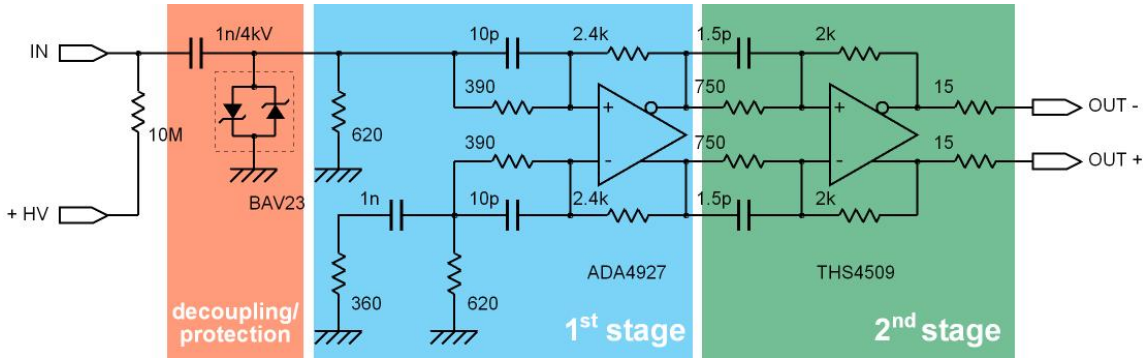

Figure 3. The schematic of the FE board.

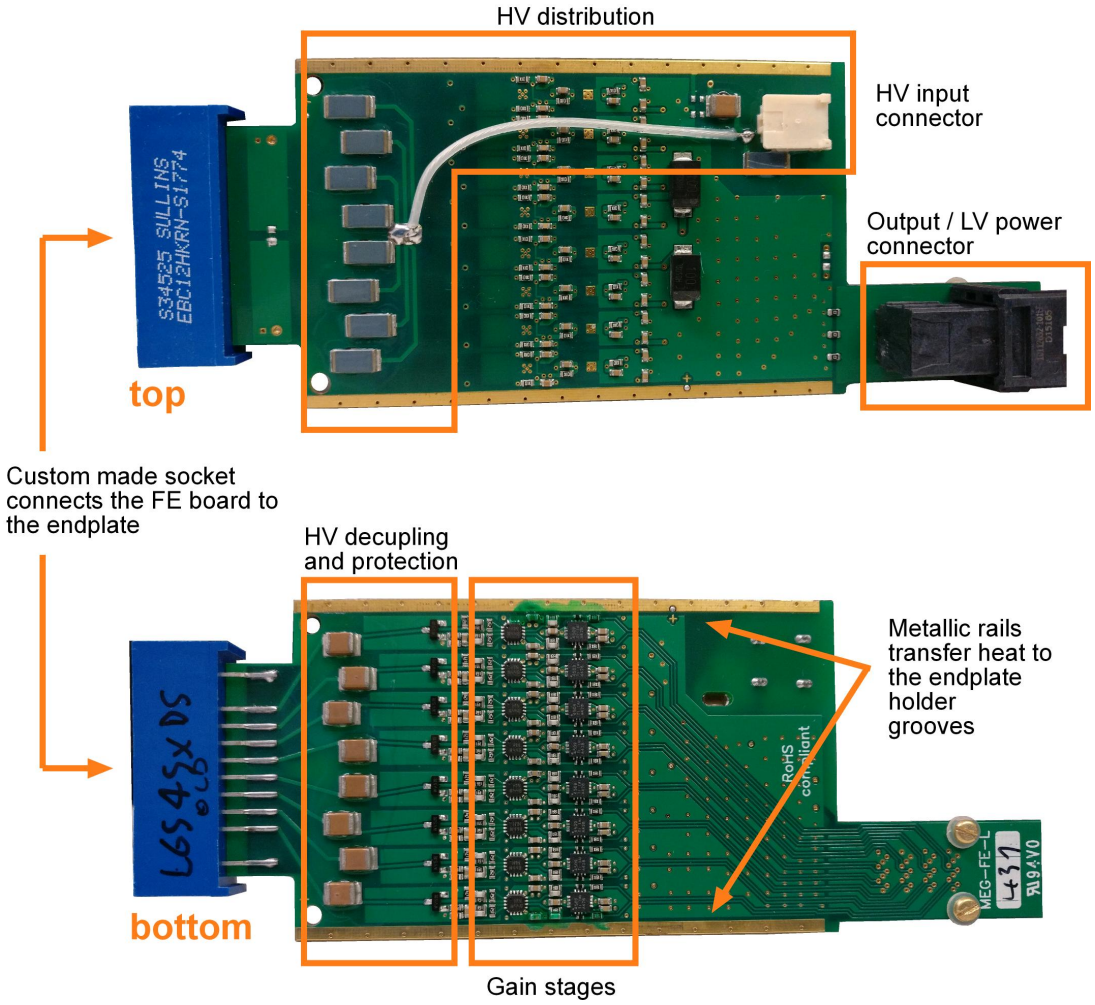

Figure 4. Top and bottom sides of the FE board.

High voltage is applied to the sense wires of the CDCH through the same connector used for read-out. The high voltage distribution network is host on the PCB plane opposite to that of the signals, for matter of security.

A specific layer of the PCB, unconnected to the others, is used for heat transfer from the gain stages to two metallic rails located on both the sides of the board.

5 Conclusions

A high performance front-end electronics board for the read-out of the new drift chamber of MEG experiment upgrade has been presented. The board introduces low distortion and low noise and offers and adequate bandwidth in order to implement the cluster timing techniques. 432 (plus spares) boards has been produced to read-out signals from both the ends of each sense wire of the drift chamber, for a total of 3456 readout channels.

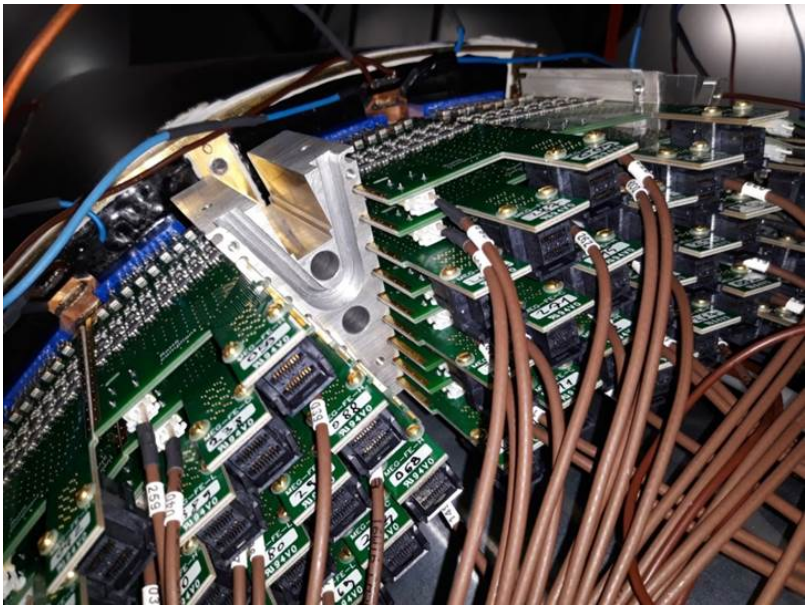

Figure 5. The pileup of the FE boards on the CDCH end-plate; only the HV cables are connected to the boards.

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2020 JINST 15 C07009