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A Low-Power Delta-Sigma Modulator ADC for Sensor System Applications

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ABSTRACT

This paper discusses a third-order tri-level quantizer delta-sigma modulator analog-digital converter (ADC) for cascaded integrators with distributed feedback (CIFB) and cascaded integrators with distributed feedforward (CIFF) structure for sensor system applications. The signal transfer function (STF) and noise transfer function (NTF) discussed for poles and zeroes. Oversampling ratio (OSR) and different quantizer level presented for the modulator structure to trade-off the targeted bandwidth and complexity of increased quantizer level. NTF zero optimization technique also implemented to further reduce in-band quantization noise by shaping at high frequency, which is later filtered by digital low-pass filter. Mismatch simulation results also performed for quantizer levels considering the performance degradation of the modulator. Operational amplifier (op-amp) for the front-end integrator optimized for minimum power consumption by considering low finite DC-gain, limited slew-rate, minimum required gain-bandwidth product (GBW). The proposed model simulations provided and discussed. Non-ideal effect for the proposed complete modulator CIFF structure for switched-capacitor circuit level implementation performed. The non-ideal parameters like thermal noise, sampling jitter, white noise, and switch nonlinearity also discussed. Modeling simulation results for CIFF structure with tri-level quantizer, shows that proposed modulator structure can achieve signal-to-noise ratio (SNR) of 133dB for sensor system bandwidth of 10kHz with OSR = 128.

Keywords: Delta-sigma modulator, Analog-to-digital converter, switched-capacitor, operational amplifier, Integrator.

1. INTRODUCTION:

Recent trends towards integrated sensors like Micro-Electro-Mechanical-Systems (MEMS) and Nano-Electro-Mechanical-Systems (NEMS) getting popular due to their integrability with silicon technology. These sensors have wide application, like from automotive, aerospace, biomedical and communications. Even in your pockets mobile phone, has sensors like image sensor, touch screen, microphone, compass, inertial sensors [1]. These sensors connected to the processor by interfacing electronics, which converts very weak sensor analog signal to digital signal that is further processed by the machine. Typically signal conditioning of these sensors are on chip to reduce the parasitic effect. The design challenge is high dynamic range and reproducibility. The ADC for these sensors requires high precision for transforming the weak analog signal into digital output. The reduced supply voltage in CMOS technologies causes analog signal a limited swing while the digital design can take advantage of this reduction. It is difficult to reduce the noise floor to enhance the dynamic range. Three design parameters for sensor ADCs are important low chip area due to integration, needs to be low power and required dynamic range. There are several type of ADCs can be used for these applications, each with its own set

of trade off. The delta-sigma modulator ADC recommended for low bandwidth applications [2], [3], [4], [5]. The key advantage is high linearity with low-bit quantizer and feedback type implementation. It uses the mechanism of oversampling and noise shaping to get high resolution. The front-end of this ADC is analog while the output is completely digital, which is big advantage. This paper describes the design of third-order tri level quantizer delta-sigma modulator ADC for sensors system application with signal bandwidth of 10 kHz. Two different structures of the ADC discussed to trade-off the simplicity and ease of implementation with low power constraints.

2. Delta-Sigma Modulator Design

In this section the modeling and simualtion of CIFB and CIFF third-order tri-level delta-sigma modulator will be discussed [6],[7]. The design uses OSR of 128 . Higher order modulator is selected due to the demand of higher dynamic range requirement while tri-level quantizer is selected due to ease of implementation of digital-to-analog converter (DAC). First the CIFB structure is analyzed for dynamic range for maximum full scale as shown in Figure 1. The signal-to-quantization-noise-ratio (SQNR) versus input signal full scale is plotted. Two different curves are shown, one is unscaled dynamic range while second is sclaed with cofficient.It is found that the modulator can achieve maximum SQNR of 133dB, which is better to keep some margin. Figure 2 shows the NTF pole-zero plot on the unit circle in z-domain. It shows clearly that the NTF zero are at the DC for maximum suppression of quantization noise and effective noise shaping. While the poles of the modulator are inside the unit circle. Figure 3 shows the STF and NTF plot. The dotted line STF show flat at low frequencies as it is low pass modulator while NTF plots shows the noise shaping curve toward higher frquencies. Figure 4 shows the NTF plot with or without zero optimization. The dotted line curve shows without zero optimization. The

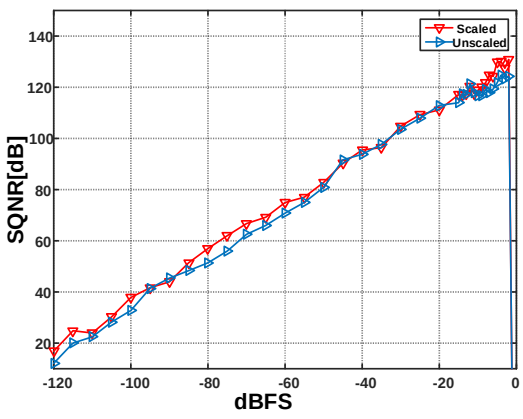


Figure 1: Dynamic Range

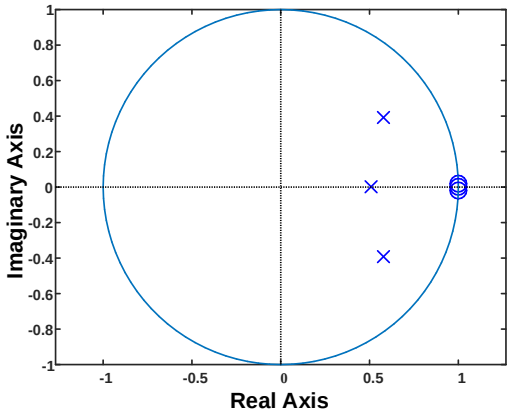


Figure 2: NTF Zero Plot On Unit Circle

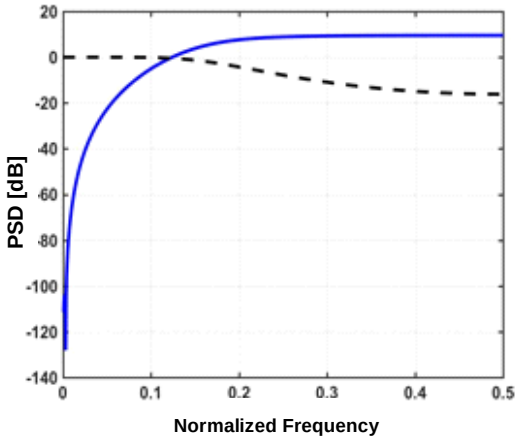


Figure 3: STF and NTF Plot For CIFB

zero optimization spread the NTF zero on DC to further enhance the SNR of the modulator, for third order it is about 8dB enhancement.

The Figure 5 shows the transient simulation output with input to show for three level quantiaztion as output. The output power spectral density (PSD) of the modulator shown in the figure 6. The figure 7 show the three integrators output states for the CIFB modulator. The swing inside the loop filter is large which demands high gain op-amp, which is power hungry. The large gain to suppress

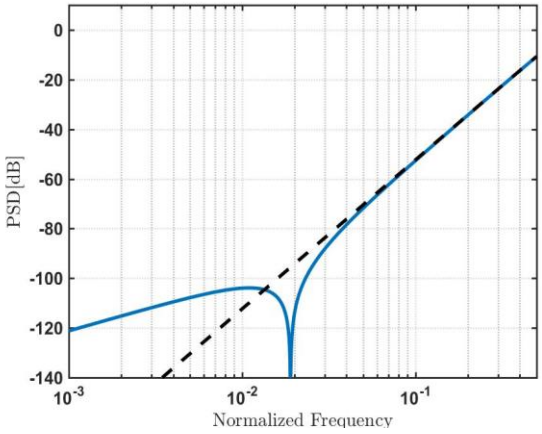


Figure 4: NTF Plot With /Without Zero Optimization

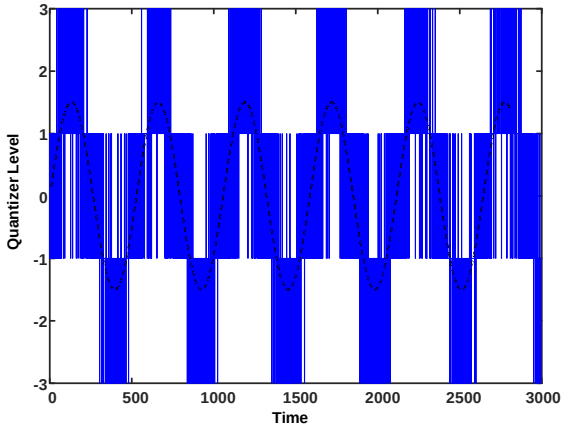


Figure 5: Transient Simulation

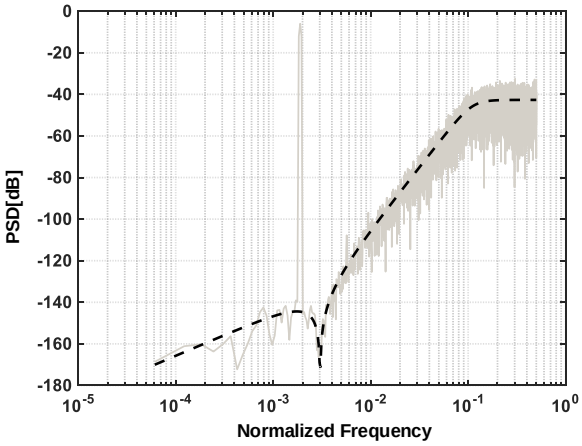
circuit non-idealities. In addition, nanoscale CMOS supply voltage is reducing putting more challenge for high gain op-amp design. Figure 8 shows the integrator output states for CIFF structure.

Table I shows the coefficient for the CIFB modulator for modeling and simulations.

Table 1: CIFB Structure Coefficient

i	a	b	c	g
1	0.3	0.3	0.6	$3.6x10^{-4}$
2	0.6	0	1	0
3	0.8	0	2.5	0

Delta-Sigma Modulator toolbox [8] used for modeling. Figure 8 shows the integrator output states for the CIFF



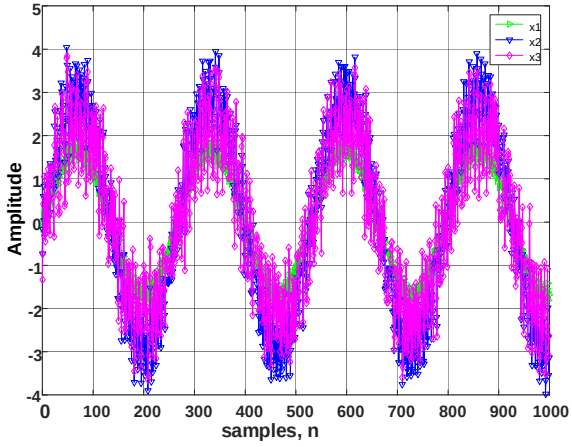


Figure 7: CIFB Integrators Output States

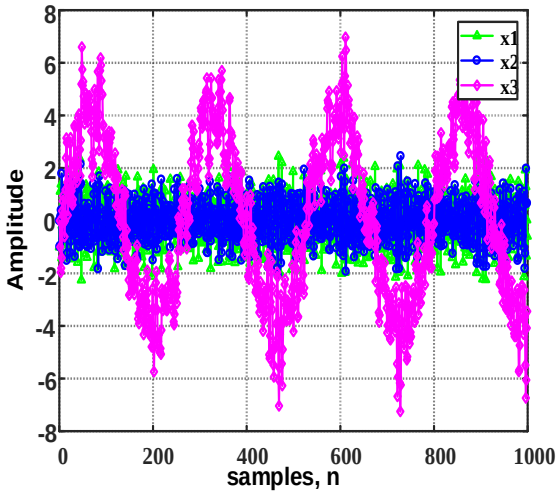


Figure 8: CIFF Integrator Output States

structure. First two integrators output are small while third integrator output swing is large. The key advantage of this structure is single feedback as it is multiple feedforward structure. It also requires one extra adder as op-amp. The first integrator design is not challenging as it has very small output processing only the quantization noise as the signal is feedforwarded to the adder in front of the quantizer. These design constraints to select CIFF modulator structure for further study. Table II shows the modulator coefficient for CIFF structure. The third-order tri-level modulator with these coefficients simulated, also considered non-idealities due to circuit implementation. Figure 9 shows the integrator op-amp dc gain simulation results performed in SDToolbox[9]. The reduced DC gain causes noise shaping degradation as a result SNR drops. Figure 10 shows the slew-rate simulation results. Limited slew-rate causes degraded noise shaping performance hence SNR drops. Figure 11 shows the bandwidth simulation of the three integrators and adder in front of the quantizer as dc gain is already fixed. The required bandwidth for the integrators is 15MHz, as the bandwidth decreased; quantization noise suppression at low frequencies degrades SNR.

Due to multi-bit quantizer, as it has three levels. Mismatch simulation for the modulator also performed and result are provide in figure 12. It shows that the front-end DAC is important and mismatch causes performance degradation.

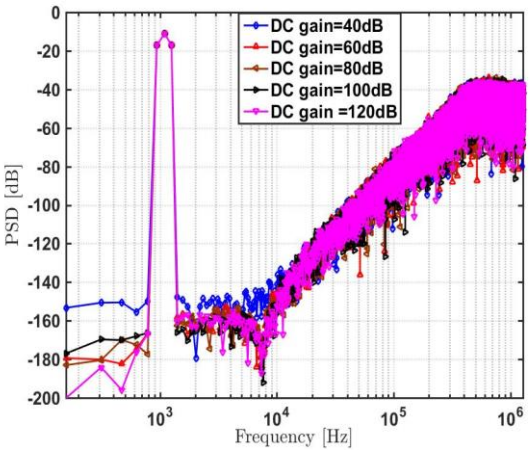


Figure 9: Op-amp Dc Gain Simulation

Table II: CIFF Structure Coefficient

i	a	b	c	g
1	2.6	0.7	0.7	0.0011
2	3	0	0.7	0
3	2.6	0	0.3	0

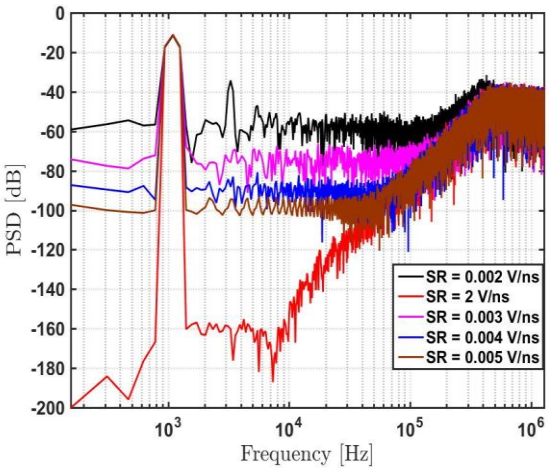


Figure 10: Slew-Rate Simulation

The circuit level implementation have many non-ideal effects like thermal noise kT/C, op-amp noise and front-end sampling switches nonlinearity [10]. To suppress the thermal noise non-ideality large capacitor required, hence more power hungry op-amp is needed to drives these large capacitors. To find an estimate the SNR of the modulator, the size of sampling capacitor C_s is varied for different non-ideal effects. The Figure 13 shows that modulator can achieve SNR of 112dB with all these non-idealities. The modulator ideally can achieve SNR of 133 dB without any non-ideal effects. Sampling jitter does not cause performance degradation due to discrete-time switched-capacitor implementation.

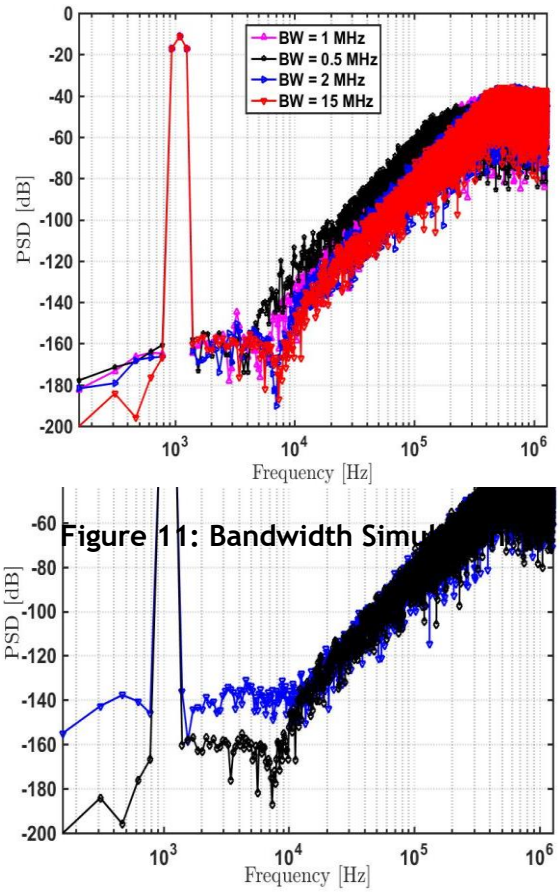


Figure 11: Bandwidth Simu

Figure 12: Quantizer DAC Mismatch

2. CONCLUSION

This paper discuss the modeling and simulation of CIFB and CIFF structure third -order tri-level modulator. Both structure can achieve SNR of 133dB. Due to small signal, swing inside the loop filter CIFF modulator selected for non-idealities simulation. It shows that modulator can achieve SNR of 112dB by considering thermal noise, sampling switch nonlinearity and op-amp noise. Op-amp dc gain, slew-rate and bandwidth is simulated and results are presented to estimate the performance degradation at the circuit level implementation.

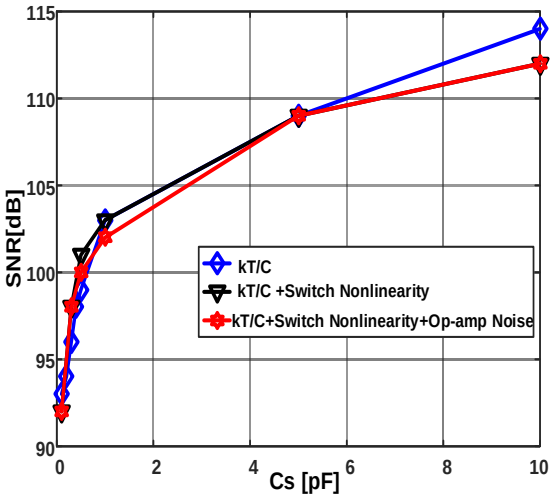


Figure 13: Non-ideal Effects

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