A low-voltage class-AB OTA exploiting adaptive biasing

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Abstract

We present a low voltage approach to design an adaptive bias circuit for a class-AB input stage, and exploit it to design a fully-differential 0.6V class-AB symmetrical OTA that also features cascode dynamic biasing and a class-AB CMFB circuit. Simulations in 0.13μm CMOS technology show a 42x increase of the bias current when signal is applied, that yields a faster settling time with respect to a class-A OTA designed with the same static current. The OTA provides 43.6dB gain and good large-signal FOM when compared with sub-1V OTAs in the literature, and is still operational at 0.4V supply voltage.

Keywords

Class AB, OTA, adaptive bias, low voltage, CMFB

1. Introduction

Very low power consumption is a fundamental requirement in many electronic applications, where the energy supply, coming from a battery or even harvested from the environment, is often limited; moreover, an excessive power dissipation could in some cases (e.g. biomedical applications [1]) result in excessive heating of the surrounding environment.

A class-AB operational transconductance amplifier (OTA) thus is a key building block for such applications, since it presents a very low quiescent power consumption, but is able to provide large peak output currents to allow fast transients or to drive small resistive loads. Different approaches have been proposed in the literature to design class-AB OTAs, and in particular class-AB input stages: an input transconductor based on four transistors with cross-coupled source terminals [2], a pair of transistors with opposite polarity signals applied both to the gate and to the source [3], or a source coupled pair with a tail current that depends on the input signal itself. Several solutions have been proposed for this latter approach, that differ in complexity, number of required additional current branches, and possible excursion of the current. The tail current can be generated by using some form of feedback [4], a Winner-Take-All (WTA) approach [5], by exploiting an estimate of the input common mode [6] or by using a replica stage [7]. A simple approach has been proposed by Stornelli et al in [8], with a separate adaptive bias circuit used to generate a variable tail current for the main stage: the proposed approach allows a very wide range for the tail current, but it is not compatible with a low voltage implementation.

Reducing the supply voltage is often required to reduce power consumption [9], to allow the use of batteries and power harvesting, and to simplify interfacing with digital blocks, and amplifiers with 0.6V supply or less have been presented in the literature for biomedical applications [10] or voltage references [11]. In this paper we propose a modified version of the adaptive bias block in [8], that is able to operate in a very low voltage environment, and to demonstrate its application we use it to design a fully-differential class-AB symmetrical OTA, featuring also a class-AB common-mode feedback (CMFB) stage. The paper is structured as follow: Section 2 reviews the basic principle of

the adaptive bias approach in [8], and presents the modified low voltage version. The design of the OTA with the class-AB CMFB is discussed in Section 3, and Section 4 presents simulation results in a 0.13-μm CMOS technology. Conclusions are drawn in Section 5.

2. Class-AB approach by replica adaptive biasing

The approach used in [8] to generate the adaptive bias current exploits the properties of the current mirror stage [12]. With reference to Fig. 1, a copy of the differential input signal $V_{id}=V_1-V_2$ is applied to the sources of a current mirror biased with a very low reference current I_B: supposing identical devices M_1 and M_2, the output current of the mirror is I_B when no differential input is applied, and in general it depends on the input differential voltage V_{id} according to:

$$I_o = \begin{cases} K\left(V_{id} + \sqrt{I_B/K}\right)^2 & \text{for } V_{id} > -\sqrt{I_B/K} \\ 0 \quad \text{otherwise} \end{cases} \tag{1}$$

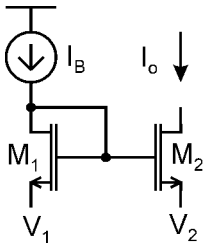

Figure 1: Core of the adaptive bias stage.

For positive V_{id}, a current much larger than I_B is generated, whereas for negative V_{id} the output current of the mirror drops to zero: two such mirrors with cross-coupled input signals are thus needed to increase the bias current when a differential input signal is applied, whatever its polarity. The overall bias current I_{BIAS} is thus given by

$$I_{BIAS} = \begin{cases} 2\left(I_B + KV_{id}^2\right) & \text{for } |V_{id}| < \sqrt{I_B/K} \\ K\left(|V_{id}| + \sqrt{I_B/K}\right)^2 & \text{otherwise} \end{cases} \tag{2}$$

and quiescent current is $2I_B$.

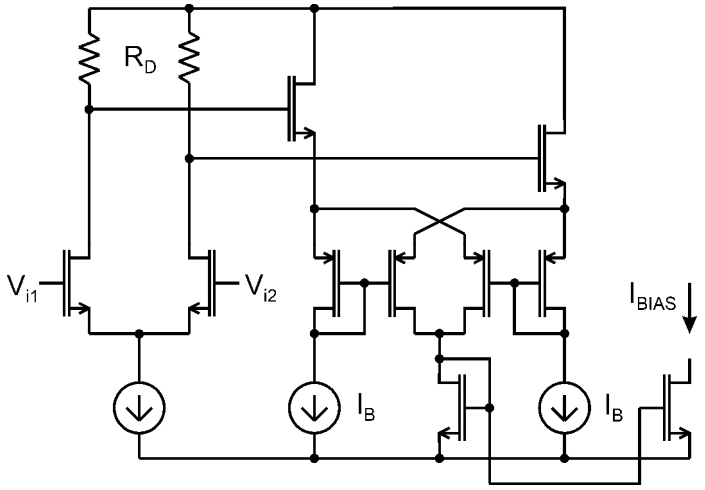

Figure 2: Adaptive bias stage in [8].

The input differential signal has to be buffered to interface the current mirrors, to avoid reducing the input impedance of the stage that exploits this biasing approach: in [8] a dummy differential pair with resistive load R_D, followed by source followers, is used as shown in Fig. 2. This requires a minimum supply voltage of

$$\Delta V + 2V_T + 3V_{ov} \tag{3}$$

where ΔV is the voltage drop on the resistors R_D and determines the maximum current for a given input voltage swing, and V_T and V_{ov} are threshold voltage and overdrive of the transistors; the resulting value could be too high to allow operation in a very low-voltage environment. To overcome this limitation, this input interface has to be modified. A lower minimum supply voltage can be achieved by substituting the buffer stage by a flipped voltage follower (FVF) [13], as shown in Fig. 3. The minimum supply voltage reduces to

$$V_{SD1} + V_T + 2V_{ov} \tag{4}$$

where V_{SD1} can be low, since M_1 can be biased in triode region, and has to be chosen as a trade-off between supply voltage and voltage swing at the sources of the current mirror. For the same voltage

swing (i.e. $V_{SD1}=\Delta V$), (3) and (4) show that a net reduction of the minimum supply voltage is achieved: the proposed solution allows lowering the minimum supply voltage of a $V_{GS}=V_T+V_{ov}$. Current in M_1 is not constant, resulting in a nonlinear buffering of the input differential signal to the sources of the current mirrors, but this is not an issue since the relationship between the voltage across the sources and the current, given by (2), is nonlinear anyway.

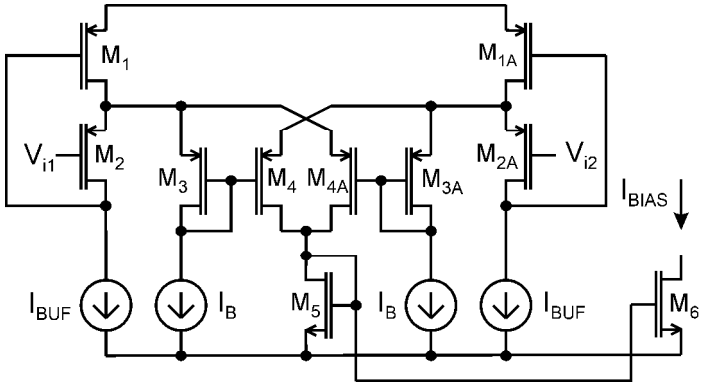

Figure 3: Proposed adaptive bias stage.

3. Class-AB OTA based on adaptive biasing

The adaptive biasing circuit shown in Fig. 3 has been exploited to design a fully differential class-AB OTA: a symmetrical OTA topology has been adopted, since it requires a single bias current source, thus it can be easily biased by the designed adaptive bias circuit. Moreover, the symmetrical OTA topology is easily suited for class-AB behavior, and is often used in class-AB designs [14]. To allow full class-AB operation, the output current of the input NMOS transconductor is not only mirrored to the output branches using PMOS current mirrors, but NMOS current mirrors are also used so to avoid constant current generators [14].

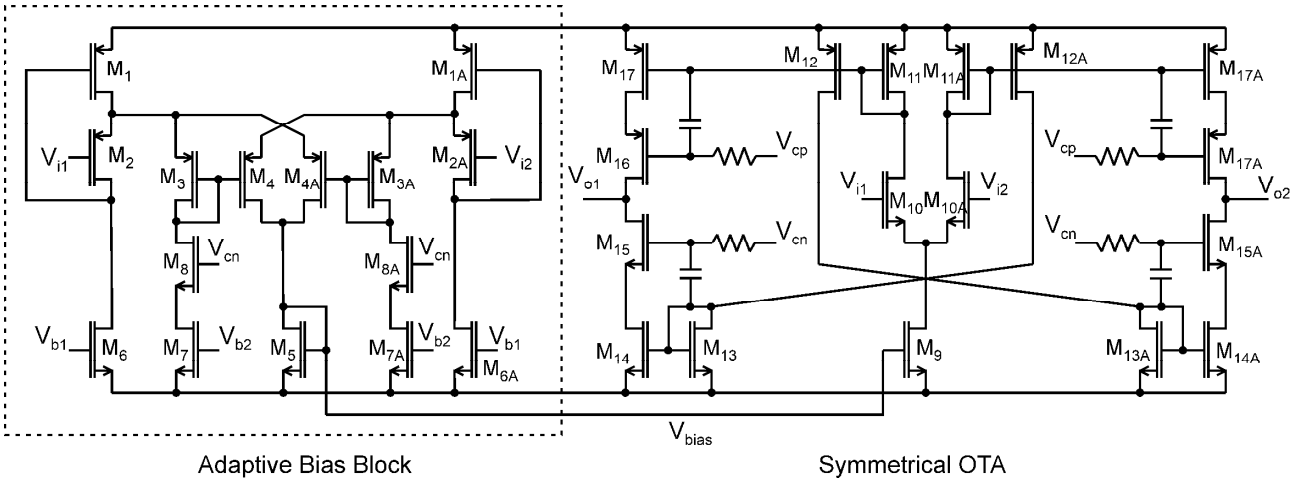

Figure 4: Fully differential OTA with proposed adaptive bias.

Fig. 4 shows the schematic of the OTA with the adaptive biasing circuit; cascoding has been used in the output branches to increase the output resistance and the gain of the OTA. A quiescent operating point in subthreshold region has been chosen for all the devices to minimize power consumption. However, to manage the large dynamic increase of the current due to the adaptive biasing circuit, a dynamic biasing technique [15] has been adopted for the cascoding devices, to avoid driving the transistors in triode region, limiting the output current. Small capacitors (to limit Silicon area) dynamically couple the gates of the cascoding devices with the gates of the common sources, resulting as constant voltage sources for high frequency transients, and large resistors are used to apply the quiescent bias voltage.

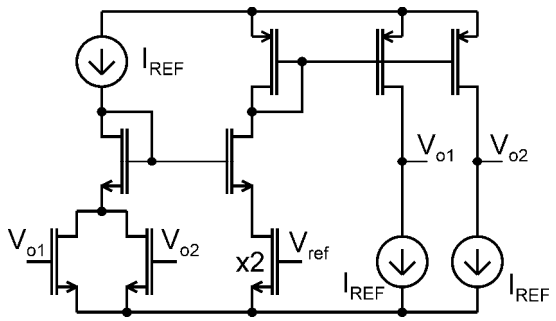

Figure 5: Simplified schematic of the CMFB circuit.

A common-mode feedback (CMFB) has to be used to impose the dc output voltage and improve the common-mode rejection ratio (CMRR). Since there is no current source that can be controlled by the CMFB, and the output is the only high-impedance node, a possible solution is to implement the CMFB as current sources in parallel to the output nodes, controlled by the difference between the output common-mode voltage and a reference voltage. Fig. 5 shows a simplified schematic of the CMFB, where the triode approach is used to compare the voltages; cascoding (not shown in Fig. 5) is used to increase the output impedance to not reduce excessively the gain of the main amplifier. To minimize power consumption, a class-AB approach is used also for the CMFB, by exploiting the adaptive bias block also to control the matched current sources I_{REF}: a low quiescent value is used, compatible with the possible quiescent current mismatches in the output branches of the OTA, but the circuit is able to provide much larger currents when the signal is applied to the OTA and the output currents increase.

4. Simulation results

The proposed fully differential class-AB OTA, exploiting the adaptive biasing technique and a class-AB CMFB, has been designed and simulated in 0.13-µm CMOS technology by STMicroelectronics. Tab. 1 reports the sizes for all the devices, with reference to Fig. 4 (main amplifier with adaptive biasing) and Fig. 6, that shows the CMFB circuit. Devices with 2 or 3 times the minimum gate length have been used where needed to increase their output resistance. Supply voltage V_{DD} is 0.6V, and quiescent currents about 100nA have been chosen; 50fF MIM (metal-insulator-metal) capacitors and 100kΩ high-resistivity polysilicon resistors are used for the dynamic biasing of the cascode devices, and 6pF load capacitances have been considered.

Table I: Device sizes.

Devices	**W / L [μm]**
M_1, M_{1A}	0.45 / 0.13
M_2, M_{2A}	4.5 / 0.13
M_3, M_{3A}, M_4, M_{4A}	2.1 / 0.13
M_5, M_9	0.6 / 0.13
M_6, M_{6A}	1.8 / 0.13
M_7, M_{7A}, M_8, M_{8A}	0.3 / 0.13
M_{10}, M_{10A}	0.9 / 0.39
M_{11}, M_{11A}, M_{17}, M_{17A}	0.975 / 0.26
M_{12}, M_{12A}	0.92 / 0.26
M_{13}, M_{13A}, M_{14}, M_{14A}	0.75 / 0.39
M_{15}, M_{15A}	0.61 / 0.39
M_{16}, M_{16A}	2.01 / 0.26
M_{18A}, M_{18B}, M_{19A}, M_{19B}	1 / 0.39
M_{20}, M_{20A}	0.15 / 0.39
M_{21}, M_{21A}	0.2 / 0.39
M_{22}, M_{22C}	0.9 / 0.39
$M_{23\text{-}30}$, M_{29A}, M_{30A}	2.5 / 0.39
M_{31}, M_{31A}, M_{32}, M_{32A}	0.2 / 0.39
M_{33}, M_{34}	0.2 / 0.39
M_{35}, M_{36}	2.5 / 0.39

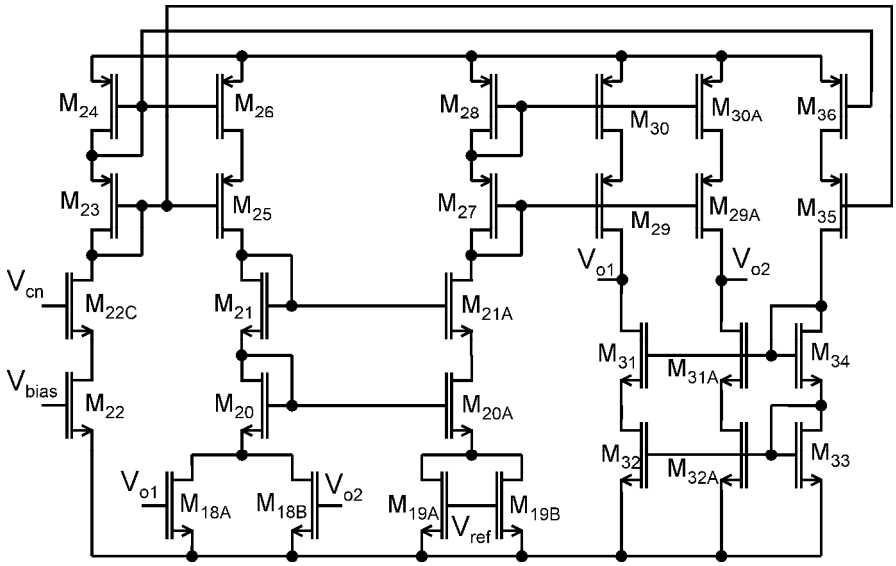

Figure 6: Complete schematic of the CMFB circuit.

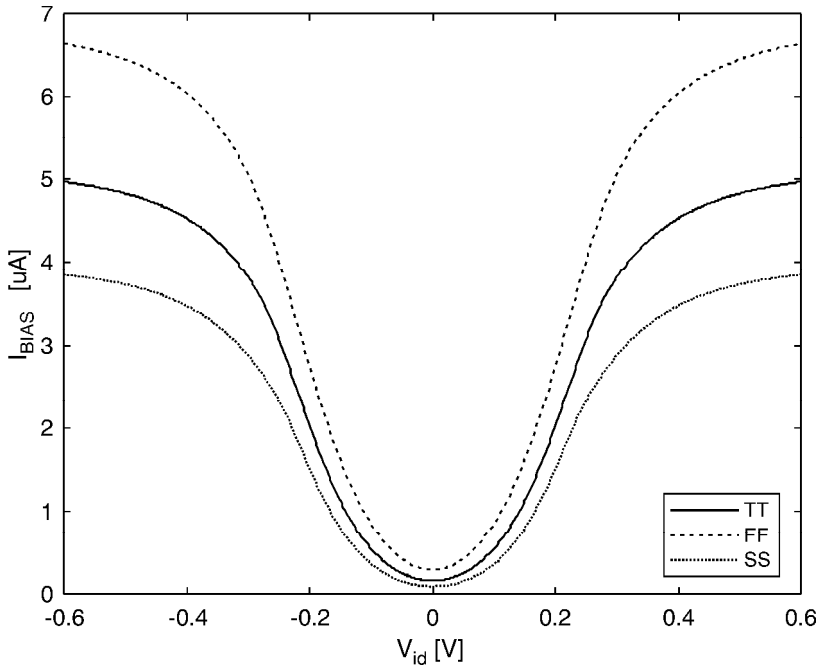

Figure 7: Characteristics of the adaptive bias stage vs. process corners.

Fig. 7 illustrates the behavior of the adaptive bias block, reporting the tail current of the differential pair (i.e. current I_{BIAS} in Fig. 3) as a function of the differential input voltage V_{id}. A net increase of the current with the absolute value of the input differential voltage is observed, as predicted by (2), up to a differential input of about 250 mV. For larger differential inputs, transistors M_1 and M_{1A} get

into deep triode region and the current tends to saturate. In typical conditions, Fig. 7 shows a 42x increase from the quiescent value of 138nA to about 5.8µA. This very large range for the bias current allows very low static power consumption, but fast transients when the load capacitors are charged and discharged. Fig. 7 also shows the effect of process variation, reporting the I_{BIAS} curves for the extreme FF and SS process corners: a ±25% variation of the maximum current is achieved, due to the small sizes of the devices.

The main performance parameters of the OTA in typical process conditions are reported in Tab. II, and Fig. 8 shows the differential mode and common mode frequency responses. The effect of process and supply voltage variations is reported in Tab. III: the variation of the bias current reflects in a variation of the unity-gain frequency f_u, and this effect could be compensated by controlling the current generators I_B in Fig. 3. Fig. 9 shows the results of Monte Carlo simulations, highlighting a good stability of voltage gain and slew rate, and the link between variation of the bias current and of the unity-gain frequency; Fig. 10 shows the dependence on the temperature.

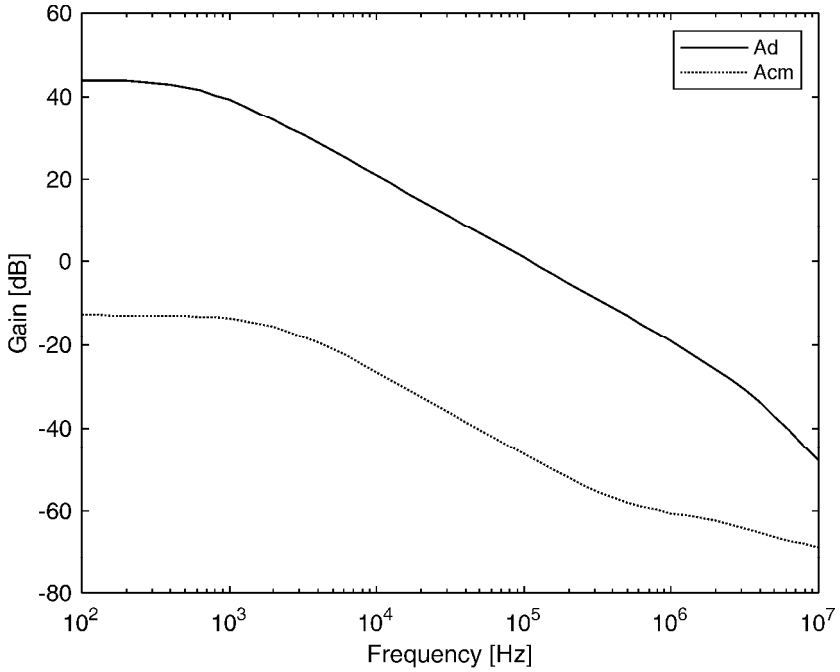

Figure 8: Differential and common-mode gain of the OTA.

Table II: OTA performance parameters and comparison with class-A design.

Performance	Class-AB OTA	Class-A OTA	Class AB (0.4Vdd)
Supply Voltage	0.6 V	0.6 V	0.4 V
Differential Gain	43.86 dB	43.86 dB	32.97 dB
Common-mode Gain	-12.76 dB	-17.5 dB	-8.01 dB
Unity-gain Frequency	112.9 kHz	113 kHz	33.14 kHz
Phase Margin	88.8°	90°	90°
Quiescent Current	3.005 µA	1.55 µA	1.073 µA
Output Swing	-294 – 291 mV	-294 – 291 mV	-180.4 – 189.2 mV
Slew Rate	0.845 V/µs	0.073 V/µs	0.181 V/µs
Settling Time (1%)	3.103 µs	20.66 µs	17.54 µs
Peak Output Current	2.8 µA	0.229 µA	0.84 µA

Table III: OTA performance vs PVT.

Corner	Temp [°C]	V_{DD} [V]	A_d [dB]	f_u [kHz]	Iq [µA]	SR [V/µs]	$I_{BIASmin}$[nA]
TT	27	0.6	43.86	112.9	3.005	0.845	138.6
FF	27	0.6	43.55	197.8	5.242	1.017	243.6
SS	27	0.6	37.96	64.12	1.908	0.638	81.3
SF	27	0.6	47.39	109.7	3.006	0.754	149.1
FS	27	0.6	42.53	118.3	3.006	0.848	130.9
TT	27	0.57	42.49	100.8	2.724	0.726	126.8
TT	27	0.63	45.89	123.9	3.289	0.955	150

A_d=differential gain

f_u=unity-gain frequency

Iq=quiescent current of the OTA including bias and CMFB

$I_{BIASmin}$=quiescent value of the bias current from the adaptive bias block

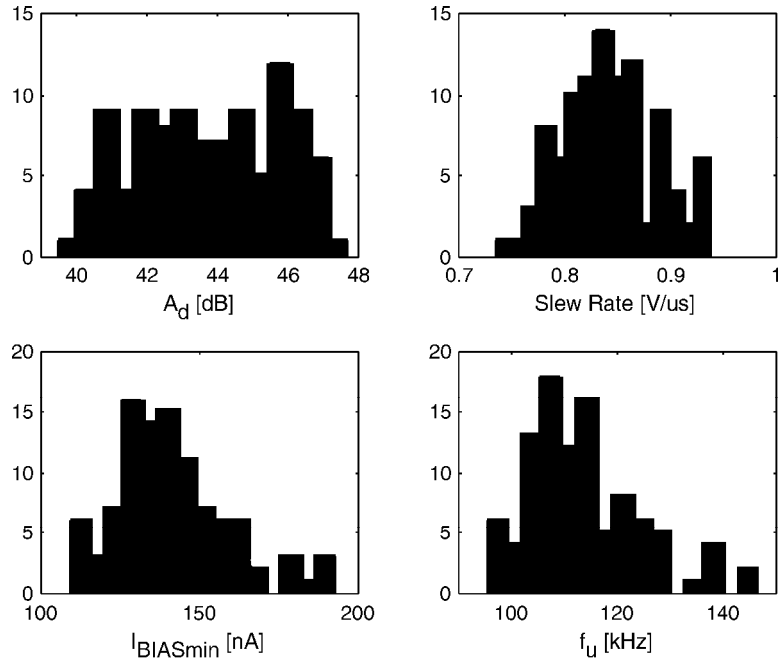

Figure 9: Histograms of differential gain, Slew Rate, quiescent tail current and unity-gain frequency.

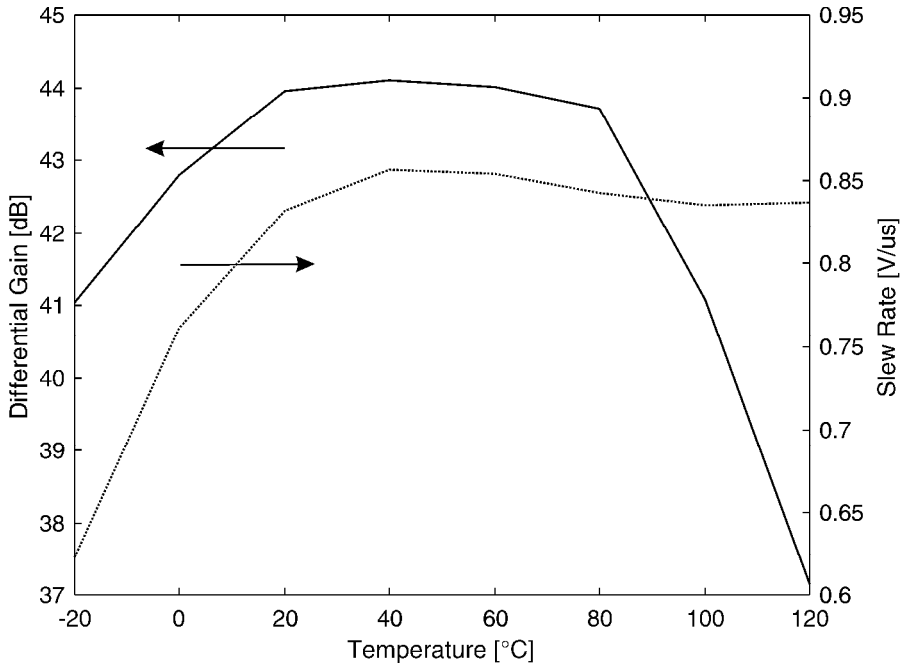

Figure 10: Differential gain and slew rate as a function of temperature.

To verify the class-AB behavior and the large signal performance of the amplifier, the OTA has been used in buffer configuration with 100MΩ feedback resistors; a class-A version of the OTA, featuring a constant 138nA tail current generator, constant current sources in the CMFB, and without the R-C groups on the cascodes, has been also designed and simulated for comparison, and Tab. II reports the main performance parameters. The increased DC power consumption of the class-AB amplifier is due to the adaptive biasing block. Fig. 11 shows the step response of both amplifiers, highlighting the advantage of the class-AB in terms of faster response. The class-A OTA is severely limited by the slew rate, due to its low bias current (equal to the quiescent current of the class-AB version), providing a much slower response to a step input. As reported in Tab. II, the class-AB OTA presents a 11.6x higher slew rate and a 6.7x shorter settling time. Fig. 12 shows the output currents for both amplifiers that justify these results: during the slewing phase, the class-A OTA provides a constant current of 229 nA to charge the capacitors, whereas the class-AB version is able to provide a 12x higher peak current, that however drops as the capacitors are charged and the differential output voltage settles.

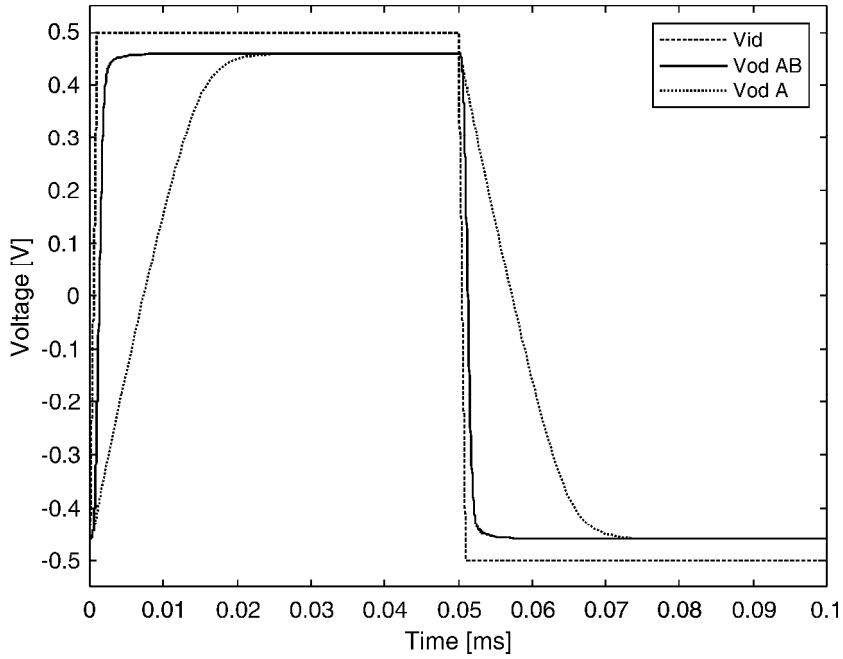

Figure 11: Step response of the OTA in unity-gain configuration.

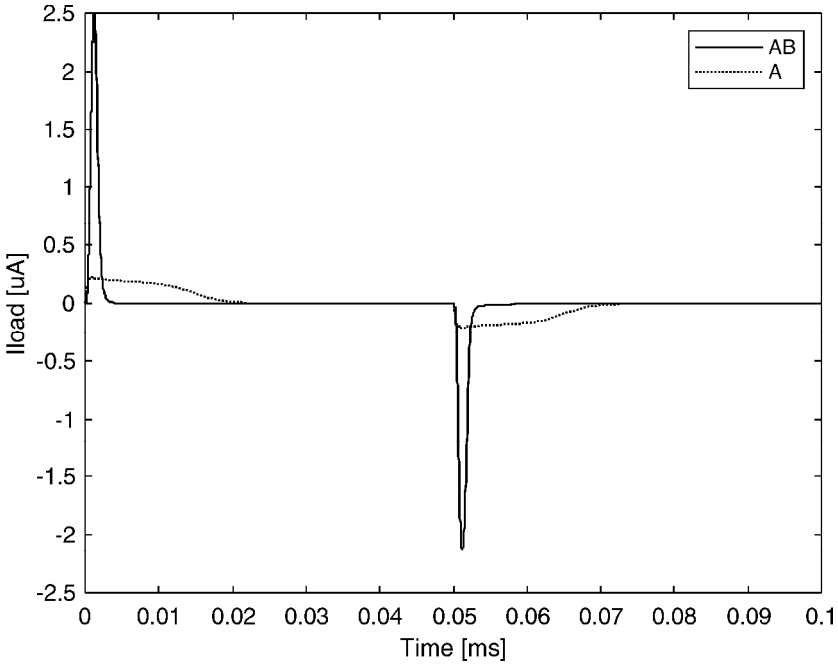

Figure 12: Output currents of the OTA for class-AB and class-A design.

The amplifier is able to operate at lower supply voltages, with reduced performance but a still acceptable gain: Tab. II reports also the simulated performance for a 0.4V voltage supply. The voltage gain reduces to about 33 dB and the unity-gain frequency to 33 kHz; obviously the lower supply voltage reduces the voltage swing at the sources of the current mirrors in the adaptive bias block, thus peak output current and slew rate, that however is still 2.5 times that of the class-A OTA at 0.6V supply.

5. Conclusions

In this paper we have proposed a modification of an adaptive bias class-AB topology to allow operation in a very low voltage environment; the proposed adaptive bias block has been used to design a 0.6V fully differential symmetrical OTA with a class-AB CMFB. The proposed amplifier allows a 11.6x increase of the slew rate of a class-A amplifier biased with the same quiescent current, with a consequent reduction of the settling time, at the cost of an auxiliary circuit that requires about 1.5μA.

The bias circuit is able to operate at very low supply voltages, and the whole OTA still shows interesting performance at 0.4V voltage supply.

The performance of the proposed OTA is compared in Tab. IV with results from the literature relative to low voltage amplifiers: the standard small-signal and large-signal figures of merit (FOMs) have been used for comparison, defined as:

$$FOM_S = f_u C_L / Iq \tag{5}$$

$$FOM_L = SR\ C_L / Iq\ . \tag{6}$$

Tab. IV shows that the proposed OTA presents performance in line with the state of the art for what concerns FOM_L, and is outperformed by some of the realizations using higher supply voltages: in fact, in class-AB OTAs the peak output current is often limited by the supply voltage, so amplifiers using higher supply voltages easily provide higher slew rates and shorter settling times. Among the very low-voltage OTAs, the topology by Kulej in [32] presents very high values of the FOM_L, but is based on a bulk-driven approach that could present limitations in some applications due to the input impedance that does not result fully capacitive. The value of FOM_S is lower than most of the other OTAs in the table, and this is due to the fact that the OTA was not optimized for small-signal performance. Figs. 13 and 14 synthesize data in Tab. IV, highlighting the link between supply voltage and the FOMs.

Table IV: Comparison of OTA performance.

Ref.	**CMOS**	**V_{DD}**	**P_d**	**A_d**	**C_L**	**f_u**	**minSR**	**FOMs**	**FOM_L**
[16]	180	0.8	1.2	51	8	57	140	0.304	0.747
[17]	350	1	197	88.3	15	11670	1370	0.889	0.104
[10]	130	0.25	0.018	60	15	1.88	0.64	0.392	0.133
[18]	65	0.35	17	43	3	3600	5600	0.222	0.346
[19]	180	0.5	0.074	99.8	15	6.26	6.35	0.634	0.643
[20]	180	0.7	25.4	57.5	20	3000	1800	1.653	0.992
[21]	180	0.5	0.07	77	40	4	2	1.143	0.571
[22]	45	1	12	100	1	25000	-	2.083	-
[23]	130	0.25	0.02	63	15	6.23	2.15	1.168	0.403
[24]	350	0.9	24.3	65	10	1000	250	0.37	0.092
[25]	180	1	50	78.6	140	2020	8100	5.656	22.68
[26]	130	1	15	58.7	50	10430	3720	34.77	12.4
[27]	40	0.6	15.73	41.3	5	8260	-	1.575	-
[28]	65	0.3	0.051	60	5	70	25.5	2.059	0.75
[29]	180	0.6	0.145	71	15	18.2	6.6	1.13	0.41
[30]	180	0.6	0.18	75.4	20	74.3	5.65	4.951	0.377
[31]	40	0.6	30	60.2	1	45000	18200	0.9	0.364
[32]	180	0.3	0.0126	64.7	30	2.96	1.9	2.114	1.357
[33]	180	0.4	0.3	81.4	5	280.4	125	1.869	0.833
This work	130	0.6	1.8	43.9	6	112.9	845	0.226	1.69
	130	0.4	0.43	33	6	33,14	181	0.185	1.01
	nm	V	µW	dB	pF	kHz	V/ms	MHz.pF/µA	(V/µs)pF/µA

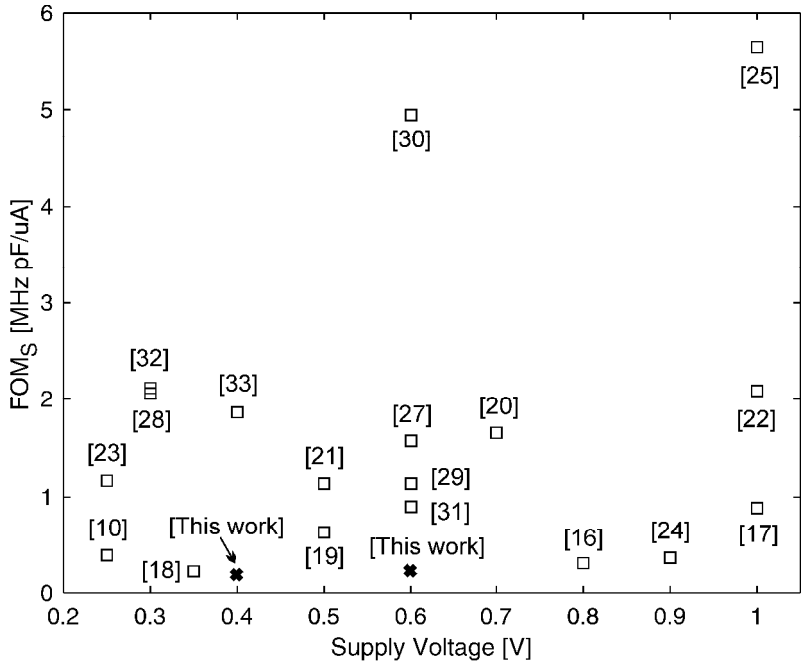

Figure 13: Values of FOM_S from the literature as a function of supply voltage (the value for [26] is out of scale).

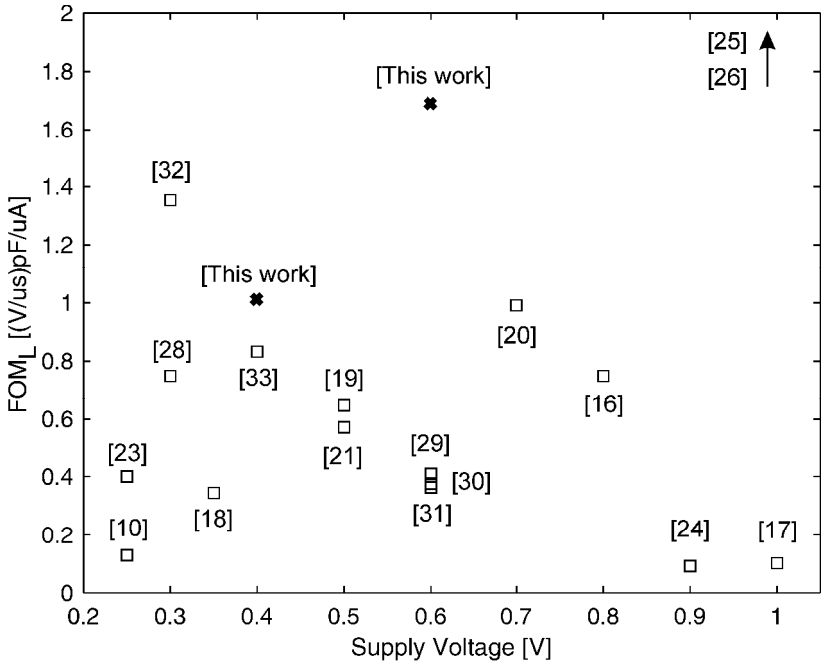

Figure 14: Values of FOM_L from the literature as a function of supply voltage (the values for [25] and [26] are out of scale).

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