Delay models and design guidelines for MCML gates with resistor or PMOS load

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Abstract

In this paper we present propagation delay models for MCML gates with resistor- or triode-PMOS-based output I-V conversion. The dependence of the parasitic capacitance of triode PMOS devices is accurately evaluated for the first time in the literature. The proposed models are able to accurately predict the propagation delay as a function of the bias current I_{SS} in different design scenarios which require different tradeoffs between speed, area and power efficiency. The proposed models are validated against transistor level simulations referring to a 28nm CMOS process showing a maximum percentage error lower than 6.5%. Based on these models, a comparative analysis is carried out and useful guidelines for the design of MCML gates are proposed.

1. Introduction

The increasing demand for high-speed circuits, often to be operated in a mixed-signal environment, has led to the development of logic families able to go beyond the limits of traditional CMOS, in terms of speed and noise. Evolving from the Emitter-Coupled Logic (ECL) and from GaAs logic families such as Source-Coupled FET Logic (SCFL) [1], the Current-Mode Logic (CML) has become the logic style of choice for extremely high frequency applications, followed in the 90s by its MOS counterpart, the MOS Current-Mode Logic (MCML) [2].

The CML/MCML logic style presents the benefits of a very high maximum operating frequency, low di/dt noise and low sensitivity to common-mode disturbances, making it suitable to a mixed-signal environment. Differently from CMOS, the power consumption is independent from frequency and switching activity: this implies that there is a static power consumption, but for high frequencies the MCML family could become more efficient than CMOS [3]. For these reasons, the CML/MCML logic family has been extensively used, typically in mixed-signal integrated circuits for applications where maximum frequency and signal integrity are the main goals, such as CORDIC circuits [4], optical communication transceivers [5-6], frequency synthesizers [7] and high-speed data converters [8]. With CMOS technology scaling, signal integrity and power dissipation have become critical limitations on microprocessor performance, and the MCML logic style has been demonstrated to be a valid alternative to CMOS for full digital applications even at frequencies where CMOS logic style could still be operated [9].

Models for CML [10-12] and subsequently MCML gates [13-15] have been proposed in the literature to develop design guidelines, with the main aim of optimizing the Power-Delay Product (PDP), that is a key FOM for digital applications. These guidelines are typically based on hypotheses that make sense for extremely high-speed mixed-signal applications, where this logic style was first used and maximum operating speed is often the main goal, but that could be not adequate when MCML logic family is used to design VLSI digital circuits like, for example, a whole throughput-oriented processor. Indeed, in this last scenario power and area consumption are often of greater

interest than maximum operating frequency, and a standard-cell based approach is a must to cope with the complexity.

In this paper, taking into account the different MCML application contexts, we analyze and compare the design of MCML logic gates considering the two most commonly adopted circuit topologies to converter the switched current into the output voltage (i.e. resistive or PMOS load). Propagation delay models have been specifically derived for both MCML gate topologies. These models allow to compare the two I-V conversion approaches in terms of speed, area and power efficiency and to provide interesting design considerations and guidelines to optimize the tradeoff between the different specifications. We also compare the effect of a constant load capacitance versus a load capacitance that scales with the bias current of the MCML standard cell, as would be the case in a highly integrated environment with each MCML gate driving one or more identical stages.

The paper is structured as follows: Section 2 briefly reviews the MCML logic style, Section 3 presents the models of the MCML inverter propagation delay under the different I-V conversion approaches and load conditions, and Section 4 discusses the design tradeoffs and guidelines in the different considered scenarios. Conclusions are drawn in Section 5.

2. MCML logic family

Fig. 1a shows the schematic of a MCML inverter: it is composed by a NMOS differential pair with a constant bias current source I_{SS} and a pair of pull-up resistors R_D. Load capacitances C_L model the input capacitance of the following stage and the parasitic capacitance of the interconnections.

The differential pair acts as a current switch controlled by the differential input voltage that steers the bias current I_{SS} to one of the output branches, and the pull-up resistors convert the current into a differential output voltage. The branch to which the current is steered results in the low output voltage $V_{DD}-I_{SS}R_D$, whereas the other branch results in the high output voltage V_{DD}, thus the logic level results

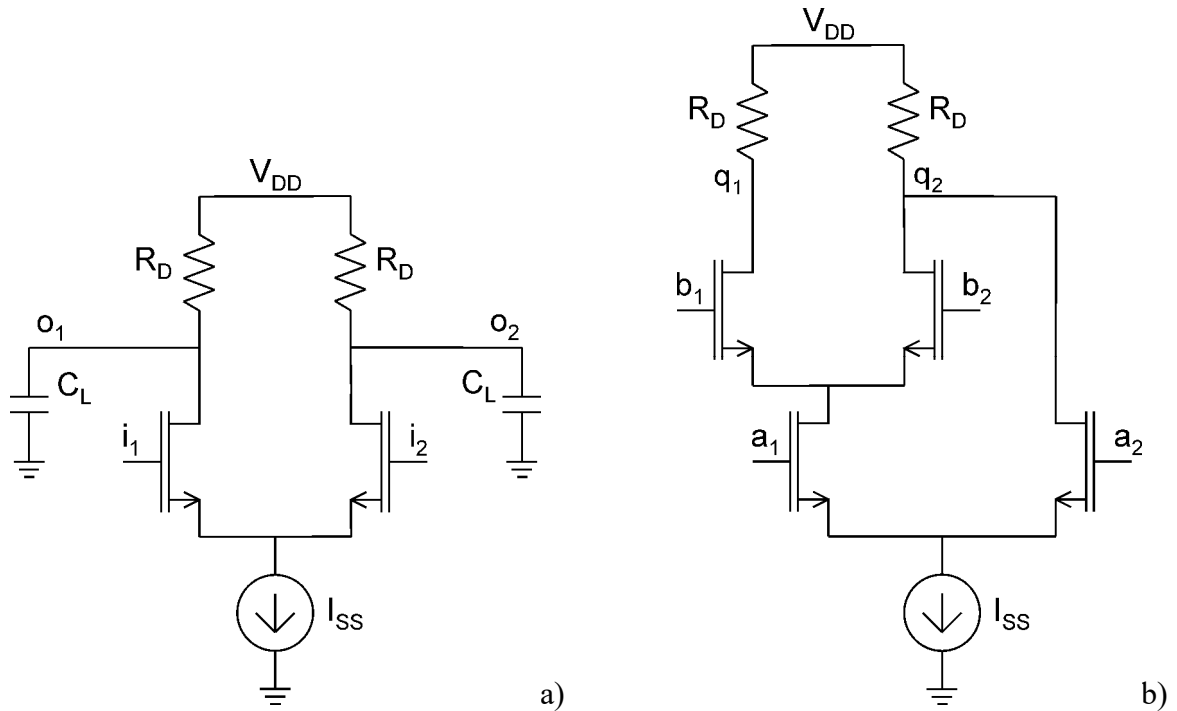$$\pm\Delta = R_D I_{SS} \tag{1}$$

providing a voltage swing

Figure 1: Schematic of MCML gates: a) inverter; b) AND/NAND.

$$V_{swing} = 2\Delta \ . \tag{2}$$

More complex logic functions can be obtained by using a series gating technique where differential pairs are stacked and used as current switches in series (an example for a 2-input logic gate is shown in Fig. 1b) [16]. Source followers are often used as level shifters to connect the output of a logic cell to the lower input of the following one. The stacking of differential pairs could in principle go ahead limited only by the available supply voltage, but common practice is to use only two levels (i.e. 2-input logic gates) to minimize the voltage [17]-[18]. When the CML logic family is implemented in CMOS technology (typically referred to as MCML or SCL), p-channel devices can be used in place of resistors to perform the current to voltage conversion at the output of the gate.

In conventional CMOS processes passive resistors R_D are usually implemented by means of polysilicon strips suitably doped to control their resistivity[1]. Since these strips introduce a parasitic

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[1] Polysilicon does not pose electromigration issues, however it is good practice to limit the current density to avoid excessive localized heating of the chip. In particular, maximum current densities of the order of 1-2 mA/μm are a safe choice in current technologies, and the minimum resistor width is set by layout rules.

capacitance to the substrate C_{RTOT}, they can be modeled by lumped RC networks with a capacitance $C_{RD}=C_{RTOT}/3$ [13].

If we now consider a triode-biased PMOS device, its small-signal resistance can be estimated using the standard BSIM3v3 MOSFET model as [19]

$$R_D = \frac{R_{\text{int}}}{1 - R_{DS}/R_{\text{int}}} \tag{3}$$

where $R_{DS}=R_{DSW}/W_p$ depends on the empiric model parameter R_{DSW}, which accounts for source-drain parasitic resistance, and

$$R_{\text{int}} = \left[\mu_{eff,p} C_{OX} \frac{W_p}{L_p} \left(V_{SG} - |V_{Tp}| \right) \right]^{-1} \tag{4}$$

represents the intrinsic resistance of the PMOS in triode region (parameters in (4) have the usual meaning). The gate can be connected to ground to minimize resistance, thus $V_{SG}=V_{DD}$ in (4), or to a suitable control voltage which can be distributed across the whole MCML core in order to compensate PVT (process, supply voltage and temperature) variations in digital applications.

It is worth noting that the PMOS devices also introduce a capacitive effect to ground, due to the parasitic capacitances between the channel and the gate and the channel and the substrate. Such capacitances are proportional to PMOS channel width W_p; more specifically, the gate-drain capacitance C_{gdP} can be estimated as [20]:

$$C_{gdP} = C_{gdP0}W_p + C_{gdP,\text{int}} \tag{5}$$

where the first term is the overlap contribution and the second one is the intrinsic contribution associated with the channel charge of the PMOS, given by

$$C_{gdP,\text{int}} \cong \frac{3}{4} A_{bulk,\max} W_p L_p C_{OX} . \tag{6}$$

3. MCML propagation delay models

Without loss of generality, we consider the delay of a MCML inverter gate (Fig. 1a), and estimate it by linearizing the circuit; then we apply the open-circuit time-constant method [21]. By following this approach, the propagation delay results:

$$t_{PD} = \tau \ln 2 \tag{7}$$

where τ is the circuit time constant. For the MCML inverter in Fig. 1a, the time constant can be calculated by referring to the small-signal differential half circuit in Fig. 2 as

$$\tau = R_D \left(C_{NMOS} + C_{RD} + C_L \right) \tag{8}$$

where

$$C_{NMOS} = C_{gdN} + C_{dbN} = C_{drain0} W_n \tag{9}$$

summarizes all the capacitive effects of the NMOS pull-down network, W_n is the width of NMOS devices, C_{RD} is the parasitic capacitance of the load resistor, C_L is the load capacitance, and we are neglecting r_{oN} with respect to R_D.
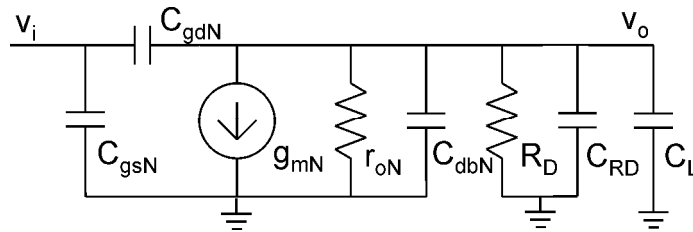

Figure 2: Small-signal half circuit for the analysis of the inverter delay.

A more complex expression can be obtained for C_{NMOS} if the effect of the zero due to C_{gdN} is taken into account [13]. Moreover, in case of more complex MCML gates, a similar result is obtained, since (8) is still valid, and the increased complexity reflects only in a different expression for C_{NMOS} [13]. Anyway, in all cases, C_{NMOS} is proportional to the width of the NMOS devices.

Design guidelines for MCML logic gates have been previously presented in [13] and [20]. These approaches start by setting the value of the logic swing in (2) and the desired value of the noise margin NM:

$$NM = \frac{V_{swing}}{2}\left(1 - \frac{\sqrt{2}}{A_V}\right). \tag{10}$$

Inverting (10), the value of the small signal gain A_V can be found. Then, assuming a quadratic model for MOS devices, and remembering that

$$\left(\frac{A_V}{V_{swing}}\right)^2 = \left(\frac{g_{mN}R_D}{2I_{SS}R_D}\right)^2 = \left(\frac{\sqrt{KI_{SS}}}{2I_{SS}}\right)^2 = \frac{K}{2I_{SS}} = \frac{1/2\mu_{eff}C_{OX}W_n/L_n}{2I_{SS}}, \tag{11}$$

the width W_n, of NMOS transistors of the differential pair can be derived as follows:

$$W_n = 2I_{SS}\left(\frac{A_V}{V_{swing}}\right)^2 \frac{2L_n}{\mu_{eff}C_{OX}}. \tag{12}$$

These results, which could be easily generalized to the case where the alpha-power MOS model is used [13], show the dependence of W_n on I_{SS} and allow to express (9) as:

$$C_{NMOS} = C_{drain0}W_n = C_{drain0}2I_{SS}\left(\frac{A_V}{V_{swing}}\right)^2 \frac{2L_n}{\mu_{eff}C_{OX}} = C_{MOS,unit}I_{SS} \tag{13}$$

Concerning the parasitic capacitance of the load network, we start by considering the topology based on passive resistors R_D. In this case the resistance value is varied by changing the length L_R of the physical resistor, according to [13]

$$R_D = rL_R \tag{14}$$

where r is the resistance per unit length of the polysilicon strip, and the parasitic capacitance results

$$C_{RD} = \frac{1}{3}cL_R = \frac{1}{3}\frac{c}{r}R_D. \tag{15}$$

where c is the parasitic capacitance to substrate per unit length of the polysilicon strip ($c=C_{RD}/L_R$); in the last term, we have obtained L_R from (14) and substituted into (15). Hence, using (1) and (2), the capacitance C_{RD} can be expressed [13] as a function of the current I_{SS}:

$$C_{RD} = \frac{1}{6}\frac{c}{r}\frac{V_{swing}}{I_{SS}} = \frac{C_{R,unit}}{I_{SS}}. \tag{16}$$

It is apparent that for high I_{SS} values a smaller resistance is needed, which means less area and a smaller parasitic capacitance. By substituting R_D and C_{RD} into (8) and exploiting (1) and (2), we get an expression for the propagation delay where the three terms present a different dependence on the bias current:

$$t_{PD} = ln2 \, R_D(C_{NMOS} + C_{RD} + C_L) = ln2 \, \frac{V_{swing}}{2}\left(C_{MOS,unit} + \frac{C_{R,unit}}{I_{SS}^2} + \frac{C_L}{I_{SS}}\right) \tag{17}$$

The first term is the capacitance of the NMOS devices for unit current[2] defined by (13). The second term is related to the parasitic capacitance intrinsic to the resistor load (16), and the third term refers to the external load capacitance. It has to be noted that in previous papers on MCML propagation delay the capacitance C_L in (17) was assumed constant and independent from the tail current I_{SS}. These assumptions are common for very high-speed applications such as optical communication systems or high-speed analog-to-digital converters. In fact, in these scenarios speed is undoubtedly the most important requirement and a resistive load topology is mandatory as will be pointed out in the following. More specifically, since resistors with fixed width are typically used, an increase of the resistance value results in a longer polysilicon strip which requires a larger area and introduces a larger parasitic capacitance. Moreover, in this design domain, the logic gates interface with different stages designed according to different criteria, thus it is reasonable to suppose the load capacitance, that models the input capacitance of the next stage, as independent from the design of the logic gate that drives it.

A completely different context arises for a MCML digital VLSI circuit such as a throughput-oriented processor in which the optimal tradeoff between speed, power efficiency and area footprint requirements has to be found. In this application scenario a logic gate drives N (where N is the gate fan out) logic gates that in principle can be thought as identical to itself (i.e. designed according to the same guidelines). Moreover, since a very dense layout is often used, interconnects parasitic capacitances can be kept much lower than the input capacitances of the loading gates. It is thus more

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[2] $C_{MOSunit}$ is related to the capacitance of the NMOS devices, whose width (and thus capacitance) increases when increasing the bias current due to constraint on swing and noise margin.

realistic to suppose that the load capacitance will scale with the bias current I_{SS} in the same way as the capacitances of the NMOS devices do. In particular, under this condition, the load capacitance C_L in (17) can be expressed as

$$C_L = NC_{in} = NC_{in0}W_n = NC_{in0}2I_{SS}\left(\frac{A_V}{V_{swing}}\right)^2\frac{2L_n}{\mu_{eff}C_{OX}} = NC_{IN,unit}I_{SS} \tag{18}$$

where C_{in} is the input capacitance of the MCML gate, which can be considered linearly dependent on the transistor width W_n, thus, using (12), on I_{SS}. $C_{IN,unit}$ in (18) is the input capacitance of the MCML gate for unit bias current. The propagation delay can thus be estimated as:

$$t_{PD} = ln2\,R_D(C_{NMOS} + C_{RD} + C_L) = ln2\left[\tau_{RD} + \frac{V_{swing}}{2}\cdot\left(C_{MOS,unit} + NC_{IN,unit}\right)\right]. \tag{19}$$

that is obtained substituting (13) and (18) in (8): now also the term related to the load capacitance does not depend on the bias current I_{SS}. We have defined in (19) $\tau_{RD}=R_DC_{RD}$ the contribution of the pull-up resistor to the time constant (8).

Now we focus on the dependence of the time constant τ_{RD} on the bias current I_{SS} for the two I-V conversion topologies. Starting from the topology based on passive resistors R_D, we assume a constant width for the polysilicon strip. In this case the resistance value is changed by varying the resistor length and, under these assumptions, from (14)-(16) we get the second term in (17). Since the voltage swing is constant, a shorter resistor is used when increasing the current, and as a consequence a parasitic capacitance reduction is achieved. Note, however, that for extremely large currents (for typical technologies, in the order of mA) the resistor width could be increased to limit the current density: in this case the resistance value is decreased by increasing its area and thus the parasitic capacitance, (14)-(16) are no more valid, instead the time constant τ_{RD} remains independent from I_{SS}.

Referring now to the I-V conversion topology based on triode-biased PMOS devices, we define R_{Dpmin} the resistance of a minimum-size PMOS transistor with its gate connected to ground, and I_{SSpmin} the bias current related to R_{Dpmin}. If we want to set the bias current of the logic gate at a value lower than I_{SSpmin}, a resistance value higher than R_{Dpmin} has to be used. This higher resistance value can be obtained by increasing the channel length L_p or by using a higher bias voltage for the gate terminal

of the PMOS device; whereas if we want to set the bias current of the logic gate at a value higher than I_{SSpmin} the resistance can be reduced by increasing the channel width W_p. Since the parasitic capacitance is proportional to the device area, this means that for $I_{SS}=I_{SSpmin}$ the PMOS load yields the minimum parasitic capacitance, C_{RDmin}, which increases both reducing or increasing I_{SS} with respect to I_{SSpmin}. Hence, remembering that the resistance value decreases when increasing I_{SS}, we get a time constant, τ_{RD}, which decreases with I_{SS} for I_{SS} lower than I_{SSpmin} and remains constant for higher values of I_{SS}. It has to be noted that this result which shows the dependence of the parasitic capacitance of the triode PMOS device on I_{SS} is reported here for the first time in the literature.

In conclusion, the above considerations show that, for both the considered I-V conversion topologies, the time constant τ_{RD} can decrease with I_{SS} or remain constant, but the difference for the two topologies is the actual I_{SS} value which triggers the change. In particular, the I_{SS} value that requires to increase the width of a polysilicon resistor is of the order of mA, whereas in advanced deep submicron technologies operated at low supply voltages I_{SSpmin} can be as low as a few μA or tens of μA. The behavior of the two kind of loads is thus very different for practical values of I_{SS}.

4. Simulations, comparisons and design guidelines

In order to validate the proposed propagation delay models and to clearly show the behavior of the propagation delay in the different design scenarios, a MCML inverter gate has been taken as case study and designed referring to a commercial 28nm FD-SOI CMOS technology. Supply voltage V_{DD} and V_{swing} have been set to 0.8V and 0.6V respectively. Transistor level simulations have been carried out by using Virtuoso.

A minimum I_{SS} of 2μA has been considered for the simulations, since it is the minimum value to guarantee a minimum-size NMOS device working in the saturation region (lower bias current values lead the NMOS differential pair into sub-threshold region). The minimum-size PMOS transistor has an aspect ratio of 80nm/30nm and an I_{SSpmin} of about 13μA (for currents up to 50μA, the maximum

width W_p is 367nm). The high-resistivity poly resistor has a width of 150nm and a length ranging from 750nm up to 17850nm for currents between 2 and 50μA, thus resulting in a much larger area.

In order to validate the τ_{RD} behavior discussed in Section 3, τ_{RD} as a function of I_{SS} has been evaluated by means of transistor level simulations for the case of resistive load and PMOS load. Fig. 3 shows τ_{RD} as a function of I_{SS} for the case of resistive load and PMOS load. Furthermore, in the latter case, for currents below I_{SSpmin}, both the resistance scaling with channel length (fixed $Vgate$) and by increasing the bias voltage at the gate terminal of the PMOS (fixed Lp) have been considered. The simulated trends of the time constant τ_{RD} with the bias current are in good agreement with the qualitative analysis presented in Section 3. In fact, it is evident from Fig.3 that τ_{RD} of the PMOS is almost constant with I_{SS} for I_{SS} values above I_{SSpmin}.
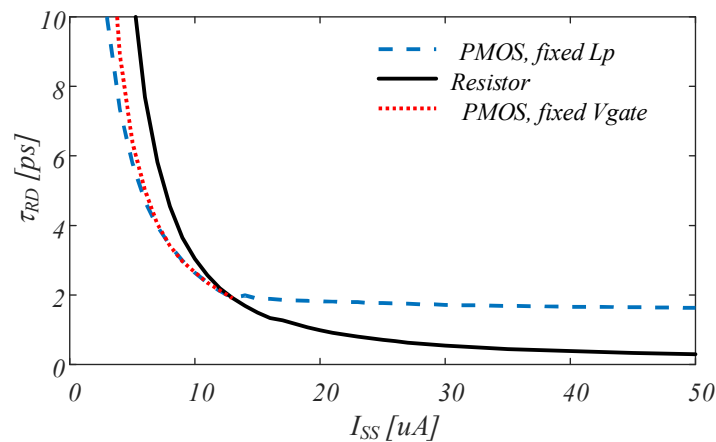

Figure 3. τ_{RD} versus bias current for different I-V conversion topologies (simulations).

In order to validate the proposed models, we have considered the following design scenarios:

   a)   Resistor load with constant C_L;

   b)   Triode PMOS load driving a MCML inverter;

   c)   Resistor load driving a MCML inverter;

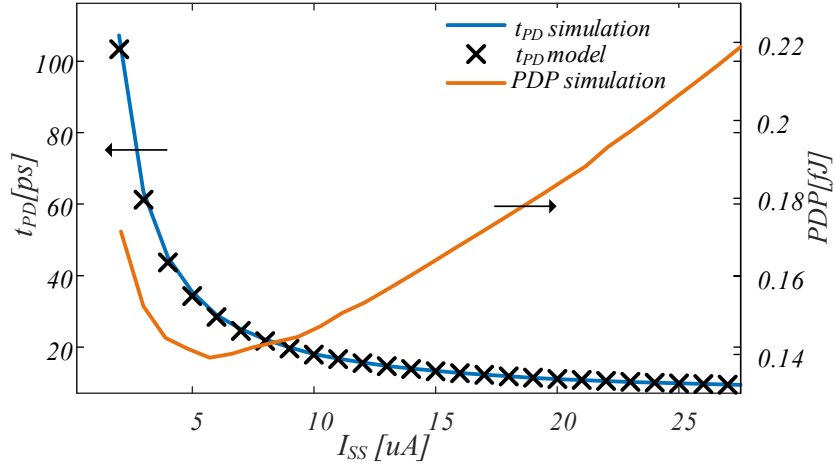I_{SS} is varied also in the load inverter for cases b) and c).

Figure 4: Propagation delay (simulation and model) and PDP (simulation) of a MCML inverter with resistive load and fixed load capacitor.

In order to validate the proposed model for the scenario a), poly resistors and a constant capacitive load of 0.5fF have been assumed. The propagation delay t_{PD} versus I_{SS} is reported in Fig. 4 (both simulation and model are shown). The propagation delay t_{PD} model has been obtained by using (17) in which $C_{MOS,unit}$ = 24.18aF/μA has been assumed and the values of τ_{RD} reported in Fig. 3 (obtained by simulations) have been used. It is apparent that the model shows a very good agreement with a maximum percentage error lower than 3.5% and an average error of 1%. Fig. 4 also shows the simulated power-delay product PDP of the MCML inverter versus I_{SS} referring to scenario a). As in [13], Fig. 4 allows to identify three operating regions: a low power region (LP), where the time constant due to the parasitic capacitance of the resistor dominates and a small increase in bias current allows a large reduction of the delay; a power efficient region (PE), where the PDP exhibits a minimum for an optimal I_{SS} of about 6μA, and power saving is achieved at the cost of a speed penalty; a high speed region (HS), where the delay smoothly tends to a minimum and speed increase is achieved at the cost of a large increase of power. Of course for extremely high-speed operation the MCML gate has to operate in the HS region with a large power dissipation, whereas for highly integrated digitals a good trade-off could be achieved in the PE region. However, in this latter case a polysilicon resistor would require a very large Silicon area and a PMOS load is more suited.
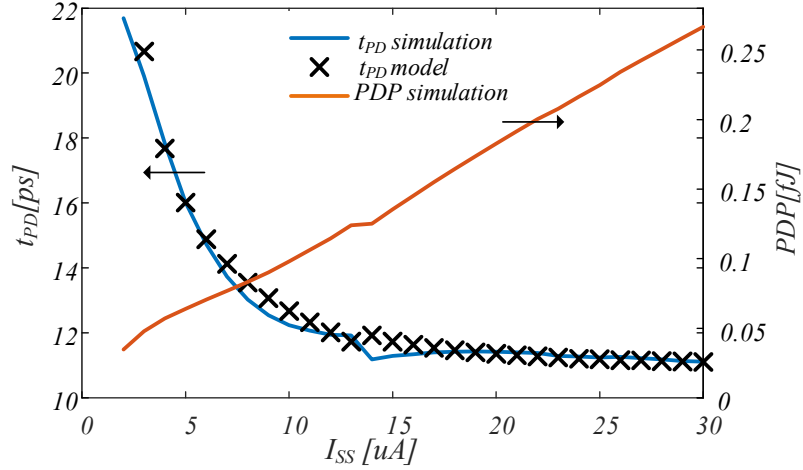
Figure 5: Propagation delay (simulation and model) and PDP (simulation) of a MCML inverter with PMOS load, followed by an identical stage.

Fig. 5 shows the simulated propagation delay and power-delay product PDP of the MCML inverter versus I_{SS} referring to scenario b)[3]. Fig. 5 shows also the propagation delay t_{PD} model estimated by (19) in which $N=1$, $C_{IN,unit} = 21.2aF/\mu A$, and τ_{RD} in Fig. 3 have been assumed. The maximum percentage error found is always lower than 6.5% and the average error is about 2.4%, showing a good agreement with simulations.

Unlike the previous case, now we have a PDP which always reduces by reducing the bias current, and we can identify a LP region, where an increase of the current reduces the delay, and a region in which t_{PD} is approximately constant. I_{SSpmin} marks the threshold of the two regions and is the optimum bias point that maximizes speed with minimum power consumption.

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[3] For bias currents below 13μA the resistance value of the triode PMOS load has been changed by varying the bias voltage at the gate terminal of the PMOS.
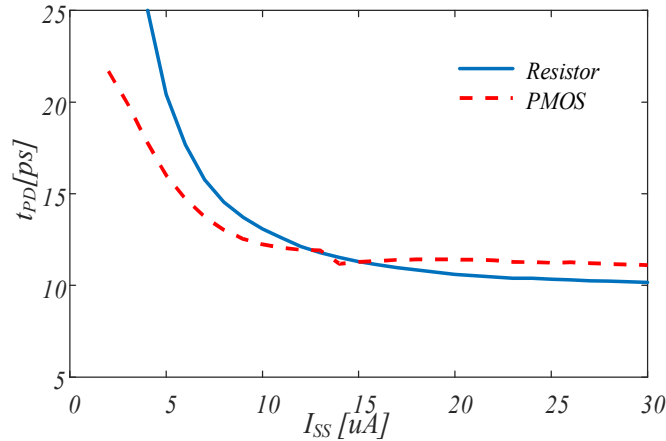
Figure 6: Simulated propagation delay of an inverter followed by an identical stage, in case of resistive or PMOS load.

To further investigate on the choice of I-V conversion approach, we compare scenarios b) and c) that differ only for the load topology. The simulated propagation delay of the MCML inverter versus I_{SS} for both scenarios is shown in Fig. 6. Fig. 6 highlights that the highest speed is achieved with a resistive load, due to the lower parasitic capacitance, but at the cost of a much larger area. On the other hand, when the maximum speed is not a mandatory target, PMOS load is the most power and area efficient solution.

5. Conclusions

In this paper, after reviewing the propagation delay model for MCML gates, we have considered different design scenarios for the topology of the output I-V converter and for the load capacitance of the gate. For the first time we have presented propagation delay models which are able to accurately predict the propagation delay as a function of the bias current I_{SS} in all the considered scenarios. The investigation showed that in the context of MCML digital VLSI circuits the PMOS load provides the minimum area and the best power efficiency which results optimal for $I_{SS}=I_{SSpmin}$. The adoption of a resistive load makes sense only if maximum speed is the only constraint, but this scenario requires a large bias current, a huge silicon area and results in a poor power efficiency.

Appendix A: Table of symbols used in the text

To make the paper more readable, we report in this appendix the list of the symbols used in the paper and their definitions.

Table 1: List of symbols used in the paper

Symbol	Definition
$A_{bulk,max}$	Maximum value of the parameter used to describe the bulk charge effect in BSIM3v3
A_V	Small-signal voltage gain of MCML inverter
c	Overall parasitic capacitance to substrate of the poly resistor of unit length
C_{dbN}	Drain-to-bulk capacitance of NMOS
C_{drain0}	Overall capacitance of NMOS at the drain node, for unit gate width
C_{gdN}	Gate-to-drain capacitance of NMOS
C_{gdP}	Gate-to-drain capacitance of PMOS
C_{gdP0}	Overlap contribution to the gate--to-drain capacitance of PMOS, for unit gate width
$C_{gpP,int}$	Intrinsic contribution to the gate--to-drain capacitance of PMOS
C_{gsN}	Gate-to-source capacitance of NMOS
C_{in}	Input capacitance of the MCML gate
C_{in0}	Input capacitance of the MCML gate for unit gate width
$C_{IN,unit}$	Input capacitance of the MCML gate for unit bias current
C_L	Load capacitance of the MCML gate
$C_{MOS,unit}$	Capacitive contribution of the NMOS pull-down network to the open-circuit time constant, for unit bias current

C_{NMOS}	Capacitive contribution of the NMOS pull-down network to the open-circuit time constant
C_{OX}	Oxide capacitance for unit area
C_{RD}	Parasitic capacitance of the pull-up resistor in the RC equivalent model
C_{RDmin}	Parasitic capacitance of the pull-up resistor implemented by a minimum-size PMOS
C_{RTOT}	Overall parasitic capacitance to substrate of the poly resistor
$C_{R,unit}$	Parasitic capacitance of the pull-up resistor in the RC equivalent model, for unit bias current
g_{mN}	Small-signal transconductance of NMOS
I_{SS}	Bias current of the MCML gate
I_{SSpmin}	Bias current of the MCML gate sized with a minimum-size PMOS pull-up resistor
K	NMOS transconductance parameter
L_n	Gate length of NMOS
L_p	Gate length of PMOS
L_R	Length of polysilicon resistor
N	Fan out of MCML gate
NM	Noise margin of MCML gate
r	Resistance for unit length of the poly resistor of fixed width
R_D	Pull-up resistance
R_{Dpmin}	Resistance of minimum-size triode-biased PMOS with $V_{SG}=V_{DD}$
R_{DS}	Source-to-drain parasitic resistance in BSIM3v3
R_{DSW}	Source-to-drain parasitic resistance per unit gate width
R_{int}	Intrinsic resistance of triode-biased PMOS

r_{oN}	Small-signal drain-to-source resistance of NMOS
t_{PD}	Propagation delay of the MCML gate
V_{DD}	Supply voltage
V_{SG}	Source-to-gate voltage of the PMOS
V_{swing}	Differential voltage swing
V_{Tp}	PMOS threshold voltage
W_n	Gate width of NMOS
W_p	Gate width of PMOS
Δ	Logic level (single-ended voltage swing)
μ_{eff}	Effective mobility of electrons in NMOS
$\mu_{eff,p}$	Effective mobility of holes in PMOS
τ	Open-circuit time constant of MCML gate
τ_{RD}	Contribution of the pull-up resistor to the open-circuit time constant

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