PROCEEDINGS OF SCIENCE

PixFEL: development of an X-ray diffraction imager for future FEL applications

Luca Lodola[*,ab] **G. Batignani**,[ef] **M. A. Benkechkache**,[c] **S. Bettarini**,[ef] **G. Casarosa**,[ef] **G.-F. Dalla Betta**,[cd] **L. Fabris**,[i] **F. Forti**,[ef] **M. Giorgi**,[ef] **M. Grassi**,[ab] **P. Malcovati**,[ab] **M. Manghisoni**,[bg] **F. Morsani**,[f] **A. Paladino**,[ef] **L. Pancheri**,[cd] **E. Paoloni**,[ef] **L. Ratti**,[ab] **V. Re**,[bg] **G. Rizzo**,[ef] **G. Traversi**,[bg] **C. Vacchi**,[ab] **G. Verzellesi**[dh] **and H. Xu**[cd]

[a] *Università degli Studi di Pavia*
via Ferrata 1. 27100 Pavia, Italy
[b] *INFN Sezione di Pavia*
via Bassi 6, 27100 Pavia, Italy
[c] *Università di Trento*
Via Sommarive 9, 38123 Povo (TN), Italy
[d] *TIFPA*
Via Sommarive 14, 38123 Povo (TN), Italy
[e] *Università di Pisa*
Largo Pontecorvo 3, 56127 Pisa, Italy
[f] *INFN Sezione di Pisa*
Largo Pontecorvo 3, 56127 Pisa, Italy
[g] *Università di Bergamo*
Via Marconi 5, 24044 Dalmine (BG), Italy
[h] *Università di Modena e Reggio*
Via Amendola 2, 42122, Modena, Italy
[i] *Oak Ridge National Laboratory*
Oak Ridge, TN, USA
E-mail: luca.lodola01@universitadipavia.it

A readout chip for diffraction imaging applications at new generation X-ray FELs (Free Electron Lasers) has been designed in a 65 nm CMOS technology. It consists of a 32×32 matrix, with square pixels and a pixel pitch of 110 μm. Each cell includes a low-noise charge sensitive amplifier (CSA) with dynamic signal compression, covering an input dynamic range from 1 to 10^4 photons and featuring single photon resolution at small signals at energies from 1 to 10 keV. The CSA output is processed by a time-variant shaper performing gated integration and correlated double sampling. Each pixel includes also a small area, low power 10-bit time-interleaved Successive Approximation Register (SAR) ADC for in-pixel digitization of the amplitude measurement. The channel can be operated at rates up to 4.5 MHz, to be compliant with the rates foreseen for future X-ray FEL machines. The ASIC has been designed in order to be bump bonded to a slim/active edge pixel sensor, in order to build the first demonstrator for the PixFEL (advanced X-ray PIXel cameras at FELs) imager.

The 25th International workshop on vertex detectors
September 26-30, 2016
La Biodola, Isola d'Elba, ITALY

*Speaker.

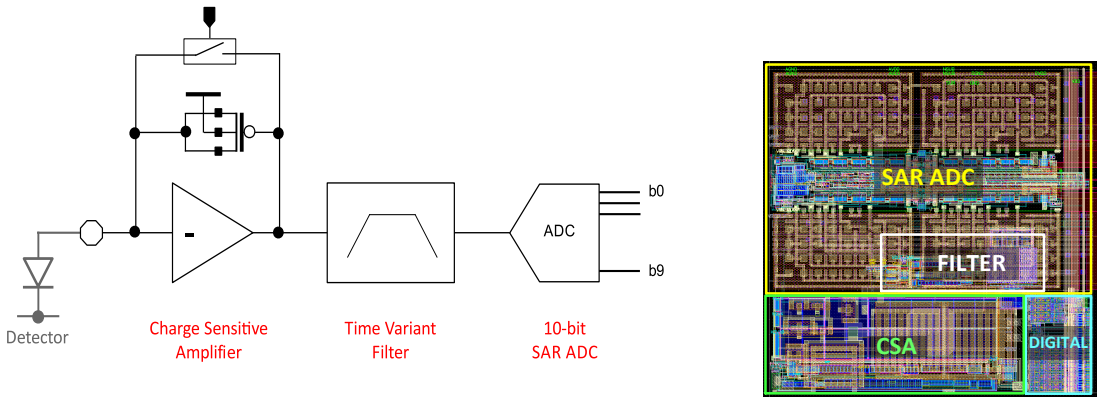
PoS(Vertex 2016)065

1. Introduction

New generation FEL facilities will be able to provide X-ray beams with unprecedented properties in terms of peak brilliance, pulse duration and repetition rates, potentially revolutionizing many research fields (e.g. structural biology and chemistry, material science and nuclear and molecular physics) [1] [2] [3]. Specific X-ray imaging detectors need to be developed to fully exploit the potential of the new generation FEL and to match the challenging requirements in terms of space and amplitude resolution, input dynamic range, frame rate and frame storage capability. The PixFEL (advanced X-ray PIXel cameras at FELs) project, founded by INFN, in the long terms aims to develop a two-dimensional pixelated imaging camera for application at future FELs and to advance the state-of-the-art of imaging instrumentation by exploring innovative solution and new technologies. This will be achieved by bump bonding a large area focal plane detector to a dual layer front-end chip. The latter will be the result of the vertical interconnection, with Through Silicon Via (TSV) techniques, between a first layer with analog front-end and ADC and second layer only reserved to memory and digital readout [4]. After the characterization of a first prototype front-end [5], a new chip has been designed and fabricated using a 65 nm CMOS technology. The chip consists of a 32×32 square cells. This work will address the design of the 32×32 readout chip, its main building blocks and their performance.

2. PixFEL readout channel

The Chip layout consists of 32×32 matrix. Each $110\ \mu m \times 110\ \mu m$ pixel of the readout chip includes a low noise charge sensitive amplifier with dynamic signal compression, a time-variant shaper with a trapezoidal weighting function, a small area, low power 10-bit SAR ADC and elementary digital blocks for channel control and data readout. The block diagram of the readout channel is shown in Fig. 1(a) and the layout in Fig. 1(b). In the following details of the blocks are discussed.

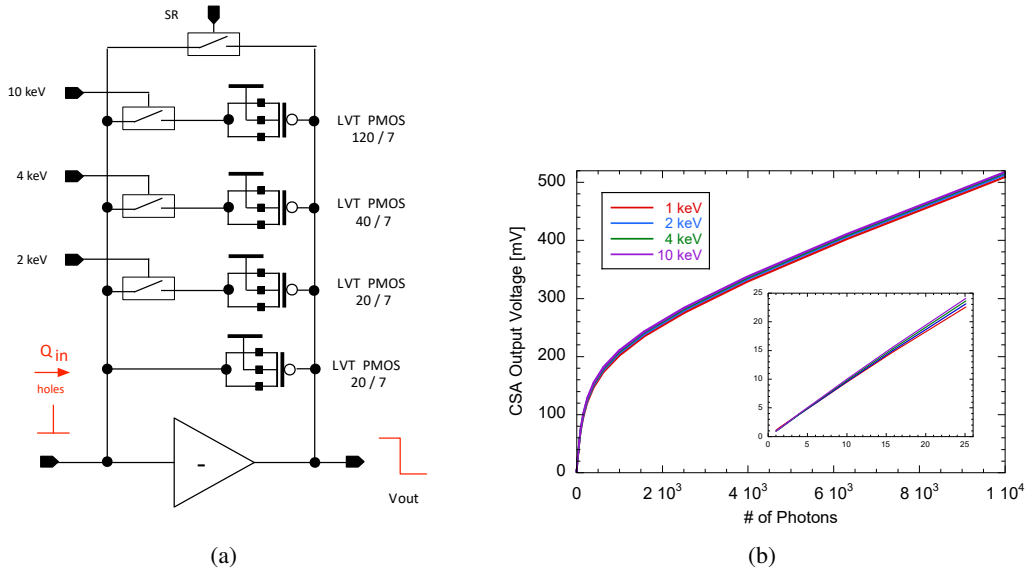


(a) (b)

Figure 1: Block diagram of the pixel readout channel (a) and its layout (b).

2.1 Charge sensitive amplifier

In order to cover the wide input dynamic range (from 1 to 10^4 photons) as requested by FEL applications, while preserving at the same time a single photon resolution for small input signals (up to 20 photons), a nonlinear input-output characteristic is needed. The CSA has a nonlinear characteristic thanks to the dynamic change of its feedback capacitance with the voltage across it. Figure 2(a) shows that the feedback capacitor is a MOS varactor [6] and that it is split into four devices with the same channel length and different channel widths. By suitably controlling the three switches through a two bit binary-to-thermometric decoder, the total area of the feedback MOS capacitor is changed so as to make the amplifier capable of processing signals from photons at 1, 2, 4, 10 keV, while preserving the input dynamic range of 1 to 10^4 photons in each photon energy configuration. Figure 2(b) shows the simulation results of the input-output characteristic for all the four energy options. The expected non-linear transfer function can be noticed, with a higher gain in the region where single photon resolution is required, shown in the inset of Fig. 2(b), and a smaller gain at large signal. The input signal interval of 1 to 10^4 fits into an output dynamic range of about 500 mV in all of the four possible sensitivity configurations.



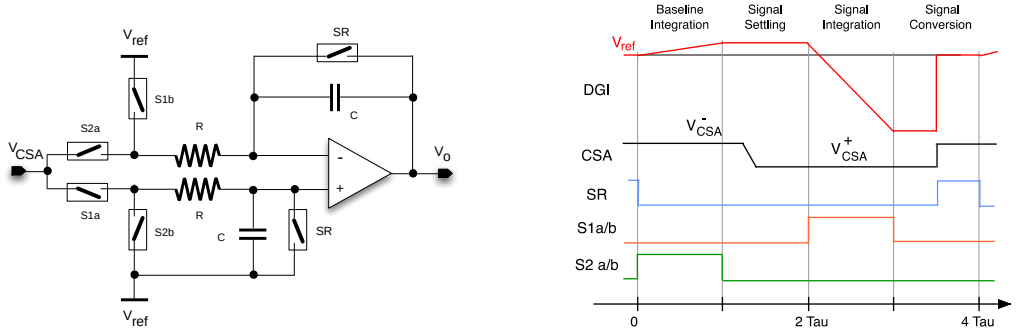
(a) (b)

Figure 2: Schematic diagram of the charge sensitive amplifier (a) and its simulated input-output characteristic (b).

2.2 Time variant filter

Half of the cell in the 32×32 array incorporates the shaper already implemented and tested in the channel prototype, based on a transconductor and on the so called flip-capacitor filter (FCF) [7]. A design improvement of the time variant shaping stage has been included for comparison in the other half of the array. A simplified schematic diagram of the new shaping stage, which is designed around the same forward gain block as the one used for the FCF (a two stage amplifier with NMOS differential input [8]) is shown in Fig. 3(a). The new proposed architecture is based on a Differential Gated Integrator (DGI), in which the input terminals are switched between the

reference voltage (V_{ref}) and the output of the CSA (V_{CSA}) to obtain, by means of a correlated double sampling (CDS) technique, a trapezoidal weighting function. With reference to the timing diagram of the switch control signals shown in Fig. 3(b), during the baseline integration interval, the non-inverting input of the DGI is connected to the output of the CSA, whereas the other terminal is shorted to V_{ref}. In the signal settling interval, both the terminals are left floating while the charge



(a) (b)

Figure 3: Schematic diagram of the DGI (a) and time diagram for the DGI control signals (b).

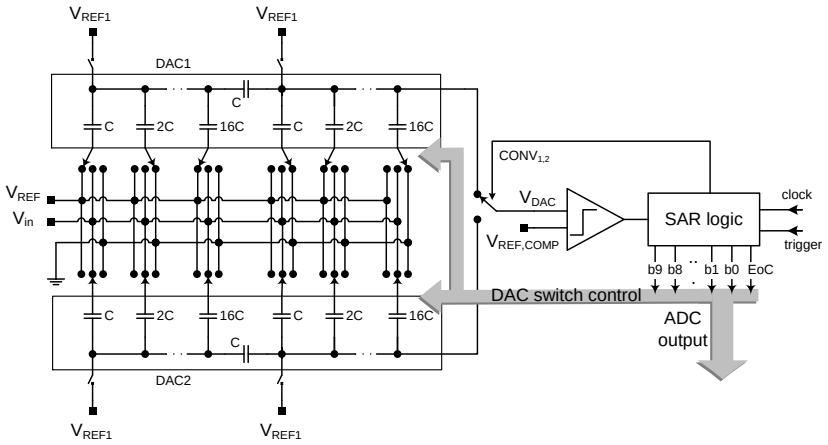
generated in the detector by the diffracted laser pulse from the FEL source induces a signal at the CSA input. A second integration is performed in the subsequent period, during which the inverting input of the DGI is connected to the CSA output. At the end of this time interval, the amplitude of the output signal V_o is proportional to the difference between the CSA output level after the photon signal arrival, V^+_{CSA}, and the baseline level, V^-_{CSA},

$$V_o(3\tau) = V_{ref} + \frac{\tau}{RC}(V^+_{CSA} - V^-_{CSA}), \tag{2.1}$$

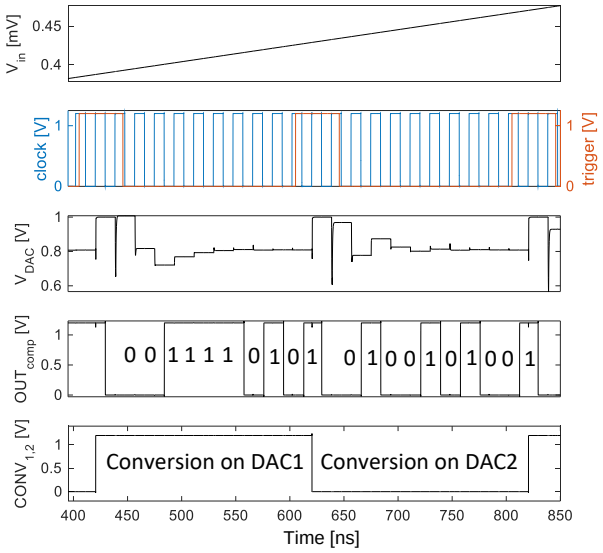
where τ is the duration of each of the four time intervals in Fig. 3(b) and R and C are the resistance and the capacitance in the scheme of Fig. 3(a). The shaper has also two selectable gains (i.e. two selectable feedback capacitances) in order to cover the full input dynamic range at rates of 4.5 MHz ($\tau \approx 55\ ns$) and 2.25 MHz ($\tau \approx 110\ ns$). At the end of 3τ, V_o is sampled by the ADC and the feedback capacitances of the charge sensitive amplifier and of the filter are reset.

2.3 Time-interleaved 10-bit SAR ADC

Each pixel includes a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) for in pixel digitization of the amplitude signal at a sampling frequency in the megahertz range, up to 5 MHz [9]. A 10-bit resolution has been chosen in order to guarantee a single photon resolution at small signals and a quantization noise much lower than the limit imposed by the Poisson noise at large signals. The ADC is based on a charge redistribution architecture, implemented through a split capacitor DAC array in order to reduce the area and the input capacitance. Besides, a time-interleaved structure has been implemented to speed up the ADC operation and to relax the driving capability requested to the previous stage (the shaper). Each ADC has two capacitive DACs. During each sampling period, the capacitors of one of the DACs are pre-charged



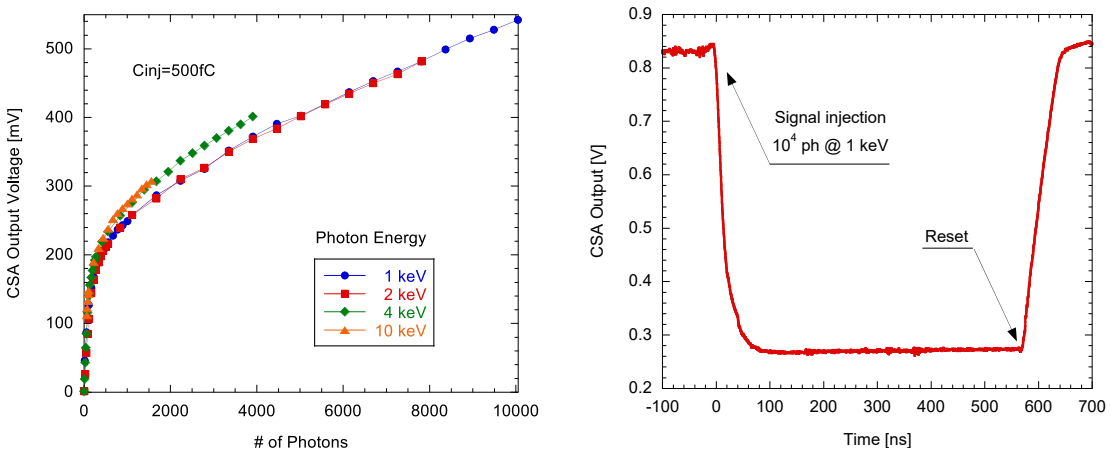
(a)



(b)

Figure 4: Simplified scheme of the time-interleaved SAR ADC (a) and simulated main signals during two consecutive conversions (b), the first giving as a result the digital word '0011110101' and the second giving '0100101001'.

by the shaper output stage, while the sample stored in the capacitors of the other DAC during the previous period is converted. Figure 4 shows a simplified scheme of the ADC architecture and the main ADC signals simulated during two consecutive conversions, also illustrating the interleaving operation. The comparator has a pre-amplification stage introduced in order to minimize kickback noise effects [10], followed by a dynamic latched comparator. The input switches, through which the capacitive DACs are pre-charged to the shaper output voltage, have to cover a wide range [0.2;



(a) (b)

Figure 5: Measured CSA input-output characteristic (a) and time response (b).

1] V. In order to keep their on-conductance constant through the whole input range, a bootstrap switch architecture has been used.

3. Preliminary experimental results

The measurement campaign on the readout channel of the new 32×32 array chip is ongoing. Preliminary measurement results on single blocks are discussed in the following. These data are representative of the behavior detected in a larger set of samples. The output of the CSA and of the shaper can be measured through four analog output pins. Figure 5(a) shows the measured CSA input-output characteristic for photons at all the selectable energies (1, 2, 4, 10 keV). The

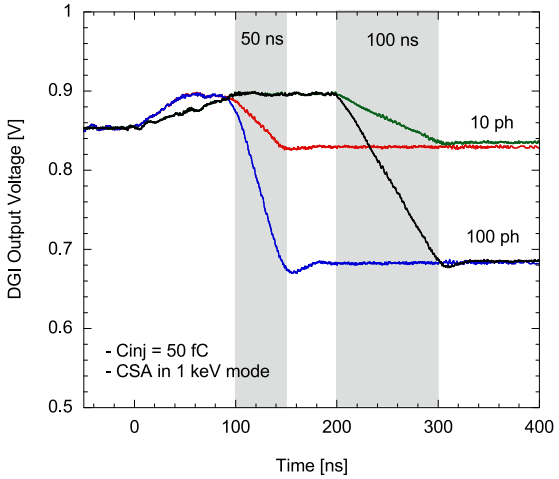


Figure 6: DGI time response to two input signals (10 and 100 photons), each obtained in the two available integration time configurations (50 ns and 100 ns).

input charge for this measurement is obtained by injecting at the preamplifier input a number of electrons from 0 to about 4×10^6, by means of an external voltage step with an amplitude from 0 V to 1.2 V applied on an input capacitance (C_{inj}) included in each pixel and with a value selectable between 50 fF or 500 fF. This means that the whole input dynamic range of 10^4 photons can be covered only in the 1 keV gain configuration. As it can be noticed, the measured input-output characteristic is in good agreement with the simulation results shown in Fig. 2(b), with a slightly higher gain for small signals in the 4 and 10 keV gain settings, probably due to poor modeling of stray capacitances in the foundry design kit. Figure 5(b) shows the time response of the CSA at the maximum input signal of 10^4 photons: the response time and the reset time (from 10% to 90%) are respectively about 41 ns and 55 ns, therefore complying with operation at rates up to 4.5 MHz.
Fig. 6 shows the response of the shaper to two different input signals (10 and 100 photons). In the two cases, the response was taken both in the 50 ns and in the 100 ns integration time configuration. As it can be noticed, when operated at $\tau = 50\ ns$, the best operating point for the chip, the DGI can comply with the target conversion rate of 4.5 MHz.

4. Conclusion

In this paper, a 32×32 matrix readout chip for diffraction imaging applications at X-ray free electron lasers has been described. Each block of the readout channel has been presented. The first circuit is a charge sensitive amplifier with dynamic signal compression, capable of fitting the wide input dynamic range from 1 to 10^4 into an output range of about 500 mV. Beside that, the preamplifier charge sensitivity can be selected in order to adapt to four different photon energies from 1 to 10 keV. Than an improved version of the time variant filter, based on a differential gated architecture, was discussed. Eventually a 10-bit time interleaved SAR ADC for in-pixel digitization was presented. The chip was designed and fabricated in a 65 nm CMOS technology. Preliminary results of the chip characterization were shown. Some discrepancy between measurements and simulation was found, but the collected data demonstrate the compatibility of the readout channel with operation at the target rate of 4.5 MHz. The measurement campaign is still ongoing in order to collect more statistics and to characterize the behavior of the full matrix.

References

[1] R. Xu, H. Jiang, C. Song, J.A. Rodriguez, Z. Huang, C.-C. Chen et al., "Single-shot three-dimensional structure determination of nanocrystals with femtosecond X-ray free-electron laser pulses", Nat. Commun., vol. 5, pp. 4061, 2014.

[2] A. Barty, J. Küpper and H.N. Chapman, "Molecular Imaging Using X-Ray Free-Electron Lasers", Annual Review of Physical Chemistry, Vol. 64, pp. 415-435, 2013.

[3] J. Feldhaus, M. Krikunova, M. Meyer, T. Möller, R. Moshammer, A. Rudenko et al., "AMO science at the FLASH and European XFEL free-electron laser facilities", Journal of Physics B: Atomic, Molecular and Optical Physics, vol. 46, no. 16, pp. 164002, 2013.

[4] L. Ratti, D. Comotti, L. Fabris, M. Grassi, L. Lodola, P. Malcovati et al., "PixFEL: developing a fine pitch, fast 2D X-ray imager for the next generation X-FELs", Nucl. Instrum. Meth. A, vol. 796, pp. 2-7, 2015.

[5] L. Ratti, D. Comotti, L. Fabris, M. Grassi, L. Lodola, P. Malcovati et al., "A 2D imager for X-ray FELs with a 65 nm CMOS readout based on per-pixel signal compression and 10 bit A/D conversion", Nucl. Instrum. Meth. A, vol. 831, pp. 301-308, 2016.

[6] M. Manghisoni, D. Comotti, L. Gaioni, L. Ratti, V. Re, "Dynamic compression of the signal in a charge sensitive amplifier: from concept to design", IEEE Trans. Nucl. Sci., vol. 62, no. 5, pp. 2318-2326, 2015.

[7] L. Bombelli, C. Fiorini, S. Facchinetti, M. Porro, and G. De Vita, "A fast current readout strategy for the XFEL DePFET detector", Nucl. Instrum. Meth. A, vol. 624, pp. 360-366, 2010.

[8] F. Maloberti, "Analog design for CMOS VLSI sysitems", Kluwer Academic Publishers, 2003.

[9] L. Lodola, "Interleaved SAR ADC for in-pixel conversion in future X-ray FEL application", 2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 81- 84, 2015.

[10] P. M. Figueiredo, J. C. Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparators", IEEE Transactions On Circuits And SystemsâĂŤII: express briefs, Vol. 53, No. 7, July 2006